Comparative analysis regarding Human Body Electrostatic Discharge

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Abstract – In the microelectronic industry, the Electrostatic Discharge has a significant importance regarding the failures within the semiconductor devices. Over the years, we're realized many studies and researches in order to develop a meaningful Human Body ESD pulse and equipment which is capable of applying that pulse for various voltage levels to a semiconductor device. The paper aims to create the context in which the electrostatic discharge phenomenon occurs in integrated circuits industry and also to characterize the behavior of the devices in terms of electrostatic events.

Keywords: Electrostatic Discharge, Human Body Model, parasitic elements

I. INTRODUCTION

Electrostatic Discharge (ESD) is a common phenomenon in the nature and results due to different materials caring static positive or negative charges resulting into a built-in static voltage. The amount of this static charge depends on the triboelectric characteristics of the material and from external parameters.

Therefore, once the statically charged material is put in contact with a grounded object, charge balance will be restored through a discharge of the electrical charged material toward the ground (EOS). Knowing the great energy stored in the charged material, the discharge is extremely fast, in the order of some tens of nanoseconds.

Considering the fact that a human body has a typical capacitance of about 100 pF and a contact resistance of about 1.5 kΩ, an electrostatic potential of several kV's may mean current up to several amperes.

The discharge of this potential through a grounded object (like, for instance, the door of a vehicle) causes only a minor discomfort for the body. In the case in which, the discharge occurs through a pin of an integrated circuit (IC): the high current (and, eventually, the high voltage) could cause an irreversible failure to the device.

Not only a human body but any charged object contacting an IC could lead to the same result: this is the case when, after manufacturing, integrated circuits have to be tested. If the equipment does not have a proper grounding, it can accumulate a potential that might discharge towards the IC's pins once these are put into the socket. In general, during all the phases of an IC manufacturing process, ESD is a primary concern and Overstress (of which ESD is a subset) it has been quantified to constitute about 38% of the overall field returns [1, 2].

Since the phenomenon is unavoidable, there is a strong need of developing protection strategies.

Over the years was observed a large increase of the costs in microelectronics industry, due to broken devices, damaged components and loss of information. The damage to these components, due to ESD events can be immediately detected or could take even years before being discovered, causing unpredictable errors in the field.

Therefore, ESD is one of the major problems in terms of safety in the integrated circuits industry. Reliability of integrated circuits can be improved using various techniques to implement protection or avoid the events of ESD.

Typically, achieving protection against electrostatic discharge ESD consists in determine procedures in which several types of circuits are provided, processed, packaged and tested using simple analysis. This approach is time consuming and does not facilitate the development of protection circuits in future technologies. A better manner includes a technique for testing and modeling the devices behavior to electrostatic discharge, for understanding the functionality of transistors, diodes, capacitors and resistors of the circuit structure and for circuit extraction of the critical parameters.

The ESD phenomenon has been studied for some time and in terms of reliability qualification, three basic models are dominant: The Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM).

In this paper, we will be focusing on the HBM Discharge and some concerns we have about the model as presently defined.

Therefore, to achieve higher quality and reliability standards for IC products and to reduce the IC product

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loss due to such ESD failure mechanisms, this phenomenon should be well controlled [3].

In order to obtain a higher ESD robustness and to evaluate the effectiveness of the protection circuitry in an integrated circuit, significant applications were elaborated for understanding the implications of the human body discharge event.

This HBM pulse is intended to simulate the human body type ESD conditions, the devices would experience during normal usage. The ESD testing is also used to determine the immunity or susceptibility level of a system or device, to the HBM ESD event.

II. Test methods of Human Body Model (HBM)

In accordance with the concepts presented, the work is based on means and methods of testing Human Body Model (HBM) and characterizing the behavior of integrated circuits from electrostatic discharge. Hence, were realized a series of tests by varying the circuit components corresponding HBM model, to determine the impact on the waveform of discharge current.

HBM testing is often the sole means of qualifying ESD reliability because the specifications of the test are standardized industry wide and because several commercial HBM testers are available [4].

To investigate the Human Body ESD event, a study of the actual human body discharge was performed. The intent of the investigation was to gather a basic understanding of the HBM ESD event and stimulate thought about the actual human body discharge pulse and the possible effect on ESD immunity or susceptibility.

Human Body Model represents the discharge of a standing individual through a pointing finger, which reproduces field failures caused by human handling. It is considered as "the ESD model" because of its common presence in the daily life in a variety of situations.

Frequently, HBM events occur at 2 – 4 kV hence, protection levels of this range are necessary.

The equivalent circuit for each ESD event can be represented by modeling the discharge current waveforms, using RLC elements shown in Fig. 2, and idealized current waveforms shown in Fig. 4.

In practice, using the models based on the real-world ESD events, ESD robustness of devices under different discharge processes can be systematically characterized. [3]

The typical circuit considered for HBM consists in a capacitor C = 100 pF, charged up to a certain voltage and then discharged through a resistor R = 1.5 kΩ, representing the body capacity and the intrinsic resistance of the arms of a human [5]. The static energy is stored in the capacitor C that, once the switch is open, can discharge through the body resistor R in the device under test (DST) – Fig. 1.

The capacitor and resistor values were precisely selected, to generate a pulse similar to that generated by an electrostatically charged human touching the pins of an IC [5].

The energy stored in the charged body and the rapid rise and fall time parameters of the ESD current can pose a great threat for the devices. Considering that, in the circuits presented, the HBM acts like a current source with a rise-time of about 5 nsec, a decay time of about 7 nsec and a current peak of 1.2 A (for 4 kV pre - charge).

Fig. 1 shows a simplified circuit of HBM ESD conditions and the schematic realized in Fig. 2 describes an equivalent circuit of the HBM using parasitic elements.

The parasitic elements (L and R) are added in order to account for the interaction between the discharge source and the measurement board: their proper evaluation is critical to assess reproducible stresses. In particular, the test board capacitor C is crucial because its discharge occurs at every snapback point in the characteristic, therefore causing an extra stress to the device under stress.

In the diagrams, the transition time of the switch (open - close), is about 1 nsec and the pulsation source used, varies the amplitude of the signal in the range 0 – 4 kV.
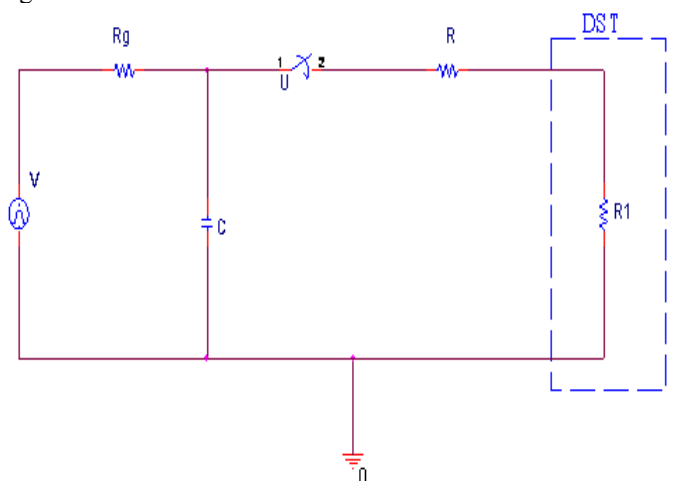

Fig. 1.The diagram of the typical circuit of Human Body Model
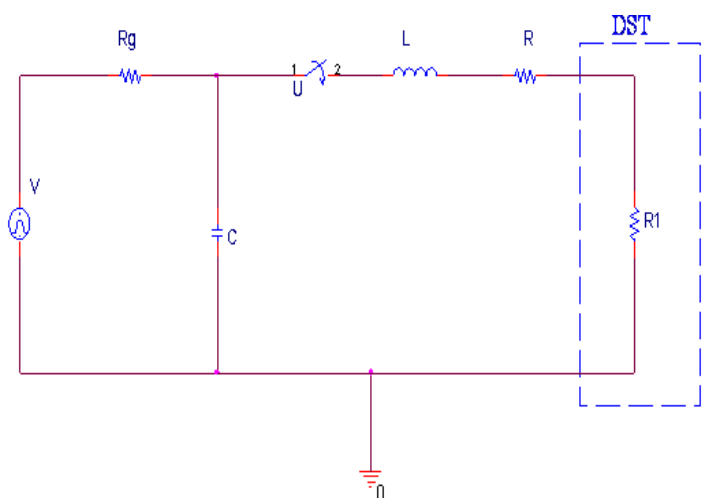

Fig. 2.The equivalent Human Body Model circuit for a charging voltage of 4 kV

The analysis made, were considered for a period of time of 300 nsec, using a 10 nsec step. The step value was chosen in terms of increasing the accuracy of the waveform display.

The characteristic current waveforms of an electrostatic discharge for an HBM charging voltage of 4 kV are presented in Fig. 3 and Fig. 4.

The figures highlight that the variation of the parasitic elements (L and R) have a major impact on the ramp, peak and duration of the current wave.

The typical Human Body ESD event has a fast, high current peak followed by a lower, more slowly decaying current pulse. Considering that, a single ESD event can cause serious damages for devices or possibly could initiate a device weakness that can cause failure with continued use.

A typical waveform of the Human Body Model is shown in Fig. 3 and the waveform corresponding the circuit with parametric elements can be observed in Fig. 4.
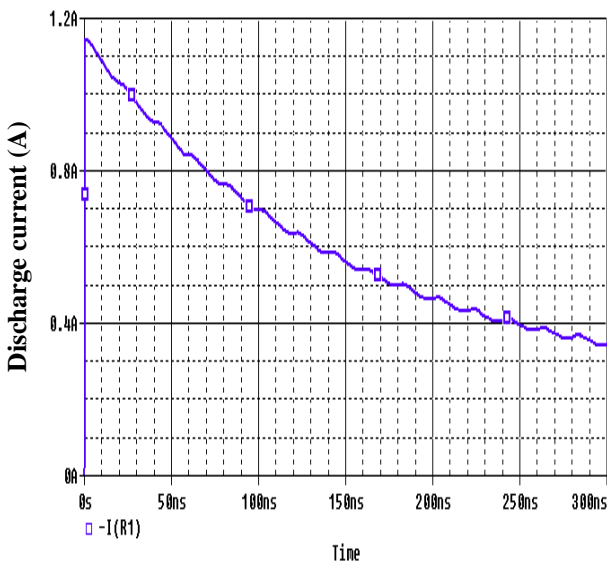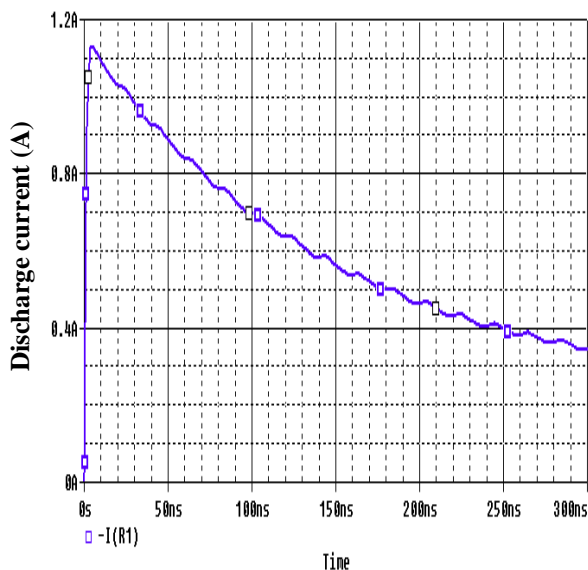

Fig. 3.The typical Human Body Model waveform

Fig. 4.Human Body Model waveform with parasitic elements

Recent research on human body ESD events shows that discharge pulses with fast rise times, on the order of 1 nanosecond or less, are the most disruptive to the normal operation of electronic equipment [6].

Hence, ESD tests using a fast rise time pulse will provide more accurately, the Human Body Discharge events.

In Fig. 5 can be observed that the supply voltage at a constant discharge resistor value (1.5 kΩ) increases with the slope of the discharge current. The supply voltage varies in the range [4 - 8] kV with a 2 kV step. Fig. 6 illustrates the variation of the discharge resistor R for different values: 1 kV, 2 kV, 3 kV, 4 kV and shows that the resistance increase implies the slope current decrease (at a constant voltage).
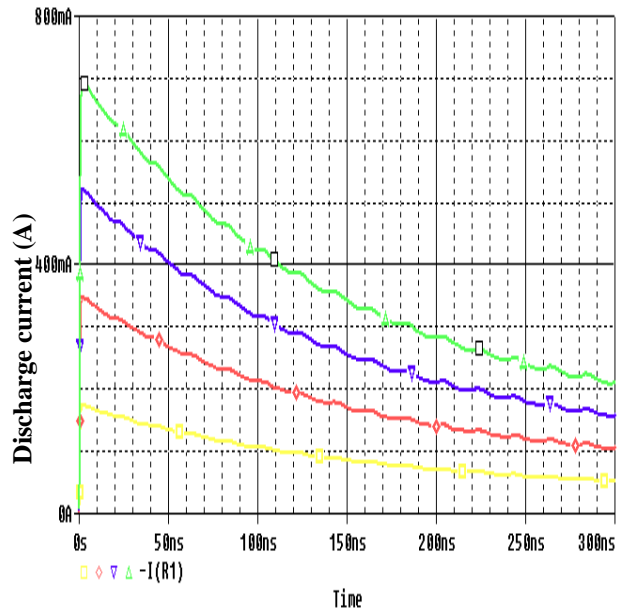

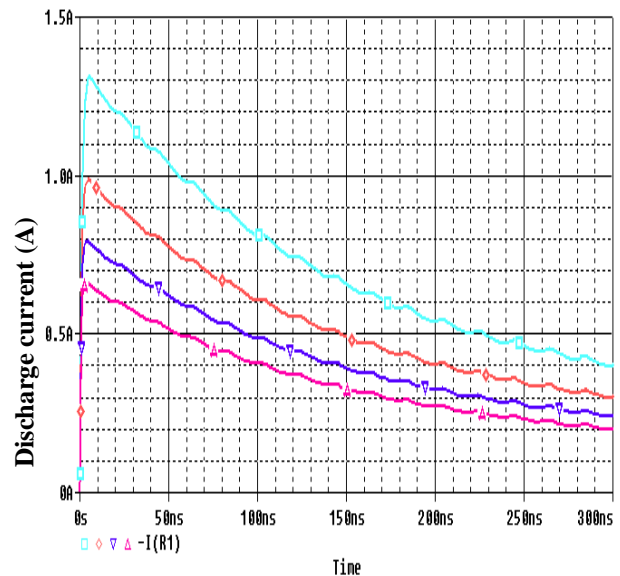Fig. 5.The waveform for the parametric analysis of the source V

Fig. 6.The waveform for the parametric analysis of the resistor R

In Fig. 7 is represented the characteristic waveform for parametric analysis of the Human Body Model

(HBM) for certain values of the parasitic inductance L for a period of time of 300 nsec.

To determine the maximum discharge current obtained when the inductance varies from 3 μH to 8 μH (with a 2 μH step), transient analysis were conducted for a period less than initially considered: 40 nsec - Fig. 8.
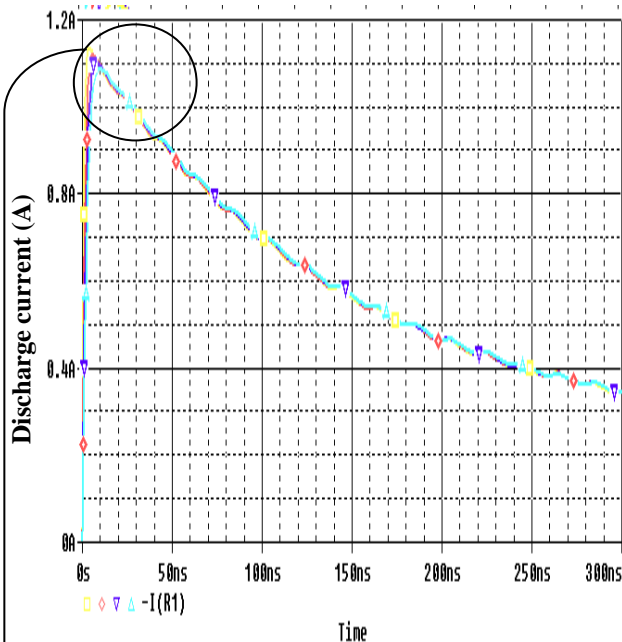

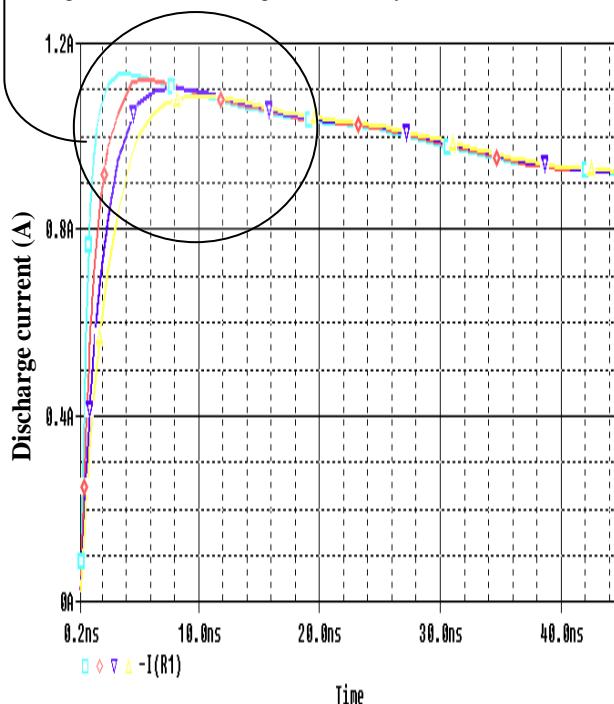Fig. 7.The waveform for parametric analysis of the inductance L

Fig. 8.The waveform for parametric analysis of the inductance L for a period of time of 40 nsec

V. CONCLUSIONS

To highlight the effects of the simulations used during this investigation and the resulting waveforms, several HBM tests were realized. These tests have a big importance in the evaluation of the protection circuitry of semiconductors or on the susceptibility level of a part to an ESD event.

Understanding the functioning of components used in circuits and the specific test methods is extremely important for implementing protection circuits and for assessing the sensitivity of integrated circuits at electrostatic discharges. The spectrum of constraints due to electrostatic discharge is quite broad, so it is quite impossible to achieve immunity to electrostatic discharges. However, using an adequate modeling of the circuits it can achieve an improved reliability of integrated circuits IC.

VI. REFERENCES

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