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CMOS-Integrated Temperature Relay Based on Wilson Mirror

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Abstract – As a première, here is presented a temperature relay scheme for CMOS chips, based on a simple structure of voltage source with two cross-connected current mirrors (of Wilson type and simple one). In this scheme the positive feedback is exploited; it is designed in such a way that, for a particular temperature, the circuit toggles. The output voltage performs a level jump, ample enough to drive an interface circuit with the relay signalisation processing part. The relay toggle condition is inferred which clears up the relay function. The releasing temperature may be programmed in a large range through one or two resistors. The simulation results are presented for the relay conceived in 0.35µm CMOS process. The releasing-temperature process variation is reduced, by a special design, to a maximum value of ±5.5°C.

Keywords: CMOS temperature relay, cross-connected current mirrors, toggle condition, process variation.

I. INTRODUCTION

In [1], the integrated-circuit designers' attention was drawn on the possibility of obtaining high performances in schemes based on two cross-connected current mirrors (named as "self-biased" current sources too). There, a current reference (using modified-Widlar and reverse-Widlar mirrors) is proposed which applies a very interesting I- and II-order thermal compensation technique. Leaving from this technique, others four types of "branch" and "total" reference current sources with superior performances have been elaborated in [2], [3], [4]. In [5] the I- and II-order thermal compensation technique of [1] has been extended to four new voltage references, one of these sources achieving special performances in respect to the process and supply-voltage variations.

In [6], [7] an idea occurs to renounce the thermal compensation of current and voltage references in [1], [2] and [5] in favour of a I- and II-order thermal sensitizing so as the used simple circuits become, by an adequate design, temperature sensors. This idea proved feasible, and finally [6], [7], more performing temperature sensors were obtained thanks to the Wilson-peaking current mirrors (fig.1) and especially to the modified-Widlar-peaking ones. Their main quality is that of achieving a very small process variation of the output voltage (which is a temperature function).

The performing smart temperature sensors are more and more used in VLSI modern systems. In [6] a great number of applications were treated, which impose their use. There were presented the numerous conditions imposed on integrated temperature sensors. From the publications, one can find out that the temperature sensors in CMOS chips have constituted an important academic and industrial research subject over the last 20 years [6].

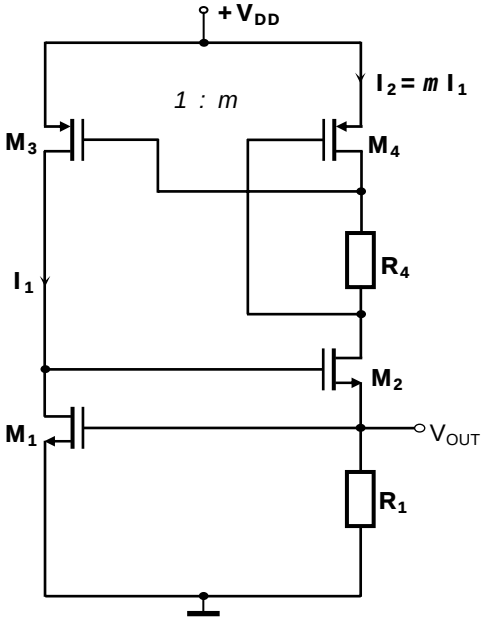

Fig. 1. Wilson-peaking temperature-sensor scheme

In this work was enunciated the idea of achieving, with a simple scheme of the same category, a temperature relay the releasing temperature of which can be modified by a resistor. The scheme conception in 0.35µm CMOS process was successful and the simulations announced promising performances. The

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utility of such temperature relay is incontestable both for the CMOS chips protection, and for signalizing the attainment of a particular temperature of ambient or industrial process/installation.

II. TEMPERATURE-RELAY FUNCTION

The scheme that was used is shown in Fig.2 (partially similar to temperature sensor in Fig.1 but the superior mirror is not a peaking one here) and was adopted thanks to the possibility of ensuring a strong enough positive feedback at a particular temperature and thus, a toggle output voltage V_{out}. The feedback is positive because of comprising two CS-connection amplifier stages in the loop and is amplified by the R_2 resistor in the M_4 drain.

However, essential for achieving the toggle condition is the fact that the resistor R_1 has a negative temperature coefficient (NTC) and the resistor R_2 has a positive temperature coefficient (PTC). The sub-micron CMOS process has the possibility to realize a great number of resistor types, with different temperature coefficients and even with great square resistance.

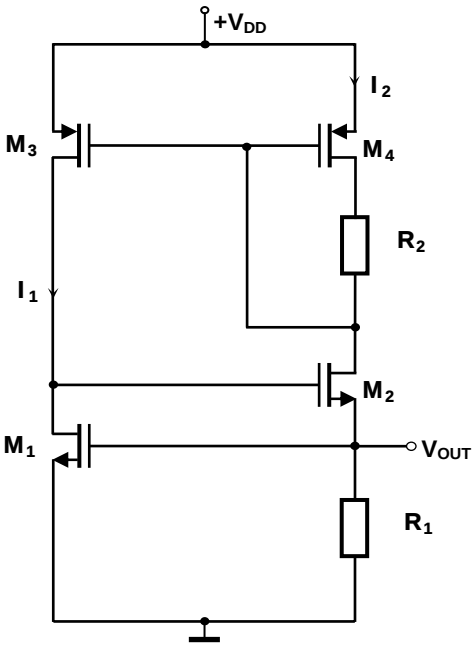

Fig. 2. Wilson-simple temperature-relay

In the circuit of Fig.2 one uses a N^+ polysilicon resistor (NTC) with temperature coefficient of maximum absolute value and a N-Well resistor (PTC) with temperature coefficient of maximum value. Both resistor types present a square resistance of great value (typically 1000Ω/ respectively 1080Ω/) so they do not occupy an exaggerated chip area.

The circuit in Fig.2 function is the following. At usual temperatures all the transistors are saturated, including M_4, because the voltage drop on resistor R_2 is small. The currents in the two branches have small values (as example 0.4μA and 12μA) which are practically imposed by the resistor R_1. The output voltage has a reduced value („low logic level").

When the temperature grows and comes near the releasing value, imposed by R_2, the R_1 value decreases, the current I_2 in the right branch grows, the value of resistor R_2 rises and produces a decrease of the drain-source voltage of transistor M_4. Consequently, this transistor comes near the saturation-region limit. Also, the increasing current causes the increase of V_{GS4} voltage and of saturation-region limit voltage, V_{DSsl} of M_4, the transistor entering the linear region more quickly. The voltage drop on resistor R_1 becomes greater and, because the R_1 value decreases with temperature, the I_2 current grows in addition, leading to a cumulative toggle regime.

At the middle of the output voltage jump, all transistors, excepting M_4, are still in saturation regime and the loop voltage gain is maximal. In this situation the I_1 current on left branch increases too. The drain-source voltages of transistors M_2 and M_3 decrease, they entering the linear regime too. Thus, for a small temperature increase (0.5°C), the I_2 current reaches an about double value in comparison with the initial value and this is the occasion to toggle the output voltage V_{out} at „high logic level". At the toggle end, M_2, M_3 and M_4 are in deep linear regime (with small V_{DS} voltage and great drain current).

III. TOGGLE-CONDITION DEDUCTION

The temperature relay function being known, a problem appears: to demonstrate theoretically the fact that, at a particular temperature – named „releasing temperature", the output-voltage toggle appears. This study will permit to better understand the relay function and to establish the important factors determining the appearance of the toggle phenomenon that is a transition accelerated by the positive feedback with increasing gain.

It was previously affirmed that a positive feedback acts in the scheme. At the usual temperature, this does not assure a voltage gain greater than the unity which could produce the circuit toggle. But, in the proposed scheme, at a particular temperature, imposed by resistors, the open loop attains a greater than 1 voltage gain and a cumulative process appears which makes the circuit to toggle for a temperature increase of only 0.5°C. In this gain increase, entering a deeper and deeper linear regime of the transistor M_4 plays the principal role.

Therefore, the condition the circuit toggles is that the open-loop voltage gain exceeds the value 1. To establish this gain the feedback loop between two branches will be opened, in the gate of transistor M_3 (Fig.2), thus obtaining the two-stage amplifier scheme of fig.3. Here, the stage 1 is achieved by transistor M_3, loaded by the stage-2 input. This last one is realized by the transistor M_2, loaded by the „modified diode" created with transistor M_4. The second stage has a series-parallel negative feedback through the transistor M_1 (it is a Wilson mirror). Because the loop comprises two CS-connection amplifier stages, one gets a total phase difference of 360° between the

output and the input, and consequently, the relay scheme feedback is a positive one.

Since the gain is estimated for a point located in the middle of current and voltage toggle jumps, the variations of which being slow, a low-frequency low-signal technique is possible to be applied. In the calculus of the input and output resistances and of the gain for the Wilson mirror, the method proposed by P. E. Gray was used [8]. This elaborates the amplifier circuit without feedback, set in ideal working conditions (with an ideal input current source and output short-circuit, as well as with input and output loadings due to the feedback circuit), and the circuit for calculating the feedback factor. Both circuits may be easily obtained by applying the P. E. Gray rules: short-circuiting to ground of input node and breaking the output loop in the M_2 source.

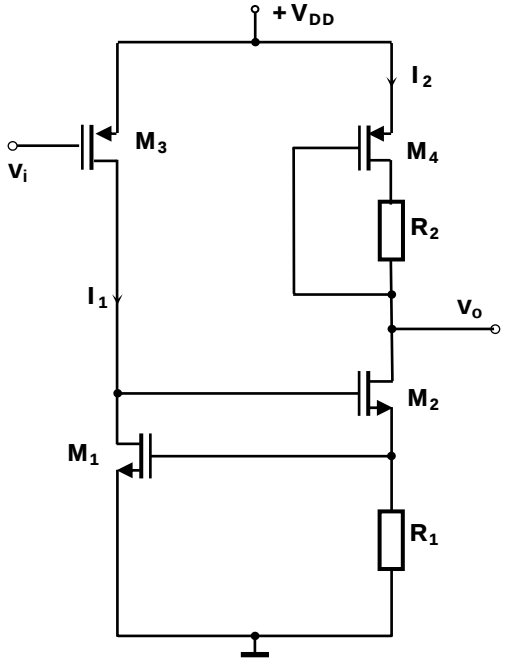

Fig. 3. The open-loop of the feedback amplifier

The 1-stage voltage gain is:

$$A_{v1} \cong -g_{m3}\left(R_{ir} \| r_{ds3}\right) \tag{1}$$

where g_{m3} and r_{ds3} are the mutual conductance respectively the drain-source resistance of the low-frequency low-signal model of transistor M_3 , R_{ir} is the feedback input resistance of the Wilson mirror:

$$R_{ir} = \frac{1}{g_{m1}} \cdot \frac{r_{ds3}}{r_{ds1} + r_{ds3}} \tag{2}$$

where g_{m1} and r_{ds1} are the mutual conductance respectively the drain-source resistance of the transistor M_1.

Now, considering the feedback input resistance $R_{ir} << r_{ds3}$, the first-stage voltage gain may be approximated by the relation:

$$A_{v1} \cong -\frac{g_{m3}}{g_{m1}} \cdot \frac{r_{ds3}}{r_{ds1} + r_{ds3}} \tag{3}$$

Omitting the feedback output resistance R_{or} in the drain of Wilson-mirror transistor M_2, which is huge in respect to the output resistance R_{o4}, the 2-stage voltage gain is:

$$A_{v2} \cong -\frac{A_{ir} R_{o4}}{R_{ir}} \cong -\frac{R_{o4}}{R_1} \cdot \frac{r_{ds1} + r_{ds3}}{r_{ds3}} \tag{4}$$

where A_{ir} is the feedback current gain of Wilson mirror:

$$A_{ir} \cong \frac{1}{g_{m1} R_1} \tag{5}$$

and R_{o4} is the output resistance of the modified diode (composed by M_4 and R_2), seen from the drain of amplifier transistor M_2 :

$$R_{o4} \cong \frac{r_{ds4} + R_2}{1 + g_{m4} r_{ds4}} \tag{6}$$

where g_{m4} and r_{ds4} are the mutual conductance respectively the drain-source resistance of the transistor M_4, working in linear regime (see APPENDIX).

So, the second-stage voltage gain may be put in the form:

$$A_{v2} \cong \frac{1}{R_1} \cdot \frac{r_{ds1} + r_{ds3}}{r_{ds3}} \cdot \frac{r_{ds4} + R_2}{1 + g_{m4} r_{ds4}} \tag{7}$$

One may write now the relay toggle condition for the open-loop gain:

$$A_{v1} \cdot A_{v2} \geq 1 \tag{8}$$

Or, after replacing and simplifying, this condition can be expressed:

$$\frac{g_{m3}}{g_{m1}} \cdot \frac{r_{ds4} + R_2}{R_1} \cdot \frac{1}{1 + g_{m4} r_{ds4}} \geq 1 \tag{9}$$

The analysis of this condition drives to the following conclusions:

- here, the transistor-M_2 mutual conductance g_{m2} does not intervene, which may be explained because its effect was negligible by the Wilson-mirror strong negative feedback,
- the resistances quicken toggle condition attainment with the temperature growth because R_2 is of PTC type while R_1 – of NTC type,
- the r_{ds4} resistance has a small value (<< R_2) after the toggle start because the M_4 transistor enter the deep linear regime, thus the R_2 effect is important,
- the conductance g_{m4} has a more and more reduced value after transistor M_4 enters the linear regime, which accelerates the toggle,
- the product $g_{m4}r_{ds4}$ (see APPENDIX) diminishes quickly with the temperature growth when M_4 enters the deep linear regime, quickening the carrying out of condition (9), where it is the most important term.

As may be seen, the relay function is better described and understood after the deduction of the toggle condition and after the made calculus.

IV. DESIGN EXAMPLE

The numeric calculus to verify the toggle condition has considered the dependence against temperature of variables g_m and r_{ds4} (through the carrier mobility μ and the threshold voltage V_t) then of the resistances R_1 and R_2, using the temperature coefficients. For

better precision it was necessary to consider the second-order temperature coefficients of the carrier mobility [2], [3] and resistors (see APPENDIX). In the conductance g_{m1} and gm_3 calculus, for saturation regime, the channel-length modulation factor (λ) was neglected. The values of parameters K'_n , K'_p , V_{tno} and V_{tpo} (at temperature of 0°C) for transistors as well as those of temperature coefficients for mobility – $k_{\mu n}$, $k_{\mu p}$ (of I order), $k_{\mu n\mu n}$, $k_{\mu p\mu p}$ (of II order) [3], of threshold voltages – k_{Vtn} and k_{Vtp} and of resistors – k_{R1} and k_{R2} (of I order), k_{R1R1} and k_{R2R2} (of II order), were found in the model-parameter list for transistors and resistors in 0.35µm CMOS process considered.

One used the values: $K'_n=87.35\mu A/V^2$, $K'_p=37.74\mu A/V^2$, $V_{tno}=0.759V$, $V_{tpo}=0.807V$, $V_{GS1}=1.385V$, $V_{GS3}=V_{GS4}=1.03V$, $V_{DS4}=0.1V$, $k_{\mu n}=-6.17\cdot10^{-3}/^oC$, $k_{\mu n\mu n}=0.0167\cdot10^{-3}/^oC^2$, $k_{\mu p}=5.07\cdot10^{-3}/^oC$, $k_{\mu p\mu p}=0.0138\cdot10^{-3}/^oC^2$ [2], $k_{Vtn}=1.978\cdot10^{-3}/^oC$ $k_{Vtp}=-1.86\cdot10^{-3}/^oC$, $k_{R1}= -2.84\cdot10^{-3}/^oC$, $k_{R1R1}=7.36\cdot10^{-6}/^oC^2$, $k_{R2}= 3.9\cdot10^{-3}/^oC$, $k_{R2R2}=0.01\cdot10^{-3}/^oC^2$. At 25°C, the resistors have the values $R_1=0.1M\Omega$, $R_2=39.5k\Omega$.

The transistor M_4, which at toggle beginning is very close to the saturation-region limit, having the voltage $V_{DS4}\approx0.15V$ while the saturation region limit voltage is $V_{DSsl}\approx0.15V$, comes up, for a 0.25 °C temperature variation, in the deep linear region, with the voltage $V_{DS4}=0.1V$, smaller than the saturation-region-limit voltage one, which becomes (by the increase of I_2 current and V_{GS4} voltage) $V_{DSsl}=0.4V$. For this situation, the fulfilment of the toggle condition was verified.

The conductance and resistance values were calculated for a temperature located at the middle of voltage and current jumps measured in simulation, that is, at the releasing temperature of 115°C (for typical – TYP – parameters of scheme components). The following values were obtained (see APPENDIX): $g_{m1}=3.5\mu A/V$, $g_{m3}=17.9\mu A/V$, $g_{m4}=124\mu A/V$, $r_{ds4}=0.00272M\Omega$, $R_1=0.0804M\Omega$, $R_2=0.0565M\Omega$.

With these values the open-loop voltage gain resulted:

$$A_{v1}\cdot A_{v2}=2.82>1 \qquad (10)$$

So, the toggle condition is fulfilled. By calculus has been possible to establish that the value 1 of the open-loop voltage gain is attained for a voltage $V_{DS4}\approx0.15V$ that is, at the toggle beginning, when the transistor M_4 enters the linear regime.

To simplify the numerical calculus some simulation results have been used. But, the deduction of the releasing temperature from the toggle condition in a pure analytical way is extremely complicated because all the factors implicated in this are temperature functions of first or second degree and the variables g_{m4} and r_{ds4} are strongly connected with the V_{DS4} voltage in the linear region.

The temperature relay submitted to simulation was designed for a releasing temperature of 115°C (for TYP parameters of components), closed to the maximal working temperature of numerous integrated circuits, produced on an industrial scale. The characteristic dimensions of transistors in 0.35µm CMOS process were those presented in Table 1 in µm, presuming transistors of 5V. The supply voltage was adopted $V_{DD}=3.3V$.

Table1. Transistor's dimensions

M_1	M_2	M_3	M_4
1/10	20/2	4/2	55/1

The resistor's values at 25°C were $R_1=100k\Omega$, $R_2=39.5k\Omega$ and their widths were $W_{R1}=0.45\mu m$ and respectively $W_{R2}=2.6\mu m$. The occupied-on-chip area was estimated of $600\mu m^2$.

As already shown in [5], [6] and [7], particular widths of the two used resistors are established in order to minimize the output-function variations against the process of the circuits configured by cross-connected current mirrors. Sometimes [5] the output variations against the process (which, without some special solutions is of order of tens percents [1], [2]) is reduced to a value of only few percents, at which point the component geometry (un-matching) errors begin to matter [7]. This procedure led to surprising performances of simulated circuits and even has effect in the minimization of standard deviation resulting in the Monte Carlo simulation [6], [7]. It is one of the special qualities of analog circuits with cross-connected current mirrors which use two resistors.

The principal result of the simulation, presented in Fig.4, is referred to the output voltage toggle, including the process variation (tests with *typical* – TYP, *best case* – BC and *worst case* – WC – parameters), for temperature growing sense.

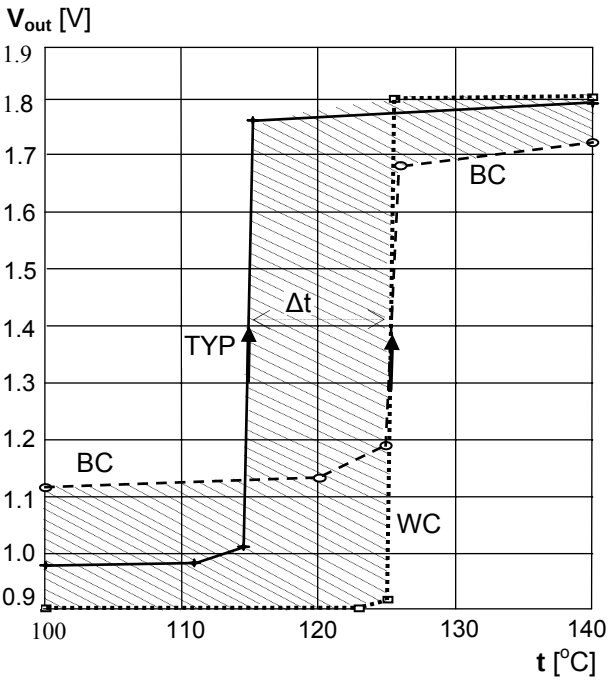

Fig. 4 Output-voltage variation with temperature and process

One can see, a relative important modification of the releasing temperature occurs in the three cases (see the hatched zone). Defining this temperature at the middle of Δt difference, measured in the middle of the voltage jump for the most unfavourable curve (BC),

one obtains a releasing temperature of 120.5±5.5°C. The total variation $\Delta t = 11^{o}C$ is measured at an output voltage level of 1.41V. The Δt-variation minimization was obtained by establishing suitable resistor widths, which assures the equality of output voltage levels for WC and BC cases, in the middle of the jump of the most unfavourable curve (BC) (fig.4).

Certainly, to achieve a better precision, it is necessary to provide a trimming operation in the manufacturing process; either a usual trimming of the R_2 or by a special circuit digitally controlled. Thanks to the Δt-error minimization, the trimming circuit will not be so much complex as the usual one included in a contemporary precision temperature sensor, with the help of which a temperature relay is configured in the present chips. The usual temperature sensors do not benefit by any minimization of process-variation (of order of tens percents) [6]. So, the trimming-control-bit quantity for the proposed relay will be smaller.

Even with such lack of precision (Fig.4), the temperature relay proposed here can have applications because of the scheme simplicity and reduced on-chip area. The improvement of the hatched zone form, firstly by the extension of the output-voltage jump for BC parameters, is possible by increasing the transistor dimensions, especially the M_4-transistor width, which is already relatively great.

The output-voltage variation against the supply voltage V_{DD} is very small, which is typical for the circuits with cross-connected current mirrors [5], [7].

The current jumps in the two branches were the following: I_1 from 0.4 to 3.35μA, I_2 from 12.4 to 21.8μA.

The form of relay characteristic is presented in fig.5, including the output-voltage variation for the temperature descending sense too, with component's TYP parameters. The hysteresis value in the zone Δt, is 22.5°C. For BC parameters this is 10°C while for WC parameters – is 32°C. It is possible, as observed in the simulation, to reduce the hysteresis by increasing the transistor areas, maintaining the W/L.

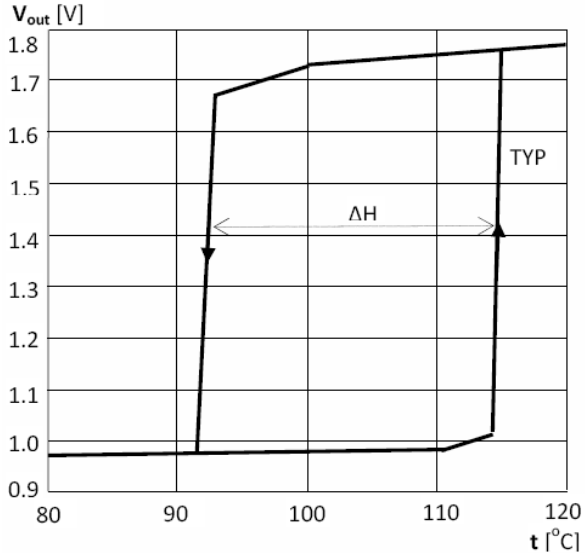

Fig.5. Hysteresis curve for TYP parameters

Another result of the scheme simulation refers to the adjusting range of the relay releasing temperature through the R_2 resistor. It is mentioned that the adjusting of this temperature can be done through the R_1 resistor too but this could lead to an important modification of the output-voltage logic levels. Fig.6 presents the variation ranges of the releasing temperature, considered in the middle of hatched zone (at the middle of Δt), as function of recommended R_2 - resistance value and having as parameter the R_1-resistance value.

In our simulation a recommended (verified) adjusting range of approximately 30°C for an adopted R_1-resistance value has been established, but this range may be extended by extrapolation of maximal and minimal recommended values for the resistance R_2.

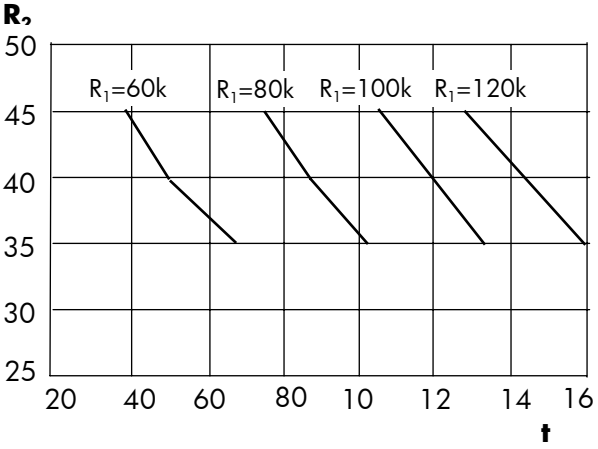

Fig.6. Releasing-temperature adjusting ranges

V. CONCLUSIONS

At present, the function of temperature relay in chips is achieved by means of a precise temperature sensor (with trimming) and a comparator circuit. These circuits have a relatively higher complexity and occupy greater area than our proposed temperature relay with trimming.

This work presents as première a temperature-relay scheme for CMOS chips, based on a simple structure of voltage source with two cross-connected current mirrors (of Wilson type and simple one), corresponding designed. Similar schemes have been proposed as temperature sensors and this led to the idea of achieving a simple temperature relay. In the proposed scheme the positive feedback is exploited, which is designed to assure, at a particular temperature, an open-loop voltage gain greater than 1, such as the circuit toggles. Its output voltage exhibits a great enough level jump to drive an interface circuit with the processing part of relay signalisation.

It was analytically established, by low-signal low-frequency positive-feedback analyses, the toggle condition which more clears up the relay function. From this, by successive trial, one can determine the relay releasing temperature.

By simulating of such a relay, conceived in 0.35μm CMOS process, the following performances were

obtained:

- minimum output-voltage jump (BC parameters): 0.54V,
- medium releasing temperature: 120.5°C,
- releasing-temperature variation against process: ±5.5°C,
- output-voltage level to act the next circuit: 1.41V,
- hysteresis value for the most un-favourable case (for WC parameters): 32°C,
- estimated on-chip area: 600μm^2.

The minimum output-voltage jump can be enlarged by increasing the transistor M_4 width while the relay hysteresis can be reduced by increasing the transistor dimensions.

The releasing temperature can be programmed in a large domain by the help of one or two resistors. Its process variation is reduced by special design procedure at a maximum value of ±5.5°C.

To achieve a better precision of the releasing temperature, it is necessary to provide a trimming operation in the manufacturing process. Thanks to the Δt-error minimization, the trimming circuit will not be so much complex as the usual one. Namely, the trimming-control-bit quantity for the proposed relay will be smaller.

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APPENDIX

The following calculus relations for mutual conductances and resistances, as temperature functions, were used. They were obtained starting from the temperature-dependence approximations of the mobility μ in [3], for 5V transistors.

$$g_{m1} = K_n' \frac{W_1}{L_1}\left(1-6.53\cdot10^{-3}t+0.0177\cdot10^{-3}t^2\right)\cdot \cdot\left[V_{GS1}-V_{tno}\left(1-1.97\cdot10^{-3}t\right)\right] \quad (11)$$

$$g_{m3} = K_p' \frac{W_3}{L_3}\left(1-5.43\cdot10^{-3}t+0.0148\cdot10^{-3}t^2\right)\cdot \cdot\left[V_{GS3}-V_{tpo}\left(1-1.86\cdot10^{-3}t\right)\right] \quad (12)$$

$$g_{m4} = K_p' \frac{W_4}{L_4}\left(1-5.43\cdot10^{-3}t+0.0148\cdot10^{-3}t^2\right)V_{DS4} \quad (13)$$

$$r_{ds4} = \frac{1}{K_p' \frac{W_4}{L_4}\left(1-5.43\cdot10^{-3}t+0.0148\cdot10^{-3}t^2\right)}\cdot \cdot\frac{1}{\left[V_{GS4}-V_{tpo}\left(1-1.86\cdot10^{-3}t\right)-V_{DS4}\right]} = \quad (14)$$

$$= \frac{V_{DS4}}{g_{m4}\left[V_{GS4}-V_{tpo}\left(1-1.86\cdot10^{-3}t\right)-V_{DS4}\right]}$$

Thus, the product $g_{m4}r_{ds4}$ becomes:

$$g_{m4}r_{ds4} = \frac{V_{DS4}}{V_{GS4}-V_{tpo}\left(1-1.86\cdot10^{-3}t\right)-V_{DS4}} \quad (15)$$

$$R_1 = R_{1(25)}\left[1-2.8410^{3}(t-25)+7.3610^{6}(t-25)^2\right] \quad (16)$$

$$R_2 = R_{2(25)}\left[1+3.910^{-3}(t-25)+0.0110^{-3}(t-25)^2\right] \quad (17)$$