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Modeling and Evaluating the Electrostatic Discharge Current Pulse Using the Transmission Line Pulse Method Test

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Abstract – This paper investigates the effects of the electrostatic discharges (ESD) in the circuit industry and characterizes the performance of a protection system under the action of the ESD stresses.

The ESD model most used in characterizing the effects of the ESD discharges on semiconductors is the Transmission Line Pulse (TLP). In the process of dealing with the failures of semiconductor devices, were evaluated the input/output current pulses of an inverter structure, in order to estimate the built-in reliability versus ESD events.

Keywords: inverter, Transmission Line Pulse (TLP), Electrostatic Discharge (ESD), protection circuit design

I. INTRODUCTION

Nowadays, the electrostatic discharge (ESD) phenomenon has become a great threat to all semiconductor devices regarding the high vulnerability of the circuits, to the high currents and voltages.

An important challenge in semiconductor ICs refers to a significant increase in the costs of microelectronic circuits due to the scaling process [1-2]. The advent of the scaling technologies has been one of the leading causes of the circuit failures.

The smaller geometry devices are more susceptible to ESD events. In this process, the devices are exposed to excessive currents up to 30 A of fast rise times (nanoseconds).

Taking into consideration that the semiconductor devices are manufactured using silicon materials, the over-currents or the over-voltages may cause permanent damages. The damage of the device depends mainly, on the intensity of the discharge. The high currents applied to the electronic devices may lead to thermal breakdown and even destruction of the device. The breakdown of the gate oxide in CMOS technologies represents one of the most important issues related to the ESD events. Preventing ESD and avoiding the semiconductor failures can be realized by introducing protection systems.

The concept of implementing protection consists in reducing the high voltages applied to the MOS gate and diverting the currents to safe levels [3]. An efficient protection circuit design should be capable to resist to different types of ESD events, without being damaged. Therefore, proper corrective actions were taken into consideration in order to implement efficient ESD protection models.

This study presents the work that has been performed in order to illustrate the proximity effects of the ESD events on a CMOS structure. The tests were realised using the Transmission Line Pulse (TLP) ESD method, for a 15 kV level, using Cadence Software Programme IC 5.3.

II. TRANSMISSION LINE PULSE ELECTROSTATIC DISCHARGE TEST METHOD

Recently, new standards were defined in order to guarantee repeatable, reproducible and meaningful results of ESD system level stress of ICs [4].

Today, one of the methods used in terms of observing and testing the electrostatic discharge events is the Transmission Line Pulse (TLP). The TLP test model represents a powerful tool used by the designers to characterize the behaviour of the semiconductor devices.

In TLP tests, a high voltage source charges the transmission line to a certain voltage which later is discharged into the pins of a test device, *DUT*, resulting a square current pulse (Fig. 1).

The role of the attenuator consists in preventing the distortion of the signal. If the attenuator is removed then the current pulse is reflected to the *DUT* and back to the power supply, where it finds a high impedance source. Further, the current pulse is reflected back again to the transmission line and back to *DUT*, with polarity inverted. The attenuator also decreases the amplitude, 10 times.

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In Fig. 1 is shown the representative schematic of the TLP method.

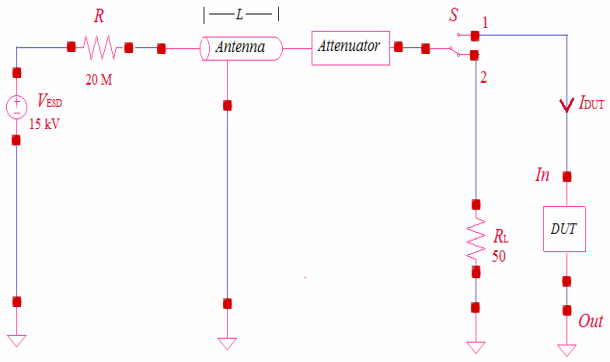

Fig. 1. The circuit diagram for the Transmission Line Pulse Model

In literature, the most commonly accepted electrostatic discharge current waveform is the one set by IEC 61000-4-2 standard.
The corresponding waveform of the TLP will differ from the standardized ESD waveforms [5].
The TLP test technique provides a number of pulses with controlled amplitude and time length, generating square waveforms. The characteristic waveform of the TLP test illustrates the basic failure mechanisms of the integrated circuits due to the ESD phenomenon.
The high voltage source of 15 kV, V_{ESD}, controls the waveform amplitude, while the pulse duration is set by the L transmission line length.
Typically, ESD circuit designers have used TLP pulses with widths between 75 ns and 200 ns [6].
Martin Rowe highlights in the paper "TLP testing gains momentum" that the best correlation between energy in a TLP test pulse and that of a 150 ns Human Body Model (HBM) ESD test standard pulse, occurs for a 80 ns TLP test pulse width [7].
The waveform of the TLP test method implemented for a pulse width of 80 ns is illustrated in Fig. 2.

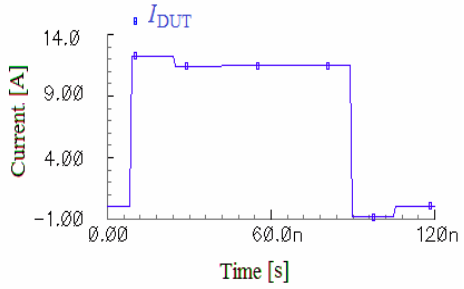

Fig. 2. The Characteristic Waveform of the Transmission Line Pulse Model

Knowing that the length of the transmission line sets the pulse length, in order to get 80 ns pulse it's necessary to have 8 m of cable.
The rise and fall times play also an important role in characterizing the TLP tests. In TLP testing, the rise/fall times should be comparable with the standard values of the HBM ESD tests (values between 2 and 10 ns [7]).
In order to stress the devices under harsher conditions than the standard ones, the analyses were made for rise and fall times of 300 ps. In these terms, the peak current produced by simulating the TLP test method was evaluated to 12.7 A.

III. DESIGN CONSIDERATIONS REGARDING THE CMOS INVERTER STRUCTURE

Over more than 20 years, in electronic applications, circuits based on transistors MOSFET have captured the interest of the designers. In terms of failure, the MOS field transistors have been reported with poor ESD reliability [8].
As represented in the inverter structure (Fig. 3), the CMOS structure combines PMOS pull-up transistors and NMOS pull-down transistors.

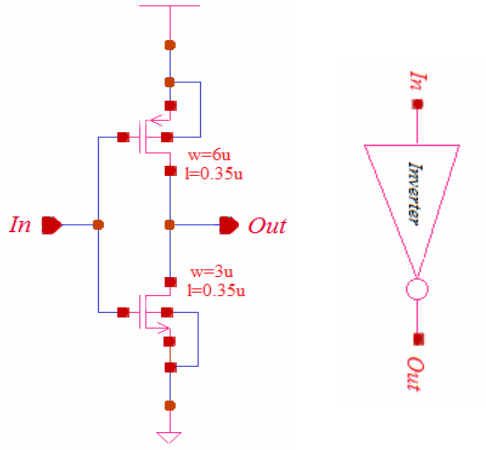

Fig. 3. The schematic and the corresponding symbol of the CMOS Inverter structure

In Fig. 4 are represented the input/output voltage pulses of a CMOS inverter. These waveforms illustrate the functionality of the CMOS inverter structure in terms of applying a voltage of 3.3 V, on the circuit input. In these tests were used pulses having a period of 20 ns duration and rise/fall times of 1ns.

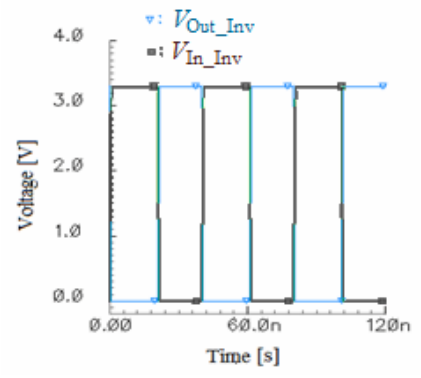

Fig. 4. The CADENCE simulated waveforms of the CMOS Inverter cell

IV. ANALYSIS OF THE TRANSMISSION LINE PULSE DISCHARGE MODEL ON THE CMOS INVERTER STRUCTURE

The Transmission Line Pulse testing provides the ability of understanding the semiconductor device,

circuit and chip response to the high current pulses [9]. The TLP testing method provides an accurate visualization of the semiconductor device response.
In this paper, as device under test was implemented a circuit with semiconductor components, a CMOS inverter structure (Fig. 5).
Initially, the tests were performed using a 80 ns TLP pulse. Further, in the paper, the simulations were made for a TLP pulse width of 20 ns. A shorter TLP pulse was used in order to better simulate the short ESD pulse threats.
The integrity of the CMOS structure was evaluated by the TLP test method having a transmission line of 2 m length.

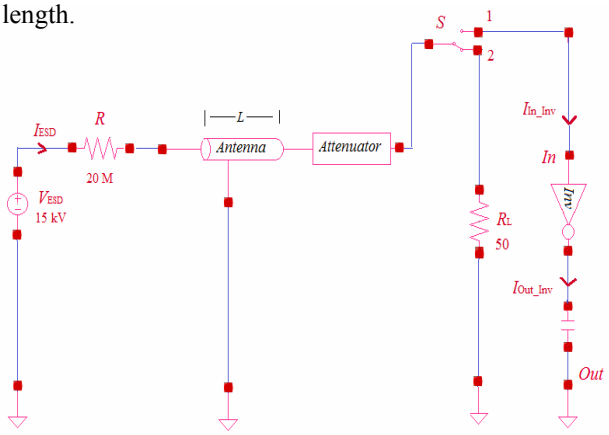

Fig. 5. TLP test model applied on the CMOS Inverter structure

The output current waveform of the inverter (Fig. 6) illustrates the device degradation. The high voltage of 15 kV delivers enough power to stress the CMOS inverter cell. The rising edge of the ESD voltage, applied using the TLP test model, has a major impact on the functionality of the CMOS Inverter implying dangerous leakage flows through circuit.

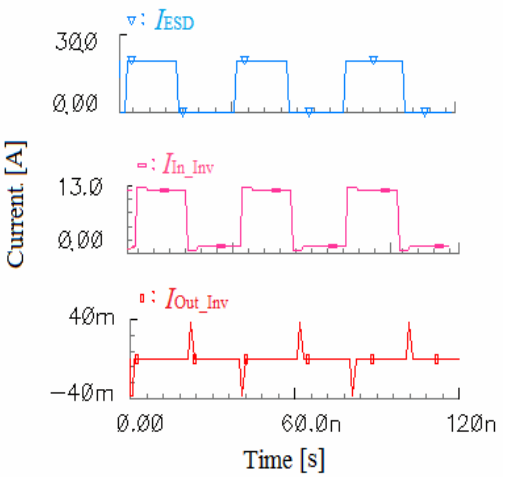

Fig. 6. The CADENCE simulated current waveforms of the CMOS Inverter during the TLP ESD test

From this point of view, ESD damage represents a critical issue in CMOS technologies, mainly due to the increased sensitivity of the n-channel (nMOS) and p-channel (pMOS) transistors.

The high peak current of 13 A applied at the input of the inverter determines the malfunction of the circuit, fact observed in the altered output waveform.

V. TLP TEST INTEGRITY OF PROTECTIVE CIRCUITRY

In the process of avoiding the circuit damage caused by the ESD events it is essential to take protective measures. In our case, a protection circuit is required to be applied at the input of the CMOS Inverter structure in order to protect the gates of MOS transistors.
A circuit able to protect the inverter against ESD events is represented in Fig. 7.

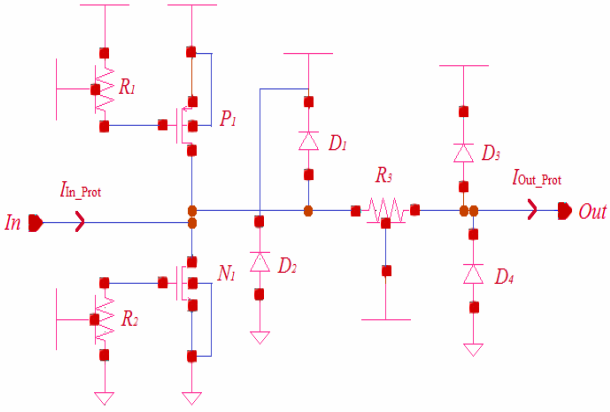

Fig. 7. The schematic of the ESD protection circuit designed for a CMOS Inverter structure

The protection structure is implemented using the gate coupling technique, a method that reduces the overstress voltage and protects the ultrathin gate oxide of the transistors [10, 11]. To sustain the high ESD peak current, the N_1 and P_1 transistors are designed having large dimensions: 1200 µm /0.35 µm and 450 µm /0.35 µm.
The input resistors R_1 and R_2 of 25 kΩ limit the ESD current flow. The resistors restrict the voltage implied by an ESD event and have no effects in the normal operation of the circuit. To assure a better current capability, are used diffused resistors.
In literature, different protection designs are implemented using pure diodes, mainly due to the smaller parasitic effect, being more suitable than the ESD protection designs with MOS devices [12].
In the circuit modeled in Fig. 7, are used clamping diodes, as protective components. The clamping diodes D_1 and D_2, D_3 and D_4 have a fast response time and a high capacity to handle the ESD peak currents. Hereby, these components have the ability of remaining undamaged during repetitive ESD events. The resistor R_3 (20 kΩ) limits the leakage current flowing throw the circuit.
The role of the clamping diodes: D_3 and D_4 consist in shunting the high ESD transient current, to the power supply lines: VDD or GND.
The entire circuit described above, is introduced in Fig. 8 in order to reduce the excessive currents.

The tests were performed for a period of time of 120 ns. In Fig. 9 are illustrated the TLP analysis on the CMOS inverter structure in case of assuring the protection of the device.

The ESD applied voltage of 15 kV implies a corresponding value of 30 A for the discharge peak current. The load resistor *R* of 20M and the attenuator yields a current of 13 A to the input of the test device. As can be noticed in the waveforms represented in Fig. 8, the output current of the protection circuit (I_{Out_Prot}) reaches a value of 3 A, meaning that, the protection device assures a current limitation.

The waveforms corresponding to the input of the protection circuit and the input of the inverter reveal a drastically current decrease of 10%. In these conditions, for a 3 A applied on the input, the inverter circuit considered, fulfills its characteristic functions.

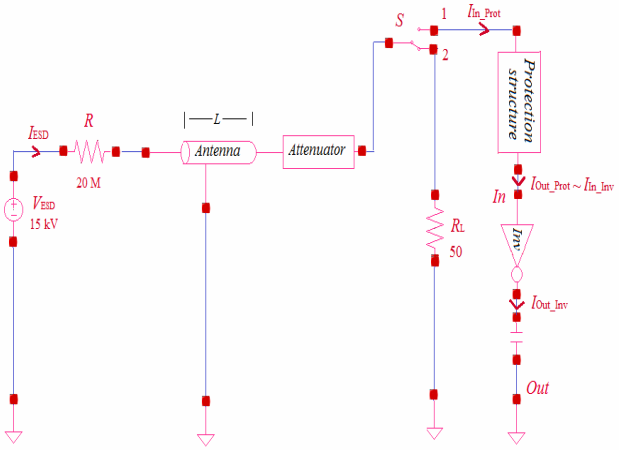

Fig. 8. TLP test model evaluating the efficiency of the protection circuit

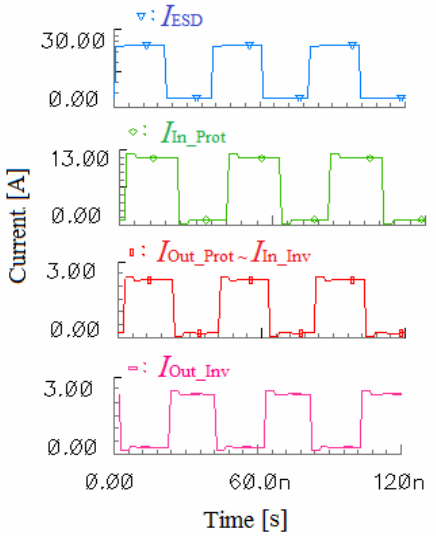

Fig. 9. The transitions of the current waveforms in evaluating the efficiency of the protection circuit

IV. CONCLUSIONS

This study aims to improve the level of understanding of the transistors behaviour in dealing with ESD events.

The effects of the ESD events were investigated using the Transmission Line Pulse test method on a CMOS Inverter circuit.

The failures observed during the tests highlight the importance of using protection structures. Various differences were noticed in the current waveforms in the case of using protection and without using it. The protection structure was implemented and tested in order to alleviate the ESD effects: to divert and limit the high currents. The protective circuit was designed taking into consideration the performances and limitations of the circuit components.

The TLP ESD tests were realized using a 0.35 µm CMOS technology.

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