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A Digital Method for Obtaining High Accurate Clock Reference Using GPS-Disciplined VCXO

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Abstract- This paper will preset the digital part of a GPS based synchronization scheme developed for WiMAX base stations. The PPS obtained from the GPS receiver will discipline the VCXO oscillating frequency. The accuracy of the clock reference will be bounded by the PPS jitter. A digital method for reducing the PPS jitter will be described. Also a controlling algorithm of the VCXO when the PPS signal is lost will be presented. The digital part of the scheme will be implemented on FPGA.
Keywords: GPS, synchronization, PPS, jitter.

I. INTRODUCTION

In communications systems using TDD, appropriate time synchronization is critically important. In order to avoid inter-cell interference, all base stations must use the same timing reference. One solution to this problem is the Global Positioning System (GPS). The users can receive accurate time from atomic clocks and can generate themselves synchronization signals. Commonly the GPS receiver generate a Pulse per Second (PPS) signal and, optionally, a 10 MHz signal, phase synchronized with the PPS.

All the transmission over the radio channel, both on downlink and uplink, should be synchronized with the PPS signal. The RP1 synchronization burst generator, called Clock Control Manager (CCM) shall provide frame timing and time stamping for each of the air interface systems independently. The quality of the PPS signal will dictate the periodicity of these synchronization bursts.

Also, algorithms for maintaining the stability of the clock reference, which can be affected by the temperature variance or by aging, can be developed based on the PPS signal. It is obvious why the PPS jitter level is a critical parameter in obtaining high synchronization performances.

This document will describe the digital method used for PPS de-jittering and the VCXO oscillating frequency controlling algorithm.

II. CLOCK REFERENCE CONTROLLING SCHEME

The controlling scheme is a hybrid one, using both analog and digital elements. The scheme is depicted in Fig. 1. In this application, the PPS input is sourced by a low cost GPS receiver called Resolution T, produced by Trimble.

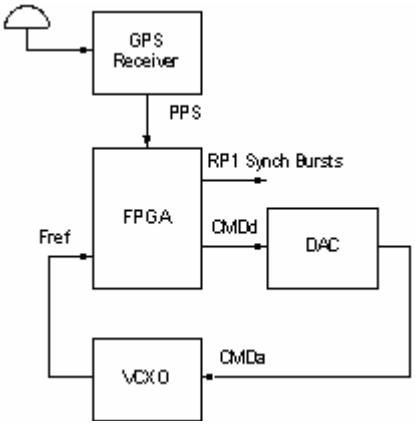

Fig.1 Controlling scheme

The scheme works as follows: the Field Programmable Gate Array (FPGA), which is a XC3S500E chip representing a Spartan 3E family member produced by Xilinx, increments a counter value on every F_{ref} rising edge and resets this counter on every PPS pulse. Let's consider the nominal frequency F_{ref}^{n} and the counter value at a time instant $count\_val$. When a new PPS pulse is received from the GPS module, before the counter reset, his value is stored and compared with F_{ref}^{n}. If the two values are not equal, the digital bloc computes a digital command CMD_d that is converted into a voltage level by a Digital to Analog Converter (DAC). The analog command CMD_a controls the VCXO and the value of F_{ref} is changed accordingly.

As it was mentioned before, the PPS jitter can produce VCXO commands that are unnecessary or imprecise. That's way the PPS signal from the GPS receiver is passed through a digital de-jittering block before it is used by the controlling algorithm and by the CCM. The bloc scheme of the digital part of the structure described in Fig. 1 is depicted in Fig. 2.

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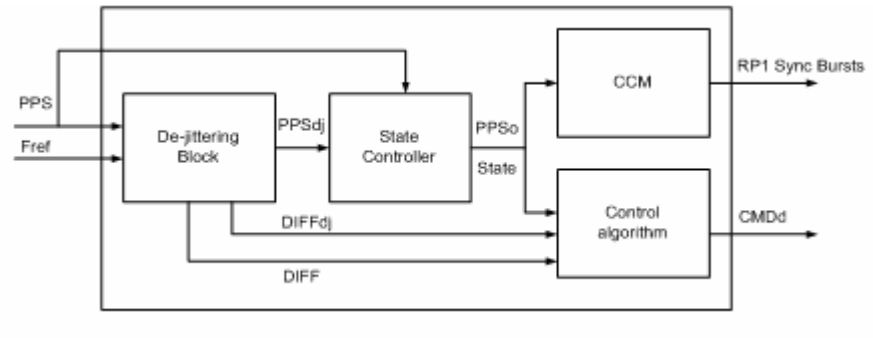

Fig. 2 The bloc scheme of the digital part

A. *The de-jittering block*

The PPS jitter characteristics are to be presented now. Fig. 3 depicts the time instant value of the jitter. One can see from this figure that the PPS jitter is in the range $\pm 20ns$ for the selected GPS receiver. Also is easy to observe that it does not have uniform distribution. For this reason a simple mean will not eliminate the jitter problem (see Fig. 4).

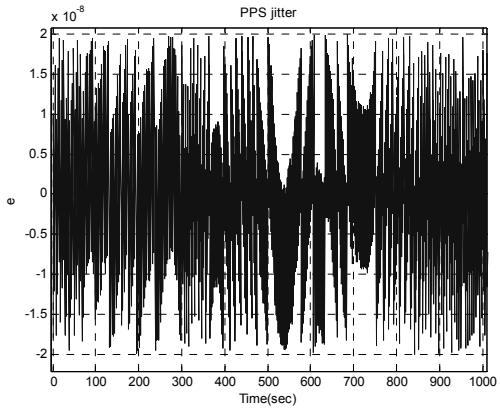

Fig. 3 PPS jitter

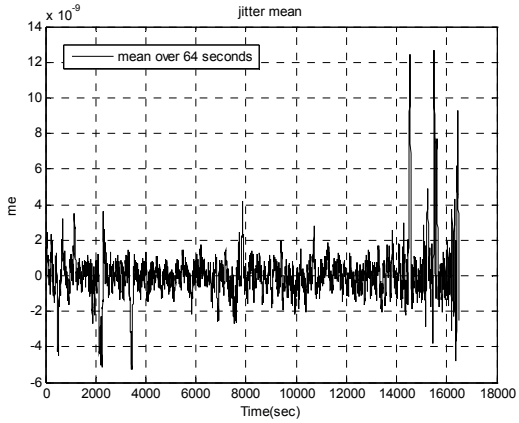

Fig. 4 PPS jitter mean

Fig. 5 depicts the Allan deviation. For all of these measurements, it is assumed that the function $e(t)$, representing the time error (the deviation from 1 second value), is sampled with N equally spaced samples, $e_i = e(i\tau 0)$, for $i = (1, 2, ..., N)$, and with a sampling interval $\tau 0$ of 1 second. The observation interval, τ, is given by $\tau = n\tau 0$. The Allan deviation is computed using equation 1:

$$ADEV(n\tau_0) = \sqrt{\frac{1}{2n^2\tau_0^2(N-2n)}\sum_{i=1}^{N-2n}\left(e_{i+2n} - 2e_{i+n} + e_i\right)^2} \quad (1)$$

where $n \in \left(1..\left\lceil \frac{N-1}{2} \right\rceil\right)$

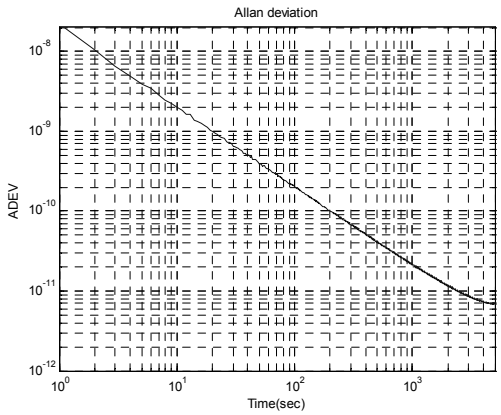

Fig. 5 PPS jitter Allan deviation

The slope of $ADEV(\tau)$ is τ^{-1}, which corresponds to white noise phase modulation and flicker phase modulation [1].

The de-jittering block contains a discreet-time Kalman filter. We will consider a particular algorithm of one-dimension Kalman filter intended for frequency estimation only in oscillators if GPS timing signals are used as the reference ones [2]. As it was mentioned before, on every PPS pulse we compute:

$$DIFF(n) = count\_val(n) - F_{ref}^n \quad (2)$$

If the oscillator frequency is F_{ref}^n then *DIFF(n)* will reflect only the PPS jitter. If not, the *DIFF(n)* will contain the frequency deviation also. These values, computed every second, are used as the Kalman filter input.

Using the notations Q for process variance and R for estimate of measurement variance, the de-jittering algorithm is as follows:

Initialization

$$\tilde{x}(1) = 0; \qquad (3)$$
$$P(1) = 1;$$

$$\begin{aligned}
&for\ n = 1 : N \\
&(Time\ update) \\
&\quad \tilde{x}_{-}(n+1) = \tilde{x}(n) \\
&\quad P_{-}(n+1) = P(n) + Q \\
&(Measurement\ update) \\
&\quad K(n+1) = P_{-}(n+1) / \left(P_{-}(n+1) + R\right) \qquad (4) \\
&\quad \tilde{x}(n+1) = \tilde{x}_{-}(n+1) + \\
&\qquad K(n+1)\left(DIFF(n) - \tilde{x}_{-}(n+1)\right) \\
&\quad P(n+1) = \left(1 - K(n+1)\right) P_{-}(n+1) \\
&end
\end{aligned}$$

The *DIFFdj* signal from Fig. 2 is the filter output, i.e. $\tilde{x}(n)$, and it is used to compute the digital command for the VCXO. Also, the de-jittering block provides a de-jittered PPS pulse, denoted *PPSdj* which should have a 1 second period.

B. *State Controller*

Some times, due to the lack of visibility, the GPS receiver might not transmit the PPS pulse. This situation should be detected by the State Controller by expecting the PPS pulse within a time window. This window depends on the oscillator stability. If the oscillator has a $\pm 25\,ppm$ variation within the temperature range and a nominal frequency of 153.6 MHz, then the maximum delay of the PPS pulse can be $153.6e6\ x\ 25e-6 = 3840$ clock periods, i.e. the PPS pulse can be found after the previous one at $153.600.000 \pm 3840$ clock periods. If it is not so, the State Controller block confirms the absence of the PPS pulse.

The Finite State Machine (FSM) of the synchronization block is depicted in Fig. 6. The four possible states are:

- IDLE: when the synchronization block waits for the first PPS
- TRAINING: when the synchronization block starts the Kalman filtering and waits T_{TR} seconds in order to obtain a stable output
- NORMAL: when the synchronization block works based on PPS pulses received form the GPS module
- HOLD OVER: when the PPS pulse is not received from the GPS module and the synchronization block works based on local PPS pulse.

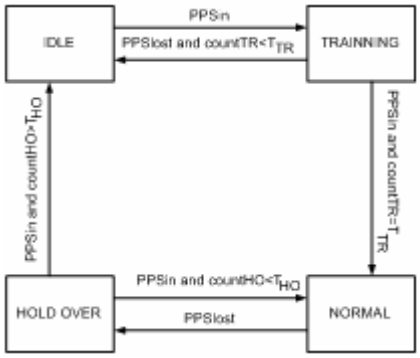

Fig. 6 FSM for synchronization block

After the first PPS received, the synchronization block switches from IDLE to TRAINNING. In TRAINING, a counter called *countTR* is incremented on every PPS pulse. If the counter value equals the T_{TR} parameter, then a transition is made in NORMAL state. Else, if the block declares the absence of the PPS pulse and the counter value is less than T_{TR} then the new state becomes IDLE.

When the FSM is in NORMAL state and the PPS is declared to be absent, a transition to HOLD OVER state is made. In this state, from the last PPS pulse received, a counter is started in order to generate an internal PPS pulse. Also, a counter called *countHO* is incremented on every local PPS pulse, counting the number of successive absent external PPS pulses. If this counter reaches T_{HO} parameter the synchronization bloc state becomes IDLE. Else, if a new PPS pulse is detected before the counter reaches the T_{HO} value, the synchronization block returns in NORMAL state.

The values of the FSM parameters are given in table 1.

Table 1. FSM parameters

Parameter	Value	Unit
T_{TR}	192	sec
T_{HO}	Depending on VCXO	sec

C. *Control Algorithm*

The Control Algorithm block receives the Kalman output and the state of the synchronization block. It also receives the Kalman input, as one can see from Fig. 2. The control algorithm should compute the VCXO command. The DAC has a 16-bit input, so 2^{16} values are used to control the range of the VCXO. For a measured frequency deviation of $\pm 16\,ppm$, result a control step of:

$$\Delta f = \frac{153.6e6\,x\,32e-6}{2^{16}} = 0.075\,Hz \approx \frac{1}{13}\,Hz \qquad (5)$$

The *CMDi* signal used as feedback for the controlling loop is selected as described in Fig. 7. The *DIFF* and *DIFFdj* are expressed in clock periods per second and so the DAC value is computed as:

$$CMD_d(k) = CMD_d(k-1) - 13CMD_i \qquad (6)$$

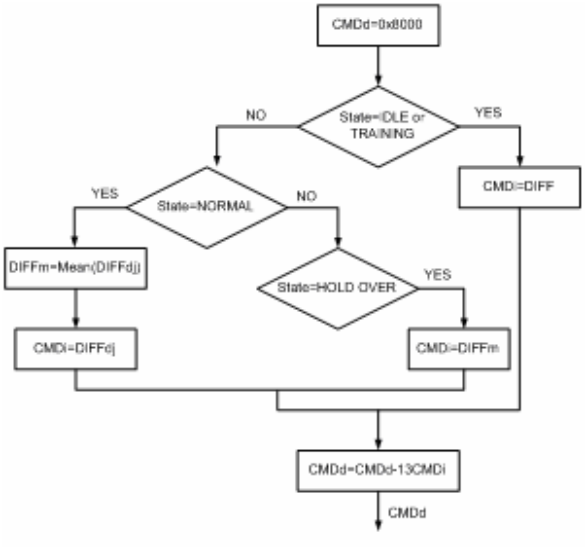

Fig. 7 Control Algorithm

The starting value is the central level of the DAC range, i.e. 2^{15}. In order to obtain a faster convergence, the starting value might be a DAC value saved when the synchronization block was in NORMAL state.

When the State Controller indicates IDLE or TRAINING the oscillator is controlled directly with the measured frequency deviation, in order to achieve fast convergence. In NORMAL state, the Kalman output is used for jitter reduction. The *DIFFdj* signal has a floating point format, so that frequency corrections less than 1 Hz can be produced. Also the mean of the N_m last values of *DIFFdj* signal is computed. The mean value is used when the State Controller is in HOLD OVER state and no valid *DIFFdj* values are received. Also this value is maintained for $T_{HO\text{-}N}$ seconds when the synchronizations state returns from HOLD OVER state to NORMAL state, in order not to produce de-synchronization due to the new position of the PPS pulse.

The values of the Control Algorithm parameters are given in table 2.

Table2. Control Algorithm parameters

Parameter	Value	Unit
N_m	128	
$T_{HO\text{-}N}$	2	sec

III. EXPERIMENTAL RESULTS

The VCXO oscillating frequency is affected by the temperature variations. The controlling algorithm should provide commands fast enough not to accumulate frequency deviations. This problem is observed at the start up too. Even if the temperature is stable, the oscillator is not in a stable thermal state and the algorithm should provide frequency corrections. Fig. 8 depicts the mean of the DAC commands, considering 0x8000 value as the reference. One can see that at start-up the oscillator has a significant frequency drift and although the temperature variation, depicted in Fig. 9, is not important, the frequency deviation is about 10Hz per 9000 seconds.

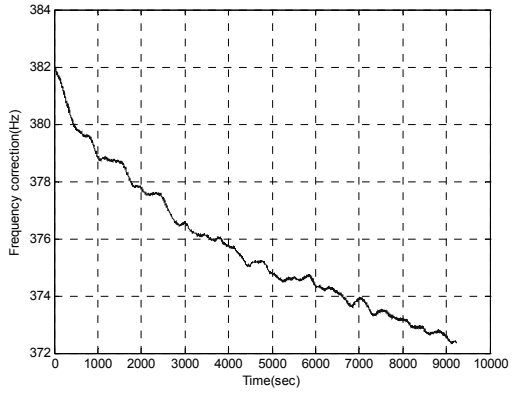

Fig. 8 Mean of frequency deviation

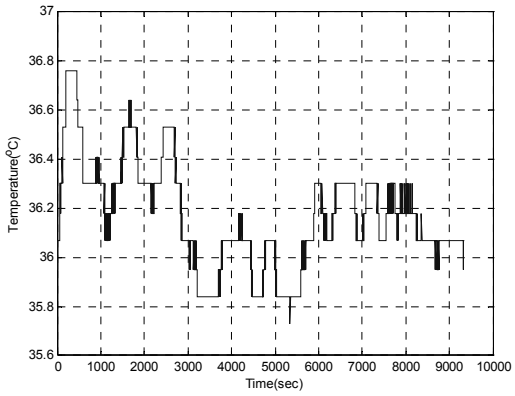

Fig. 9 Temperature variation

Fig. 10 depicts the deviation measured at the input and of the Kalman filter, while Fig. 11 depicts the deviation measured at the output of the Kalman filter One can see that the initial deviation is the jitter level ($\pm 20ns \, x \, F_{ref} \approx \pm 3$ clock periods) plus some temperature randomly added deviation. At the output of the de-jittering structure, the level of the jitter is much lower.

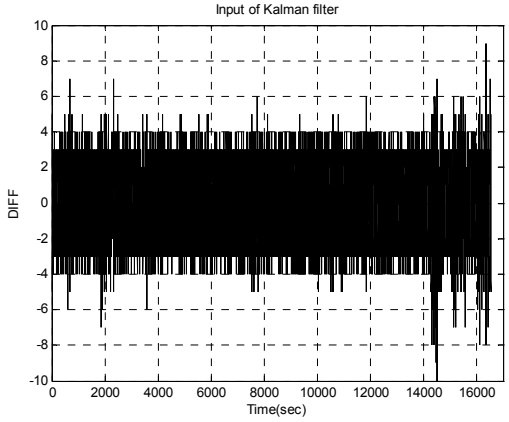

Fig. 10 DIFF values in clock periods

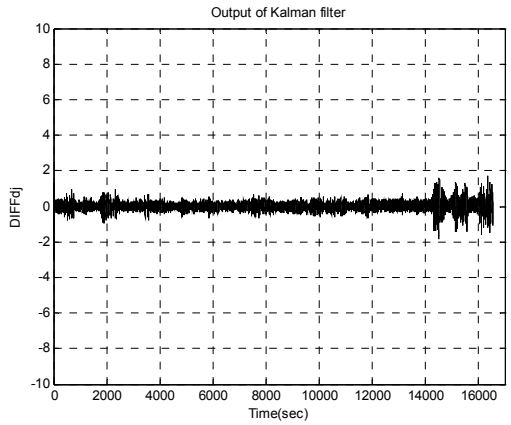

Fig. 11 DIFFdj values in clock periods

Fig. 12 and Fig. 13 depicts the deviation measured at the input and output of the Kalman filter while a frequency deviation of 1 Hz per second was added for 500 successive seconds and subtracted for the next 500 seconds. One can observe that the *DIFFdj* signal indicates the need of about 1 Hz reduction of the oscillating frequency for the first 500 seconds and then the need of about 1 Hz adding for the next 500 seconds.

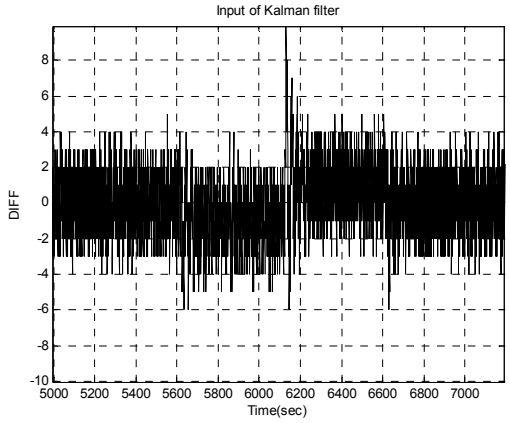

Fig. 12 DIFF values in clock periods

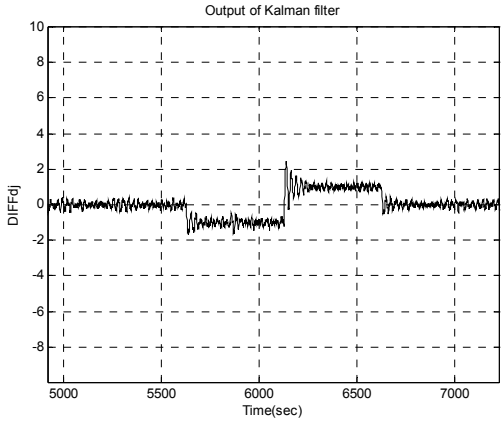

Fig. 13 DIFFdj values in clock periods

The results presented in this section were obtained using a hardware platform compliant with Fig. 1. The inputs and the outputs of the algorithm were transferred to the PC using a UART interface. The pictures were obtained using Matlab.

IV. CONCLUSIONS

This paper presented a digital method of reducing the jitter level of the PPS signal generated by a GPS receiver. Also a controlling algorithm of a VCXO oscillating frequency was described. The results indicated that the frequency correction was applied only when the thermal state of the oscillator was not stable. False corrections due to the PPS jitter were almost completely eliminated.

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