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Electrically tunable CMOS Biquad Cells Implementation of High-Order Filters

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Abstract – This paper presents a new design approach which generates high-order electrically tunable HF IC-compatible filters. The realized circuits are composed only from CMOS linear transconductance elements and grounded capacitors. We propose a new CMOS universal multiple inputs biquad filter cell, which permits independent electric controls of filter parameters. Several of these biquad cells are incorporated in a low-sensitivity coupled-biquad structure in order to realize an active HF filter. This structure implements a node-voltage simulation of an equivalent LC ladder passive filter. A fifth-order lowpass filter is simulated with the end to demonstrate the performances of CMOS linear transconductors in the achievement of HF high-orders filters.
Keywords: CMOS technology, active biquads, active filter synthesis.

I. INTRODUCTION

The current trend is to put complete signal processing systems consisting of analog and digital circuitry on IC chips. Therefore, the designs must be electronically tunable and should be compatible with the dominant IC technology. In high-frequency continuous-time integrated filter design, one of most successful approach uses CMOS transconductors and grounded capacitors. For CMOS processes, transconductance-capacitor designs are particularly useful, since both types of components are easily to implement in this technology [1]-[3]. In these cases, the gain of transconductors g_m is used as a design parameter in the same way as the R's are used in conventional active-RC filters. The main advantage of using g_m as a design parameter is that it can be varied or programmed by an external controlling voltage. Section II of the paper introduces the CMOS linear transconductor and Section III describes some basic blocks of circuits composed of transconductors and grounded capacitors

This paper main goal is to investigate the CMOS transconductor capability to implement HF high-order active filters. As prototypes for active filters, we use passive double loaded ladder networks because their low sensitivity is preserved by an active implementation. The simulation method employs coupled-biquad filter cells in order to implement mesh equations of the passive network, a procedure well-documented in our previous papers [4] and [5]. In this case, each biquad cell implements the currents equations that take place in one of circuit meshes. With that end in view, an important effort was done to establish an optimal CMOS transconductance-capacitor biquad cell that suits best to coupled-biquad applications. Therefore, an optimal CMOS biquad has multiple inputs action, realizes all types of filtering functions and contains only CMOS linear transconductors and grounded capacitors. The CMOS transconductance-capacitor biquad cell presented in Section IV fulfils all these requirements and besides, it permits independent controls of biquad parameters, while Section V recalls the principles of coupled-biquad simulation of passive ladder filters.

In order to validate the design procedure of CMOS coupled-biquad filters, Section VI implements the project of a CMOS coupled-biquad elliptic fifth-order lowpass filter. SPICE simulations using 0.35μm CMOS process is used to validate the theoretical models proposed in the paper. The possibility of independent controls of filter characteristics through tuning voltages is well-documented and demonstrated in this Section.

II. THE CMOS LINEAR TRANSCONDUCTANCE ELEMENT

The simplest voltage-to-current (VCT) transducer implemented in CMOS technology is the well-known CMOS inverter. As shown by experiment and simulation, the inverter has excellent frequency response and very low distortion; however, its power supply rejection (PSR) is poor and the linear behavior depends critically on the matching between the p-channel and n-channel transistors; i.e., the parameter $\mu_{eff} C_{ox} W/L$ must to be the same for both transistors. The MOS parameters in the previous expression have their usual meaning. Unfortunately, the effective mobilities μ_{eff} of electrons and holes depend on doping, bias voltages, and temperature so perfect matching is difficult to achieve in practice. The solution of this

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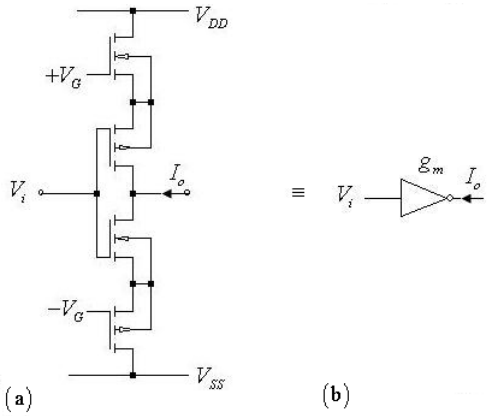

Fig. 1. The CMOS linear tunable transconductance (a) circuit implementation, (b) circuit symbol.

problem is the four-transistor CMOS transconductance element proposed in [2] and [3], whose operation resembles in most respect that of the CMOS inverter but without having PSR or matching problems. The circuit, which is shown in Fig. 1, has the additional advantage of tunability.

With all transistors in saturation ($V_{DS} > VGS - V_{Tn}$; $V_{SD} > V_{SG} - |V_{Tp}|$ for n- and p-channel devices respectively), the transconductance realized by the circuit in Fig. 1(a) is [2]:

$$g_m = 2k_{eff}\left[2V_G - \left(V_{Tn1} + V_{Tn3} + |V_{Tp2}| + |V_{Tp4}|\right)\right]. \quad (1)$$

where:

$$k_{eff} = \frac{k_n k_p}{\left(\sqrt{k_n} + \sqrt{k_p}\right)^2}, \quad (2)$$

and

$$k_{n,p} = 0.5\left[\mu_{eff} C_{ox} W/L\right]_{n,p}. \quad (3)$$

It must be observed that g_m is tunable by changing gate voltages $\pm V_G$, as Fig. 2 shows. The dependency between the output current of CMOS element, I_o and the input voltage of the cell, V_i is quite linear, especially for $V_G \le V_{DD}$.

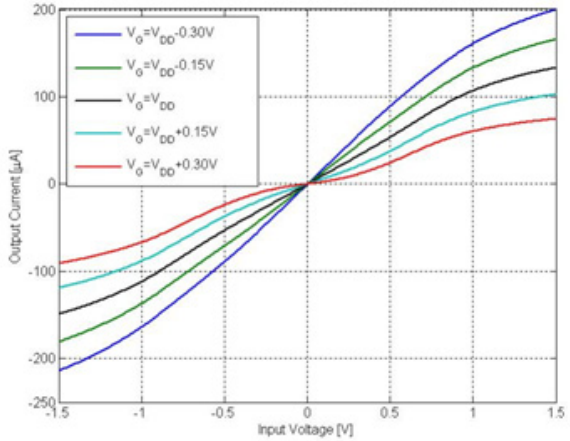

Fig. 2. The static characteristics of a CMOS transconductance element.

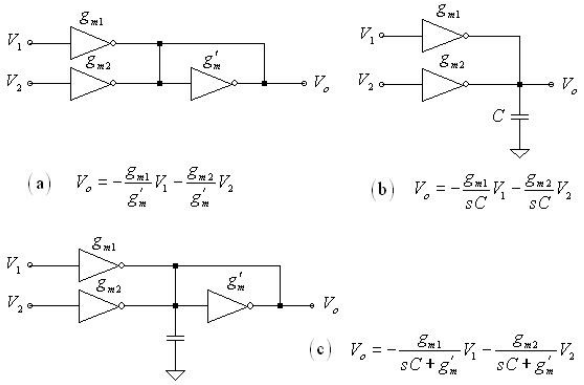

Fig. 3. Basic blocks of CMOS transconductor circuits: (a) Voltage amplifier/adder, (b) Voltage integrator and (c) First-order filter.

III. BASIC BUILDING BLOCKS OF CMOS TRANSCONDUCTANCE CIRCUITS

The CMOS linear transconductors represented in Fig. 1(a) is an inverting transconductor, being symbolized in Fig. 1(b). Because in general, both positive and negative transconductances are needed, the suitable realization and the symbolic representation of a non-inverting transconductor are given in Fig. 3(a) and (b). A remark must be made on the first two stages in Fig. 3(a) which implement a voltage inverter with the second element being a grounded resistor of value $1/g'_m$.

The circuits in Fig. 1 and Fig. 3 are used to build up the basic CMOS transconductance circuit blocks in Fig. 4. Joining together on a grounded admittance Y the outputs of many inverting transconductors $g_{m1}, g_{m2}, \ldots$ and expressing their input voltages by $V_1, V_2, \ldots$, the output voltage V_o of this circuit is written as

$$V_o = -\frac{g_{m1}}{Y}V_1 - \frac{g_{m2}}{Y}V_2 - \ldots \quad (4)$$

The ideal voltage amplifier and integrator correspond to $Y = g'_m$ and $Y = sC$, respectively (see Fig. 4(a) and (b)). The voltage addition is realized simply by connecting together many CMOS elements outputs as is shown in Fig. 4(a).

To obtain a first-order lowpass filter, the same simple circuit is used but in this case, the admittance connected at the output of circuit in Fig. 4(c) becomes $Y = sC + g'_m$.

IV. CMOS BIQUAD MULTIPLE INPUT FILTER CELL

A convenient CMOS transconductance-capacitor biquad filter cell is a two-input device able to perform second-order functions with identical poles but different zeros regarding the inputs. The CMOS biquad itself may not have the simplest structure, viewing the necessity to provide an independent tuning of parameters ω_o and Q. To build this cell, we use a distributed-feedback (DF) two-integrator

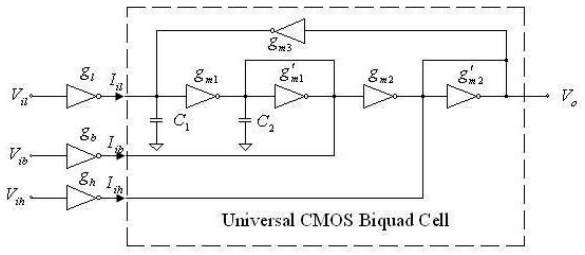

Fig. 4. Multiple input, single output, CMOS universal biquad filter cell.

loop structure [6], [7]. Fig. 4 presents the resulting circuit.

Strictly speaking, the basic biquad cell works a current-voltage converter between the input nodes I_{il}, I_{ib}, I_{ih} and the output low-impedance node V_o. In order to achieve voltage transfer functions, the input voltages V_{il}, V_{ib}, V_{ih} are applied to input nodes through supplementary CMOS elements g_l, g_b, g_h, whose transconductances are used to control the gains and the zeros locations of the biquad transfer function. Since an input of the basic biquad cell is low-impedance too, more than one CMOS transconductor output can be connected to this point, allowing a multiple-input filter cell. With regard to voltage inputs, the circuit output voltage can be expressed as follows

$$\frac{V_o(s)}{V_{il}(s)} = \frac{\dfrac{g_l}{g_{m3}}}{s^2 \dfrac{g'_{m2}}{g_{m3}} \dfrac{C_1 C_2}{g_{m1} g_{m2}} + s \dfrac{g'_{m2}}{g_{m3}} \dfrac{g'_{m1}}{g_{m2}} \dfrac{C_1}{g_{m1}} + 1} \quad (5)$$

$$\frac{V_o(s)}{V_{ib}(s)} = \frac{-s \dfrac{g_b}{g_{m3}} \dfrac{C_1}{g_{m1}}}{s^2 \dfrac{g'_{m2}}{g_{m3}} \dfrac{C_1 C_2}{g_{m1} g_{m2}} + s \dfrac{g'_{m2}}{g_{m3}} \dfrac{g'_{m1}}{g_{m2}} \dfrac{C_1}{g_{m1}} + 1} \quad (6)$$

$$\frac{V_o(s)}{V_{ih}(s)} = \frac{s^2 \dfrac{g_h}{g_{m3}} \dfrac{C_1 C_2}{g_{m1} g_{m2}} + s \dfrac{g_h}{g_{m3}} \dfrac{g'_{m1}}{g_{m2}} \dfrac{C_1}{g_{m1}}}{s^2 \dfrac{g'_{m2}}{g_{m3}} \dfrac{C_1 C_2}{g_{m1} g_{m2}} + s \dfrac{g'_{m2}}{g_{m3}} \dfrac{g'_{m1}}{g_{m2}} \dfrac{C_1}{g_{m1}} + 1} \quad (7)$$

It is obvious that by combining the previous three expressions, any kind of biquad transfer function can be implemented.

As will be shown below, the coupled-biquad simulation technique used in this paper imposes for some circuit configurations, to implement, besides normal biquad cells with finite-Q, cells having infinite-Q second order transfer function. This kind of frequency behavior can be obtained by removing in the diagram of Fig. 4, the CMOS transconductor g'_{m1}.

V. COUPLED-BIQUAD ACTIVE FILTER SYNTHESIS PROCEDURE

Consider a general RLC ladder network with nodes, as shown in Fig. 5. The work of the passive network can be described using the voltages in the nodes of the

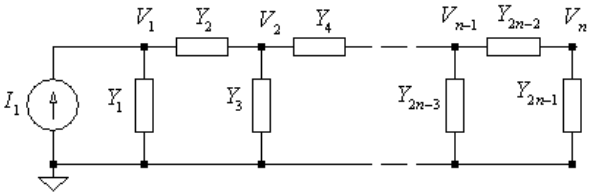

Fig. 5. An RLC ladder network filter is completely described by its node voltages.

network: $V_1, V_2, \ldots, V_n$. The most general form of the equation that can be written for any node of the network is

$$V_k = \frac{I_k}{Y_k^n} + \frac{Y_{2k-2}}{Y_k^n} V_{k-1} + \frac{Y_{2k}}{Y_k^n} V_{k+1}, \quad k = 1, 2, \ldots, n \quad (8)$$

where Y_k^n is the total admittance connected to node k of the network ($Y_k^n = Y_{2k-2} + Y_{2k-1} + Y_{2k}$). I_k represents the value of current sources connected to the node. Only for $k = 1$, $I_1 \neq 0$ and $V_0 = 0$. In the last node of the network: $V_{k+1} = 0, k = n$.

According to eq. (8), the ladder filter network can be implemented using RC active circuits cells with multiple inputs. Moreover, as the denominators of all the terms on the right side of (8) are identical, Y_k^n, a unique active circuit cell with multiple inputs can be used to implement the desired functions that appears in eq. (8) relating to one loop of passive filter. Depending on the position of the node in the RLC network, these functions are first or second order RC active circuits transfer functions. Referring to node k, we will denote the corresponding transfer functions in eq. (8) as

$$T_{ik}(s) = \frac{1}{Y_k^n}; T_{k-1,k}(s) = \frac{Y_{2k-2}}{Y_k^n}; T_{k+1,k}(s) = \frac{Y_{2k}}{Y_k^n} \quad (9)$$

Consequently, an active filter cell will realize the equation

$$V_k = T_{ik} I_k + T_{k-1,k}(s) V_{k-1} + T_{k+1,k} V_{k+1}, \quad k = 1, 2, \ldots, n \quad (10)$$

The active filter circuit structure composed of coupled biquad that implement (10) is shown in Fig. 6.

There are two forms of RLC ladder filter structures: T-shaped and π-shaped circuits. Both of them can be implemented by this method, but it is normal to choose for simulation the most efficient one, viewing that the emulation of first-order transfer functions uses almost the same number of CMOS transconductors as second-order function cells. From this point of view, π-shaped circuits are the choice,

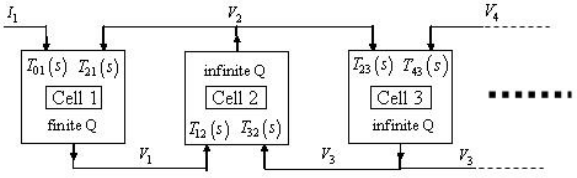

Fig. 6. Block diagram of the node-voltage coupled-biquad active filter emulation of ladder filter in Fig. 5.

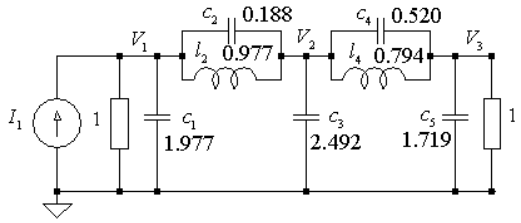

Fig. 7. Fifth-order elliptic low-pas passive ladder filter used as prototype in node-voltage emulation method.

because, with the exception of the last node in an even-order filter, all transfer functions in (10) are second-order rational functions.

VI. FIFTH-ORDER ELLIPTIC LOWPASS CMOS FILTER DESIGN EXAMPLE

The design procedure of a CMOS active filter based on the node-voltage emulation method starts by the selection of an appropriate RLC ladder prototype. Next, a description of passive network work is made by its set of node-voltage equations. Then, each equation is replaced by a CMOS biquad cell from the previous Section. Drawing a parallel between the passive network equations and the transfer functions of CMOS transconductor filter cell, the values of capacitances and transconductances of CMOS elements are computed. Finally, the neighboring filter cells are connected in accordance with passive filter equations.

To illustrate the node-voltage approach, a fifth-order low-pass elliptic passive filter prototype will be used to obtain equivalent CMOS transconductor coupled-biquad filters. The LC ladder prototype shown in Fig. 7 has 1dB ripple in the passband and minimum 55db attenuation in the stopband. Node-voltage analysis leads to the following system of equations:

$$V_1 = T_{01}(-I_1) + T_{21}V_2 = \frac{sl_2 I_1 + \left(s^2 c_2 l_2 + 1\right)V_2}{s^2(c_1+c_2)l_2 + sl_2 + 1}$$

$$V_2 = T_{12}V_1 + T_{32}V_3 \qquad (11)$$

$$= \frac{\left(s^2 c_2 \frac{l_2 l_4}{l_2+l_4} + \frac{l_4}{l_2+l_4}\right)V_1 + \left(s^2 c_2 \frac{l_2 l_4}{l_2+l_4} + \frac{l_2}{l_2+l_4}\right)V_3}{s^2(c_2+c_3+c_4)\frac{l_2 l_4}{l_2+l_4} + 1}$$

$$V_3 = T_{23}V_2 = \frac{\left(s^2 c_4 l_4 + 1\right)V_2}{s^2(c_4+c_5)l_4 + sl_4 + 1} \qquad (11)$$

Each pair of these transfer functions (f.i. T_{01} and T_{21}) have the same poles but different zeros. This enables the realization of each equation in (11) by one CMOS biquad circuit cell. The result for the fifth-order filter under discussion consists of three CMOS coupled biquad cells with a total of 25 CMOS elements. The complete schematic of CMOS coupled biquad filter is shown in Fig. 8. The values of parameters of electronic components in Fig. 8 is established by comparing the transfer functions (5)-(7) with the expressions in (11). Denoting the cut-off frequency of the active low-pass filter by ω_o and choosing g_0 as the value of the transconductance of a CMOS standard element, Table 1 gives the design relationships for all the circuit components of the active filter.

VII. SIMULATION RESULTS

To verify the theoretical analyses, we simulated the fifth-order active filter shown in Figure 8 in a SPICE circuit simulation program, using a TSMC035 level-49 Spice simulation [8]. The cut-off frequency of the filter is imposed to be $f_o = 1\text{MHz}$ The supply voltages of CMOS transconductors are $V_{DD} = 1.65V$, $V_{SS} = -1.65V$ and the command voltage lines $\pm V_G$ in Figure 1 being, usually, connected to supply rails. The MOS transistors of a standard CMOS cells, that exhibits a value of transconductance equal to g_o has the following parameters: $W_o/L = 20\mu/1\mu$ for the n-MOS transistor, respectively $W_o/L = 40\mu/1\mu$ for the p-MOS transistor. In these conditions, the transconductance of the standard CMOS cell is $g_o = 456\mu S$, and the values of all the other elements of the schematic diagram in Fig. 8 (transconductances and capacitors) are computed in accordance with Table 1. Even if at low-values of transconductance, the linearity between the geometrical dimensions of MOS transistors and the transconductance of the CMOS linear elements is poor, in the first instance, in order to compute these dimensions for the CMOS cells in

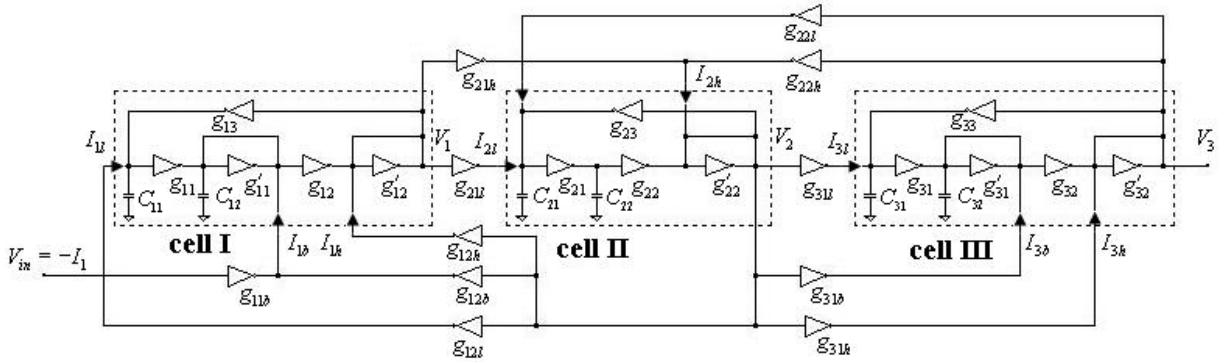

Fig. 8. The CMOS transconductor elements realization of fifth-order elliptic lowpass ladder prototype filter in Fig. 7.

Table 1. Design relationships used for circuit elements in lowpass fifth-order elliptic CMOS filter presented in Fig. 8.

Cell No. I – finite Q	Cell No. II – infinite Q	Cell No. III – finite Q
$g_{11}=g_{12}=g'_{12}=g_{13}=g_0$	$g_{21}=g_{22}=g'_{22}=g_{23}=g_0$	$g_{31}=g_{32}=g'_{32}=g_{33}=g_0$
$C_{11}=C_{12}=g_0\sqrt{(c_1+c_2)l_2}/\omega_0$	$C_{21}=C_{22}=g_0\sqrt{(c_2+c_3+c_4)\frac{l_2l_4}{l_2+l_4}}/\omega_0$	$C_{31}=C_{32}=g_0\sqrt{(c_4+c_3)l_4}/\omega_0$
$g'_{11}=g_0\sqrt{l_2/(c_1+c_2)}$	-	$g'_{31}=g_0\sqrt{l_4/(c_4+c_3)}$
-	$g_{21l}=g_0\frac{l_4}{l_4+l_2}$	$g_{31l}=g_0$
$g_{11b}=g_0\sqrt{l_2/(c_1+c_2)}$	-	$g_{31b}=g_0\frac{c_4}{c_4+c_3}\sqrt{l_4/(c_4+c_3)}$
-	$g_{21h}=g_0\frac{c_2}{c_2+c_3+c_4}$	$g_{31h}=g_0\frac{c_4}{c_4+c_3}$
$g_{12L}=g_0$	$g_{22l}=g_0\frac{l_2}{l_4+l_2}$	-
$g_{12b}=g_0\frac{c_2}{c_1+c_2}\sqrt{l_2/(c_1+c_2)}$	-	-
$g_{12h}=g_0\frac{c_2}{c_1+c_2}$	$g_{22h}=g_0\frac{c_4}{c_2+c_3+c_4}$	-

schematic, we assume a perfect proportionality between these two terms. As a consequence, the dimensions W/L of all MOS transistors are expressed by reference to the values of the standard cell W_o/L.

In the first instance, the active filter circuit is achieved, using strictly the design relationship of Table 1. Then, in order to fight against the effect of short-width nonlinearity and to make fine tuning corrections of frequency characteristics of the filter, the transconductance voltage control lines of CMOS elements $\pm V_G$ are disconnected from supply rails and biased independently. Two very edifying examples are presented further on.

Fig. 9 illustrates the cut-off frequency tuning of the active filter through the control voltages $\pm V_G$ of some selected CMOS transconductance elements of the circuit in Fig. 8. The CMOS transconductances that affect the cut-off frequency of the circuit without modifying the shape of the frequency response, are the first three elements situated on the direct way of each biquad cell that constitute the circuit. By example, in the first biquad cell, the CMOS elements g_{11}, g'_{11} and g_{12} are subject to frequency control through $\pm V_G$ lines. Similar elements are controlled through $\pm V_G$: g_{21} and g_{22} in the second cell and g_{31}, g'_{31} and g_{32} in the third cell. All the other CMOS elements of Fig. 8 remain unaffected by the frequency control through $\pm V_G$ lines, their control voltages being connected to supply rails.

The second experiment demonstrates the effectiveness

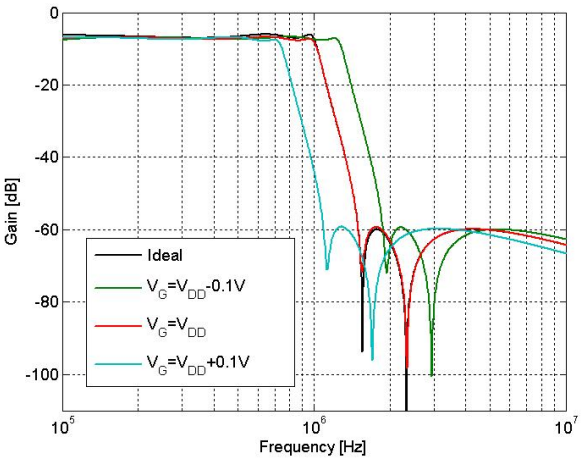

Fig. 9. Fifth-order elliptic CMOS active lowpass filter frequency characteristics: cut-off frequency tuning through the control voltages of CMOS elements of biquads.

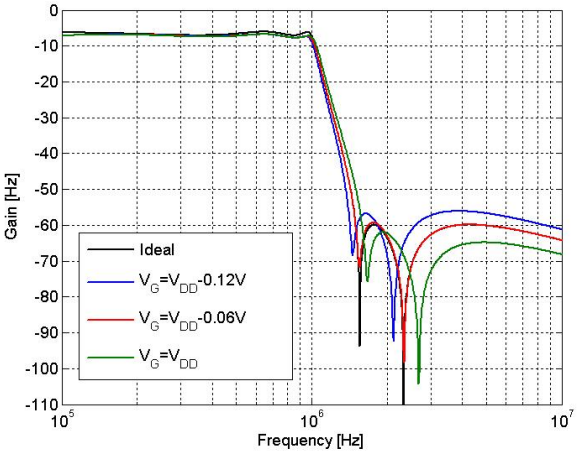

Fig. 10. Fifth-order elliptic CMOS active lowpass filter frequency characteristics: fine tuning adjustment of frequency response through the control voltages of CMOS elements used to interconnect biquad cells.

of fine tuning of active filter transfer function through the control voltages $\pm V_G$ of some CMOS elements used to interconnect the biquad cells that constitute the active filter. The result of the fine tuning action is shown in Fig. 10 and it demonstrates that only the finite-zeros of the filters are affected, the cut-off frequency being unmodified by this adjustment. Not all the CMOS elements of the active filter are assigned to $\pm V_G$ control, but only the elements with the transconductance lower than 20% of the standard value g_o. This choice is justified by the strong nonlinearity between the transconductances of these CMOS elements and their geometrical dimensions. The CMOS transconductor that are subject to this voltage control are g_{12b} and g_{12h} that are connected to the first biquad, g_{21h} and g_{22h} connected to the second biquad and g_{31b} and g_{31h} that are connected to the third biquad.

VIII. CONCLUSIONS

This paper proposition is to use very simple and versatile active devices, the four transistors CMOS transconductance elements, and grounded capacitors in order to generate HF IC-compatible active filters. By using two-integrator loop filter architectures, a basic CMOS biquad filter cell is developed. Amongst the main features of these structures are: realization of all standard functions of an universal filter without any matching constraints, use of only two grounded capacitors, independent tunability of biquad parameters, and low sensitivities. TSMC 0.35 μm process Spice simulations are included to validate the theoretical predictions of filtering performances and to demonstrate the way we can control electronically the filter parameters.

In order to demonstrate the effectiveness and versatility of the CMOS transconductors, the coupled-biquad simulation method was used to implement a fifth-order elliptic lowpass CMOS filter. The method implements the passive network by the interconnection of multiple inputs biquad cells. The simulation results agree very well with theoretical suppositions.

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