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Redundancy and Testability in Digital Filters

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Abstract – Threat issues in specific applications of digital filters are investigated. Since these redundant faults tend to appear in the same general location as test-resistant faults, the presence of many redundant faults can hide significant untested faults despite high overall test coverage. Classes of redundant faults that arise in digital filters are described and we propose a suite of technologies for identifying and eliminating the most common redundancies based on arithmetic optimization.

I. INTRODUCTION

With more commercial products incorporating digital signal processing (DSP) functions, testable design has become a "pressing issue among DSP designers". Developing high coverage tests for application-specific is considerably complicated by the presence of these random-test-resistant faults.

We will focus on the finite-impulse response (FIR) filters since they are perhaps the most widely implemented class of digital signal processing applications and are a basic building block of many more complex systems. However, the general approach is geared towards any system that can be described as a network of shift, add, delay sign extension, and truncation elements.

In order to gauge the efficacy of the approach across a fairly broad slice of designs, we will use fire filter specifications selected from the literature [1],[2] that include three lowpass filters, a wide-band bandpass filter used in video processing, and a predistorsion filter.

The overall approach is shown in Fig. 1, where we will be focusing on the shaded partition.

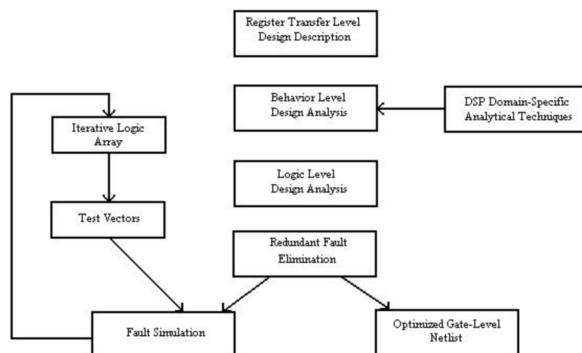

Fig. 1 Overview of design flow

The register-transfer-level (RTL) design description is analyzed to identify structures that are redundant, and the logic is marked to indicate the specific redundancies that are embodies. The designs will be implemented using three different common architectures: cascaded ripple-carry adders, carry-save pipelines, and adder tree structures.

II. FAULT MODEL

Since the principal active element in all the designs was the full-adder cell, the fault model used for this cell is of a same concern. We used the common gate-level model shown in Fig. 2, where the faults modeled are the stuck faults at gate input and output pins. Often, the hardest tests to apply using pseudorandom techniques are those associated with overflow conditions at the next-to-MSB full adder.

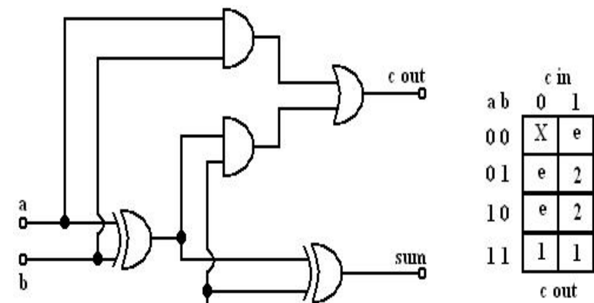

Fig. 2 Full adder gate-level model and associated carry logic test

If the c input is the carry input to the full adder, under this fault model, testing the carry logic requires fire tests: the three labeled e (essential) on the right half of Fig. 2, and one from each of the two equivalence classes 1 and 2. Under this model, overflow test 6 is nonessential, since the logic test by it can also be easier (more probable) test 7.

III. SCALING

The single most important design for testability optimization that can be performed on filters is to scale signal widths to the minimum width needed

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eliminating redundant sign bits. Computing the minimum width needed to hold a signal can be performed using any member of the standard fixed-point scaling techniques [3]. In redundancy elimination we use L_1 scaling since it is the most conservative scaling technique, guaranteeing that the circuit behavior will not be altered. Mode w_k can be characterized using the idealized impulse response of the subfilter that outputs at the interval mode:

$$w_k[n] = \sum_{i=0}^{M_k} h_k[i]x[n-i] \quad (1)$$

Where $h_k[i]$ is the impulse response of the subfilter and M_k is the order of the subfilter.

Using the property that the magnitude of a sum is less than or equal to the sum of the magnitudes of it's terms, and then replacing $x[n-i]$ with x_{Max} (the maximum input signal magnitude) we obtain:

$$|w_k[n]| \le \sum_{i=0}^{M_k} |h_k[i]||x[n-i]| \le x_{Max} \sum |h_k[i]| \quad (2)$$

This gives an upper bound on the signal amplitude at the internal mode. Without knowing more about the characteristics of the input signal, we assume that it is capable of swinging through the full range available to it ($x_{Max} = 1$). The upper bound on the signal amplitude is then:

$$|w_k[n]| \le B \quad (3)$$

and:

$$B = \sum_{i=0}^{M_k} |h_k[i]| \quad (4)$$

IV. APPLICATION

The target applications will focus on where the finite impulse response (FIR) filters are. To provide a brief review of terms and definitions, FIR filters essentially perform a weighted moving average of a sequence of input sample. This is described by the linear constant coefficient difference equation:

$$y[n] = \sum_{i=0}^{M} h_i x[n-i] \quad (5)$$

Where M is the filter order, $y[n]$ is the output signal at time n, $x[n]$ is the input at time n, and $h_i, 0 \le i \le n$ is the set of filter coefficients, which also corresponds to the impulse response of the filter.

The designer frequently has some flexibility in choosing the filter coefficients, and it is often possible to select the h_i, such that they can be expressed as a power of two or the sum or difference of two powers of two, which leads to efficient VLSI implementations.

V. CONCLUSION

Redundant fault can be an obstacle to gauging the true effectiveness of any test scheme, particularly in application specific digital filters where these faults can be hard to distinguish from highly test resistant fault. Analysis of the register-transfer-level design using arithmetic techniques based on scaling theory and signal phase and magnitude constraints provides an efficient means of identifying and eliminating most redundant faults in these designs.

Elimination of these faults can be done as a preprocessing phase for more accurate fault simulation or it can be used to eliminate redundant logic from the design itself, in which case it is possible to make significant area reductions as compared to moderately optimized designs.

In many cases, smaller than the area of the logic removal by redundant fault eliminations for a net reduction in area over the nonoptimized design with no self test capabilities.

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