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Time-Problem in Hopfield Neural Networks with Parasitic Capacitances

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Abstract –A continuous time neural network of $O(N^2)$ interconnections is considered. A maximum selector is built by a proper choosing of parameters. It processes a sequence of lists and the speed is a performance criterion. The main point here is a formula for the processing time which takes into account the parasitic capacitances between inputs.

Keywords: neural networks, winner-takes-all, Hopfield networks, parasitics, time evaluations.

I. INTRODUCTION

The Hopfield networks have proved to be powerful analog machines [1]-[4], [12], [15]. They can compete well with their digital counterparts as their huge parallelism leads to remarkable high speed of processing. Therefore, setting up the clocking time of an analog neural computational network is essential [1], [8]-[11], [13]. On the other hand, the extensive interconnection between cells can damage the time performances. This is why attentive studies on parasitic or fault capacitive coupling have been carried out [14], [16]. We report here some of our results on time evaluation of Winner Take All networks when all pairs of inputs are affected by mutual coupling. We are interested in closed form expression of processing time, from where the circuit and list parameters can be properly chosen for a certain performance. The results here are extensions of those in [16].

II. THE WTA CIRCUIT

Fig.1 displays one of the N-cells of a Hopfield neural network. The amplifier is described by $v_i = mg(\lambda u_i)$ where $g:\Re \to (-1,1)$ is a C^1 function with $\lim_{x\to\pm\infty} g(x) = \pm 1$, $0 < g'(x) \le a$ and $\lim_{x\to\pm\infty} xg'(x) = 0$. m and λ are the amplitude and the gain, respectively. p is the interconnection conductance of negative feedback, C_0 and ρ are the ground capacitance respectively resistance of each cell. Each (u_i, u_j) input pair has a mutual capacitance δ as a parasitic effect. Thus each input is capacitively coupled through δ with all other inputs. Although this is certainly a rough approximation of real parasitics (or faults) its symmetry allows the time evaluations below.

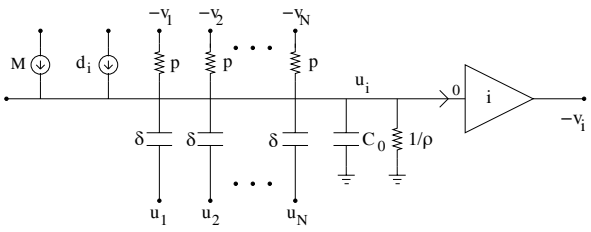

Fig. 1. The i-th cell with all its interconnections

Our circuit should process a list of N items given by the currents d_i of each input where M, a bias source, is also applied. The list elements are distinct, with the minimum mutual distance Δ corresponding to a list density $z = \dfrac{\Delta(N-1)}{d_m}$. Here $[0, d_m]$ is the admission interval. Suppose the list elements are ordered as

$$d_{\sigma(1)} > d_{\sigma(2)} > \cdots > d_{\sigma(N)} \qquad (1)$$

The WTA circuit should signal the fact that the element of rank $\sigma(1)$ is the largest one. This will be done by splitting the list of output voltages in two parts: $v_{\sigma(1)}$ above a positive threshold ξ and all other beneath $-\xi$, i.e.

$$v_{\sigma(1)} > \xi > -\xi > v_{\sigma(j)} \text{ for all } j \in \overline{2,N}$$

III. BASIC PROPERTIES

Our circuit obeys the equation

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$$C\frac{\mathrm{d}u}{\mathrm{d}t} = -lu - Tv + b \qquad (2)$$

Here $u = (u_1, u_2, \cdots u_N)^{tr}$, $v = (v_1, v_2, \cdots v_N)^{tr}$, $v_i = mg(\lambda u_i)$, $b = (b_1, b_2, \cdots b_N)^{tr}$ where $b_i = M + d_i$. C is the matrix, with $C_{ii} = C_0 + (N-1)\delta$, $C_{ij} = -\delta$ for all $i, j \in \overline{1,N}$, $i \neq j$. T is the interconnection matrix, with $T_{ii} = 0$, $T_{ij} = p$ while $l = \frac{1}{\rho} + (N-1)p$. The main convergence result tells that for every $u(t)$ solution of (2) there exists a stationary state $\bar{u}$ such that $\lim_{t\to\infty} u(t) = \bar{u}$. Even more, if the gain λ is sufficiently high, then any stationary solution with $|\bar{v}_i| \geq \xi$ is asymptotically stable.

IV. TIME EVALUATION

Starting from zero at $t = 0$ one can show that, for all $t > 0$, the relative order of state components is exactly the same as the list order (1):

$$u_{\sigma(1)}(t) > u_{\sigma(2)}(t) > \cdots > u_{\sigma(N)}(t) \qquad (3)$$

This is true provided that $\lambda > \frac{l}{pam}$ and it extends to the vector of $v_{\sigma(i)}(t)$ and to the stationary state $\bar{u}$ or $\bar{v}$ as well [13], [16]. Further on, we distinguish two cases (see Figs. 2 and 3). The first one, supposes $u_2(t)$ passes the WTA threshold $-\beta$ before $u_1(t)$ crosses its $+\beta$ level. Rigorously speaking, we suppose $\alpha \in [0, 2\beta]$ and taken the moment t_α when $u_1(t_\alpha) = \beta - \alpha$, $u_2(t_\alpha) = -\beta$ and for all $t > t_\alpha$, $u_2(t) < -\beta$. The second case supposes $u_1(t)$ reaches $+\beta$ in advance of $u_2(t)$ reaching $-\beta$. In this case we call t_α the moment when $u_1(t_\alpha) = \beta$, $u_2(t_\alpha) = -\beta + \alpha$ and for all $t > t_\alpha$ $u_1(t) > \beta$. In both cases above we call t_p -processing time-, the first moment after t_α when $u_1(t_p) \geq \beta$ and $u_2(t_p) \leq -\beta$. With these, the problem of finding the clocking time T_p reduces to search for upper bounds $\bar{t}_\alpha$ and $\overline{t_p - t_\alpha}$ of t_α and $t_p - t_\alpha$ respectively. We have $T_p(\alpha) = \bar{t}_\alpha + \overline{t_p - t_\alpha}$.

The first bound $\bar{t}_\alpha$ comes from "the difference equation"

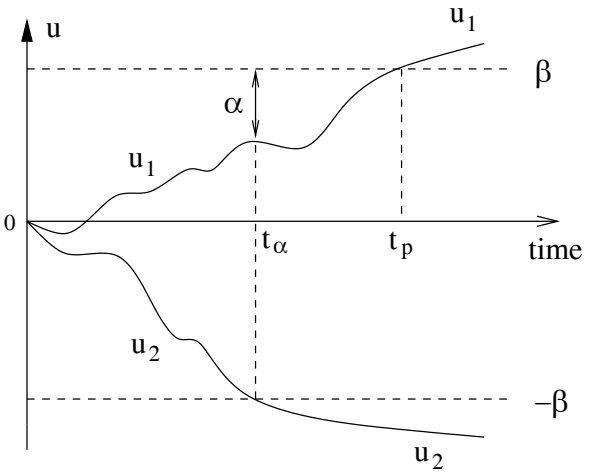

Fig. 2 The processing phase - case 1. The $u_{\sigma(1)}$ winner surpasses the threshold β after the moment when the losers $u_{\sigma(2)}$ fall under $-\beta$

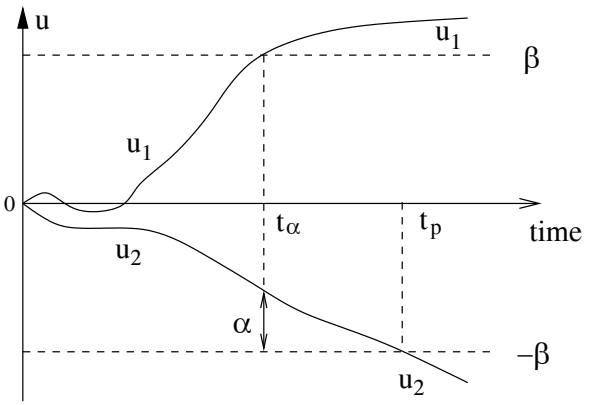

Fig. 3 The processing phase - case2. The $u_{\sigma(1)}$ winner goes above β before the moment when $-\beta = u_{\sigma(2)}$.

The first bound $\bar{t}_\alpha$ comes from "the difference equation"

$$C_n \frac{\mathrm{d}}{\mathrm{d}t}(u_1 - u_2) = -l(u_1 - u_2) + p(v_1 - v_2) + d_1 - d_2$$

where $C_n = C_0 + N\delta$. With $(u_1 - u_2)(0) = 0$ and $(u_1 - u_2)(t_\alpha) = 2\beta - \alpha$ we get

$$t_\alpha \leq \bar{t}_\alpha = \frac{C_n}{l} \ln \frac{\Delta}{\Delta - l(2\beta - \alpha)} \qquad (4)$$

This is valid equally for the two cases and all $\alpha \in [0, 2\beta]$.

The evaluation of $t_p - t_\alpha$ in case 1 comes from the first equation in (2) written as:

$$C_0 \frac{\mathrm{d}u_1}{\mathrm{d}t} = -lu_1 - \delta \sum_{j=1}^{N} \frac{\mathrm{d}}{\mathrm{d}t}(u_1 - u_j) - p\sum_{j=2}^{N} v_j + b_1$$

It yields

$$t_p - t_\alpha \le \overline{t_p - t_\alpha} = \frac{C_0}{l} \ln \frac{W - l\beta + l\alpha}{W - l\beta} \qquad (5)$$

where

$$W = p\xi(N-1) + \underline{d}_1 + M - \\ - \frac{\delta}{C_n}[2pm(N-1) + \sum_{j=1}^{N} \overline{d}_{1j}] \qquad (6)$$

Here $\underline{d}_1 = zd_m$ and $\overline{d}_{ij} = d_m - (N-j)\Delta$.
For the case 2 we use the second equation in (2)

$$C_0 \frac{\mathrm{d}u_2}{\mathrm{d}t} = -lu_2 - \delta \sum_{j=1}^{N} \frac{\mathrm{d}}{\mathrm{d}t}(u_2 - u_j) - p\sum_{\substack{j=1 \\ j\neq 2}}^{N} v_j + b_2$$

and get again (5) where

$$W = p\xi - pm(N-2) - \overline{d}_2 - M - \\ - \frac{\delta}{C_n}\left[2pm(N-1) + \overline{d}_{12}\right] \qquad (7)$$

Here $\overline{d}_2 = d_m - \Delta$ and $\overline{d}_{12} = d_m - (N-2)\Delta$.
Now, (4) and (5) give the bound $T_p(\alpha)$ of processing time for every $\alpha \in [0, 2\beta]$. By imposing $\frac{\mathrm{d}T_p}{\mathrm{d}\alpha} < 0$ we find $\max T_p(\alpha) = T_p(0)$ which gives a final bound:

$$t_p \le T_p(0) = \frac{C_n}{l} \ln \frac{\Delta}{\Delta - 2l\beta} \qquad (8)$$

The above imposion results in $W - l\beta > 0$ for both two cases, and also $\Delta - 2l\beta > 0$. These inequalities are made true by a proper choosing of circuit parameters M, ξ, β, m, p, d_m when the minimum list density z and the maximum parasitic capacitance δ are given. Our evaluations works for $\delta \in [0, C_0/N-2]$.

V. CONCLUSION

Taking into account the more and more squeezed chip dimensions of today technology, the cross-coupling capacitances can be essential for the working speed of a neural network.
Our work succeeds to give an explicit processing time formulae for a WTA neural network affected by parasitic capacitances between inputs. The clocking time expression is remarkable simple. It is valid for a certain set of parameters including a limitation in parasitic capacitances.

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