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The Micropower Translinear Network Implementation of Rational Approximated Functions

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Abstract – In this paper are presented several translinear topologies suitable for static and dynamic analog signal processing at very low supply voltage. The one variable objective functions, firstly are rational approximated, then are decomposed in continued fractions and finally implemented with CMOS translinear networks. Such implementation is preferred in application that required small errors of signal procesing.

Keywords: analog signal processing circuits, translinear circuits, CMOS integrated circuits, low power and low voltage circuits.

I. INTRODUCTION

Nonlinear objective-functions are widely applied in practical VLSI electronic systems and there are many cases in which the translinear networks are the best solutions of implementation of these. The synthesis of nonlinear networks is a heavy task. However a systematic procedure for the synthesis of translinear circuits was developed by Evert Seevinck [5]. The proposed synthesis method consists in three parts: objective-function approximation, approximate-function decomposition and realization of translinear network for the function obtained after decomposition. Using at starting point the Seevinck synthesis method in period 1999-2003 I have developed the algorithms and I have realized a few programs in C++ code which permit the automatic synthesis of translinear circuits but only whit bipolar transistors, named TLSS, [1], [2], [3].

In practical CMOS VLSI mixal signal electronic systems the power supply voltage continues to scale down. Future analog circuits will have to operate successfully at supply voltages slightly higher than the MOS threshold voltage. The suitable topologies for signal processing at such low values of supply voltages are the translinear circuits because are operating in current domain and in this way the very small voltage swings are avoided. The MOS transistors have exponential current-voltage characteristics in weak inversion (or sub-threshold) region. Therefore in these circuits the MOS transistors will operate in this region. The main problems of this operating region are the relatively low speed capability and inferior matching. But these problems are relatively solved in sub-micron technology.

In this paper are presented several CMOS translinear topologies that implement one variable objective functions, rational approximated and decomposed in continued fractions. Such functions processing leads to implementations with small errors and relatively small number of devices.

II. THE MOS TRANSISTORS IN WEAK INVERSION

In above section was argued that the MOS transistor in low-voltage translinear circuits will operate in weak inversion. It is well known the general expression of drain current of MOS transistor:

$$I_D = \beta \cdot \int_{V_S}^{V_D} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}V \qquad (1)$$

with

$$\beta = \mu \cdot C_{ox} \cdot (W / L) \qquad (2)$$

where

W, L width, length of the channel;
C_{ox} gate capacitance per unit area;
μ charge carrier mobility;
Q_i induced mobile charge in channel;
V_D, V_S drain, source voltages referred to the local substrate;
V channel potential.

This expression may be decomposed into:

$$I_D = \beta \cdot \int_{V_S}^{\infty} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}V - \beta \cdot \int_{V_D}^{\infty} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}V = I_F - I_R \qquad (3)$$

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where I_F is called forward current (controlled by source voltage V_S) and I_R is called reverse current (controlled by drain voltage V_D).
In weak inversion we have [4]:

$$Q_i / C_{ox} \sim \exp\left(\frac{V_P - V}{V_T}\right) \tag{4}$$

where

V_P pinchoff voltage which is a nonlinear function of gate voltage V_G and represents the body effect;
V_T thermal voltage ($k \cdot T / q$).

Thus we have the following proportionality

$$\begin{aligned} I_F &\sim \beta \cdot \exp\left(\frac{V_P - V_S}{V_T}\right) \\ I_R &\sim \beta \cdot \exp\left(\frac{V_P - V_D}{V_T}\right) \end{aligned} \tag{5}$$

and the drain current has the expression

$$I_D = I_S \cdot \exp\left(\frac{V_P}{V_T}\right) \cdot \left[\exp\left(-\frac{V_S}{V_T}\right) - \exp\left(-\frac{V_D}{V_T}\right)\right] \tag{6}$$

or in terms of V_{GS} and V_{GD} as follows

$$I_D = I_S \exp\left(\frac{V_P - V_G}{V_T}\right) \cdot \left[\exp\left(\frac{V_{GS}}{V_T}\right) - \exp\left(\frac{V_{GD}}{V_T}\right)\right] \tag{7}$$

where I_S is specific current (limit of weak inversion). The specific current is proportional to W/L, follows explicitly shown:

$$I_S \cdot \exp\left(\frac{V_P - V_G}{V_T}\right) = \frac{W}{L} \cdot I_\Diamond(V_G) \tag{8}$$

with $I_\Diamond(V_G)$ the zero-bias ($V_{GS} = 0$) current for a square transistor, which represents the body effect. So, the forward and reverse currents become:

$$\begin{aligned} I_F &= \frac{W}{L} \cdot I_\Diamond(V_G) \cdot \exp\left(\frac{V_{GS}}{V_T}\right) \\ I_R &= \frac{W}{L} \cdot I_\Diamond(V_G) \cdot \exp\left(\frac{V_{DS}}{V_T}\right) \end{aligned} \tag{9}$$

If $I_R << I_F$, then the MOS transistor is saturated, otherwise the MOS transistor is non-saturated. In figure 1.a are shown the two operation regions for weak inversion, which are defined by the ratios I_D / I_F and V_{DS} / V_T [8].

Therefore, each of the drain current components (expressed by (9)) of a non-saturated transistor may be relate to an equivalent saturated transistor with gate-source voltage V_{GS} and V_{GD} respectively and the non-saturated transistor may be decomposed into two identical saturated transistors connected anti-parallel [9]. This is symbolically shown in figure 1.b. The transistor that corresponds to reverse current component is shown in dashed line, and represents the effect of the non-saturated operation of the real transistor.

III. THE CMOS TRANSLINEAR IMPLEMENTATION OF RATIONAL APPROXIMATED OBJECTIVE FUNCTIONS

The objective-functions are first normalized, so that theirs variables to take values only in interval [-1, 1]. Then the one variable normalizes functions are approximated by using *Padé approximation* or *Chebyshev rational approximation* so that the maximum relative error of approximation to be $0.01\% \div 0.1\%$. Finally, it is changed the x variable of the rational function in auxiliary variable $y = y(x)$ so that $y > 0$, $\forall x \in [-1;1]$.

The result of these processes must be manipulated into products of linear terms in the input and output variables. These linear terms have real coefficients and they must always remain positive for all combinations of input variable values. In conformity with decomposition algorithm developed by me and presented in [3], the general final form of continued fraction that incorporate all cases that can be encountered in the decomposition process is:

$$f_{ar}(y) = h_0 + \cfrac{g_1}{h_1 + \cfrac{g_2}{h_2 + \cfrac{g_3}{h_3 + \ldots \cfrac{}{h_{q-1} + \cfrac{g_q}{h_q}}}}} \tag{10}$$

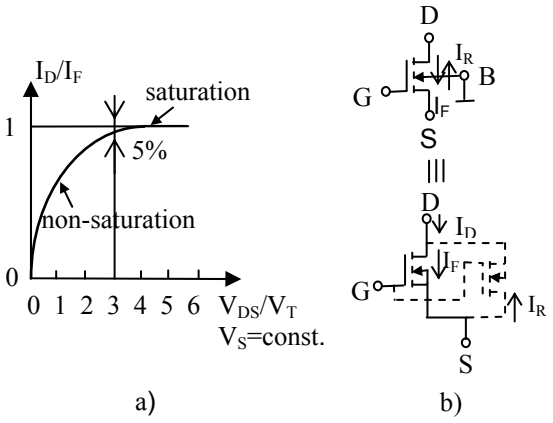

Figure 1. a) The operation regions in weak inversion of the MOS transistor; b) Non-saturated MOS transistor equivalent to two saturated transistors connected anti-parallel.

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The significance of used function g_i and h_i in (10) in function of encountered cases is presented by fallow expressions:

$$h_0 = \begin{cases} 0 & \text{when the dominator of } f_{ar} \text{ is positive} \\ & \text{or real roots of dominator are not placed} \\ & \text{in the range of y variation} \\ \dfrac{b_0}{c_{00}} - p_0 \cdot y; & p_1 \div p_{q-1} = 0 \end{cases}$$

$$g_i = \begin{cases} c'_{10} \cdot y^{i_1} & \text{when } h_0 = 0,\ i = 1 \\ c_{i0} \cdot y^{1+i_i} & \text{when } p_0 \neq 0 \\ c'_{i0} \cdot y^{i_i+1} & \text{when } h_0 = 0 \end{cases} \Bigg\} \begin{array}{l} c'_{i0} = a_{i-1} \cdot c_{i0} \\ i = 1 \div q \end{array}$$

$$\underset{i=1\div(q-1)}{h_i} = \begin{cases} a_{i-1} \cdot c_{i-1,0} & \text{when } p_i = 0 \\ a_{i-1} c_{i-1,0} - p_i y^2 & \text{when} \begin{cases} p_i \neq 0 \\ p_{i+1} \div p_{q-1} = 0 \end{cases} \end{cases}$$

$$h_q = \begin{cases} c^*_{q-1,0} + c^*_{q-1,1} \cdot y & \text{when } \exists p_i \neq 0 \\ c'_{q-1,0} & \text{when } \forall p_i = 0 \end{cases}$$

$$c^*_{q-1,j} = \begin{cases} c^*_{q-2,0} \cdot c^*_{q-3,j+1} - c^*_{q-3,0} \cdot c^*_{q-2,j+1} & \text{for q even} \\ c^*_{q-1,0} \cdot c^*_{q-2,j+1} - c^*_{q-2,0} \cdot c^*_{q-1,j+1} & \text{for q odd} \end{cases}$$

$$a_i = \begin{cases} 1 & \text{when the denominator} \\ & c'_{i0} + c'_{i1} \cdot y + c'_{i2} \cdot y^2 + \ldots + c'_{ir_i} \cdot y^{r_i} \\ & \text{is positiv in the variation range of } y \\ < 0, & a_i \in \mathbf{Z} \end{cases} \quad (11)$$

For the one variable function decomposed in the general form (10) the following set of equations must be implemented:

$$\begin{cases} g_q = g'_q \cdot g''_q \\ z_q \cdot h_q = g'_q \cdot g''_q \\ \ldots \\ (z_i + h_{i-1}) \cdot z_{i-1} = g'_{i-1} \cdot g''_{i-1}; \quad i = 2,\ldots,q \\ g_{i-1} = g'_{i-1} \cdot g''_{i-1} \\ \ldots \\ z = f_{ar}(y) = h_0 + z_1 \end{cases} \quad (12)$$

These equations can be easily implemented using the expandable generic network presented in figure 1.a. It is very easy to see that in this network, all transistors, except T_{i8} and T_{i10} transistors of the current sources, are saturated, $I_R << I_F$ and therefore to good approximation we have:

$$I_{Dij} = I_{Fij} = \frac{W_{ij}}{L_{ij}} \cdot I_\Diamond(V_{Gij}) \cdot \exp\left(\frac{V_{GSij}}{V_T}\right) \quad (13)$$
$$i = \overline{1,q},\ j = \overline{1,9}\ j \neq 8$$

For a minimum supply voltage, the current-source transistors T_{i8} and T_{i10} will be non-saturated. Therefore, in accordance with decomposition technique described in section two (see figure 1.b.), the fictitious transistors T'_{i8} and T'_{i10} are added in order to account the non-saturation of these transistors (see figure 2.b). From those presented in previous section, it follows that all shown network transistors can now be regarded as saturated. The section i of proposed network are three translinear loops: $T_{i1} - T_{i6}$, next T_{i3}, T_{i5}, T_{i7} and T'_{i8} and finally T_{i4}, T_{i6}, T_{i9} and T'_{i10}, which are immune from the body effect. Assuming equal-sized transistors for the translinear loops and applying the Kirchoff low to those it is obtained the following expressions:

$$\begin{aligned} &V_{GS_{i1}} + V_{GS_{i3}} + V_{GS_{i6}} = V_{GS_{i2}} + V_{GS_{i4}} + V_{GS_{i5}} \\ &V_{GS_{i3}} + V'_{GS_{i8}} = V_{GS_{i5}} + V_{GS_{i7}} \\ &V_{GS_{i4}} + V'_{GS_{i10}} = V_{GS_{i6}} + V_{GS_{i9}} \end{aligned} \quad (14)$$

It can see that the oppositely connected transistor pairs T_{i1} - T_{i2}, T_{i3} - T_{i5}, T_{i4} - T_{i6}, T_{i7} - T'_{i8} and T_{i9} - T'_{i10} have the same gate voltage:

$$\begin{aligned} &V_{G_{i1}} = V_{G_{i2}};\ V_{G_{i3}} = V_{G_{i5}};\ V_{G_{i4}} = V_{G_{i6}} \\ &V_{G_{i7}} = V'_{G_{i8}};\ V_{G_{i9}} = V'_{G_{i10}} \end{aligned} \quad (15)$$

It is follows that

$$\begin{aligned} &I_\Diamond(V_{Gi1}) = I_\Diamond(V_{Gi2});\ I_\Diamond(V_{Gi3}) = I_\Diamond(V_{Gi5}) \\ &I_\Diamond(V_{Gi4}) = I_\Diamond(V_{Gi6}) \\ &I_\Diamond(V_{Gi7}) = I_\Diamond(V'_{Gi8});\ I_\Diamond(V_{Gi9}) = I_\Diamond(V'_{Gi10}) \end{aligned} \quad (16)$$

and the equation (14) becomes a classical translinear relationship independent of the body effect:

- for the first loop

$$(g'_i + I_{0i}) \cdot I_{Di1} \cdot I_{0i} = I_{0i} \cdot I_{Di2} \cdot (z_i + I_{0i}) \quad (17)$$

- for the second loop

$$(g''_i + I_{0i}) \cdot I_{0i} = (g'_i + I_{0i}) \cdot I'_{Di8} \quad (18)$$

with

$$I'_{Di8} = g''_i + I_{0i} - I_{0i} - I_{Di1} = g''_i - I_{Di1}. \quad (19)$$

- for third loop

$$I_{0i} \cdot (h_i + z_{i+1} + I_{0i}) = I'_{Di10} \cdot (z_i + I_{0i}) \quad (20)$$

with

$$I'_{Di10} = h_i + I_{0i} - I_{Di2} - I_{0i} = h_i - I_{Di2}. \quad (21)$$

Eliminating I_{Di1} and I_{Di2} yields:

$$(z_{i+1} + h_i) \cdot z_i = g'_i \cdot g''_i \quad (22)$$

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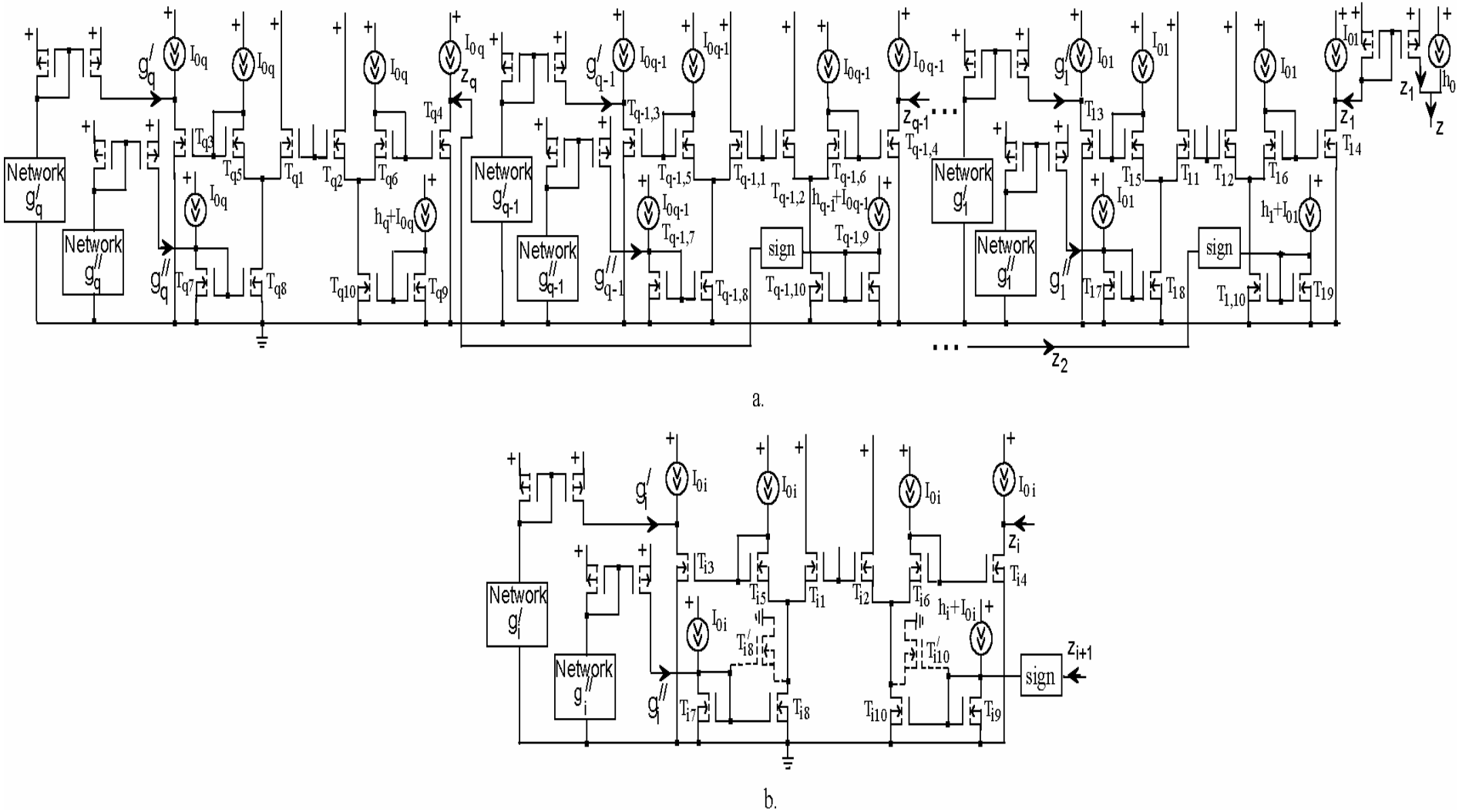

Figure 2.a. The CMOS translinear expandable generic network that implements
the one variable rational approximated objective functions; b. The i section of generic network.

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The expressions for the drain currents of transistors T_{i1} and T_{i2} are:

$$I_{Di1} = \frac{g_i^{/} \cdot g_i^{//} - I_{0i}^2}{g_i^{/} + I_{0i}}$$
$$I_{Di2} = \frac{g_i^{/} \cdot g_i^{//} - I_{0i}^2}{z_i + I_{0i}} \qquad (23)$$

and relive that

$$\min\left|g_i^{/} \cdot g_i^{//}\right| > I_{0i}^2 \qquad (24)$$

for a well operating of network.

The supplementary networks used for implementation of h_i functions and $g_i^{//}$ functions are presented in figures 2 and 3. The analisys for this networks is similary with those maked for the section i of general network. In conformity with these analisys it is obtained:

- for the h_i network

$$\left|p_i\right|^{-1} \cdot \left(a_{i-1} \cdot c_{i-1,0} - h_i\right) = y \cdot y$$
$$h_i = a_{i-1} \cdot c_{i-1,0} - \left|p_i\right| \cdot y^2 \qquad (25)$$

- for the g_i network

$$\left|c_{i0}\right|^{-1} \cdot g_i = y \cdot y^{i_i}$$
$$g_i = \left|c_{i0}\right| \cdot y^{1+i_i} \qquad (26)$$

Must mentioned that in the case of the g_i network, in function of values of i, h_0 and p_0, we have different forms for the network. So, when h_0=0 and i=1 the network presented in figure 3 will be easy changed: $c_{i0}^{/}$ instead of c_{i0}, y^{i_1-1} instead of y^{i_1}. When h_0=0 and $i \neq 1$ then c_{i0} will be changed with $c_{i0}^{/} = a_{i-1} \cdot c_{i0}$. The functions y^{i_i} are obtained using similar topology with those presented in figure 3, but instead of $\left|c_{i0}\right|^{-1}$ will be 1 and instead of y^{i_i} will be y^{i_i-1}. Similarly will be obtained the y^{i_i-1} as is suggested in figure 3 by quadripoles N_{i_i}.

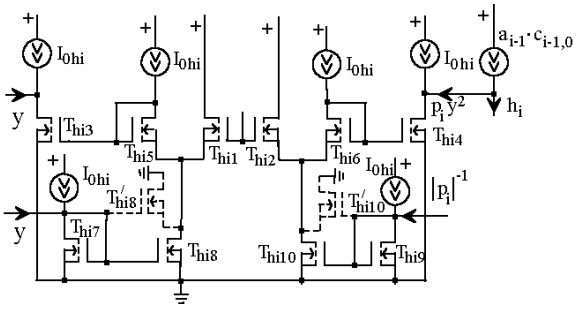

Figure 2. The network that implements the h_i functions

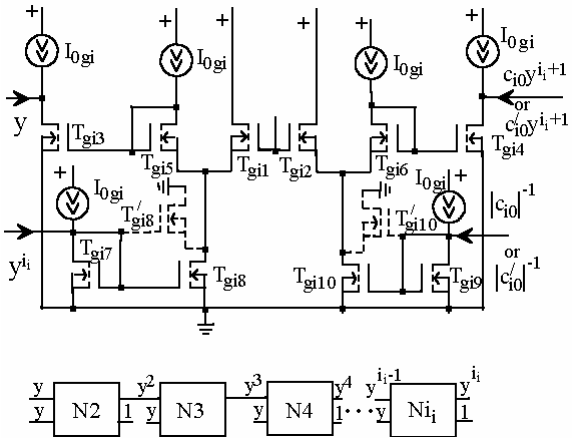

Figure 3. The networks that implement the g_i functions.

The network for changing the sign in conformity with a_I is, in MOS technology, a simple current mirror and for that she wasn't presented.

We must pointed that the current-mode signals are natural for translinear circuits, but in the real-word systems voltage-signals are generally used and therefore voltage-current interfacing will be needed in practice.

IV. CONCLUSION

The suitable topologies for signal processing at very low values of supply voltages are the translinear circuits because are operating in current domain and in this way the very small voltage swings are avoided. In this paper are presented several translinear topologies suitable for static and dynamic analog signal processing in mixed-signal chips fabricated in digital CMOS technology and operated at very low supply voltage. First, it is presented the expandable generic translinear network that is implementing the rational approximated one variable functions that are continue in entire definition domain. The minimum value of supply voltage required for this circuit is given by the sum of the MOS transistor threshold voltage and the drain-source saturation voltages of current sources. Next it is presented the g_i and h_i networks used for obtaining the necessary signals for expandable network. Like expandable network, these can operate at minimum value of supply voltage. Since the value of the supply voltage is low and the require of translinear principle to have a exponential I-V characteristic, the all transistors of these networks will operated in weak inversion. Therefore, bandwidth will be limited and the circuits will be sensitive to the threshold voltage matching.

For the previous presented networks will be developed algorithms so those to be integrated to the TLSS synthesis program. The TLSS is a program in C++ code, realized by me in period 1999-2000, which

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permits the automatic synthesis of translinear circuits. Also, will be studied the bandwidth, noise and errors due to transistors mismatching and will try to correct them.

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