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Controlling a Hi-Fi Audio Amplifier on I^{2}C Bus Using Microcontroller AT89S8252

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Abstract – The paper presents the hardware structure of a Hi-Fi audio amplifying chain consisting of a sound fader control circuit and a power amplifier, both digitally controlled by microcontroller AT89S825 on I2C bus.
The authors have built in practice this application within the university's laboratory. The user is able to control the operation the audio amplifier using switches and a LCD.
The command program that the authors wrote in assembly language, operates in real-time and presents the user with an interactive way to activate various features and to adjust the amplifier's parameters.
Keywords: Hi-Fi audio amplifier, sound fader control circuit, ATMEL microcontroller, I^{2}C bus.

I. INTRODUCTION

The basic structure of a Hi-Fi audio amplifier digitally controller using a microcontroller is shown in fig.1.
The notes have the following meanings: S – stereo audio signal source from compact disc player (CD), digital versatile disc (DVD), radio receiver (Tuner), television set (TV), cassette player (CAS), video cassette player/recorder (Video) and microphone (Mic); SFCC – sound fader control circuit; FPA – final power amplifier; I – interface of the control unit to the audio amplifier; UCC – command and control unit; AS – the audio speaker system, including both filters and loudspeakers (FLS – front left speaker, FRS – front right speaker, RLS – rear left speaker, RRS – rear right speaker); PS – the power supply unit.

II. SOUND FADER CONTROL CIRCUIT

The audio signal is processed using a sound fader control circuit TEA6320, which is an integrated circuit designed for Hi-Fi play of stereo sound. The main features of this circuit are:
- possibility to select from four stereo signal sources and one mono source;
- interface for noise reduction circuits;
- interface for the use of an external equalizer;
- volume, balance and fader control;
- special loudness characteristics automatically controlled in combination with volume setting;
- bass and treble control;
- command of functions available on I^{2}C bus;
- mute function, controlled by audio signal zero crossing, using I^{2}C bus and an external pin of the integrated circuit;
- internal power supply with power-on initializing circuit, etc.

The basic structure of the TEA6320 circuit is shown in figure 2; notes have the following meanings: SM - input audio source selection multiplexer; V1LLC – V1 volume and loudness left control circuit; V1LRL – V1 volume and loudness right control circuit; BLC - bass left control circuit; BRC - bass right control circuit; TLC - treble left control circuit; TRC - treble right control circuit; MFZCD - mute function zero cross detector; V2BFRLC – V2 volume, balance and fader rear left control circuit; V2BFRRC – V2 volume, balance and fader rear right control circuit;

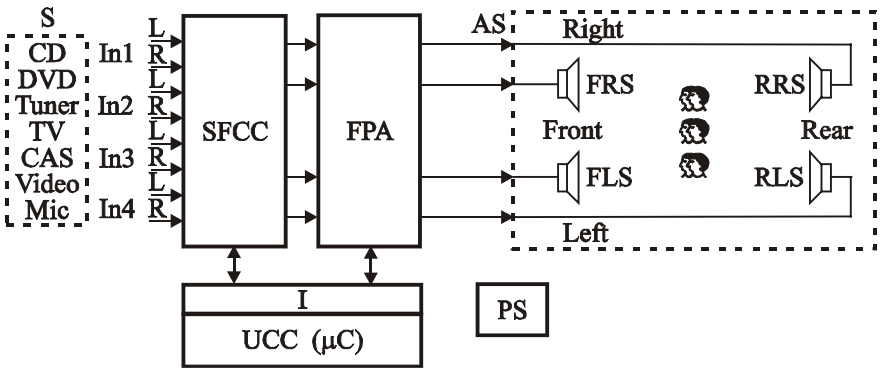

Fig. 1.

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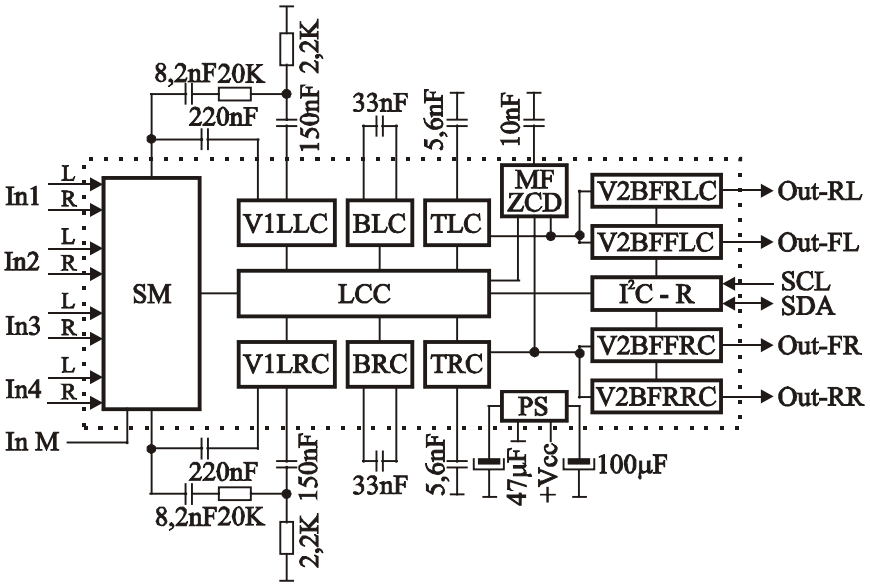

Fig. 2.

V2BFFLC - V2 volume, balance and fader front left control circuit; V2BFFRC - V2 volume, balance and fader front right control circuit; I^2C-R - I^2C bus receiver; LCC – circuit command and control logic; PS – power supply.

The maximal voltage level of the stereo signal input must not exceed 2 V for normal operation.

The volume control function is distributed on two sections, in the volume control block V1 of the first stage and in the volume control block V2 of the second stage. The volume control block of the first stage performs an amplification/attenuation of the audio signal ranging from +20 dB to –31 dB, with 1 dB step. The volume control block of the second stage performs an attenuation of the audio signal going from 0 dB to –50 dB, also with 1 dB step. Theoretically, the volume can be controlled from +20 dB to –86 dB, thus a dynamic range of 106 dB, but the producer only recommends a range between +20 dB and –66 dB, the dynamic range being limited to 86 dB.

The V1 volume control block includes also a loudness correction that uses an external RC filter, its characteristics depending on the values of the external components (20 KΩ, 8.2 nF, 2.2 KΩ, 150 nF). The loudness correction varies the frequency response of the first stage amplifier in order to obtain optimal audition at various volume levels. This feature is necessary because the sensibility of the human ear has non-linear variation in the audio frequency range. For a 20 dB amplification of the first stage amplifier, the filter is linear. The characteristics rises in the 32 dB range and reaches a maximum for a level of –12 dB, where it becomes constant even if the volume continues to drop.

The bass correction block requires only one 33nF capacitor for each channel. The capacitors, combined with the block's internal resistors, constitute a correction filter. The range of the bass corrector is between –15 dB and +15 dB with 1.5 dB step for a 40 Hz input signal.

The treble correction block requires a 5.6 nF capacitor for each channel that, in combination with the internal resistors, constitute the correction filter. The range of the treble corrector is between –12 dB and +12 dB with 1.5 dB step for a 15 KHz input signal.

The last control section for the audio signal is the second volume control stage. This section includes four independent attenuators, each on every of the following outputs: rear-left, front-left, front-right and rear-right. The functions performed by this block are volume, balance and fader control.

The mute function of the circuit has three operation modes:

- enable when connecting the corresponding circuit pin to a logical 0 level;
- quick enable through a command placed on I^2C bus by the command and control unit;
- enable by I^2C bus when audio signal crosses zero; the maximal delay for audio signal zero crossing is 100 ms.

III. THE FINAL POWER AMPLIFIER

It consists of four Hi-Fi power amplifiers. Each one is built using the TDA2613 integrated circuit.

This circuit insures an audio signal pre-amplification, delivers the excitation currents for the final levels, performs a current amplification in the final levels, suppresses unwanted input signals which appear during power-on and power-off, insure thermal protection for the final levels and offers the possibility of symmetric or asymmetric voltage supply.

The structure of a power amplifier using symmetric voltage supply is shown in figure 3.

IV. THE COMMAND AND CONTROL UNIT

The command unit is equipped with the AT89S8252 microcontroller which includes, on a single chip, the following resources: a processor optimised for command and control applications, the 8 Kbytes

FLASH program memory, the 256 bytes RAM data memory, the 2 Kbytes EEPROM date memory, a memory space for special functions registers, four 8-bit parallel ports, three 16-bit counters, programmable hard watchdog timer, a unit for the serial asynchronous data communications (UART), serial peripheral interface (SPI), nine interrupt sources on two priority levels , internal oscillator (f_{max}=24MHz), etc.

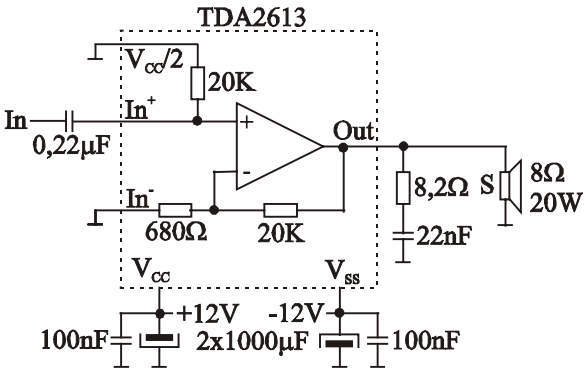

Fig. 3.

From the previous enumeration one can notice that the microcontroller has a large number of inputs and outputs that allow a simple interfacing with other circuits.

The command unit (fig.4) includes around the microcontroller chip: a 20 MHz quartz crystal and two 30 pF capacitors for the clock oscillator, an RC group (10 KΩ and 10 µF), a 1N4148 diode and a switch K for initialization, and two capacitors (100 nF and 10 µF) for decoupling.

The command of the sound fader control circuit is made by microcontroller AT89S8252 through the serial interface I^{2}C. But the microcontroller does not feature this interface and it must be therefore implemented by software.

The communication between the microcontroller AT89S8252 as master and the sound fader control circuit as slave is made using port P0, that has open-drain lines, and two 10 KΩ resistors (fig.5).

The START condition is obtained by a high-to-low transition for the data signal SDA, while clock signal SCL is maintained in high. The STOP condition is determined by a low-to-high transition of the data signal, during which the clock signal is held in high.

The unidirectional line P0.0 of the microcontroller delivers the clock signal SCL. Connecting the microcontroller's output line P0.1 and input line P0.2 obtains the bidirectional data line SDA. When I^{2}C communication is not used, the clock and data lines are held in logical 1.

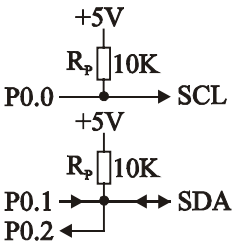

Fig. 5.

A data transfer on bus I^{2}C starts by generating the START condition, then continues by transmitting data and ends by generating the STOP condition by the master, as depicted in fig.6.

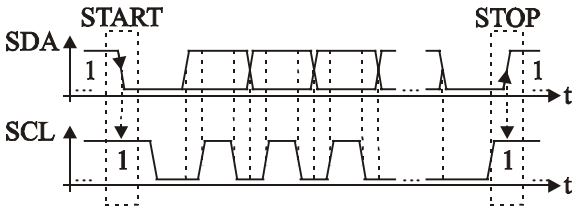

Fig. 6.

The data bits transmitted change during the low level of the clock signal. On the high level of the clock signal, the data is maintained stable. The data transmitted on I^{2}C bus is eight-bit long, the most significant bit being transmitted first. After transmitting eight data bits, the receiving circuit generates an acknowledge bit. Using a low level, the receiver informs the transmitter that it has received the data byte. During the acknowledgement bit, the master circuit generates the clock and its data line is maintained in the high level.

The slave receiver generates the acknowledgement bit after receiving each data byte and will not generate this bit if it is not able to receive data. In this situation, the master transmitter will initiate the STOP condition.

The data format on I^{2}C bus when the master microcontroller transmits towards the slave sound fader control circuit is depicted in fig.7; the notes are:

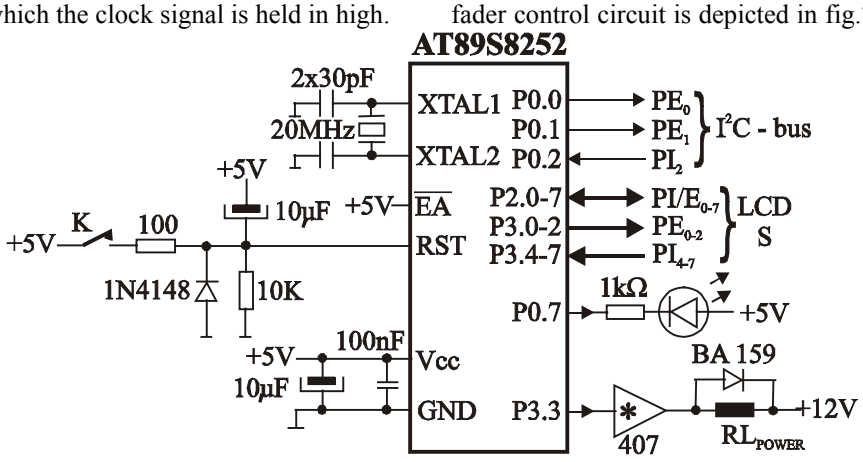

Fig. 4.

Fig. 7.

START - transmission initiation condition; MAD - slave address byte; A – acknowledgement bit; SAD - sub-address byte; DATA - data byte; STOP - transmission termination condition.

The slave address byte of the sound fader control circuit has the value 80H=1000 0000B.

The sub-address byte has the role to select one function for the sound fader control circuit from the following: general volume control (V); fader control front right (FFR); fader control front left (FFL); fader control rear right (FRR); fader control rear left (FRL); bass control (B); treble control (T) ; sound selector control (S).

Table 1 contains the binary values of the functions from the sub-address byte. The five most significant bits are zero logical and the three last significant bits constitute the binary value of the function.

Table 1

Functions	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
V	0	0	0	0	0	0	0	0
FFR	0	0	0	0	0	0	0	1
FFL	0	0	0	0	0	0	1	0
FRR	0	0	0	0	0	0	1	1
FRL	0	0	0	0	0	1	0	0
B	0	0	0	0	0	1	0	1
T	0	0	0	0	0	1	1	0
S	0	0	0	0	0	1	1	1

The data byte for each selected function has the structure detailed in table 2; the notes in the table stand for: ZCM – zero crossing mode; LOFF – switch loudness on/off; GMU – mute control for all outputs.

Table 2

Functions	bit7	bit6	bit5	bit4	bit3	Bit2	bit1	bit0
V=00	ZCM	LOFF	V5	V4	V3	V2	V1	V0
FFR=01	-	-	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
FFL=02	-	-	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
FRR=03	-	-	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
FRL=04	-	-	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
B=05	-	-	-	B4	B3	B2	B1	B0
T=06	-	-	-	T4	T3	T2	T1	T0
S=07	GMU	-	-	-	-	S2	S1	S0

Bits GMU and ZCM provide the mute function as follows:

- GMU=0 and ZCM=0 for direct mute off;
- GMU=0 and ZCM=1 for mute off delayed until next zero crossing;
- GMU=1 and ZCM=0 for direct mute on;
- GMU=1 and ZCM=0 for mute on delayed until next zero crossing;

LOFF bit switches the loudness control as follows:

- LOFF=0 - V1 volume control using loudness;
- LOFF=1 - linear V1 volume control.

The control bits for V1 general volume have binary values from 111111B to 001100B in order to provide a level gain ranging between +20 dB and –31 dB with 1 dB step (table 3).

Table 3

G V1	V5	V4	V3	V2	V1	V0
+20 db	1	1	1	1	1	1
+19 db	1	1	1	1	1	0
……	……					
0 db	1	0	1	0	1	1
……	……					
-31 db	0	0	1	1	0	0

When loudness is on, the increment of the loudness characteristics is linear at every volume step in the range from +20 dB to –11 dB. The loudness characteristics stays constant for a gain ranging from –12 dB to –31 dB. For the binary values of the volume ranging from 001011B and 00000B, the gain steps between –28 dB and –31 dB are repeated.

The control bits for the second stage volume V2 provide on each separate channel i.e. fader front right, fader front left, fader rear right and fader rear left. The binary values from 111111B to 001000B provide a gain ranging from 0 dB to –55 dB with 1 dB step (table 4).

Table 4

G V2	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
0 db	1	1	1	1	1	1
-1 db	1	1	1	1	1	0
-2 db	1	1	1	1	0	1
……	……					
-55 db	0	0	1	0	0	0

The binary values from 000111B to 000000B for the volume control of second stage from any channel enable mute function. By soft volume may vary on each channel and left-right or front-rear balance function may be implemented.

The control bits for bass have binary values from 11011B to 00110B for a gain ranging from +15 db and –15 db with 1.5 db step (table 5).

Table 5

G B	B4	B3	B2	B1	B0
+15 db	1	1	0	1	1
+13.5 db	1	1	0	1	0
……	……				
+1.5 db	1	0	0	1	0
0* db	1	0	0	0	1
0 db	1	0	0	0	0
-1.5 db	0	1	1	1	1
……	……				
-13.5 db	0	0	1	1	1
-15 db	0	0	1	1	0

The binary values of the bass control ranging from 11111B to 11100B provide the +15 dB and +13.5 dB level, by means of repetition, while the values between 00101B and 00100B provide the –13.5dB and –15 dB levels. The numeric range between 00011B and 00000B disables the bass corrector.
The control bits for treble have binary values from 11001B to 01000B for a gain ranging from +12dB and –12dB with 1.5 dB step (table 6).
Table 6

G T	T4	T3	T2	T1	T0
+12 db	1	1	0	0	1
+10,5 db	1	1	0	0	0
……	……				
+1,5 db	1	0	0	1	0
0* db	1	0	0	0	1
0 db	1	0	0	0	0
-1,5 db	0	1	1	1	1
……	……				
-10,5 db	0	1	0	0	1
-12 db	0	1	0	0	0

Gain levels of +12 dB and +10.5 dB are obtained using repeatedly binary values of the treble control between 11111B and 11010B. The binary value range between 00111B and 00000B disables the treble corrector.
The binary value 00000B for bass and treble control is intended for the use of an external equalizer.

The input selection bits S connect one of the four stereo signals or the mono one, as detailed in table 7.
Table 7

Functions	S2	S1	S0
Input stereo In 1	1	1	1
Input stereo In 2	1	1	0
Input stereo In 3	1	0	1
Input stereo In 4	1	0	0
Input mono In M	0	-	-

The commands of the Hi-Fi amplifier such as on/off, input selection, setting the audio source, the first stage volume control, the left-right, front-rear balance and the fader control are all displayed on a LCD.
A M1632, two rows, 16-characters/row display module is used. The circuit HD44780 included in the module performs the display control.
The display module is connected to the microprocessor using parallel input/output ports as in figure 8; characters having ASCII codes from 20H to 7FH can be displayed (uppercase and lowercase letters, digits and punctuation marks) but also a series of special characters having ASCII codes ranging from A0H to FFH. The main features of the display module are: internal character generator, display data memory, read/write memory access and various functions for clearing, moving the cursor in the upper-left corner, enabling/disabling the display or the cursor, cursor and display shifting, blinking display and so on.

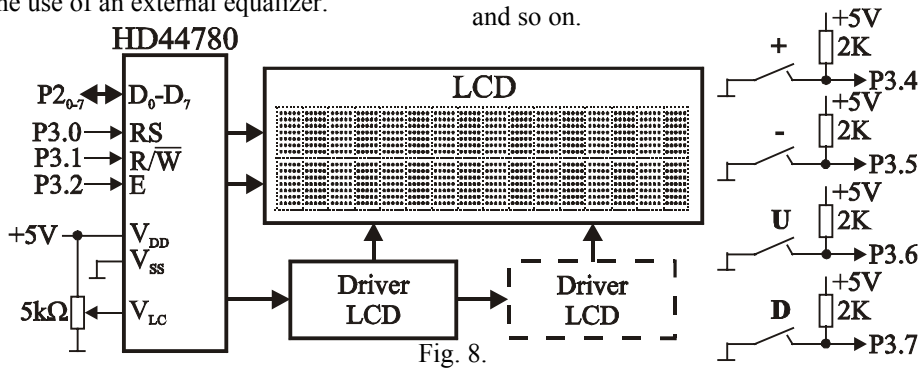

Fig. 8.

The input and edit of certain commands are made using four switches (figure 8).
Two switches (‘**U**’ - up and ‘**D**’ - down) select the current command from a list, while the other two switches (‘**+**’ increment, ‘**-**’ decrement) are used to set the current numeric value.
The command program is interrupt-based and consists of a main program and a program sequence for interrupt requests treating.
The main program detects the switches’ status, updates the software image of the process in the internal data memory of the microcontroller and displays the commands from a list on the display module.
The command list is:

1. POWER
OFF
ON
2.INPUT SELECT
In 1
In 2
In 3
In 4
(In M)
3. SOURCE SELECT
CD
DVD
Tuner
TV
CAS
Video
MIC
4. AUDIO CONTROL

Volume	*+3db*
Balance left-righ	*0 db*
Balance front-rear	*0 db*
Fader front right	*-3 db*
Fader front left	*-3 db*
Fader rear right	*-3 db*
Fader rear left	*-3 db*
Treble	*+12 db*
Bass	*+9 db*

The EEPROM data memory of the microcontroller contains the updated values of the commands set by the user, which are not to be lost at power-off.
The program sequence for handling interrupt requests, issued every 0.1 ms, performs the communication on I^2C bus between the sound fader control circuit and the microcontroller.

V. CONCLUSIONS

The hardware structure of the Hi-Fi audio chain that the paper presents, consisting of the sound fader control circuit and the power amplifier, is digitally controlled by microcontroller AT89S8252.
This structure has a minimal hardware volume thanks to the circuit selected for the application, that present many integrated features.
The authors have built in practice this application within the "The Architecture of Systems Based on Microprocessors and Microcontrollers" university laboratory.
The microcontroller selected has an EEPROM non-volatile data memory where the user settings for the audio chain functions are stored and updated, feature that compensates for the down-side of the missing I2C interface, since this interface was implemented by software.
The command program, written by the authors using machine code language, operates in real-time and takes up to 4 Kbytes of Flash program memory, while the user data structure requires some 500 bytes of the data EEPROM memory.
The software designed by the authors gives the user access to an interactive solution, based on switches and LCD, to select functions with desired operating features and parameters.

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