Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 53(67), Fascicola 1, 2008

Results of Inductor Modeling Using ASITIC and Cadence Compared to Real Austriamicrosystems Inductors Models

Srdjan Stanarevic[1], Alena Djugova[1], Mirjana Videnovic-Misic[1]

Abstract – This paper presents a comparison of spiral inductors, modeled in ASITIC and Cadence Spiral Inductor Modeler, with inductors form austriamicrosystems 0.35µm CMOS technology. The maximum Q-factor comparison for given shape and dimensions of inductor has been done with two inductors made using normal top metal and two inductors using thick top metal. The obtained results show advantages and drawbacks modeling inductors this way. Despite the limitations, the accuracy of the results that these tools provide makes them useful as a first approximation step in the design of an inductor.

Keywords: radiofrequency integrated circuit (RFIC), spiral inductor, ASITIC, Cadence, eddy current, Q-factor.

I. INTRODUCTION

Modern CMOS technologies provide high performance devices in terms of noise and cutoff frequencies, allowing RFIC's to compete with GaAs IC's with reduced costs and high production levels. Still the main obstacle in massive CMOS process introduction into the RF part is poor quality factor of integrated passive components. Especially notorious are inductors since their size and quality determine price and performance of an low-noise amplifier (LNA), voltage-controlled oscillator (VCO), power amplifier (PA). Better results may be achieved by integrating the inductors in top metal layers which are now sufficiently wide and potentially sufficiently thick that higher quality factor (Q) can be achieved.
The first problem for RFIC designer, when designing devices for low-gigahertz region, is lack of technology provided low area consumption, high-quality optimized inductors from 0.1 to 20 nH. If one chooses another option to design needed inductors with available tools new problems, such as accuracy and speed of the tools used, emerge.
Today there are a lot of software tools for modeling inductors, from EM solvers to the simple geometric calculators. Usage of EM solver software tools, such as HFSS and Sonnet can be quite expensive, time consuming and demanding very good knowledge of the physics but gives more accurate results. Alternatively, a good and simple tools like ASITIC (Analysis and Simulation of Inductors and Transformers for Integrated Circuits) [1] and Cadence [2] Spiral Inductor Modeler (SIM), may provide designers with close to optimal integrated inductors.
This paper will examine these alternative tools first describing how the tool works and next through analysis of several practical examples.

II. SPIRAL INDUCTOR MODEL

Good inductor model, valid over a wide range of frequencies, is of the utmost importance in RFIC design. That complex model takes into account most of physical phenomena which makes overall RFIC design more accurate. There are two usually used models: narrow-bandwidth Π-model [3] valid in a small-range of frequencies and wideband Π-model [4] that permits characterization of an inductor over a wide range of frequencies.
In this section will be presented inductor models used by ASITIC and Cadence SIM.

A. *ASITIC inductor model*

ASITIC is a tool for the analysis of passive elements fabricated on the Si substrate. ASITIC uses narrow-band Π-model, shown in Fig. 1, where $\mathbf{L_s}$ is serial inductance, $\mathbf{R_s}$ models the serial resistance, $\mathbf{C_{s1}}$ and $\mathbf{C_{s2}}$ represent sum of oxide capacitance between the spiral and the substrate and capacitive effects of the substrate, $\mathbf{R_{s1}}$ and $\mathbf{R_{s2}}$ model ohmic losses in the substrate, while $\mathbf{C_p}$ represents the capacitive coupling due to the electrical field between the spiral tracks and the electric field between the spiral and the cross-under.

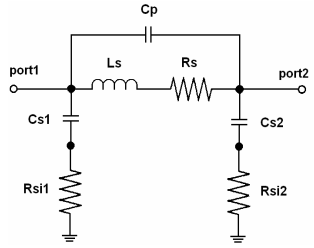

Fig. 1. ASITIC Π-model

[1] Faculty of Technical Sciences, Department for Power, Electronics and Communications engineering,
Trg D. Obradovica 6, 21000 Novi Sad, Serbia, e-mail: srdjee@gmail.com, alenad@uns.ns.ac.yu, mirjam@uns.ns.ac.yu

Parameters of the ASITIC Π-model do not really model the spiral but in fact represent the 2-port parameters of the structure at a particular frequency.
Physically L (inductance) should decrease as a function of frequency since at higher frequencies internal inductance decreases as the magnetic field is prevented from penetrating the volume of conductors reducing the inductance to its asymptotic external limit. But when the Π-model parameters for a high Q inductor are analyzed, inductance increase near the self-resonant frequency can be noticed before changing sign as the characteristic cross the self-resonant frequency. For a low Q inductor the inductance decreases monotonically.
This effect is caused by the capacitance in shunt with the inductor, which has two components, a high-Q coupling capacitance through the air/oxide and a low-Q substrate capacitance. Due to this capacitance the inductance eventually resonates resulting in negative reactance or simply capacitive behavior beyond self resonance.
Calculation of 2-port parameters of a spiral structure is managed using electromagnetic analysis with **pix** command (pix <spiral name> <freq> <spiral gnd>). There is no limitation on the structure of the spiral and thus the spiral can be an arbitrary interconnection (shunt or series) of metal segments. There is an quasi-static assumption which limits the highest frequency of analysis but usually this frequency is well beyond the self-resonant frequency of the inductor.
The basic partial inductance matrix is calculated with Grover-Greenhouse method in free air which means that any magnetic or conductive properties of the substrate are ignored. The real part of inductance matrix increases as a function of frequency as it models skin and proximity effects.
The capacitance matrix is calculated by dividing up segments in width and length only. The thickness of segments is assumed to be small enough so that charge density does not vary significantly over the thickness of the conductor. This assumption is valid form most thin IC metal layers but will result in errors for very thick metals. The 3-D capacitance matrix is calculated using the Green function which includes the lossy and coupling effects of the substrate.
The substrate back-plane is by default grounded. This default can be changed by employing a non-conductive layer as the first layer in the technology file (epoxy glue or other dielectric materials). Command **pix** have an option <spiral gnd> which enables simulation of the electrical effects of a shield. For instance, <spiral gnd> might consists of a substrate tap only or a conducting wire touching the substrate or ring of substrate contacts surrounding the inductor or metal pads etc [5]. Usually, shielding effect and potential gain in Q is modeled with a solid metal layer placed below the spiral and connected to the ground. The effect of the shield is included in the capacitance matrix but ignored by the inductance matrix calculation.
Substrate induced current losses can be introduced into the model by setting the eddy current flag ON. Now the structures with Manhattan geometries pass through the eddy current calculation engine. The results of substrate losses are introduced into the Inductance matrix more precisely only to the real part of the inductance (R_s). In reality, if significant eddy currents flow, the inductance will also decrease as substrate currents produce a magnetic field that tends to cancel the impressed magnetic field.
The self resonant frequency (SRF) f_{rez} obtained by ASITIC is just a guess. The actual SRF can be determined by finding the frequency when overall impedance is zero.
Inductor quality factors at particular frequency are also calculated by ASITIC with **pix**, **q**, **pi** commands. Parameter Q_1 represents the Q of the 2-port if the inner port of the spiral is grounded. Similarly, parameter Q_2 represents the Q looking in from the inner port and grounding the outer port. Usually Q_1 is greater then Q_2 since Q_2 has extra substrate losses associated with the bottom metal layer. For symmetric inductors Q_1 is approximately equal to Q_2. Parameter Q_3 or Q_d represents the differential Q if inductors are driven differentially. This parameter is greater then $\max(Q_1,Q_2)$ since the substrate injection is minimized [1].
As a conclusion, ASITIC includes skin and proximity effects, mutual inductance, substrate electrical and magnetic coupling with inductor.

B. *Cadence SIM*

As a part of analog design environment in Cadence, there is the SIM program for modeling spiral inductors. This program provides inductor parameters for given dimensions, shape and working frequency. The solver for the on-chip passive modeler employs a PEEC (Partial Element Equivalent Circuit) algorithm to generate macromodels for the spiral segments. Electro-static and magneto-static EM solvers are called separately, as in ASITIC, to extract the capacitive and inductive parameters of the structure.
The inductance solver is based on Fasthenry. It considers skin-depth effects, and models the substrate effect by treating the lossy layers as lossy conductor planes.
The capacitive parameter extraction solver uses the BEM (Boundary Element Method), which computes the lossy substrate using a complex Green's function, as in ASITIC, and the solver is SVD (Singular Value Decomposition) accelerated.
With the extracted parameters, a multi-Π equivalent circuit is created. Depending on the bandwidth, the modeler generates either a narrow-bandwidth or wide-bandwidth model.
In this work, narrow-bandwidth model parameters for inductors are extracted due to specified use in narrow-bandwidth LNA. The general narrow-bandwidth model is shown in Fig. 2, where every segment is represent by one Π-equivalent circuit.

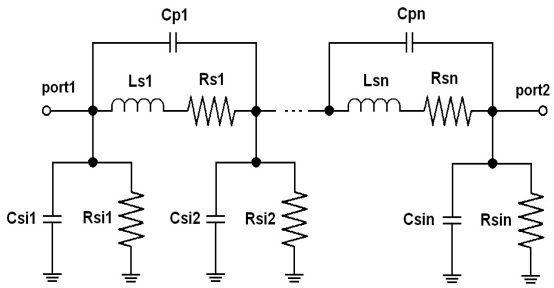

Fig. 2. Cadence model

The number of Π segments (Πs) in the equivalent circuit depends on the number of turns in the spiral inductor. For single layer spiral inductors and double layer spiral inductors with parallel connection of inductors in different layers, the number of Πs equals the number of turns. For double layer spiral inductors with series connection of inductors in different layers, the number of Πs equals twice the number of turns. Circuit parameters are as follows:

$\mathbf{L_{s1}}$, $\mathbf{L_{s2}}$, ..., $\mathbf{L_{sn}}$ – series inductances,
$\mathbf{R_{s1}}$, $\mathbf{R_{s2}}$, ..., $\mathbf{R_{sn}}$ – series resistances,
$\mathbf{C_{p1}}$, $\mathbf{C_{p2}}$, ..., $\mathbf{C_{pn}}$ – parallel shunt capacitances,
$\mathbf{C_{si1}}$, $\mathbf{C_{si2}}$, ..., $\mathbf{C_{sin}}$ – substrate capacitances,
$\mathbf{R_{si1}}$, $\mathbf{R_{si2}}$, ..., $\mathbf{R_{sin}}$ – substrate resistances

SIM does not have possibility for optimization so inductor parameters just for required dimensions, shape and working frequency can be obtained such as:

- $\mathbf{R_s}$ **(**Series Resistance): The AC resistance of the spiral at the working frequency with the skin-depth effect included.
- $\mathbf{L_s}$ **(**Series Inductance): The total inductance of the spiral inductor with the skin-depth effect included.
- **Q (**Quality Factor): The Q-factor at the working frequency.
- $\mathbf{Q_{max}}$ (Maximum Quality Factor): The maximum quality factor of the inductor within the 10 MHz to 20 GHz frequency range.
- **Frequency of $\mathbf{Q_{max}}$**: The frequency at which Q_{max} occurs.
- $\mathbf{f_{rez}}$ (Resonant Frequency): The frequency where Q = 0. The search is from 10 MHz to 20 GHz. If no resonant frequency is found, a value of -1 is displayed.

As a conclusion, SIM includes skin effect, substrate magnetic coupling, substrate electrical coupling, mutual inductance.

III. RESULTS

For accurate technology specific simulation results process files for both ASITIC and Cadence SIM have to be created. These files contain confidential information about technology process such layer thickness, resistivity and permittivity for both the metal and the substrate layers.

In order to verify accuracy of the inductors generated by ASITIC and Cadence SIM, simulation results were compared with austriamicrosystems ( ) foundry

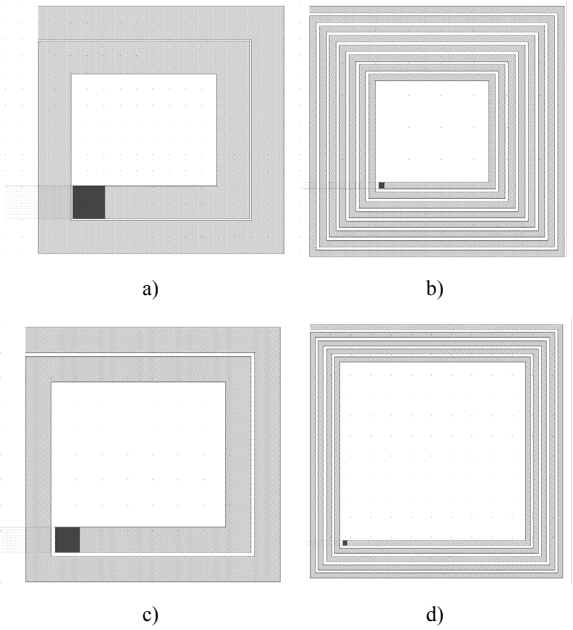

Fig. 3. Inductors generated with ASITIC:
a) sq1, b) sq2, c) sq3, d) sq4

provided inductors' Π model with the same geometry and technology specifications. From the shape and dimensions of specific inductors in 0.35µm austriamicrosystems CMOS technology geometry parameters of the inductors have been measured and given in Table 1. Geometry parameters are defined as follows: outer diameter – $\mathbf{d_{out}}$, width of the metal strip – **w**, space between neighboring segments – **s**, number of turns – **n**, input path length – $\mathbf{l_{inp}}$ and return path length – $\mathbf{l_{ret}}$.

Table 1. Geometry parameters of austriamicrosystems inductors

	$\mathbf{d_{out}}$ [µm]	**w** [µm]	**s** [µm]	**n**	$\mathbf{l_{inp}}$ [µm]	$\mathbf{l_{ret}}$ [µm]
sq1	300	40	2	1.75	54	110
sq2	155	4	2	7.75	50	100
sq3	200	20	3	1.75	70	112
sq4	250	5	3	4.75	54	91

Based on technology and geometry parameters, inductors have been generated in ASITIC, shown in Fig. 3, and Cadence SIM. Inductors with the shape sq1 and sq2 were simulated using normal top metal while inductors sq3 and sq4 were simulated using thick top metal. Simulation results of $\mathbf{Q_d} = \mathbf{Q_{max}}$, $\mathbf{L_s}$, $\mathbf{R_s}$ and $\mathbf{f_{rez}}$ for inductors are given in Table 2.

Two simulations, with and without solid shield, have been done in ASITIC in order to see what effect it has on the inductance and serial resistivity. In both cases eddy current flag was set ON. From results presented in Table 2 can be seen that there are inductor inductance decrease and resistance change after shield introduction.

Negative R_s value for ASITIC sq4 model at frequency 5 GHz is physical attributed to capacitive domination in inductor behavior as a result of increased thickness and more capacitive coupling structure.

Table 2. Simulation results obtained with ASITIC and Cadence SIM

	f [GHz]		L_s[H]	R_s[Ω]	Q	Q_{max}	f_{rez} [GHz]
sq1	1.575	Cadence	1.13n	1.98	5.17	7.55@3.17GHz	5.55
		ASITIC	1.21n	3.94	2.99	4.18@6.65GHz	11.48
		ASITIC shield	1.20n	3.92	2.99	4.14@6GHz	9.29
	2.4		1.34n	n/a	6.1	6.8@3.8GHz	>6
		Cadence	1.12n	2.08	6.58	7.18@3.19GHz	5.57
		ASITIC	1.20n	4.99	3.51	4.18@6.65GHz	12.85
		ASITIC shield	1.18n	4.93	3.51	4.14@6GHz	11.48
	5		1.38n	n/a	6.2	6.8@3.8GHz	>6
		Cadence	1.11n	2.26	3.03	6.61@3.25GHz	5.59
		ASITIC	1.19n	8.11	4.11	4.18@6.65GHz	17.05
		ASITIC shield	1.09n	6.89	4.10	4.14@6GHz	9.81
sq2	1.575	Cadence	9.06n	36.59	2.11	2.62@2.55GHz	4.47
		ASITIC	9.15n	35.22	2.44	5.59@5.5GHz	6.97
		ASITIC shield	8.98n	34.95	2.44	6.05@6GHz	6.06
	2.4		9.98n	n/a	3.3	3.5@3.3GHz	>6
		Cadence	9.05n	36.84	2.59	2.6@2.55GHz	4.47
		ASITIC	9.19n	34.23	3.60	5.59@5.5GHz	7.46
		ASITIC shield	8.88n	34.72	3.61	6.05@GHz	7.6
	5		12.7n	n/a	2.5	3.5@3.3GHz	>6
		Cadence	9.04n	38.21	-1.59	2.51@2.55GHz	4.47
		ASITIC	9.47n	27.84	5.50	5.59@5.5GHz	9
		ASITIC shield	7.58n	25.85	5.80	6.05@6GHz	6.55
sq3	1.575	Cadence	970p	1.10	8.46	21.99@6.01GHz	10.69
		ASITIC	937p	2.28	4.02	5.39@11.4GHz	19.43
		ASITIC shield	935p	2.28	4.02	5.38@11GHz	16.88
	2.4		1.04n	n/a	8.7	11.9@4.4GHz	>6
		Cadence	965p	1.161	14.87	21.15@6.07GHz	10.73
		ASITIC	930p	2.99	4.58	5.39@11.4GHz	21.03
		ASITIC shield	924p	3	4.59	5.384@11GHz	17.11
	5		1.05n	n/a	11.8	11.9@4.4GHz	>6
		Cadence	959p	1.26	18.52	19.48@6.15GHz	10.75
		ASITIC	924p	5.15	5.29	5.39@11.4GHz	26.25
		ASITIC shield	899p	5.025	5.31	5.38@11GHz	17.45
sq4	1.575	Cadence	9.63n	10.08	7.62	8.24@2.05GHz	3.69
		ASITIC	9.66n	9.32	8.34	11.1@3.3GHz	5.44
		ASITIC shield	9.43n	10.26	8.39	11.97@3.4GHz	4.93
	2.4		12.08n	n/a	6.8	7.2@2.0GHz	>6
		Cadence	9.61n	10.66	7.52	7.83@2.07GHz	3.69
		ASITIC	9.70n	7.34	10.41	11.1@3.3GHz	5.83
		ASITIC shield	9.08n	10.09	10.71	11.97@3.4GHz	5.048
	5		19.23n	n/a	1.1	7.2@2.0GHz	>6
		Cadence	9.56n	12.59	-12.9	6.67@2.09GHz	3.69
		ASITIC	10.2n	-9.7	9.4	11.1@3.3GHz	7.05
		ASITIC shield	7.47n	2.50	11.09	11.97@3.4GHz	5.58

Value of quality factor Q for sq2 and sq4 inductors obtained from Cadence SIM at frequency 5 GHz is negative as inductors operating frequency is higher than f_{rez} where Q decreases to 0.

The inductance of the ASITIC and Cadence SIM designed inductors decreases with the frequency increase. This behavior is not in agreement with austriamicrosystems where inductance increases with frequency increase, especially at high frequencies. The larger the inductance the higher is the difference between those results. It can be noticed that inductance deviation from the austriamicrosystems obtained value is smaller for ASITIC generated inductors, while quality factor deviation from the austriamicrosystems obtained values is smaller for Cadence SIM generated inductors.

Concerning quality factor of sq3 and sq4 inductors it is shown that there is significant difference between obtained values. Cadence SIM gives much higher values while ASITIC gives smaller values than austriamicrosystems reference.

Comparison of SRF for different tools can not be done as ASITIC gives not even approximate values. However, it can be noted that Cadence SIM gives SRF values close to austriamicrosystems data.

IV. CONCLUSIONS

Generating technology description files for ASITIC and Cadence SIM is taken very seriously concerning our knowledge about specific technology parameters so obtained results may differ.

It is noticed that the usage of ASITIC and Cadence SIM is justified only for frequencies below 5 GHz and inductors made in standard metal.

Moreover, Cadence SIM gives slightly better results and since it is a part of Cadence tools it can easily be used for modeling, simulation and layout design of inductors for one who does not have needed inductors in technology which is using nor third party software tools for inductor design.

REFERENCES

[1] www.eecs.berkeley.edu/-niknejad/asitic.html

[2] www.cadence.com

[3] Nguyen N., "A 1.8GHz Monolithic LC Voltage-Controlled Oscillator", *IEEE Journal of Solid State Circuits*, vol. 27, March 1992.

[4] José R. Sendra, Javier del Pino, Antonio Hernández, Benito González, Javier García,Andrés , García-Alonso and Antonio Nunez, "Integrated Inductors Modeling for Library Development and Layout Generation", *Journal of Analog Integrated Circuits and Signal Processing*, 35, 121–132, 2003

[5] Jaime Aguilera and Roc Berenguer, *"Design and Test of Integrated Inductors for RF Applications"*, Dordrecht, Kluwer Academic Publishers, 2003.