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CMOS Current Conveyor for High-Speed Application

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Abstract – The work presents the possibility of using CMOS current conveyors for high speed application. It is used a simple current conveyor bidirectional, self-biased, where the static current is not imposed by auxiliary current sources. One shows the deduction of the self-biasing current equation, which depends especially on the transistor channel width and the supply voltage. The simulation results are presented which confirm the correct and precise calculation and behavior of these conveyors and.

Keywords: CMOS, current conveyor, self-biased current conveyor.

I. INTRODUCTION

The analog circuits are more and more included in VLSI circuits, performed in simple and low-cost CMOS technology, destined especially to digital processing techniques.

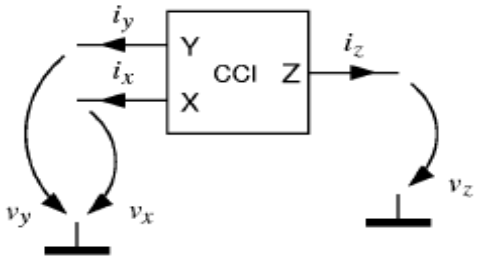

Fig.1. First-generation current-conveyor symbol

To assure the precision in these analog circuits, missing the operational amplifiers which do not attain the necessary quality with CMOS transistors, one applies a new type of circuits, included in the general category of "non-conventional-principle circuits" [1].

From these, one uses frequently the current-mode ones, with basic exponent – the current conveyor. The first-generation current conveyor has a symbol given in Fig.1.

The definition matrix and the voltage and current equations of a first-generation current conveyor have the form:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

$$\Rightarrow \begin{cases} i_x = i_y = i_z \\ v_x = v_y \end{cases}$$

The function accuracy of these circuits is achieved with the help of the geometric precision of the transistor pairs in CMOS process. The conveyor basic elements are the current mirrors, where, assuring close drain-source voltages for the two branch transistors, one avoids the Early effect and one obtains a very good current symmetry. To obtain a very good matching in the current mirrors it is necessary to apply special strategies in layout design. The designer aims to assure the same physical dimensions and threshold voltages for the processed transistors, but also the similar neighboring effects (compensated by dummy transistors), the same distance versus the well boundary, symmetrical exposure to temperature gradient, etc.

In the general case of using first-generation current conveyor, which are the simplest ones, one introduces a forced current biasing [2], we observed the possibility of self-biasing, the standing current being imposed by the transistor channel width and the supply voltage. Thus, the first-generation current-conveyor schemes become simpler and may be used in applications. Eventually, it is necessary to attach a simple start circuit to conveyors.

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II. SELF-BIASING-CURRENT CALCULATION IN A BIDIRECTIONAL CCI+

The generation I self-biased bidirectional current-conveyor scheme is showed in Fig.2. It is of CCI+ type because the output-current direction is the same as the input current one.

To analyze the standing regime the inputs will not be supplied by currents, thus the output do not furnishes current to, and, thanks to the vertical symmetry, the input and output voltages will be theoretically null. To achieve this it is still necessary to establish the p-MOS transistor width greater than the n-MOS one so that their transconductances become equal. In the designing process the widths are adjusted so that the input and output voltages to be roughly null.

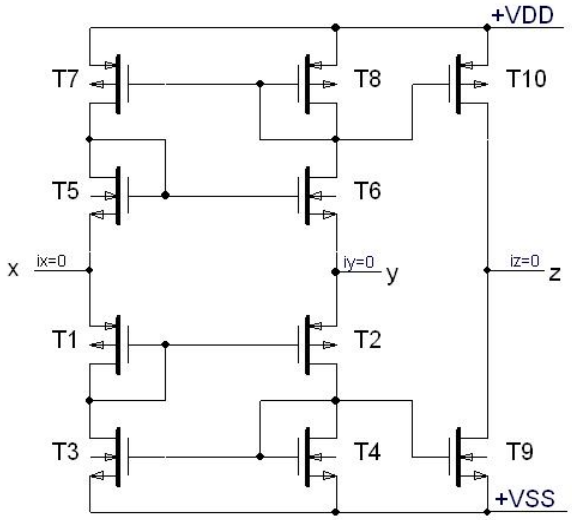

Fig.2. The generation I self-biased bidirectional current-conveyor scheme (CCI+).

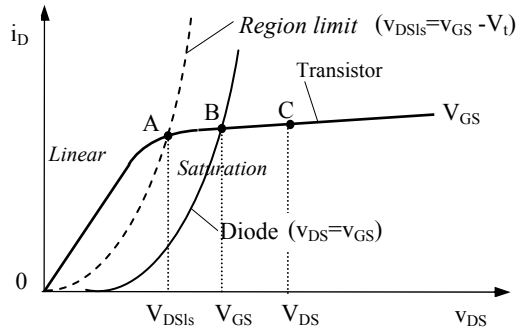

Fig.3. MOS transistor and diode characteristics

In the following calculation one will use the saturation drain-current equations, resulting for the B and C points on a transistor output static characteristic (Fig.3). The point B corresponds to a "diode"-connected transistor and the point C – to a normal transistor, which may bring a greater v_{DS} voltage. The point A corresponds to the saturation-region limit and is located on the square parabola given by the equation:

$$i_D = \frac{K}{2}(v_{GS} - V_t)^2 = \frac{K}{2}v_{DS}^2 \qquad (1)$$

This approximate equation shows that in the point A exist a static characteristic discontinuity [3], [4] because, immediately in the right part of this point (in the saturation region) another current equation is valid:

$$i_D = \frac{K}{2}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \cong \frac{K}{2}v_{DS}^2(1 + \lambda v_{DS}) \qquad (2)$$

Since in the simulation of CMOS schemes this discontinuity may produce some problems, the transistor models use also in the linear region a more precisely current equation, which includes the channel-length modulation effect, it signifies the factor. Thus, the above discontinuity is eliminated.

The current in the point C respects with sufficient accuracy the equation:

$$i_D = \frac{K}{2}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \qquad (3)$$

The point B is located on a curve similar to a diode characteristic, having the voltage drop $v_{DS}=v_{GS}$, in next equation (4):

$$i_D = \frac{K}{2}(v_{DS} - V_t)^2(1 + \lambda v_{DS}) = \frac{K}{2}(v_{GS} - V_t)^2(1 + \lambda v_{GS}) \qquad (4)$$

Thus, for the branches including the transistors T1 and T3 respectively T2 and T4 one may write the drain-current equations, supposed the same in both the branches, admitting the following: the conveyor up and down half-circuits are symmetric, the transistors are in saturation (the diode transistor are evidently in saturation) and all the transistors have the same transconductance K:

$$\text{(for T1)} \quad I_{Do} = \frac{K}{2}(V_{GSp} - V_{tp})^2(1 + \lambda_p V_{GSp}) \qquad (5)$$

$$\text{(for T2)} \quad I_{Do} = \frac{K}{2}(V_{GSp} - V_{tp})^2(1 + \lambda_p V_{DSp}) \qquad (6)$$

$$\text{(for T3)} \quad I_{Do} = \frac{K}{2}(V_{GSn} - V_{tn})^2(1 + \lambda_n V_{DSn}) \qquad (7)$$

$$\text{(for T4)} \quad I_{Do} = \frac{K}{2}(V_{GSn} - V_{tn})^2(1 + \lambda n V_{GSn}) \qquad (8)$$

For the implicated here voltages one may write to, supposing $vx=vy=0$, the equations:

$$V_{DSn} + V_{GSp} = V_{DD} \qquad (10)$$

$$V_{DSp} + V_{GSn} = V_{DD} \qquad (11)$$

Comparing the current equations for transistors T1 and T2 respectively T3 and T4 it is visible that:

$$V_{GSp} = V_{DSp} \qquad (12)$$

$$V_{GSn} = V_{DSn} \qquad (13)$$

This means all the same-type transistors (*p* or *n*) from the scheme have in standing regime the same B operation point (that is they are in saturation as admitted), so, the transistor and the diode in an horizontal pair have the same voltage drop $V_{DS}=V_{GS}$. Having close-value voltages V_{GSp} and V_{GSn} , it also means these voltages come close to value *VDD/2*.

If now equals the right members of equations (5) and (7), substitutes $V_{DSn}=V_{GSn}$ and simplifies *K/2* one obtains equation (14):

$$(V_{GSp}-V_{tp})^2(1+\lambda_p V_{GSp})=(V_{GSn}-V_{tn})^2(1+\lambda_n V_{GSn}) \quad (14)$$

Having $Vt_p > Vt_n$, $\lambda_p > \lambda_n$ this equality seems be possible even in the situation when the p and n transistors have not the same transconductance.

The equation (14) may be written using the relations (10) and (13):

$$\begin{aligned}&(V_{GSp}-V_{tp})^2(1+\lambda_p V_{GSp})=\\&=(V_{DD}-V_{GSp}-V_{tn})^2[1+\lambda_n(V_{DD}-V_{GSp})]\end{aligned} \quad (15)$$

From this, after parenthesis detachment and term ordering, one obtains a third degree equation (16) in V_{GSp}:

$$\begin{aligned}&(\lambda_p+\lambda_n)V_{GSp}^3-[3\lambda_n V_{DD}+2(\lambda_p V_{tp}-\lambda_n V_{tn})]V_{GSp}^2+\\&+[V_{DD}(2+3\lambda_n V_{DD}-4\lambda_n V_{tn})]V_{GSp}-\\&-[2(V_{tp}+V_{tn})+\lambda_p V_{tp}^2+\lambda_n V_{tn}^2]V_{GSp}\\&-(1+\lambda_n V_{DD})(V_{DD}-V_{tn})^2+V_{tp}^2=0\end{aligned}$$

Direct solution of this equation is difficult but this may be solved (heaving a single real root) by trials, knowing that $V_{GSp}\approx VDD/2$ but some smaller. Another solution is to use equation solving programs like Matlab or Octave.

III. PRACTICAL DESIGN CONSIDERATIONS

Today we face with a rapid increasing in integrated circuits design and productions. In the same time there are new and powerful CMOS technologies. In the same time with scaling of the CMOS transistor features the models for simulations became very complex. Older technology with feature size greater than 5µm used only few simple equations and some parameters (Spice LEVEL 1 model). New technologies lower than 1µm use for spice simulations many equations and a lot of empirical parameters. Our 0.35µm CMOS technology uses for spice modeling of the MOS devices about 16 pages of equations and almost 150 parameters (Spice LEVEL 7).

Always, the IC designer starts the project with hand calculations. It will be used the well known MOS equation (3) that correspond to Spice LEVEL 1 modeling. But the results are far from simulation results (using Spice LEVEL 7). As the technology grows, hand calculation is less precisely.

However there is a way to obtain hand calculations results close to simulation results. It is necessary to obtain precise values for some parameters that are includes in MOS transistor equations:

Table1.

Vt0
λ
K’
Vgs – Vt0

These parameters can be obtained from simulations, from pMOS and nMOS transfer characteristics [6]. We choose the geometric dimensions W and L for transistors and get from simulations the transfer characteristics. Using MOS equations applied on these characteristics we can compute the parameters from Table 1, and the values are listed in Table 2.

Table2.

Parameter	**NMOS**	**PMOS**
W	20µ	20µ
L	1µ	1µ
Vt0	0,759 V	0,807 V
λ	0,029 V^{-1}	0,0408 V^{-1}
K’	87.35 µA/V^2	37.74 µA/V^2
Vgs – Vt0	0,241 V	0,193 V
Vds = Vgs	1 V	1 V
Ids	52,15 µA	14,6 µA

Based on Table 2 and using the geometric scaling method [7] we can compute the currents and dimensions for any transistors.

But we must notice that large changing of the W and L dimensions from Table 2 will change operating point and leads to changing of process parameters in Table 2. In this case, the hand calculation can give big errors.

Using Table 2 and the obtained by calculation V_{GSp} value may be determined the current I_{Do} from equation (11). This will represent the static conveyor self-biasing current. Thus, for a conveyor heaving the scheme in Fig. 2, with transistors in 0.35µm CMOS process, VDD=2,5V, VSS=-2,5V, L=1µm, Wn=8.65µm, Wp=20µm, one obtains V_{GSp}=1.272V. The voltage V_{GSn} represents the difference from *VDD* hence V_{GSn}=1.228V. So, the self-biasing-current value will be I_{D0}=86µA.

If a fast evaluation of the self-biasing current is wanted, it is possible to consider $V_{GSp}\approx VDD/2$.

The first-generation conveyor CCI- scheme is shown in Fig.4. With the help of two complementary mirrors the output current direction is changed by comparison with the CCI+ in Fig.2. The above calculations for the CCI+ conveyor are valid for this conveyor to.

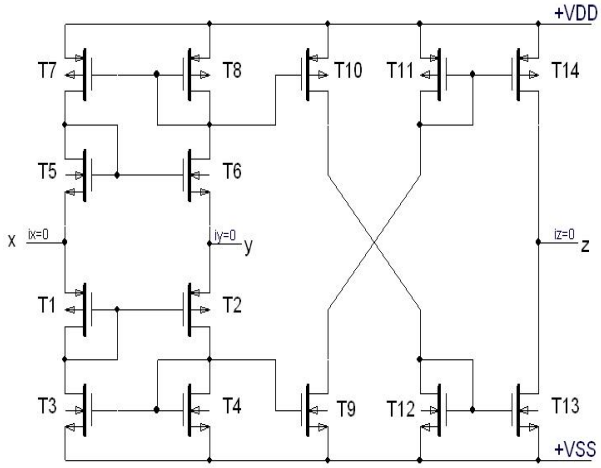

Fig. 4. Bidirectional self-biasing CCI- scheme

IV. SIMULATION RESULTS

The obtained by calculations I_{D0} and V_{GS} values help to evaluate physical dimensions of conveyor transistors. For simulation we use PSpice. The simulation in a static regime of the conveyors in Fig.2 and Fig. 4, with above transistor dimensions, gives the current I_{D0}=85.7μA, very close to the calculated one (86μA). The same current is observed in the output branch to. The established by self-biasing input voltages v_x, v_y and the output voltage v_z are of negligible value (close to 0).
The simulation scheme is presented in Fig. 5.

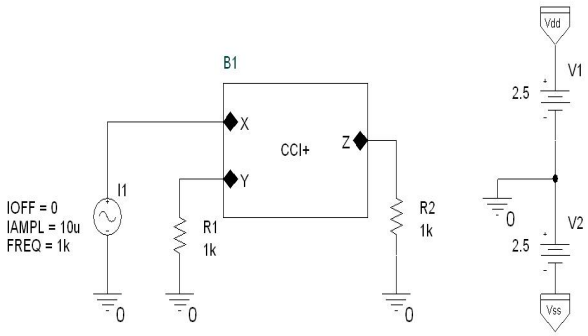

Fig. 5. Dynamic simulation circuit

The current conveyors have been simulated in dynamic regime to. Fig.6 shows the time domain simulation, when on the conveyor input has been applied a sine current. At the output is mirrored the input form and value, the phase difference of those depending of the topology – CCI+ or CCI-.

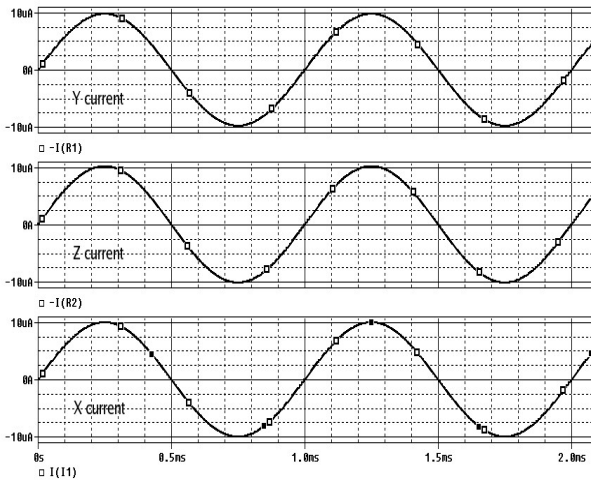

Fig.6. Sine input and output simulated conveyor currents

First generation current conveyor acts different regard to its inputs X and Y. One input, X is "current" input, Y input is "voltage" input. A current forced into X input will "convey" a same amount of current into Z output and also into Y input, regardless load on this ports. A voltage set on Y input will force the same voltage on port Y.

The studied self-biasing current conveyors have a precise linear region of the transfer characteristic. The DC simulation proves it. This is presented in Fig.7. The linear current range is some greater than the standing current I_{Do} as observes in figure. It is present a current range from -100μA to +100μA. At value $i_x \approx I_{Do}$=85.7μA the non-linearity of the transfer characteristic is close to 2%.

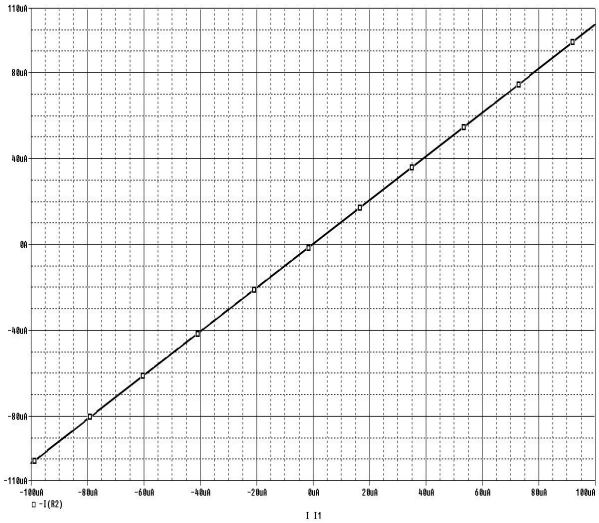

Fig. 7 . Transfer characteristic iz=f(ix) obtained by simulation.

AC simulation results are presented in Fig. 8. The tested current conveyor has a bandwidth of 180MHz, at small signal. The circuit is intrinsic "current mode" circuit so frequency of operation is high. Also there is no feedback and no stability problems.

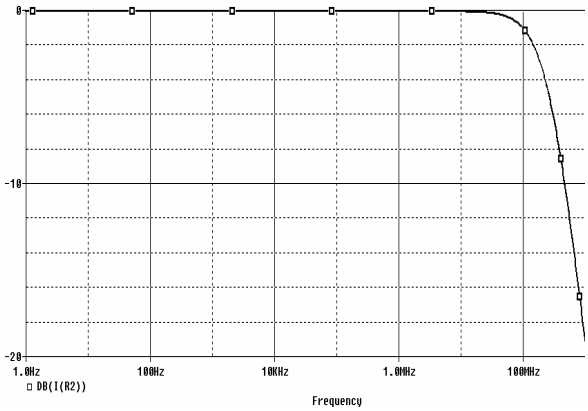

Fig. 8 Frequency characteristic

Current conveyor acts at the output like a current source. One of the most important characteristic of the current conveyor is the output impedance. This impedance must be as big as possible. Our current conveyor has 400kΩ output impedance from dc to 1MHz output frequency. The output impedance characteristic is plotted in Fig. 9.

Fig.9. Output impedance characteristic

V. CONCLUSIONS

The work presents the possibility of using simple CMOS first-generation bidirectional current conveyors where the static current is not imposed by auxiliary current sources. One shows the deduction of the self-biasing current equation, which depends especially on the transistor channel width and the supply voltage. Also it is presented a methodology to keep the hand calculations at the begining of design in reasonable error limits. The simulation results, for 0.35μm CMOS process, are presented which confirm the correct and precise behaviour of these conveyors. The bandwidth of the conveyor resulted of 180MHz for small signal. The standing current, calculated as 86μA was measured in the simulation as 85.7μA which denotes a very good precision of the theoretical calculation. A very good linearity of the transfer characteristic was obtained in a current range equal to the self-biasing current. Also the output impedance is high on very large frequency bandwidth 0 to 1MHz.

VI. FUTERE WORK

The current conveyor has a lot off application in analog designs due to its intrinsic current mode operation. High speed circuits require small amount of electric charge to be moved, - small voltage shift, and thereby current mode circuits.
Our goal is to use this kind of simple self-biased current conveyors to build high speed, high precision, low cost sine oscillators in CMOS.
Another feature of this is high output impedance. The output impedance can be increase changing output topology (e.g. cascode structure). Such a circuit with high output impedance (>1MΩ over all frequency bandwidth) and high bandwidth (>1MHz) it is ideal for EIT (electric impedance tomography).

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