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New Control for Charge Pump Buck Converter

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Abstract – The paper proposes a new voltage control methodology for the "Charge Pump Buck Converter". During each commutation, the converter pumps a defined charge to the load circuit. The original circuit was improved and is able to control the output current both through the switching frequency and through the amount of electrical charge which is delivered to the load during each commutation. The control through the charge is very efficient for low rates between output voltage and input voltage. The main equations that can be used for the converter's design are also presented in the paper.

Keywords: dc/dc power converter

I. INTRODUCTION

The circuit presented in this paper tries to respond to present dc/dc converters' demands: high reliability, fast transient response and small values for the passive L-C components involved both in the converter topology and in the dc output filter's circuit. The circuit presented in Fig.1 assures high reliability and a less power switcher's stress due to zero current switch (ZCS) for all turn off commutations. The output frequency of the output current pulses is two times greater than the devices' switching freque variation.

II. OPERATION PRINCIPLES AND OPERATION

The circuit scheme of the proposed converter is shown in Fig.1. The circuit is composed by switches $S_1 \div S_4$ and capacitor C, which is equivalent to a controlled switch, the equal inductances $L_1=L_2=L$ and the switches S_5 and S_6 used as controlled turn on diodes. One time the switches S1 and S3 are turned on and the switches S_2 and S_4 are turned off and the input current i_i (Fig.1) flows through inductance L_1 . When the voltage across S_5 riches a defined value ($u_{S5}=U_X \geq 0$), the S_5 is turn on and the current i_{L1} is transferred through device S_5 . The other time the switches S_2 and S_4 are turned on and the switches S_1 and S_3 are turned off and the input current i_i flows through inductance L_2 . Device S_6 will assure the current flows through inductance L_2 in the same conditions as device S_5 . During the commutation process, the voltage across capacitor C varies between the limits $\pm(U_i+U_X)$ where U_X represents the positive voltage across S_5 or S_6 that determines the turn on command of these devices and U_i is the input dc voltage.

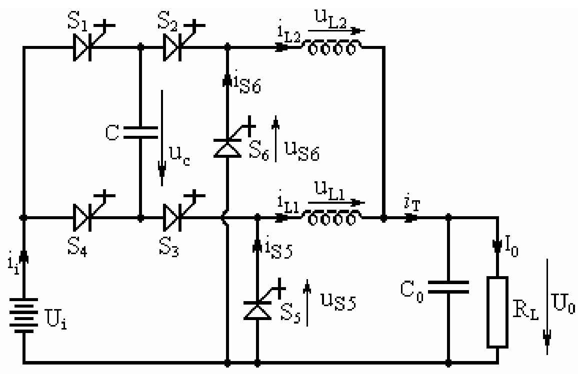

Figure 1. Proposed circuit topology

With respect to the shape of the inductance current i_{L1} and i_{L1}, two conduction modes can be performed:

- Discontinuous operation mode, when the current through the inductor L_1 or L_2 has zero value intervals.
- Continuous operation mode, when the current through the inductor L_1 or L_2 has no zero value intervals.

III. DISCONTINUOUS MODE OPERATION

Discontinuous operation mode is described in Fig.2. There are six stages. The voltage across the capacitor C, the currents $i_{S1}=i_{S3}$, the voltage u_{S5} and the current i_{S5} are plotted with continue line the current i_{L2} and the voltage u_{S6} are plotted with dot line.

D.1. The First stage

The First stage [$t \in (t_{0d1}\ ;\ t_{1d1})$] starts at t_{0d1} when S_1 and S_3 are soft (ZCS – zero current switch) turned on. The voltage across capacitor C at point t_{0d1} is $-(U_i+U_X)$. In this stage, the resonant L_1-C circuit

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assures a resonant charge of the capacitor C, from $-(U_i+U_X)$ to $+(U_i+U_X)$. For this stage the input current $i_i(t)$ is equal to inductance current $i_{L1}(t)$ (Fig.2). The equivalent circuit for this stage is plotted in Fig.3. The equations which describe the behaviour of the circuit are:

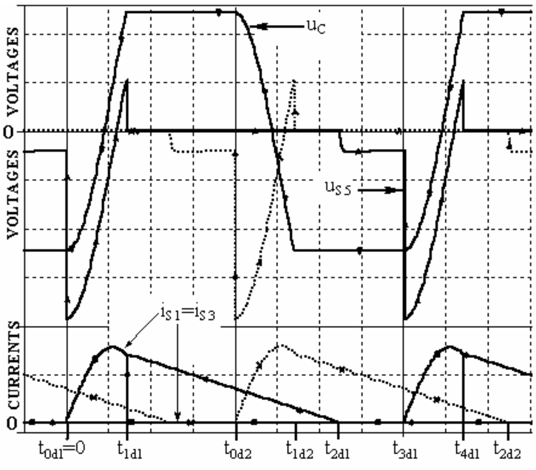

Fig. 2. Discontinuous mode circuit operation

$$U_i = u_C(t) + u_{L1}(t) + U_0 \qquad (1)$$

We suppose that the input voltage U_i and the output voltage U_0 have constant DC values.
The relations (2) are also available.

$$u_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} \qquad u_C(t) = \frac{1}{C}\int i_{L1}(t) \qquad (2)$$

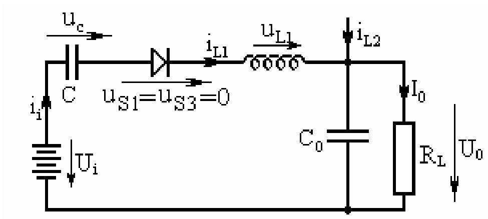

Fig. 3. Equivalent circuit for stage 1

Relations (2) are inserted in equation (1) and equation (3) might found out:

$$\frac{d^2 i_{L1}(t)}{dt} + \omega_0^2 i_{L1}(t) = 0 \quad \text{where} \quad \omega_0^2 = \frac{1}{L_1 C} \qquad (3)$$

At the point t_{0d1}=0 the values of the current through the inductance and voltage across capacitor C are:

$$i_L(t_{0d1}=0) = 0 \quad \text{and} \quad u_C(t_{0d1}=0) = -(U_i+U_X) \qquad (4)$$

From equation (1) the voltage across inductance, at point t_{0d1} is :

$$u_L(t_{0d1}=0) = U_i - u_C(t_{0d1}) - U_0 = 2U_i + U_X - U_0 \qquad (5)$$

Solving equation (3) according to the initial conditions (4) and (5), the main circuit's electric parameters may be found out:

$$\begin{aligned} i_L(t) &= C\omega_0(2U_i + U_X - U_0)\sin\omega_0 t \\ u_C(t) &= U_i - U_0 - (2U_i + U_X - U_0)\cos\omega_0 t \\ u_L(t) &= (2U_i + U_X - U_0)\cos\omega_0 t \end{aligned} \qquad (6)$$

The voltage across switch S_5 (Fig. 1.), is:

$$u_{S5}(t) = -U_0 - (2U_i + U_X - U_0)\cos\omega_0 t \qquad (7)$$

At the point t_{0d1}=0, the voltage across switch S_5 is $-(2U_i+U_X)$ and represents the maximum reverse voltage of this device. At the point t_{1d1} , the voltage across switch S_5 is $U_X \geq 0$, and S_5 is turn on. The point t_{1d1} can be found out from equation (7):

$$t_{1d1} = \frac{1}{\omega_0} arccos\left(-\frac{U_0 + U_X}{2U_i + U_X - U_0}\right) \qquad (8)$$

At the point t_{1d1} the voltage across capacitor C has a maximum value of:

$$u_C(t_{1d1}) = U_i + U_X \qquad (9)$$

The capacitor C must be a bipolar one with a breakdown voltage larger than (U_i+U_X).

The maximum current I_{LMd} through the inductance is performed when $\omega_0 t=0.5.\pi$ (from equation 6).

At point t_{1d1} the current I_{1d1} through the inductance L_1 may be found out from equations (6) and (8).

$$I_{LMd} = i_{L1}\left(\frac{\pi}{2\omega_0}\right) = C\omega_0(2U_i + U_X - U_0) \qquad (10)$$

$$I_{1d1} = i_{L1}(t_{1d1}) = 2C\omega_0\sqrt{U_i^2 + U_iU_X - U_iU_0 - U_0U_X} \qquad (11)$$

In case $U_X = 0$, S_5 is soft turn on, and it behaves as a diode.

D.2. The Second stage

The Second stage [$t \in (t_{1d1} ; t_{2d1})$] starts at point t_{1d1} when the voltage across capacitor C is (U_i+U_X), switch S_5 turns on and the currents through S_1 and S_3 becomes zero. During this stage the devices S_1 and S_3 may be soft (ZCS) turned off before point t_{2d1} . The currents $i_{L1}(t)$ and $i_{S5}(t)$ are equal and linearly decrease to zero in the time interval $t_{1d1} \div t_{2d1}$. The equivalent circuit for this stage is presented in Fig.4.

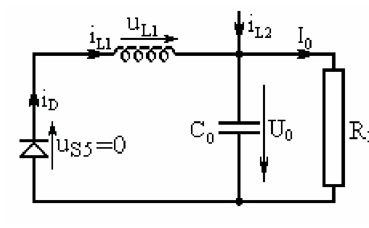

Figure 4. Equivalent circuit for stage 2

The equations that describe the behaviour of the circuit are:

$$\begin{aligned} u_{L1}(t) &= L_1 \frac{di_{L1}(t)}{dt} \qquad t \in [t_{1d1}, t_{2d1}] \\ u_{L1}(t) &+ U_0 = 0 \end{aligned} \qquad (12)$$

Solving the equation (12) according to the restriction presented in relation (11), the current variation through inductance L, may be found out:

$$i_L(t) = -\frac{U_0}{L_1}(t - t_{1d1}) + 2C\omega_0\sqrt{U_i^2 + U_iU_X - U_iU_0 - U_0U_X}$$
$$t \in [t_{1d1}, t_{2d1}] \quad (13)$$

From the equation (13), the point t_{2d1} when the current $i_{L1}(t)$ becomes zero, may be found out:

$$t_{2d1} = t_{1d1} + \frac{2}{\omega_0 U_0}\sqrt{U_i^2 + U_iU_X - U_iU_0 - U_0U_X} \quad (14)$$

D.3. The Third stage

The third stage [$t\in(t_{2d1} ; t_{3d1})$] is characterized by zero current values for all semiconductor devices. In this stage the load is fed by the energy stored in the output capacitor C_0, and by the current which flows through L_2. The next three stages are associated to the contribution of the current i_{L2} to the output current i_T, (Fig.1).

D.4. The Fourth stage

The fourth stage [$t\in(t_{0d2} ; t_{1d2})$] starts at t_{0d2} when S_2 and S_4 (Fig.1) are soft (ZCS – zero current switch) turned on. In this stage, the resonant L_2-C circuit assures a resonant charge of the capacitor C, from $+(U_i + U_X)$ to $-(U_i + U_X)$. For this stage the input current $i_i(t)$ is equal to inductance current $i_{L2}(t)$. Due to this fact, the equivalent circuit from Fig.3 is valid, but the capacitor C is connected in a reversed position. All the equations presented till now are valid with the correction (15).

$$\begin{aligned} &u_C(t) \to -u_C(t) \\ &L_1 \to L_2 \\ &i_{L1}(t) \to i_{L2}(t) \\ &t_{0d1} \to t_{0d2} = 0.5\cdot(t_{0d1} + t_{3d1}) \\ &t_{nd1} \to t_{nd2} \quad were \quad n = 1;2;3; \end{aligned} \quad (15)$$

The currents behaviour is similar to those described in the first stage. At the point t_{1d2} the voltage across capacitor C is $-(U_i + U_X)$ (see Fig. 1 and Fig,2). The devices S_2 and S_4 naturally turn off because the current flow is transferred to device S_6.

D.5. The Fifth stage

In this stage [$t\in(t_{1d2} ; t_{2d2})$] the current through the inductance L_2 (Fig.1, 2 and 3) linearly decreases to zero. The equations (12), (13), (14) and the equivalent circuit plotted in Fig. 4 are also valid. The turn off command for the devices S_2 and S_4 (Fig.1) may be performed in this stage too.

D.6. The Sixth stage

This stage is similar to the third stage (Fig.2). The currents through the inductance L_2 and through the switch S_6 are zero, and the load is fed by the energy stored in the output capacitor C_0 and by the current $i_{L1}(t)$.

IV. ENRGETIC EVALUATION

During the first and the fourth stage, the input source U_i, delivers to the circuit a charge quantity equal to:

$$\Delta Q = \int_{t_{0d1}}^{t_{1d1}} i_{L1}(t)dt = C[u_C(t_{1d1}) - u_C(t_{0d1})] = 2C(U_i + U_X) \quad (16)$$

That means that for each turn on operation, the input source U_i, delivers to the circuit a quantity of energy ΔW, equal to:

$$\Delta W = \int_{t_{0d1}}^{t_{1d1}} U_i \cdot i_{L1}(t)dt = U_i\cdot\Delta Q = 2CU_i(U_i + U_X) \quad (17)$$

The power absorbed from the input source is:

$$P_i = \Delta W f = 2fCU_i(U_i + U_X) \quad (18)$$

where f is the frequency of 'switch on' signals, equal to the frequency of current pulses of the output current $i_T(t)$. This frequency is two times greater than devices $S_1 \div S_6$ switching frequency.

$$f = \frac{1}{T} = \frac{1}{t_{0d2} - t_{0d1}} = \frac{2}{t_{3d1} - t_{0d1}} \quad (19)$$

If we consider no loses in the circuit, the output power P_0 is equal to the input power P_i.

$$P_0 = P_i \Leftrightarrow U_0 I_0 = 2fCU_i(U_i + U_X) \quad (20)$$

If it is imposed a fix dc output voltage, the control of the average output current I_0, may be done either through the switch frequency 'f' (if devices S_5 and S_6 are turned on when the voltage across them riches a imposed value $U_X \geq 0$ eq.21), or through the voltage level, U_X, across devices S_5 and S_6, that performs the turn on command of these devices (considering a constant switch operation-eq.22).

$$I_0 = \frac{2CU_i(U_i + U_X)}{U_0}\cdot f \quad (21)$$

$$I_0 = \frac{2CfU_i}{U_0}\cdot U_X + \frac{2CfU_i^2}{U_0} \quad where \quad U_X \geq 0 \quad (22)$$

The conclusion which results from equations 21 and 22 is that the control of the converter presented in Fig.1 can be linearly done. Also it is possible to control the converter both through frequency and the voltage's value U_X. In this case a very good dynamical behaviour for the pulsed output current i_T, can be obtained.

V. CONTINOUS MODE OPERATION

For continuous mode operation, the switch frequency must be larger than f_{DM}, defined in the equation (23). In this case, the current through the inductances L_1 and L_2 will never have a zero value. The stages three and six from Fig.2, are not present any more.

$$f_{MD} = \frac{2}{t_{2d1} - t_{0d1}} = \frac{2}{t_{2d2} - t_{0d2}} \quad (23)$$

The behaviour of the circuit can be described in four stages, only two of them being different (Fig.5). The pulsed output current, (Fig. 1), is the sum between the currents i_{L1} and i_{L2}.

The first stage [$t\in(t_{0c1} ; t_{1c1})$] may be defined almost identically like in the discontinuous mode operation. The equivalent circuit is also the same (Fig. 3) and the equations which described the circuit behaviour are similar to equations (1), (2) and (3).

The initial conditions are different. These are:

$$i_{L1}(t_{0c1}) = I_{L0} \quad \text{and} \quad u_C(t_{0c1}) = -(U_i + U_X) \qquad (24)$$

According to these initial values, the relations of the main circuit's electric parameters may be found out:

$$i_{L1}(t) = C\omega_0(2U_i + U_X - U_0)\sin\omega_0 t + I_{L0}\cos\omega_0 t$$
$$u_{L1}(t) = (2U_i - U_0)\cos\omega_0 t - \omega_0 L I_{L0}\sin\omega_0 t \qquad (25)$$
$$u_C(t) = U_i - U_0 - u_{L1}(t)$$

where I_{L0} represents the initial (or minimal) value of the current through the inductance L_1 or L_2 (equation 24).

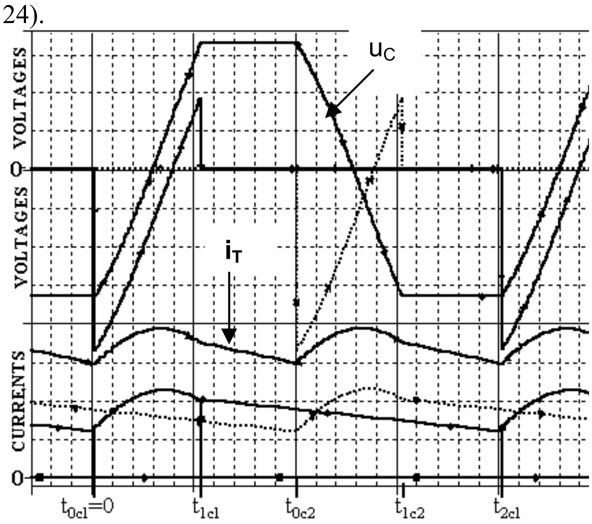

Fig. 5. Continuous mode circuit operation

At the point t_{1c1} the voltage across S_5 and the voltage across the capacitor C becomes equal to U_X and $+(U_i + U_X)$, respectively. According to equations (25), the equation (26) might be written:

$$\omega_0 L I_{L0}\sin\omega_0 t_{1c} - (2U_i + U_X - U_0)\cos\omega_0 t_{1c} = U_0 + U_X \quad (26)$$

Also, at the point t_{1c1}, the current through the inductance L_1, will be :

$$I_{1c} = C\omega_0(2U_i + U_X - U_0)\sin\omega_0 t_{1c} + I_{L0}\cos\omega_0 t_{1c} \qquad (27)$$

The second stage [$t \in (t_{1c1}\ ;\ t_{2c1})$] starts at the point t_{1c1}, when the current through the devices S_1 and S_3 is transferred through the switch S_5. At the point t_{2c1} a new turn on commutation of the devices S_1 and S_3 is performed. The point t_{2c1} is given by the equation:

$$t_{2c1} = t_{0c1} + 2T = 0 + 2T = 2T \qquad (28)$$

where $(T)^{-1}$ is the circuit output current (i_T) pulses frequency. The current through the inductance L, has a similar equation as in the discontinuous mode operation:

$$i_{L1}(t) = -\frac{U_0}{L_1}(t - t_{1c}) + I_{1c1} \qquad t \in [t_{1c1}, t_{2c1}] \qquad (29)$$

At the point t_{2c1} the current through inductance L_1 will have again the value I_{L0} . Combining (28) with (29), results:

$$I_{L0} = I_{1c} - \frac{U_0}{L_1}(2T - t_{1c}) \qquad (30)$$

From equations (26), (27) and (30), the values of t_{1c1} and I_{L0} may be found out.

The stages tree and four are similar to the stages one and two. In this case the current flows through S_2 , S_4 , L_2 and S_6 . The position of the point t_{0c2} is:

$$t_{0c2} = 0.5 \cdot (t_{0c1} + t_{2c1}) \qquad (31)$$

In the continuous operation mode, the relations (20÷22) are preserved, so both control methodologies methodology may be used to assure the needed average output current I_0.

Continuous mode of operation is recommendable due to the less output current pulse ripple.

VI. CONCLUSIONS

The circuit presented in this paper has the following advantages comparing to the conventional buck circuit:

- The output current depends on the circuit switch frequency, on the value of capacitor C and on a dc control voltage (which control in fact the voltage variation across the capacitor C). Because the dc output voltage is controlled only by the converter's output current, a very small ratio between output voltage U_0 and input voltage U_i may be achieved. These small rates are difficult to be assured by the standard Buck converter at a high frequency.
- Using both control modes (frequency and voltage) a very good dynamic of the output current may be obtained.
- The circuit assures turn off soft commutations for all the devices, and the output current frequency is two times greater than the switching frequency for each device. The devices involved in the circuit may be selected only according to their turn on capabilities. For high power operation, fast thyristors may be used.
- The possibility to design and select the inductances L_1 and L_2 in relation to capacitor C, gives the designer the opportunity to select a lesser value for the inductances than in the case of standard Buck converter for the same performances.

The circuit can be used for both high power and small power as well.

REFERENCES

[1] A. Lazar, M. Florea, D. Alexa and Lumminita-Camelia Lazar, "Charge Pump Buck Converter",*The ETC'04 Symposium, Timisoara,* Romania oct.2004

[2] Robert W. Erickson; Dragan Maksimovic. "*Fundamentals of Power Electronics*" , Kluwer academic Publishers 2001

[3] Haci Bondur, A. Faruk Bakan : "An Improved ZCT-PWM DC-DC Converter for High-Power and Frequency Applications," IEEE *Trans. On Industrial Electronics*, vol.51, no.1, Feb.2004, pg.89-95

[4] Ned Mohan, Tore M. Undeland, William P. Robbins: "*Power Electronics*", John wiley&Sons, Inc

[5] Nicola Femia, Giovanni Spagnuolo, Massimo Vitelli : "Steady-State Analysis of Hard and Soft Switching DC-to-DC Regulators;" *IEEE Trans. On Power Electronics*, vol. 18, no.1, Jan. 2003, pg.51-64.