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A New CMOS Second-Order Temperature-Compensation Total-Current Reference

Radu D. Mihăescu [1]

Abstract – A new compact total-current reference source is proposed here, which is composed of two cross-connected classical current mirrors: a modified-Wilson mirror and a Widlar mirror. This type of current reference can be interconnected simply, serially, with a charge having one grounded or connected to the voltage supply end. The first and second-order current-thermal-compensation conditions are deduced. The source design and simulation results are presented. The second-order thermal-compensation source has the performances: maximum current variation of only 0.5% across the temperature range 0…100°C and a supply regulation of only 1670ppm/V.
Keywords: CMOS analog integrated circuits, current references, temperature compensation.

I. INTRODUCTION

The simply and compact reference current sources, composed of two cross-connected current mirrors have been re-launched by paper [1]. There it was imposed and controlled first time the temperature dependence of the source two-branch current ratio. This fact allowed the design of the current source composed of cross-connected modified-Widlar mirror (completed with diode) and a "reverse"-Widlar mirror (fig.1), to achieve a spectacular reference-current second-order thermal compensation (for a branch current I_1), which leads to very good performances.

But in [1] is not shown or discussed the solution to extract the reference current towards a charge having one grounded or connected to the voltage supply end. Of course, this current can be conveyed in the charge by a supplementary current-mirror branch but, such as the simulations shows, the current ratio in this new simple mirror is affected by the temperature too. So, the output current should have, in an important degree, a compromised stability in comparison with the performance obtained for the main source branch. Moreover, a simple supplementary branch cannot assure always an acceptable "supply regulation" for the output circuit.

Paper [2] presents a simple solution to extract the reference current from a source main branch for his injection in the charge with grounded end. Achieving the new mirror (branch) also with second-order temperature compensation, the stability performances of the output current can be even improved in comparison with the two-branch-only scheme.

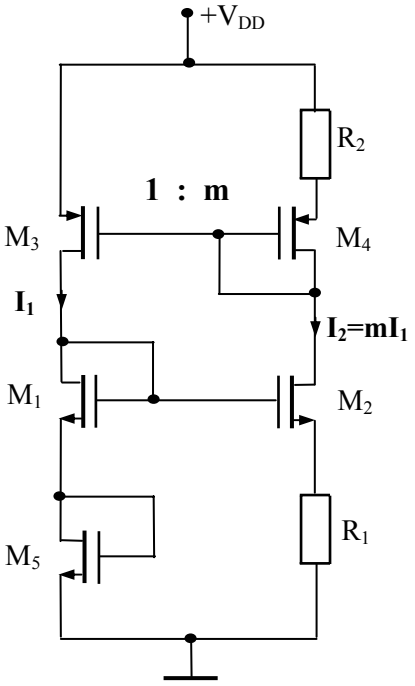

Fig.1. Second-order temperature compensation branch-current reference (Fiori-Crovetti)

In papers [3] and [4] one introduced for this kind of compact sources the notion of reference "**total**" current, representing the sum of the two source-branch currents. It is a new concept, permitting a very simple, serial, interconnection of the reference current source and the grounded-end charge and, with corresponding change, a supply-end one. This kind of solution achieves good performances related to maximum current variation for a given temperature range and the supply regulation parameter. Some total-reference-current-source performances suffer because of an increased resistance value with undesired effect on minimum supply-voltage value and occupied-on-chip area. Maybe, using another process [5], with negative

[1] Alcatel-Lucent, Str. Gheorghe Lazăr, Nr.9, 300081, Timişoara, e-mail : radu.mihaescu@alcatel-lucent.ro

temperature-coefficient resistor, will lead to an attenuation of these disadvantages.
In the present work another solution which achieves a **total** reference current is proposed, based on a combination (unused until the paper [2] signalled this issue) of cross-connected classical mirrors: a modified-Wilson mirror and a normal-Widlar one. The modified-Wilson mirror (using 3 components) may implicitly assure the first-order temperature compensation with a certain value of the diode-replacing resistance and is simpler than diode-completed-Widlar mirror (4 components in view of first-order temperature compensation, [1]). Moreover, thanks to Wilson mirror, the proposed here reference current source can assure a better supply regulation.
In the Section II of this work the first-order-thermal-compensation condition for the reference current is established. In Section III the second-order-thermal-compensation condition is deduced. Then, Section IV shows the performed simulations and their results. The work finishes with conclusions (Section V).

II. TOTAL-CURRENT FIRST-ORDER TEMPERATURE COMPENSATION

The new proposed in [2] current reference is given in fig.2. It is composed of lower modified-Wilson mirror (with M_1, M_2, R_1) and a upper normal-Widlar mirror (with M_3, M_4, R_3), which are cross-connected. Without the R_3 resistance it is a known classical scheme. With the help of R_3 here will be achieved the second-order-thermal compensation of total I_t current.

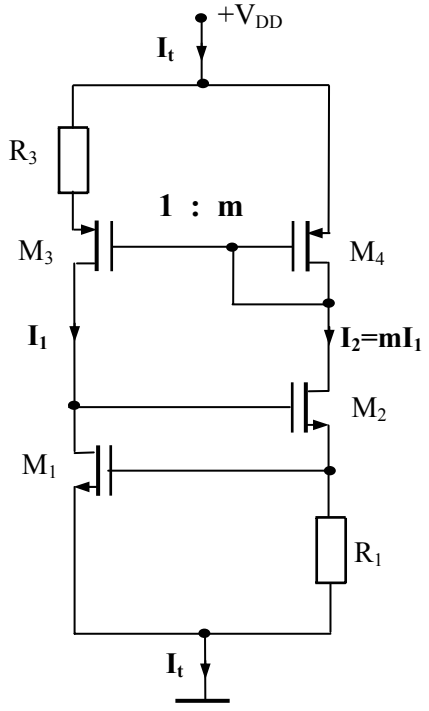

Fig.2. Proposed second-order-thermal-compensation total-current reference

Paper [1] presents a reference current source composed of lower modified-Widlar mirror and a upper reverse-Widlar mirror, which are cross-connected, wherein a second-order thermal compensation for the I_1 current in left branch of fig.1 is achieved.
The authors established that it is necessary to force a specially temperature dependence of branch-current ratio m (I_2=mI_1). In [1] the current equation and first-order temperature-compensation condition are deduced. It is shown the thermal compensation is not possible without the "diode"-connected transistor M_5. Thus, the lower current mirror is a modified- Widlar one. The reverse-Widlar mirror (M_3 , M_4 , R_2) performs a ratio m with positive first-order temperature coefficient k_m. The scheme in fig.1 is named further the Fiori-Crovetti source.
Unfortunately, the thermal-compensated current I_1 cannot be extracted from the left branch and used in the charge without affecting the circuit and the desired thermal compensation. The extraction by supplementary mirror-branch, with improved second-order compensation, has been performed in [2].
For first-order thermal compensation of the proposed-source current I_t (fig.2), will be established now the condition which the resistance R_1 must fulfil. The current I_t equation can be obtained starting of that written on source lower loop:

$$V_{GS1} = I_2 R_1 = mI_1 R_1 \quad sau \quad V_{Tn} + \sqrt{\frac{I_1}{\beta_n \alpha_1}} = mI_1 R_1$$

where $\beta_n = \mu_n C_{ox}/2$ is the gain factor of NMOS transistors (the same for all transistors, non-considering dimensions); α_1 represents the transistor dimension-ratio W_1/L_1 ; V_{Tn} is the NMOS -transistor threshold voltage (the same for all transistors, non-considering dimensions) and m is the branch-current ratio (I_2=mI_1). From the above relation, having

$$I_t = I_1 + mI_1 = (1+m)I_1,$$

one obtains the equation:

$$\frac{m}{1+m} R_1 I_t - \sqrt{\frac{I_t}{(1+m)\beta_n \alpha_1}} - V_{Tn} = 0 \qquad (1)$$

Replacing here the above β_n expression, it becomes:

$$\frac{m}{1+m} R_1 I_t - \sqrt{\frac{2I_t}{(1+m)\mu_n C_{ox} \alpha_1}} - V_{Tn} = 0 \qquad (2)$$

To establish the first-order thermal-compensation condition for the total current I_t in relation (2), noted as f(T), one uses the total derivative of the function

$$f(T) = f(I_t, \mu_n, R_1, V_{Tn}, m) = 0 \qquad (3)$$

wherein all variables are temperature functions:

$$\frac{\delta f}{\delta I_t}\frac{dI_t}{dT}+\frac{\delta f}{\delta \mu_n}\frac{d\mu_n}{dT}+\frac{\delta f}{\delta R_1}\frac{dR_1}{dT}+\frac{\delta f}{\delta V_{Tn}}\frac{dV_{Tn}}{dT}+\frac{\delta f}{\delta m}\frac{dm}{dT}=0 \tag{4}$$

Introducing, such as in [1], the (relative) temperature coefficients for five variables, defined in the form

$$k_v=\frac{dv}{vdT} \quad or \quad \frac{dv}{dT}=vk_v \tag{5}$$

(with a variable noted here as "v") and representing the relative variation of that variable with temperature, one obtains the following equation:

$$\frac{\delta f}{\delta I_t}I_t k_{It}+\frac{\delta f}{\delta \mu_n}\mu_n k_{\mu n}+\frac{\delta f}{\delta R_1}R_1 k_{R1}+\frac{\delta f}{\delta V_{Tn}}V_{Tn}k_{VTn}+\frac{\delta f}{\delta m}mk_m=0 \tag{6}$$

After the partial derivative calculus in relation (2) and replacing the radicals by the expression taken out from the same equation, namely:

$$\sqrt{\frac{2I_t}{(1+m)\mu_n C_{ox}\alpha_1}}=\frac{m}{1+m}R_1 I_t-V_{Tn} \tag{7}$$

it results in:

$$\begin{aligned}&\frac{1}{2}\left(\frac{m}{1+m}R_1I_t+V_{Tn}\right)k_{It}+\frac{1}{2}\left(\frac{m}{1+m}R_1I_t-V_{Tn}\right)k_{\mu n}+\\&+\frac{m}{1+m}R_1I_tk_{R1}-V_{Tn}k_{VTn}+\\&+\left[\frac{m}{(1+m)^2}R_1I_t+\frac{1}{2}\frac{m^2}{(1+m)^2}R_1I_t-\frac{1}{2}\frac{m}{1+m}V_{Tn}\right]k_m=0\end{aligned} \tag{8}$$

If imposes here the condition of total-current first-order thermal compensation, $k_{It}=0$, one obtains the necessary value for the resistance R_1

$$R_1=\frac{1+m}{m}\cdot\frac{V_{Tn}}{I_t}\cdot\frac{k_{\mu n}+2k_{VTn}+\frac{m}{1+m}k_m}{k_{\mu n}+2k_{R1}+\frac{2+m}{1+m}k_m} \tag{9}$$

which is simpler than the obtained in [3] one and which, for the used here process, leads to a positive value for R_1.

In this relation they exist really two unknown variables: R_1 and k_m. If the obtained in simulation R_1 value (for that the variation slope of I_1 current against temperature is minimum) is introduced here one obtains, for the adopted process, a temperature coefficient k_m of negative value. Consequently, to achieve the second-order temperature compensation of current I_1, it must be used an upper mirror of normal-Widlar type (M_3, M_4, R_3) unlike the used in fig.1 one, of reverse-Widlar type (in [1], to achieve a temperature coefficient k_m of positive value).

A first finding is that the necessary value of resistance R_1 is greater than obtained in [1] one, what means the increase of the occupied-on-chip area as well as the increase of minimum V_{DD} circuit supply voltage. The increase of R_1 resistance has only the advantage of growing the source output resistance, meaning the supply-regulation-parameter enhancement [3].

A second finding is that, to maintain a smaller value for the resistance R_1, it must be used a ratio m as great as possible. In reality, the resistance R_1 value depends especially on ratio *(1+m)/m* because the fraction including the temperature coefficients is very close to a constant as against m (close of 3 for the process and models used in this work) [4].

An important finding is referred to the voltage drop on R_1 which is mI_1R_1 (9). This is done by the product of V_{Tn} and the fraction which is nearly constant (9). So, knowing that $k_{\mu n}$ is negative and has a great absolute value, to reduce the voltage drop on R_1, it is necessary to choose a process having an integrated resistor with very small or negative temperature coefficient k_{R1}. Because the value of resistance R_1 is relatively great it is recommended to use a resistor type having great resistance per square, thus limiting the chip area.

III. TOTAL-CURRENT SECOND-ORDER TEMPERATURE-COMPENSATION

To establish the second-order compensation condition for the reference current I_t in fig.2 one proceeds as in [1] and [3]. Thus, the reference-current temperature coefficient from relation (8) is written in the form:

$$\begin{aligned}k_{It}=&\frac{1}{V_{Tn}+\frac{m}{1+m}R_1I_t}\cdot\left[V_{Tn}\left(k_{\mu n}+2k_{VTn}+\frac{m}{1+m}k_m\right)-\right.\\&\left.-\frac{m}{1+m}R_1I_t\left(k_{\mu n}+2k_{R1}+\frac{2+m}{1+m}k_m\right)\right]=\frac{N(T)}{D(T)}\end{aligned} \tag{10}$$

If now is imposed the second-order temperature-compensation condition, that is $k_{Itlt}=0$, having D(T) as finite quantity, with the procedure of [1] or [2], the following condition results:

$$\frac{dN(T)}{dT}=0 \tag{11}$$

The calculus of this condition is developed here and it will consider that for the adopted process, in conformity with the transistor and resistor-model-parameters table, the parameters k_{VTn} and k_{R1} do not depend on temperature, thus, for the variables V_{Tn} and R_1 do not exist second-order temperature coefficients. Also, one will consider the current I_t is constant with the temperature, this fact just representing the current-first-order-temperature-compensation condition.

After the evaluation of derivative in (11), introduction of first and second-order temperature coefficients for μ_n, V_{Tn} and m, it gives:

$$V_{Tn}\left(k_{\mu n}+2k_{VTn}+\frac{m}{1+m}k_m\right)k_{VTn}+$$
$$+V_{Tn}\left[k_{\mu n\mu n}+\frac{m}{(1+m)^2}k_m^2+\frac{m}{1+m}k_{mm}\right]-$$
$$-\frac{m}{1+m}I_tR_1\left[\left(k_{\mu n}+2k_{R1}+\frac{2+m}{1+m}k_m\right)\left(k_{R1}+\frac{1}{1+m}k_m\right)+\right.$$
$$\left.+k_{\mu n\mu n}-\frac{m}{(1+m)^2}k_m^2+\frac{2+m}{1+m}k_{mm}\right]=0 \qquad (12)$$

Here one used notations with repeated index for the second-order temperature coefficients, defined as the first-order temperature-coefficient derivative against temperature [1], [3]. In (12) is replaced the factor

$$\frac{\frac{m}{1+m}I_1R_1}{V_{Tn}}=\frac{k_{\mu n}+2k_{VTn}+\frac{m}{1+m}k_m}{k_{\mu n}+2k_{R1}+\frac{2+m}{1+m}k_m} \qquad (13)$$

deduced from relation (9) (the first-order thermal-compensation condition) and, after simplifications, one obtains the second-order thermal-compensation condition, similar as form with showed in [4] one:

$$k_{\mu n\mu n}+\frac{m}{(1+m)^2}k_m^2+\frac{m}{1+m}k_{mm}-\left(k_{\mu n}+2k_{VTn}+\frac{m}{1+m}k_m\right)\cdot$$
$$\cdot\left[-k_{VTn}+k_{R1}+\frac{1}{1+m}k_m+\frac{k_{\mu n\mu n}-\frac{m}{(1+m)^2}k_m^2+\frac{2+m}{1+m}k_{mm}}{k_{\mu n}+2k_{R1}+\frac{2+m}{1+m}k_m}\right]=0 \qquad (14)$$

In relation (14) there exist terms which give a negative quantity and others which give a positive one. Thus, the second-order temperature-compensation condition will fulfil for a particular pair of values of m and σ. These can be calculated with approximation by repeated trials. With their help can be calculated approximately the resistances R_1 and R_3 values that will be used at start in simulation.

Because the scheme in fig.2 includes an upper normal-Widlar mirror the relations for coefficients k_m and k_{mm} imposed by this type of mirror will be those deduced in work [4]. They have the form:

$$k_m=\frac{\sqrt{\sigma m}-1}{\sqrt{\sigma m}+\left(\sqrt{\sigma m}-1\right)\frac{m}{1+m}}\cdot\left(k_{\mu p}+2k_{R3}\right) \qquad (15)$$

wherein $\sigma=\alpha_3/\alpha_4$ that is, the ratio of dimension ratios for transistors M_3 and M_4 and must be fulfilled the condition:

$$\sigma m>1 \qquad (16)$$

respectively:

$$k_{mm}=\frac{\left(\sqrt{\sigma m}-1\right)\left[\frac{1}{2}\sqrt{\sigma m}-\left(\sqrt{\sigma m}-1\right)^2\frac{m}{(1+m)^2}\right]}{\left[\sqrt{\sigma m}+\left(\sqrt{\sigma m}-1\right)\frac{m}{1+m}\right]^3}\cdot$$
$$\cdot\left(k_{\mu p}+2k_{R3}\right)^2+\frac{\sqrt{\sigma m}-1}{\sqrt{\sigma m}+\left(\sqrt{\sigma m}-1\right)\frac{m}{1+m}}\left(k_{\mu p\mu p}+2k_{R3R3}\right) \qquad (17)$$

The coefficient $k_{\mu p\mu p}$ has been established in paper [2] while the coefficient k_{R3R3} is comprised in the table of integrated-resistor model parameters. For the process used in the present work and the N^+ diffusion-sheet-resistance type, $k_{R3R3}=0$.

After the adoption of ratio m [3] and, considering the condition (16) for dimension ratio σ, k_{mm} can be calculated. But, the calculus precision will not be very good because of using typical-parameter values given in model tables for certain transistor-channel dimensions. It is known, in the 0.35μm process, transistor parameters depend moreover on dimensions in the proximity of smaller as few μm values.

IV. SIMULATION RESULTS

The simulation of scheme in fig.2 in view of finding optimal values for transistor dimensions and resistances with the goal of achieving the second-order-temperature compensation of current I_t, has been done starting from the situation obtained after first-order thermal compensation. There have been already established the transistor M_1, M_2, M_4 dimensions and the resistance R_1 value. Then, the W_3 value for transistor M_3 has been found which assures the necessary ratio σ (fulfilling the condition (16)).

Simulations have been achieved, for different m and σ values and for a total current comprised in the range 8...15μA. The performance results have been similar: the maximum current I_t variation in the temperature range of 0...100°C is situated around 0.5% (Fig.3), minimum supply voltage is V_{DDmin}=4.7V, the „supply regulation" parameter is SR=1670ppm/V. This results correspond to values: I_t=15μA, m=1, σ=10.27, L_1=20.4μm, $L_{2,3,4}$=5μm, $W_{1,2}$=2μm, W_3=37μm, W_4=3,6μm, R_1=270kΩ and R_3=56.5kΩ.

Comparing the above obtained performances with the reported in [1] and [4] ones one may see they are close (0.35%...0.5%) concerning the maximum variation of the reference current across the temperature range of 0-100°C. A particular performance of the proposed here reference is the attained supply regulation which is, at near current values, 2.4 times better than the reported in [1] one, 2.6 times better than the reported in [2] one and 4.6 times better than the announced in [4] one. This is due to the using of a lower modified-Wilson-type mirror.

The minimum necessary supply voltage for our circuit is relatively great, 4.7V, such as expected [3], [4]. For that reason, the models 5V of transistors have been used in simulation.

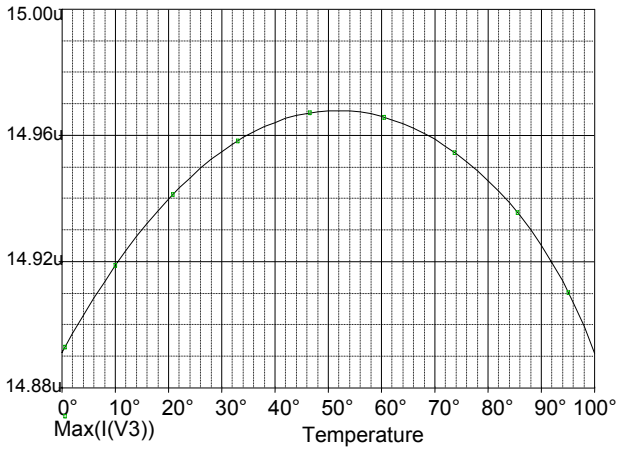

Fig.3. Reference-(total) current variation against temperature in the range of 0-100°C

V. CONCLUSIONS

In this paper has been analyzed the idea of second-order thermal compensation of the total current of a reference composed of two cross-connected usual current sources. This kind of current reference has the goal of allowing very simple serially interconnection with a charge having grounded or connected to voltage supply end, without significantly modify the current value. In the present paper is deduced, by a similar method as in [1] and [4], the first and second-order thermal compensation conditions for the reference total current.

The total current reference has the advantages: circuit simplicity, simplest charge connection to the current reference and good performances. But the thermal compensation of total current brings a disadvantage too: the increase of a resistance of the modified-Widlar current source (R_1). This causes two undesirable consequences: the increase of occupied-on-chip area and the increase of minimum supply voltage (V_{DD}). These problems can be solved if a process having a resistor with very small or negative temperature coefficient is used. It is necessary to use a resistor type having great resistance per square, to reduce the chip area.

The obtained performance of maximum reference current variation across the temperature range of 0-100°C, of 0.5%, is comparable with the reported in [1] and [4] one. But the proposed-reference supply rejection, of 1670ppm/°C, is 2.4 times better than the reported in [1] one, 2.6 times better than the reported in [2] one and 4.6 times better than the announced in [4] one.

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