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DEAN'S WELCOME SPEECH

Dear colleagues,

*I wish you a warm welcome to the seventh edition of the "**Symposium of Electronics and Telecommunications – ETc 2006**".*
We started the first edition in 1994, as a national event, with Proceedings printed in Romanian. With each edition, every second year, we saw a continuous increase in both quantity and quality of papers, submitted by well known researchers from universities and industry, from Romania and abroad. The Symposium became quickly an international event, having papers published in English, in our Scientific Bulletin of the Politehnica University.
During the last years, the Bulletin and the Symposium have been supported by an international reviewers committee, with increased expertise and exigency. As a result, for the present edition, the committee accepted only 89 papers for presentation and publication, out of 122 submitted papers, resulting a rejection ratio of 27 %. I wish to express my gratitude to the members of the International Scientific Committee for the hard work and the time they dedicated to the revision of manuscripts.
Our Organizing Committee is proud to have the opportunity to publish such highly ranked papers in two dedicated volumes of the Scientific Bulletin, and congratulates the authors for their success.
Besides the scientific and informative value of the published volumes, the next purpose of our Symposium is to be, for all participants, a forum for exchange of ideas and socialization, for emphasizing the feeling of belonging to a highly specialized and expert community.
*In order to offer such a frame for the most dynamic category of researchers – the PhD students, we launched, in 2005, the "**Doctor ETc**" conference, dedicated to PhD Students in Electronics and Telecommunications, as a national event, with selected papers published in the Scientific Bulletin. This conference will be organized every second year, alternatively with the ETc Symposium.*
The present edition of the Symposium, in addition to the accepted papers, is honored by three keynote speeches, delivered by well known personalities from the research and economic world: Dan Bedros, CEO of Alcatel Network Systems, Romania, Dr. Christian Baier-Welt form Siemens VDO, and Prof. Dr. Rolf Dieter Schraft, from IPA Stuttgart, Fraunhofer Institute, Germany.
This symposium would not have been possible without the gracious help of our sponsors, to whom we express our gratitude.
I am also honored to express my thanks to you, all the participants, for attending the Symposium, to wish you a successful and profitable audience through the sessions, and a nice stay in Timisoara. I am looking forward of meeting you again in 2007 (Doctor ETc '07) and in 2008 (Symposium ETc '08).

Chairman of Symposium ETc '06,
Dean, Prof. Dr. Eng. Marius Otesteanu

Timisoara, September 21st, 2006

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Tom 51(65), Fascicola 1, 2006

Table of Contents

Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

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A Generic Building Block for Hebbian Neural Network with On-Chip Learning

Alin Tisan[1], Ciprian Gavrincea[2], Ştefan Oniga[3]

Abstract – In this paper, we present a digital hardware implementation of an artificial neuron on-chip unsupervised trained with Hebbian rule. The main characteristics of this solution are on-chip learning algorithm implementation and high reconfiguration capability and operation under real time constraints.
Keywords: fpga, learning on-chip, ANN

I. INTRODUCTION

In respond to highly parallelism, modularity and dynamic adaptation, the artificial neural network (ANN) become the most explored data processing algorithms. In addition to this the digital hardware implementation of ANNs in reconfigurable computing architectures like FPGAs circuits, become the easiest and fastest way to reconfigure in order to adapt the weights and topologies of an ANN.

In this paper we present an extendable digital architecture for the implementation of a Hebbian neural network using field programmable gate arrays (FPGAs) and we propose a design methodology that allows the system designer to concentrate on a high level functional specification. For this reason we developed a new library Simulink blocksets constituted by Simulink Xilinx blocks and VHD blocks. With these new created blocks, the designer will be able to develop the entire neural network by parameterize the ANN topologies as number of neurons and layers.

The implementation goal is achieved using the Mathworks' Simulink environment for functional specification and System Generation to generate the VHD code according to the characteristics of the chosen FPGA device.

The design methodology is not new; there have been recent

II. HEBBIAN NEURAL NETWORK

The Hebbian neural network is a multilevel model of perception and learning, in which the 'units of thought' were encoded by 'cell assemblies', each defined by activity reverberating in a set of closed neural pathways The essence of the Hebb synapse is to increase coupling between coactive cells so that they could be linked in growing assemblies. Denoting the neurons by n_i and n_j and the weight that connect the n_j and n_i by w_{ij} and if neuron n_i receives positive input x_j while producing a positive output y_i, the hebbian rule states that for some learning rate $\eta > 0$:

$$w_{ij} := w_{ij} + \Delta w_{ij}, \tag{1}$$

where the increase in the weight connecting n_j and n_i can be given by:

$$\Delta w_{ij} := \eta y_i x_j, \tag{2}$$

Here

$$y_j = f(net) = f\left(\sum_{i=1}^{N} w_{ij} x_i - b\right) \tag{3}$$

where *f(net)* is defined by the discontinuous threshold activation function *sgn(net)*:

$$\mathrm{sgn}(net) = \begin{cases} 1 \text{ if } net \geq 0 \\ -1 \text{ if } net < 0 \end{cases} \tag{4}$$

Of all the learning rules, Hebbian learning is probably the best known. It established the foundation upon which many other learning rules are based. For this reason, we developed this learning rule first.

Hebb proposed a principle, not an algorithm, so there are some additional details that must be provided in order to make this computable:

- It is implicitly assumed that all weights w_{ij} have been initialized (e.g. to some small random values) prior to the start of the learning process.
- The parameter η must be specified precisely (it is typically given as a constant, but it could be a variable).

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- There must be some type of normalization associated with the increase of the weight or else w_{ij} can become infinite;
- Positive inputs tend to excite the neuron while negative inputs tend to inhibit the neuron.

III. BLOCKSET NEURAL NETWORK DESIGN

In order to learn on-chip, the Mc Culloc - Pitts neuron model, i.e. each of the input vector components xi is multiplied with the corresponding weight w_{ij}, and these products are summed up yielding the net linear output, upon which the threshold activation function is applied to obtain the activation which is either 1 or −1, was modified to make the calculate the weights according to a certain learning rule and to update the new weights into a weight memory block, figure 1.

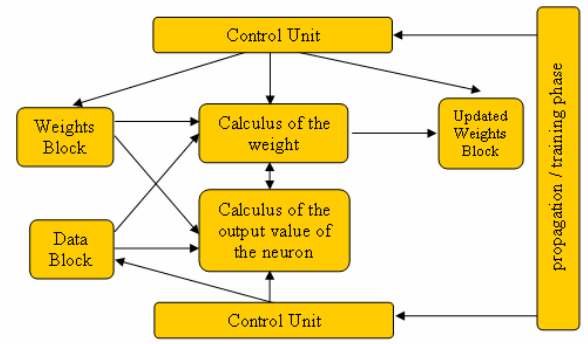

Fig.1. Block level representation of the neuron with on-chip learning

The parallelism adopted is a node parallelism one and requires one multiplier per neuron, therefore all neurons will work in parallel. If data inputs are memorized in a single memory block, the weights storage will be private for each neuron because all the neurons have to access their correspondent weight memories at the same time.

The proposed model of the neuron is constituted by two major blocks: a control logic bloc and a processing block.

The control logic block will manage the control signal of the processing bloc in order to initialize and command the processing components.

The processing block is design to calculate the neural output, the weights according to learning rule adopted, in this case the Hebbian rule, and to update these weights.

A. *Control logic block*

The control logic block is described in VHDL code and is incorporated into design by a black box HDL, figure 2.

The role of this bloc is to load from Mathlab workspace the following variables: the number of vectors used for training and the number of bits used for data representation.

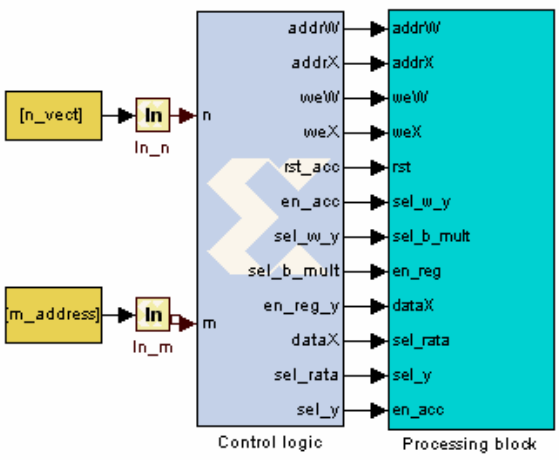

Fig. 2. Blockset architecture of neuron

Depending on these variables, the control logic block will configure the size of the RAMs used for data and weights storage and will manage the enable signals of the processing elements of the processing block in order to run the processing block in a propagation phase or in a training phase, figure 3..

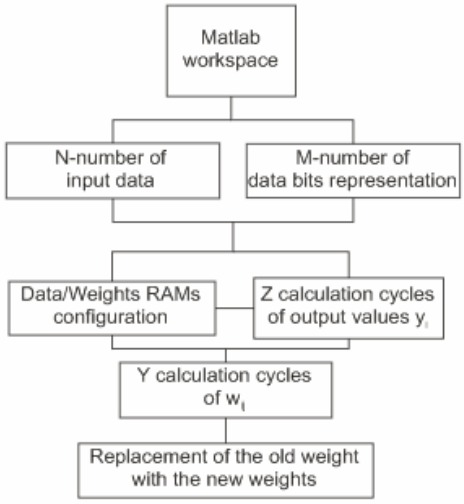

Fig.3. Block level representation of the neuron with on-chip learning

The enabling algorithm of processing elements depends on the number of input neurons, the size of the block memories that storage the data or weights vectors and the delays introduced by the different processing or storage elements.

B. *Processing Block*

The processing block is the main block of the design. It incorporates both the artificial neuron and the logic for on-chip learning algorithm.

The structure of the artificial neuron consist in two memory blocks, one for data samples and one for weight coefficients, and one MAC unit, figure 4.

The logic for the learning algorithm requires a MAC unit too, but in order to save hardware resources we decide to use the MAC unit of the artificial neuron for the implementation of the learning algorithm. To

achieve this, the design requires a number of multiplexer blocks and special control logic.

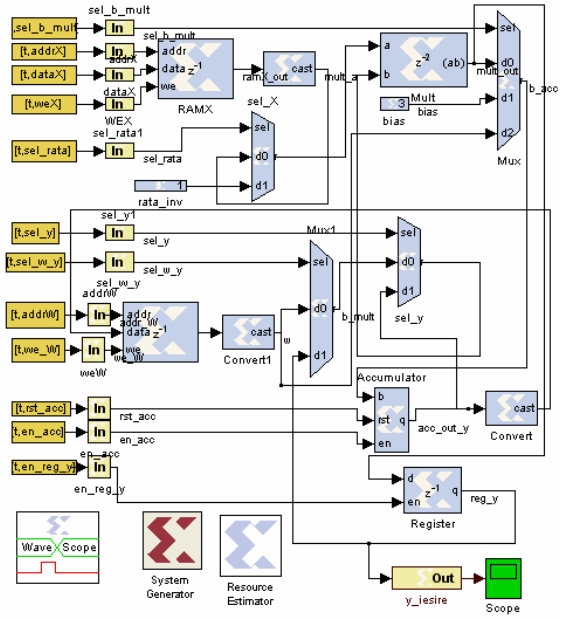

Fig. 4. Architecture of the processing block.

Artificial neuron with on-chip learning has two modes of operation: propagation mode on which the design acts as a regular artificial neuron and learning mode. On learning mode there are two stages: on the first stage an output of the artificial neuron is calculated based on the data provided by training vector and on the second stage weight coefficients are recalculated based on Hebbian learning rule.

By using one MAC unit it saves hardware resources but execution time slightly increases. This happens only on the learning mode and doesn't affect the propagation mode. For an artificial neural network time constrains are important only on propagation mode of operation, and having a longer learning period doesn't affect the performance of the artificial neural network.

IV. HARDAWARE IMPLEMENTATION

The design is implemented into Digilab 2E (D2SB) development board featuring the Xilinx Spartan 2E XC2S200EPQ208-6 FPGA. This chip has 2352 slices (control unit which includes two 4-inputs look-up tables (LUT) and two flip-flops) and 14 block RAMs. The resources usage of a single neuron were estimated by ISE Xilinx and by Simulink Resource Estimator Block and are shown in fig. 5 and fig. 6

The differences between these two estimators come up because of different way of resource usage calculation of the logic blocks implementation in FPGA

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	48	4,704	1%
Number of 4 input LUTs	104	4,704	2%
Logic Distribution			
Number of occupied Slices	58	2,352	2%
Number of Slices containing only related logic	58	58	100%
Number of Slices containing unrelated logic	0	58	0%
Total Number of 4 input LUTs	104	4,704	2%
Number of bonded IOBs	30	142	21%
Number of Block RAMs	2	14	14%
Number of GCLKs	1	4	25%
Number of GCLKIOBs	1	4	25%
Number of RPM macros	1		
Total equivalent gate count for design	34,063		
Additional JTAG gate count for IOBs	1,488		

Fig. 5. The resource estimation by ISE Xilinx of a single neuron

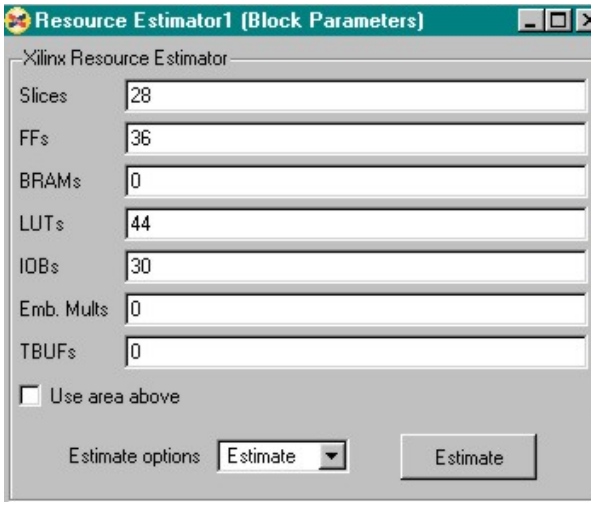

Fig. 6. The resource estimation by Simulink Resource Estimator of a single neuron

Because Spartan 2E doesn't have implemented dedicated MAC units, we designed a multiply and accumulate structure with Xilinx blocks of Simulink Xilinx Blockset library, figure 7.

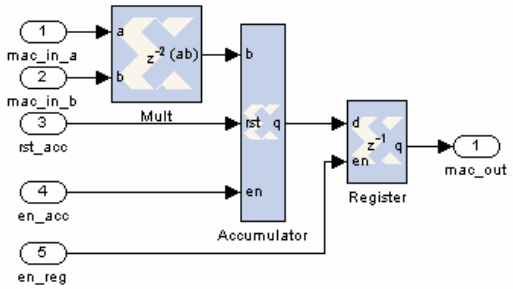

Fig. 7. MAC structure designed with Xilinx blocks

Fig. 8. Waveforms of a neuron in training phase

Because, multiplication block use the largest resources, 12 slices, and in order to implement the three multiplications needed to calculate the updated weights and the neuron output with one multiplication and accumulation block is necessary to add three more multiplexers block to select the right signal to add or to multiply.

The total delay is gave by the number of training vectors plus 3 other cycles (1 for RAM, two for the multiplier) for neuron output calculation and 2 x number of training vectors plus 12 cycles to calculate the new weights and to update the weight RAM.

The total number of cycles needed to calculate and update the weights is presented in fig. 8.The waveforms confirm the calculation algorithm, for a given number of training vectors, of total delay for a neuron in training phase and propagation phase

V. CONCLUSION

We have presented hardware architecture of artificial neuron with on-chip learning controlled by a generic control unit described in VHDL code. This method uses minimal hardware resources for implementation of this kind of artificial neuron. The main advantage of this solution is highly modularity and versatility in neural network designing.

In order to design and to implement the neuron we used the Mathworks' Simulink environment for functional specification, System Generation to generate the VHD code according to the characteristics of the chosen FPGA device and ISE Xilinx to simulate the design at different stages of implementation and to generate the bit file.

The neuron designed is a generic module and can be used to design neural networks that have the following features:

- the training is on-line;
- the learning is on-chip;
- all weights have been initialized prior to the start of the learning process;
- the learning parameter must be specified precisely;
- there must be some type of normalization associated with the increase of the weight or else w_{ij} can become infinite;
- positive inputs will tend to excite the neuron while negative inputs will tend to inhibit the neuron;
- the initialization of the data and weigh RAMs must be done through m file from Matlab environment.

These results will be used to design other learning rules starting from a Hebbian one, and also to make the ANN design more modularized so that its size can be modified as randomly increased or decreased of the neuron number in order to find out that ANN which fits to a specific application. In this way the FPGA hardware implementation makes ANN more convenient to be carrying, modularized and reconfigurable.

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Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

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A New 450 kW Electric Motor – It Can Withstand Temperature Of 400°C Over A Period Of Two Hours

Robert Pucher[1], Karl Pucher[2]

Abstract – Due to national guideline RVS 9.261, a heat resistance of 400°C over a period of 120 minutes has to be verified for exhaust ventilators in Austria. For this reason a 450 kW electric motor was tested in a chamber in a 400°C environment. The test gave evidence that the motor could be operated under load for approximately 165 minutes without serious problems.
Keywords: Fire, Road Tunnel, Heat Resistance, RVS 9.261.

I. INTRODUCTION

Austria has many long motorway tunnels, for instance the Plabutschtunnel (10 km long), Gleinalmtunnel (8 km), Pfändertunnel (7 km), Tauertunnel (6,4 km), Katschbergtunnel (5,4 km) and others. All these tunnels where planed for two tubes. But the traffic amount 30 years ago was low, so only one tube was built at that time. These tunnels are equipped with a transverse ventilation system. The cross section of such transversely ventilated tunnels consists of three ducts: the tunnel itself (traffic room), the fresh air duct and the exhaust duct. Fresh air and exhaust air duct are separated from the tunnel by the false ceiling and a separating wall is between the fresh air and exhaust duct.

In normal case of operation fresh air is sucked on by the fresh air fan and pressed into the fresh air duct. The fresh air streams via small fresh air openings (0.1 m^2) into the tunnel. The fresh air dilutes the car exhaust gases in the traffic room. This exhaust air was sucked out of the tunnel into the exhaust duct every 12 m via small exhaust hoods (0.5 m^2). This ventilation system was not changed in case of fire. The idea was to suck up the smoke in case of fire to the false ceiling and extracted it over a long part of the exhaust duct. The advantage of this solution was thought to have a smoke free bottom zone on the one hand and a not extreme hot smoke in the exhaust duct because of mingling with fresh air on the other hand. So the temperature on front of the exhaust fans will not be higher than 250°C.

The authors found out it is better to suck off the smoke directly near the fire place into the exhaust duct through large adjustable exhaust dampers (open area ~12 m^2) to avoid smoke propagation in the tunnel. The adjustable smoke dampers are installed every 100m. In normal case of operation all dampers are a little bit open, so that the same amount of exhaust air can be sucked off through each damper. But in case of fire only this damper will be opened fully which is closed by the fire place and all others will be closed. So a concentrated smoke extraction is possible. With smoke extraction there is no mixing with cold fresh air. Therefore the smoke temperature can be very hot when the smoke extraction is near the exhaust fan. So the new requirement in the Austrian guideline (RVS 9.261) is: the electric motor from the exhaust fans must withstand a temperature of 400°C over a period of two hours.

For the exhaust fans of the new Plabutschtunnel (this tube was opened for the traffic in January 2005) we needed electric motors with a power output of 450 kW. At that time no company was able to guarantee that their electric motor can withstand 400°C over a period of two hours. Therefore a acceptance trial had to be made [1-5].

II. EXPERIMENTAL SET UP AND PERFORMANCE

The new 400°C electric motor was manufactured by Flender / Loher AG, Munich, Germany and tested in the research laboratory of the Institute of Building Climate Control and Housing Technology, TU-Munich.

The experimental set up was formed by a test chamber, holding the test motor and a coupled generator to simulate varying loads. The latter was necessary for two reasons:

- The electric motor should be run loaded under 400°C.
- The electric current produced by the generator could be used as a source, thus, the

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external energy demand for the test could be reduced.

In order to simulate the radial forces, which emerge by axial impellers mounted on a shaft-stump, a radial load was installed behind the electric motor.

A constant temperature of 400°C was generated by using gas burners in the test chamber. The test chamber, together with the shaft opening in the wall, was insulated, such that no temperature deviations from the 400°C occurred close to the outer walls. Observations of the electric motor during the 400°C test were possible by means of several special windows of glass.

In order to obtain a constant temperature within the test chamber, it was heated for several hours before the test. During the test the electric motor was operated with the frequency converter at 990 rpm, the same as in the tunnel operation. Due to the decreasing load down to 44 % of the power rating (approximately 220 kW) in the case of fire – because of the lower density of air – the load was also reduced during the test.

III. RESULTS

Figure 1 shows the temperature of the ambient air in the middle of the motor during the test. Except at the beginning of the test, where the temperature was still adjusted, it was kept constant throughout the test at 400°C

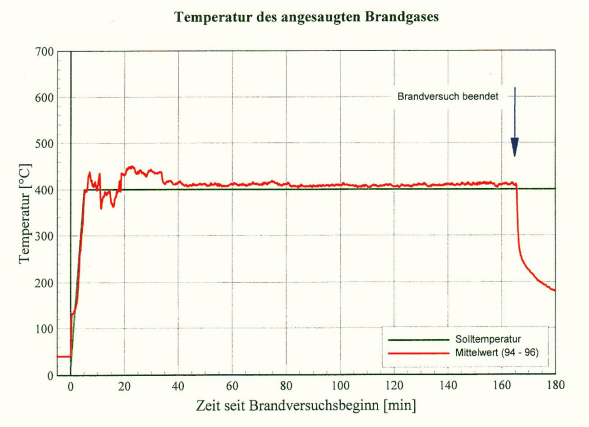

Fig. 1: Measured temperature of air sucked into the test chamber.

Figure 2 depicts the observed temperatures in the motor versus time. In the bid regarding the electric motors and exhaust ventilators, 120 minutes of operation at 400°C was demanded. This requirement could be accomplished. Temporarily temperatures at certain locations exceeded more than 400°C (a detailed explanation has not been found yet).

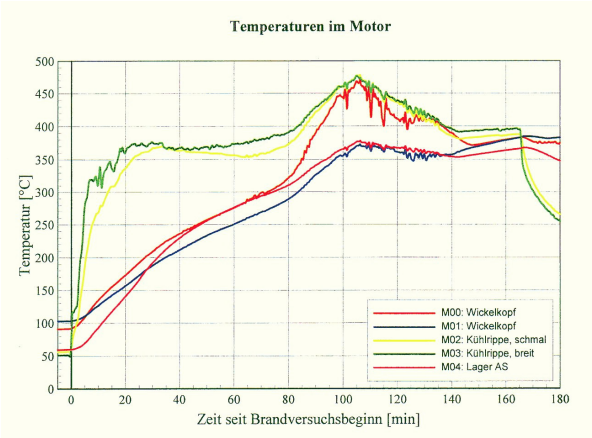

Fig.2. Observed temperature in different parts of the motor during the test

After the motor passed the test (400°C over a period of 120 minutes), it was decided to continue the operation of the motor in the 400°C environment. The temperatures in the motor fell below 400°C after 140 minutes. The motor could be operated for a further 45 minutes without serious problems and finally was switched off but driven with a low frequency for cooling purposes. After about 17 minutes later the motor stopped moving and it could not be used anymore.

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A PFC Circuit Based on a DCM Operated BOOST Converter with Integration Control

Dan Negoiţescu[1], Dan Lascu[2], Viorel Popescu[3]

Abstract – In the present paper is presented a power factor correction circuit based on a DCM operated BOOST converter. The proposed circuit uses an integration control method having the main benefit that it does not need input current sensing. There are also presented some simulation results and the main merit parameters for the proposed circuit
Keywords: DCM BOOST converter, power factor circuit, integration control

I. INTRODUCTION

For a DCM operated BOOST converter in PFC applications, with constant switching frequency and duty-cycle, it is well known that the input current wave shape is imposed in an automatic way. But, despite the fact that the control circuit is a simple one, the main disadvantage is that the input current wave shape is distorted. These unwanted current distortions became smaller when the DCM BOOST converter operates with an output voltage much bigger than the input voltage. Therefore this operation mode is generally suitable for high voltage applications [4].
By operating the BOOST converter at the limit between continuous and discontinuous conduction modes (critical mode control) the current distortions can theoretical be eliminated, but this type of control needs variable switching frequency and depending of the control method at least one multiplier. In many applications a variable switching frequency on a large range is an unwanted option. Other control methods such as the one with the second order current harmonic injection requires a complex accorded adaptive control circuit and also presents practically difficulties in control [4].
On other hand it is possible to maintain the input current proportional with the mains supply voltage by using a current loop, a good example being the non-linear carrier control method. This control method needs current sensing, reason that makes her more suitable for high power applications with continuous conduction mode operation [2].

The proposed integration control method for the PFC circuit based on a DCM operated BOOST converter presents the following advantages: provides unity power factor, does not require that the output voltage to be significantly greater compared to the input one, operation at constant switching frequency, no needing of multipliers or other complex circuits, does not need the input current sensing, easy to be implemented [1].

II. PFC OPERATION WITH INTEGRATION CONTROL

Taking into consideration a PFC circuit based on a DCM BOOST converter, having the mains supply voltage $v_g = V_M \sin\omega t$ and V_o the output voltage, the duty cycle must be time-variable in order to emulate a resistive character at the input. The inductor current waveform for the DCM BOOST converter is presented in Fig.1.

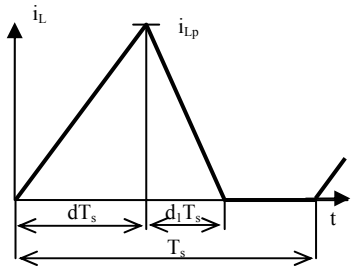

Fig.1. Inductor current waveform for a DCM BOOST converter

From Fig.1 the inductor current averaged value on a switching period, T_s, results:

$$\bar{i}_L = \frac{1}{T_s}\frac{1}{2}(d+d_1)T_s i_{Lp} = \frac{1}{2}(d+d_1)i_{Lp} \qquad (1)$$

The peak value of the inductor current can be expressed in two different ways, assuming of course that the switching frequency is much greater than the main frequency, meaning that on a mains period the

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supply voltage can be considered to be a constant one. On the dT_s switching interval, when the transistor is on, the inductor current peak value is:

$$i_{Lp} = \frac{v_g}{L} dT_s \tag{2}$$

Regarding the d_1T_s switching interval, when the diode is on, leads to the following value of the same current:

$$i_{Lp} = \frac{V_o - v_g}{L} d_1 T_s \tag{3}$$

From (2) and (3) results:

$$d_1 = \frac{v_g}{V_o - v_g} d \tag{4}$$

By replacing d_1 from (4) in (1) and using the i_{Lp} expression given by (2) the averaged value of the inductor current will be:

$$\bar{i}_L = \frac{1}{2Lf_s} \frac{V_o v_g}{V_o - v_g} d^2 \tag{5}$$

where $f_s = 1/T_s$ is the operation switching frequency. Because the inductor current represents in fact the input current for the PFC circuit, $i_g = i_L$, and imposing the operation condition for a power factor correction circuit, $\bar{i}_g = v_g/R_e$, where R_e is the emulated resistance, the (5) relation becomes:

$$\frac{v_g}{R_e} = \frac{1}{2Lf_s} \frac{V_o v_g}{V_o - v_g} d^2 \tag{6}$$

The last equation can be rewritten as follows:

$$V_o - v_g = \frac{V_o R_e}{2Lf_s} d^2 \tag{7}$$

Relation (7) shows that the controller can be easily implemented by using a universal trailing edge modulator. More than that, the same relation reveals that the duty-cycle does not depend on any current, meaning that the PFC circuit is not containing current traductors, this fact being another big advantage of the proposed application. In order to define the control voltage, V_m, it can be observed that the last equations right part has a large value, uncommon to a control circuit. Therefore, both members in the (7) equation can be multiplied with a sub-unitary constant factor K, small enough to provide typical values for a control circuit. Practically, this fact requires the using of some simple resistive dividers. The (7) relation will be then:

$$K\left(V_o - v_g\right) = K \frac{V_o R_e}{2Lf_s} d^2 \tag{8}$$

From this last equation the control voltage of the trailing edge modulator can be defined as:

$$V_m = K \frac{V_o R_e}{2Lf_s} \tag{9}$$

The final form of the controller equation will be then:

$$K\left(V_o - v_g\right) = V_m d^2 \Rightarrow K\left(V_o - v_g\right) = V_m \left(\frac{t}{T_s}\right)^2 \tag{10}$$

In Fig.2 is presented the circuit schematic for the PFC circuit based on the DCM BOOST converter controlled by a universal PWM trailing edge modulator with two integrators.

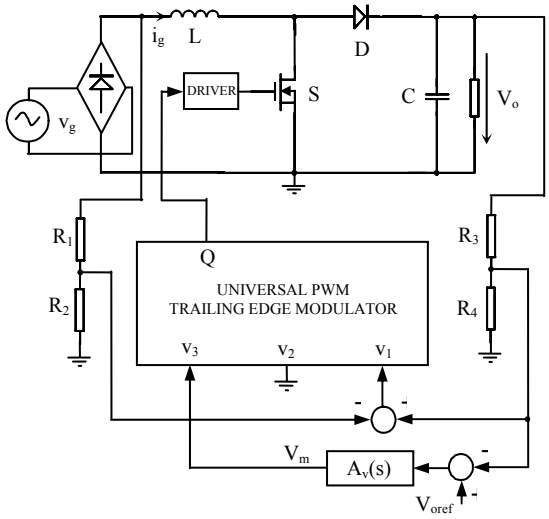

Fig.2. The PFC circuit based on the DCM BOOST converter with the universal PWM trailing edge

The universal PWM trailing edge modulator [3] with two integration steps, presented in Fig.3, implements a general type modulation equation such as:

$$v_+(t) = v_2 \frac{t}{T_s} + v_3 \left(\frac{t}{T_s}\right)^2 \tag{11}$$

In this relation, v_1, v_2, v_3 can be considered to have insignificant variations regarding the switching frequency, $v_+(t)$ being a polynomial function in t/T_s and representing the carrier signal for the modulator.

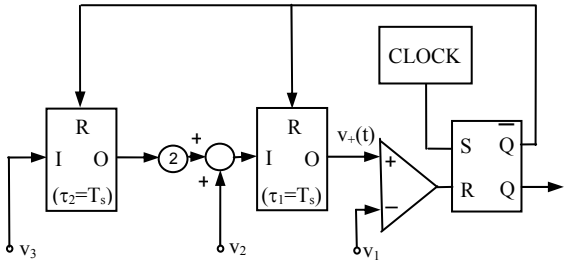

Fig.3. The universal PWM trailing edge modulator with two integration steps

From (9), the emulated resistance by the circuit is:

$$R_e = \frac{2Lf_s}{K}\frac{V_m}{V_o} \tag{12}$$

Now, knowing the values for V_m, K, V_M, the output power, $P_o = V_M^2 / 2R_e$, and the circuit elements, the output voltage provided by the circuit will result:

$$V_0 = \frac{4Lf_s}{K}\frac{P_o}{V_M^2}V_m \tag{13}$$

If the PFC circuit supplies a resistive load, then by replacing in (13) the output power as $P_o = V_o^2 / R$ it will lead to the output voltage relation as follows:

$$V_o = K\frac{R}{4Lf_s}\frac{V_M^2}{V_m} \tag{14}$$

III. HARDWARE IMPLEMENTATION OF THE CONTROLLER

The control circuit for the PFC circuit presented in Fig. 2 can be implemented by the schematic presented in Fig.4. It contains a clock generator for f_s , one latch, a comparator, two integration circuits which can be reseted through S_1 and S_2. By identifying the control signals with the ones from Fig.3 it can be easily observed that $v_1=K(V_o - v_g)$, $v_2=0$, $v_3=V_m$.

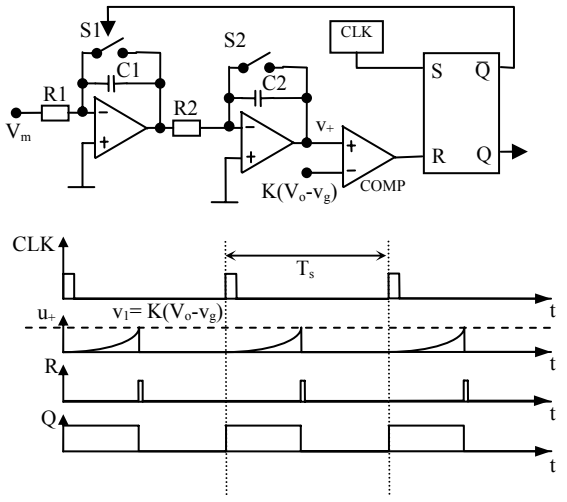

Fig.4. The integration control circuit schematic and his corresponding waveforms

On each clock signal, $Q=1$ and the transistor S is on. In the same time S_1, S_2 are in off state meaning that the integration circuits are performing the integration function. Assuming that the control voltage has a constant value, at the second integrator exit the resulting voltage will be given by:

$$v_+ = \frac{V_m}{2R_1C_1R_2C_2}t^2 \text{ , } 0 \le t \le T_s \tag{15}$$

When v_+ equals v_1 the latch will be reseted, the transistor S will be in off state, S_1 and S_2 will be on permitting for C_1, C_2 to be discharged in order to obtain $v_+=0$, meaning that the control circuit is ready for another switching period. Because $v_1 = v_+$ and taking into consideration (10) and (15), the integration control equation for the modulator circuit will be then:

$$K\left(V_o - v_g\right) = V_m \frac{T_s^2}{2R_1C_1R_2C_2}\left(\frac{t}{T_s}\right)^2 \tag{16}$$

From (7) and (16) the emulated resistance results:

$$R_e = \frac{V_m}{V_o}\frac{2Lf_s}{K}\frac{T_s^2}{2R_1C_1R_2C_2} \tag{17}$$

Considering the circuit operation at unity power factor ($V_M^2/(2R_e)=V_o^2/R$) and replacing R_e from (17) it will result the output voltage value:

$$V_o = \frac{V_M^2 R}{2V_m}\frac{K}{2Lf_s}\frac{2R_1C_1R_2C_2}{T_s^2} \tag{18}$$

In the last equation the load resistance can be replaced as $R=V_o^2/P_o$, meaning that (18) will finally become:

$$V_o = \frac{2V_mP_o}{V_M^2}\frac{2Lf_s}{K}\frac{T_s^2}{2R_1C_1R_2C_2} \tag{19}$$

The inductor L value results from the condition of unconditioned operation in DCM mode for BOOST converters [2], ($R=V_o^2/P_o$, $M_{min}=V_o/V_M$), as follows:

$$L < \frac{V_o^2}{4f_sP_oM_{\min}^2}\left(1-\frac{1}{M_{\min}}\right) \tag{20}$$

Finally, the value for the control voltage of the modulator circuit, assuming the operation at unity power factor, results from (19):

$$V_m = \frac{1}{2}K\frac{V_oV_M^2}{P_oL}f_s\tau_1\tau_2 \tag{21}$$

where $\tau_1=R_1C_1$, $\tau_2=R_2C_2$. The value of the dividing ratio between V_o and v_g , K, must be chosen in order to obtain a value for the control voltage V_m normally between *0* and *15* volts. Having V_m it is easily to find the value of the product between τ_1 and τ_2. Practically the R_1C_1, R_2C_2 values (usually $\tau_1 = \tau_2$) can be find by imposing that the exit values of the integration circuits are to remain in the range of their supplying voltages.

IV. SIMULATION RESULTS

In order to verify the correct behavior of the proposed PFC circuit, a simulation was performed in the CASPOC medium (Simulation Research).

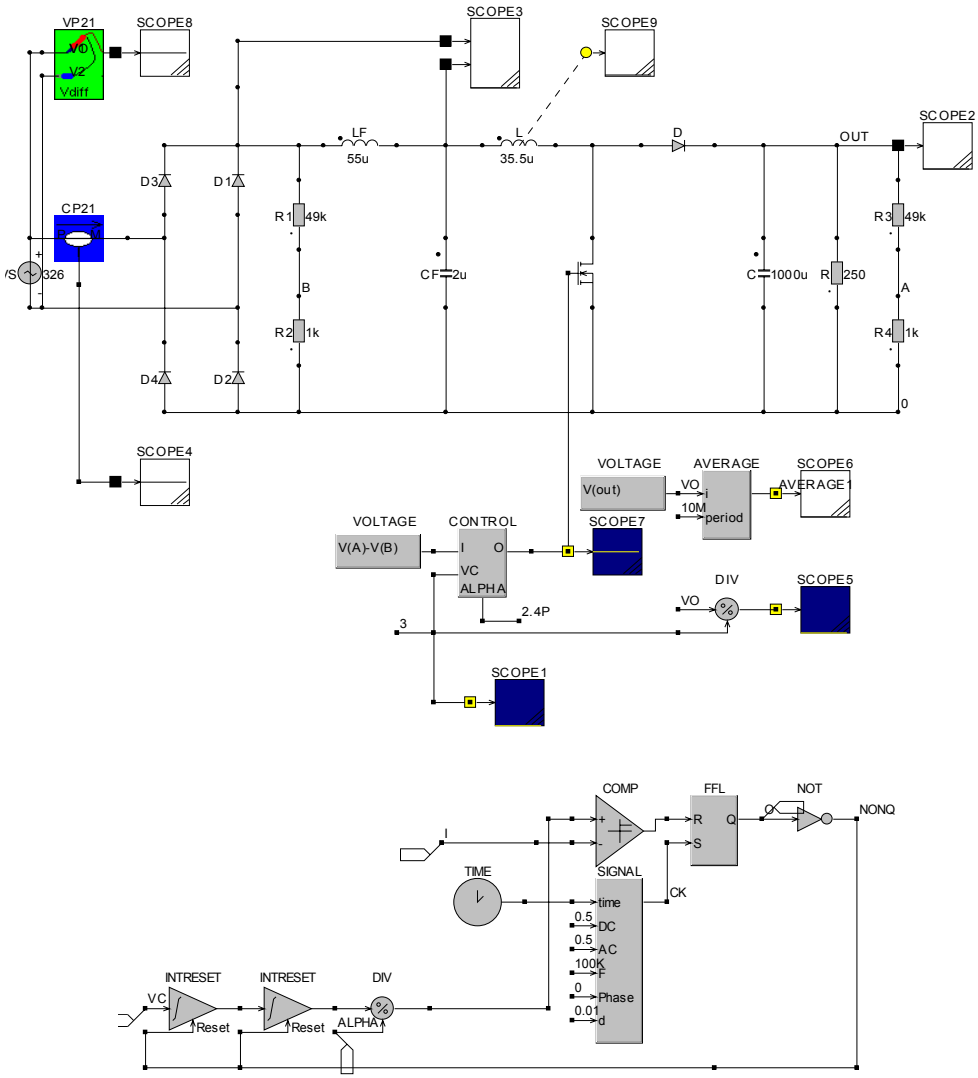

Fig.5. Simulation circuit in CASPOC for the DCM BOOST PFC circuit with integration control and the architecture of the integration control circuit (CONTROL.lib)

The peak mains voltage is *326V* at *50Hz* frequency, the value of the *L* inductor is *35.5μH*, the output power P_o*=1.44kW* and output voltage V_o*=600V* are corresponding to a resistive load *R=250Ω*. The circuit used for simulation, containing a RF input filter and the library block architecture of the integration control circuit are presented in Fig.5.

The waveforms corresponding to the input current, absorbed from the mains supply by the PFC circuit, together with the mains supply voltage, are presented in Fig.6. It can be easily observe that the input current shape is sinusoidal and also it is in phase with the mains input voltage.

The converter inductor current waveform and also a detailed section of the same current, showing the DCM operation mode, are presented in Fig.7.

The spectral analysis of the input current (in the presence of a RF input filter) performed in MATLAB, presented in Fig.8, reveal very good values for the merit parameters as it can be seen from Table1 (only harmonics until the 20th order were considered) and Tabel2 (all the harmonics were considered).

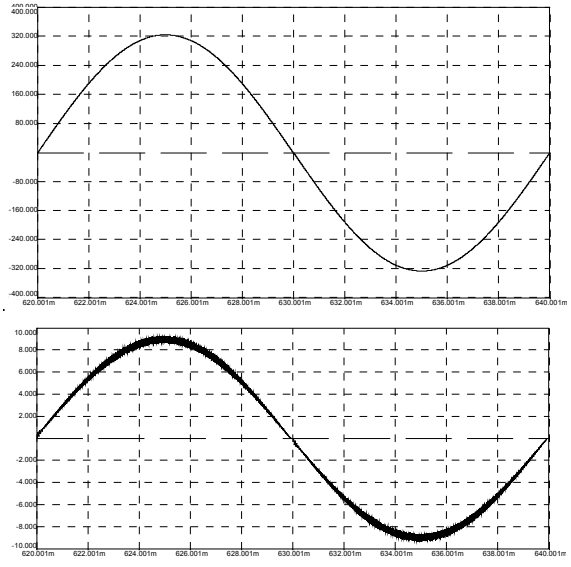

Fig.6. The mains supply voltage (up) and the input current of the PFC circuit (down)

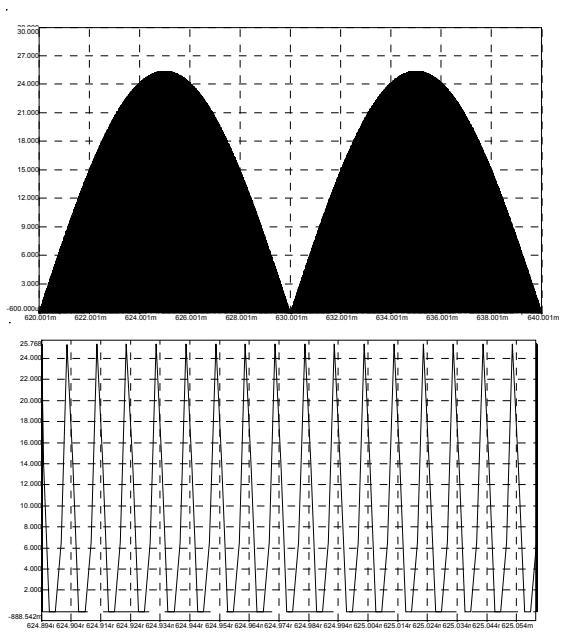

Fig.7. The inductor current, i_g, (up) and a detailed part revealing the DCM operation mode (down)

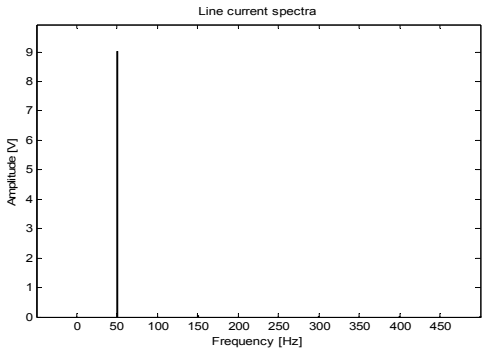

Fig.8. Spectral analysis of the PFC circuit input curent in the presence of a RF input filter

Table 1

THD_tr [%]	***Kd_tr***	***Φ1 [deg]***	***Kφ***	***PF_tr***
0.3353	1.0000	2.7033	0.9989	0.9989

Table 2

THD_tot [%]	***Kd_tot***	***Φ1 [deg]***	***Kφ***	***PF_tot***
2.6035	0.9997	2.7033	0.9989	0.9985

The resulted merit parameters which are presented in the tables above are: total harmonic distortion factor *THD*, distortion factor K_d, the angle between the input current fundamental and the supply voltage φ_1, displacement factor K_φ and the power factor *PF*

V. CONCLUSIONS

The classical approaches of the PFC circuits based on DCM operated BOOST converters are presenting a series of main disadvantages due to the necessity of eliminating the current distortions, such as: an output voltage value much larger than the input one, variable switching frequency and at least one multiplier in critical mode control or complex control circuits, the necessity of current sensing in non-linear carrier control method.

The proposed integration control method for a DCM BOOST PFC circuit presents a series of major advantages: provides unity power factor, does not require that the output voltage to be significantly greater compared to the input one, operation at constant switching frequency, no needing of multipliers or other complex circuits, does not need the input current sensing. The integration control circuit, based on the universal PWM trailing edge modulator, is easy to be implemented in a simple manner with two integration circuits, a comparator and a latch.

As the simulation results are showing, very good values of the main merit parameters can be obtained.

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A Quadratic Boost Converter with PFC Applications

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Abstract – A novel quadratic boost converter capable of delivering a high output voltage is introduced. Dc-dc operation in continuous conduction mode (CCM) and discontinuous inductor current mode (DICM) are analyzed. A simple and versatile feedforward (FF) circuit is proposed in order to be used with the new converter when operated in CCM. Another application is the use of the converter as a power factor correction (PFC) circuit. At low power levels DICM operation is chosen because of the converter natural capability of emulating a resistor at low frequency. Design equations, simulation results and merit parameters are presented for all the investigated topologies.

Keywords: converter synthesis, quadratic converters, feedforward, power factor correction, simulation.

I. INTRODUCTION

It is known that in high-voltage/low current applications such as TV-CTR's, lasers, X-ray systems, ion pumps, electrostatic systems, etc. a capacitor-diode voltage multiplier is preferable to a transformer. The solution of a BUCK converter followed by a push-pull multiplier has the drawback of using three active switches and therefore a complex control. Moreover, as the input current is discontinuous an input filter is invariably required.

In dc-dc converters applications operating with a wide range of input and/or output voltages, conventional PWM converters must operate at very small or very large values of the duty cycle. These operation modes are severe restricted by the transistors on-time (t_{ON}) or off-time (t_{OFF}) minimum values. These drawbacks are eliminated by the quadratic converters [1], having the static conversion ratio M ($M = Vo/Vg$) as a rational function of two polynomials, at least one of them being of second order.

The novel single-stage high voltage converter proposed in the paper is suitable to provide a high voltage. Converter topology is derived and CCM operation is analyzed in Section II. Converter operation in DICM mode is investigated in Section III, while its power factor correction capability is revealed in Section IV. The theoretical concepts are verified by simulation in Section V while Section VI is devoted to conclusions.

II. THE NEW QUADRATIC BOOST CONVERTER

It is known [1], [4] that quadratic converters cannot be realized with less than two capacitors, two inductors and four switches, but the number of transistor switches can be reduced to one. The technique based on rotating basic switching cells [2] is employed here for deriving the new BOOST topology. Namely, assuming the input source and the load share a common terminal, as Fig. 1 presents, a three-terminal switching cell is connected between the terminals *g*, *l* and *c* in all the six possible ways and for each topology switch synthesis [4] is performed. The basic

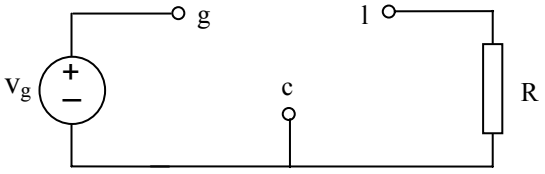

Fig. 1. The supply voltage and the load sharing the same ground terminal.

cell used here is drawn in Fig. 2. Switches S_1 and S_3 are synchronously driven, while S_2 and S_4 are complementary driven to S_1 and S_3. This is denoted by the negation sign accompanying them. The duty cycle D is related to switches S_1 and S_3.

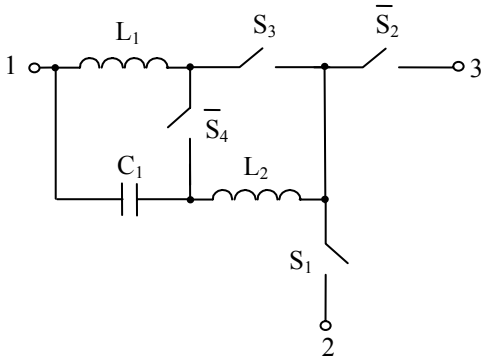

Fig. 2. The basic switching cell.

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The new converter topology corresponds to the connection $1 \to l, 2 \to c, 3 \to g$ and after switch implementation the resulting structure is that shown in Fig. 3.

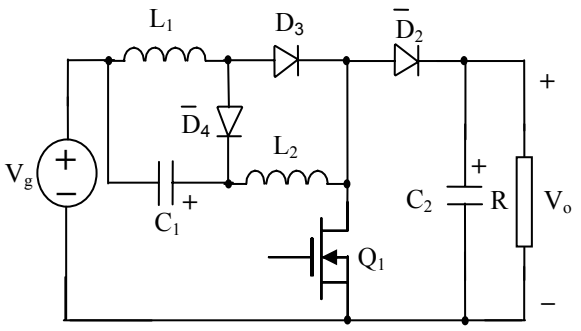

Fig. 3. The new BOOST converter topology.

Assuming ideal components and CCM operation, during the first topological state, when Q_1 and D_3 are on and D_2 and D_4 are off, the input voltage is applied across inductor L_1, while the voltage across L_2 equals $V_{C1}+V_g$. In the second topological state V_{C1} is opposite applied across L_1, while $V_{C1}+V_g-V_{C2}$ is applied across L_2. Imposing volt-second balance over L_1 and L_2 one obtains:

$$DV_g + (1-D)(-V_{C_1}) = 0 \quad (1)$$

$$D(V_{C_1} + V_g) + (1-D)(V_{C_1} + V_g - V_{C_2}) = 0 \quad (2)$$

From (1) and (2) the static conversion ratio is:

$$M = \frac{V_o}{V_g} = \frac{1}{(1-D)^2} \quad (3)$$

Given the output power, the output voltage and the input voltage the average semiconductor currents and voltage stresses are presented in Table 1. The stresses are computed in CCM assuming that ac ripples of the inductor currents and capacitor voltages are negligible. For comparison, the same stresses in the classical BOOST converter operating under the same conditions are provided in Table 2.

Comparing the results in the two tables it can be easily seen that for Q_1 and D_2 the current and voltage stresses are the same as the transistor and diode stresses in the classical BOOST converter, while for D_3 and D_4 the voltage stresses are lower than in the classical converter.

III A FEEDFORWARD CIRCUIT FOR CCM OPERATION OF THE NEW CONVERTER

For switching converters feedforward compensation is effective in reducing effects of source disturbances on converter outputs and improving steady-state and dynamic responses. A converter with FF behaves at low frequencies as a linear power amplifier with constant gain, independent of operating conditions.

In deriving the FF controller let us impose the average output voltage V_o to be equal to the control voltage v_m

Table 1.

	Proposed BOOST quadratic converter
V_{Q1}	V_o
I_{Q1}	$P_o\left(\frac{1}{V_g}-\frac{1}{V_o}\right)$
V_{C1}	$V_g\left(\sqrt{\frac{V_o}{V_g}}-1\right)$
V_{C2}	V_o
I_{L1}	$\frac{P_o}{V_g}$
I_{L2}	$\frac{P_o}{V_o}\sqrt{\frac{V_o}{V_g}}$
V_{D2}	V_o
I_{D2}	$\frac{P_o}{V_o}$
V_{D3}	$V_o\left(1-\sqrt{\frac{V_g}{V_o}}\right)$
I_{D3}	$\frac{P_o}{V_g}\left(1-\sqrt{\frac{V_g}{V_o}}\right)$
V_{D4}	$\sqrt{V_o V_g}$
I_{D4}	$\frac{P_o}{V_o}\sqrt{\frac{V_o}{V_g}}$

Voltage and current stresses in the proposed quadratic BOOST converter.

Table 2

	Classical BOOST converter
V_Q	V_o
I_Q	$P_o\left(\frac{1}{V_g}-\frac{1}{V_o}\right)$
V_C	V_o
I_L	$\frac{P_o}{V_g}$
V_D	V_o
I_D	$\frac{P_o}{V_o}$

Voltage and current stresses in the classical BOOST converter.

multiplied by the constant gain A:

$$V_o = A \cdot v_m \quad (4)$$

On the other side, the input and output voltages are related by the static conversion ratio given by (3). From (3) and (4) it results that:

$$v_m(1-D)^2 - \frac{v_g}{A} = 0 \quad (5)$$

As it is known [6], trailing-edge, leading-edge or both-edge pulse width (PWM) modulators can be used. For the proposed converter a leading-edge (LE) modulator is proposed. Although a trailing-edge modulator could also be used, this choice is more convenient because it is much simpler. In a LE modulator the falling edge of the output logic-level function coincides with the short-pulse constant frequency clock, while the rising edge corresponds to the zero crossing of the modulator function. The modulator function is found from (5) if we let $D \to 1 - \frac{t}{T_s}$, resulting in:

$$v_m\left(\frac{t}{T_s}\right)^2 - \frac{v_g}{A} = 0 \qquad (6)$$

It can be seen that in the modulator function (the right hand side of (6)) the term $v_m\left(\frac{t}{T_s}\right)^2$ occurs. This term can be implemented without fast multipliers or relatively complex nonlinear elements. The implementation makes use of integrators with reset, just as in conventional PWM controllers and is based on the observation that the control voltage v_m is a slow varying signal compared to the switching frequency. Practically, in open loop operation v_m is constant. Mathematically, we can use the following approximation:

$$v_m\left(\frac{t}{T_s}\right)^2 \cong \frac{1}{\frac{T_s}{2}}\int_0^t\left(\frac{1}{T_s}\int_0^t v_m(u)du\right) \qquad (7)$$

Relationship (7) clearly suggests that the implementation of the term $v_m\left(\frac{t}{T_s}\right)^2$ consists of a cascade of two integrators with reset having the time constants equal to the switching period T_s and half of the switching period respectively. The practical implementation is shown in Fig. 4. Beside the two integrators only a comparator and a flip-flop are needed. The FF circuit can be easily constructed as an integrated circuit or with general-purpose components such as comparators, flip-flops and operational amplifiers. One can easily derive that in case of the architecture in Fig. 4 the output voltage is:

$$V_o = \left(1 + \frac{R_1}{R_2}\right)\cdot\frac{1}{2R_3C_3R_4C_4f_s^2}\cdot v_m \qquad (8)$$

IV OPERATION IN DISCONTINUOUS INDUCTOR CURRENT MODE AND AS A POWER FACTOR CORRECTION CIRCUIT

As three passive switches are present in the converter, theoretically DCM modes can be related to any of the diodes. However, only D_2 and D_4 can induce discontinuous inductor current operation (DICM) as the current through D_3 has a positive slope during the

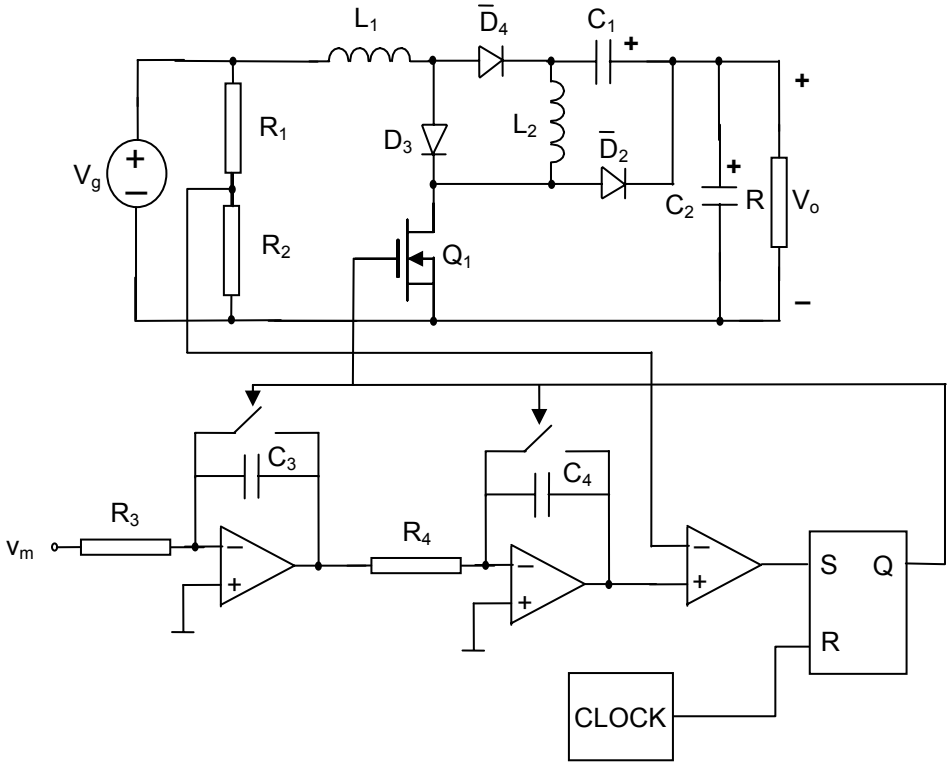

Fig. 4. The new quadratic BOOST converter and the feedforward circuit.

first topological state. It can be demonstrated that the DICM operation induced by D_4 is quantitatively given by the condition:

$$\frac{2L_1 f_s}{R} \le D(1-D)^4 \tag{9}$$

In case of DICM operation because of D_2, the condition becomes:

$$\frac{2L_2 f_s}{R} \le D(1-D)^2 \tag{10}$$

Because during its on state the averaged input current equals i_{L1}, it becomes obvious that in DICM due to D_1 the averaged input current shape is the same as in the conventional boost converter. The inductor current i_{L1} waveform is presented in Fig. 5.

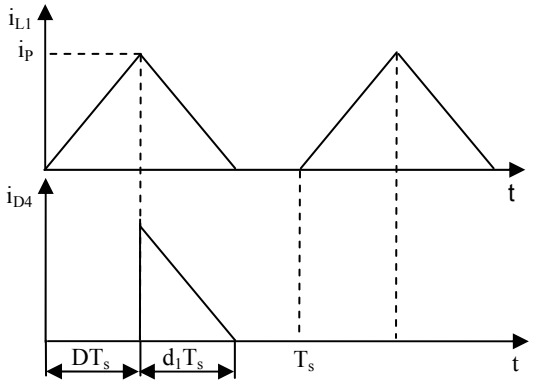

Fig. 5. Input inductor and diode D_4 waveforms.

The operation in DICM due to D_4 and the waveforms in Fig. 5 suggest the possibility to use the converter as an "automatic" or "natural" current shaper when operating in DICM. This is similar and "inherited" from the classical BOOST converter, being a simple solution at low power levels. Keeping in mind that v_g is now the output of a full wave uncontrolled rectifier fed by a sinusoidal voltage of angular frequency ω and amplitude V_M, we have

$$v_g = V_M \left|\sin \omega t\right| \tag{11}$$

Quasi steady state operation related to the line frequency and constant voltage on C_1, are assumed [6]. Therefore we can admit that $\overline{i_{C_1}} = 0$ and $\overline{i_g} = \overline{i_{L_1}}$

Volt-second balance on L_1 provides:

$$Dv_g + d_1(-V_{C_1}) = 0 \tag{12}$$

resulting in:

$$d_1 = D\frac{v_g}{V_{C_1}} \tag{13}$$

On the other side, i_P is given by:

$$i_P = \frac{v_g}{L_1} DT_s \tag{14}$$

The averaged value of the input current is given by:

$$\overline{i_g} = \overline{i_{L_1}} = \frac{1}{T_s}\frac{1}{2}(D + d_1)T_s i_p \tag{15}$$

In (15) if d_1 is replaced from (13) and i_P from (14), it follows that:

$$\bar{i}_g = \frac{v_g}{R_e} \cdot \left(1 + \frac{V_M}{V_{C_1}}\left|\sin \omega t\right|\right) \tag{16}$$

where the emulated resistance is:

$$R_e = \frac{2L_1 f_s}{D^2} \tag{17}$$

From (16) the power factor (PF) and the total harmonic distortion coefficient (THD) can be evaluated as:

$$PF = \sqrt{\frac{2}{\pi}} \frac{\int_0^0 \sin^2\theta(1 + a\sin\theta)d\theta}{\sqrt{\int_0^\pi \sin^2\theta(1 + a\sin\theta)^2 d\theta}} \tag{18}$$

$$a = \frac{V_M}{V_{C1}} \qquad THD = \sqrt{\frac{1}{PF^2} - 1} \tag{19}$$

These two merit parameters are represented in Fig. 6 as a function of the ratio V_{C1}/V_M. It can be seen that very good PF and THD can be obtained when V_{C1}/V_M >0.5, which in practice can be easily achieved.

Inductor L_1 design equation is obtained imposing DICM operation over the whole line half cycle when operated as a PFC circuit. This condition will significantly differ from that of DICM operation as a dc/dc converter given by (9). The design equation can be derived as in [4] and finally results in:

$$L_1 \le \frac{V_M^2}{4P_o f_s}\left(1 - \sqrt{\frac{V_M}{V_o}}\right) \tag{20}$$

V SIMULATION RESULTS

All simulations were performed using the CASPOC package (Simulation Research) [7]. First the new quadratic BOOST converter with feedforward, similar to the architecture presented in Fig. 4, was simulated. Converter parameters were:

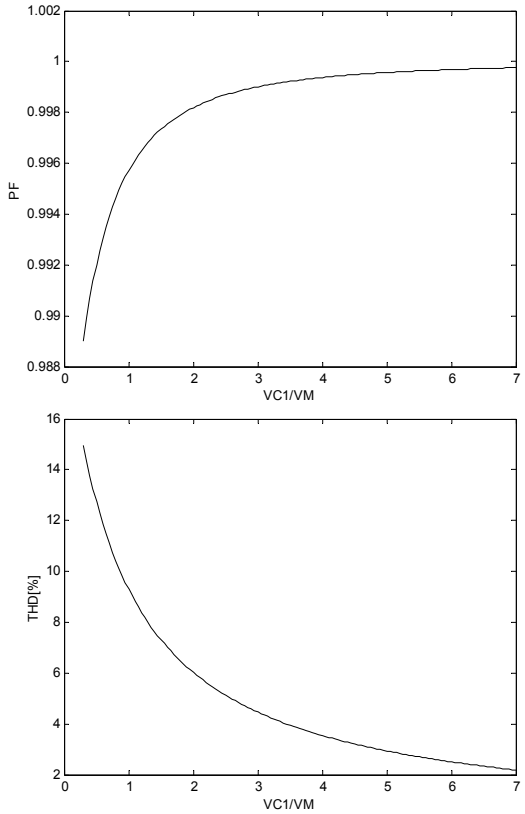

Fig. 6. Power factor and input current TDH as a function of the ratio V_{CI}/V_M in DICM.

$$L_1 = 237\mu H;\ L_2 = 415\mu H;\ C_1 = C_2 = 10\mu F;$$
$$R = 100\Omega;\ f_s = 40kHz;$$
$$v_m = 3V;\ R_1 = 90k\Omega;\ R_2 = 10k\Omega;\ R_3 = R_4 = 2k\Omega;$$
$$C_3 = 12.5nF;\ C_4 = 6.25nF$$

The input voltage was forced to vary with a square waveshape between 8V and 14 V. The simulation results are shown in Fig. 7. It can be seen that after short transients the output voltage tightly follows the prescribed 30V value.

Then the converter was simulated in a PFC application with DICM operation. The parameters of the PFC circuit were:

$$V_M = 70V;\ L_1 = 30.6\mu H;\ L_2 = 0.5mH;\ C_1 = 1\mu F;$$
$$C_2 = 470\mu F;\ P_o = 40W;\ V_o = 400V;\ R = 100\Omega;$$
$$f_s = 40kHz;\ D = 0.2;$$

After the uncontrolled bridge supplying the converter, a small high frequency filter with L_F=80μH and C_F=2μH was used, in order to suppress the high frequency components from the input current which are large in DICM. In Fig. 8 the input voltage and current waveforms are presented. The expected output voltage of 400 V was confirmed by the simulation which provided an output voltage of 406 V. It can be seen that qualitatively the input current has a closely sinusoidal shape and tightly follows the input voltage. Harmonic analysis of the input current was performed. The input current spectrum is shown in Fig. 9. The input current total harmonic distortion (THD) coefficient was 2.52%, while unity

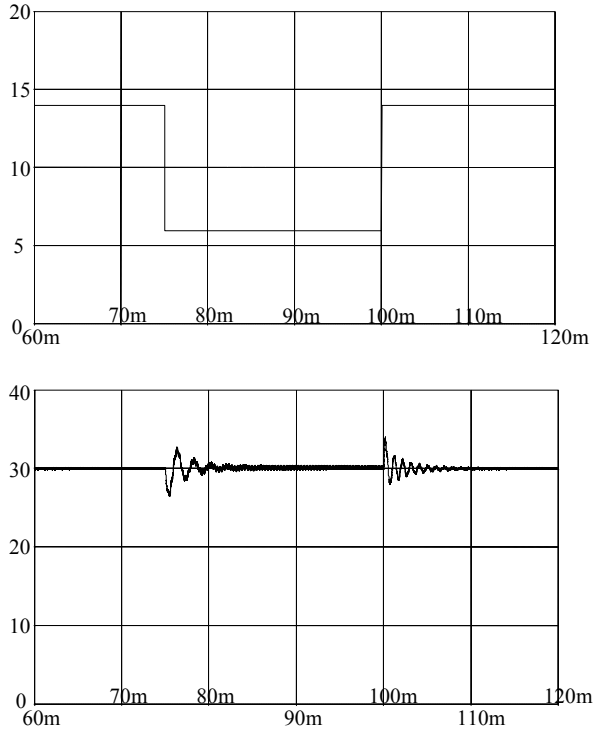

Fig. 7. Dynamic operation of the quadratic BOOST converter with FF. Input voltage (up) and output voltage (down).

displacement power factor was found. An excellent total power factor of 0.996 was achieved.

VI CONCLUSIONS

A novel quadratic BOOST converter is proposed. Containing only a single transistor and three diodes, the converter can be easily controlled. The proposed topology exhibits better efficiency compared to a two stage configuration. High output voltages can be obtained and because the minimum off-time is much less restrictive, the converter can operate at a relatively high frequency (500 kHz). A feedforward circuit is developed to be used with the proposed converter. It consists of only two integrators, one comparator and a flip-flop and therefore it can be implemented on an integrated circuit or with general-purpose components.

The proposed converter is well suited for PFC applications at low power levels. DICM operation of the converter can be exploited because its natural property to be an "automatic" current shaper. This solution leads to a very simple control, without a current loop. Design equations, and DICM operation conditions are provided both for dc/dc and for PFC operation in order to quickly design the required topology.

The simulation results confirmed all the theoretical predictions regarding the converter, the feedforward controller and the PFC applications.

Thus the new converter together with the proposed controller provides simple solutions for wide range dc/dc applications and for low power level power factor correctors.

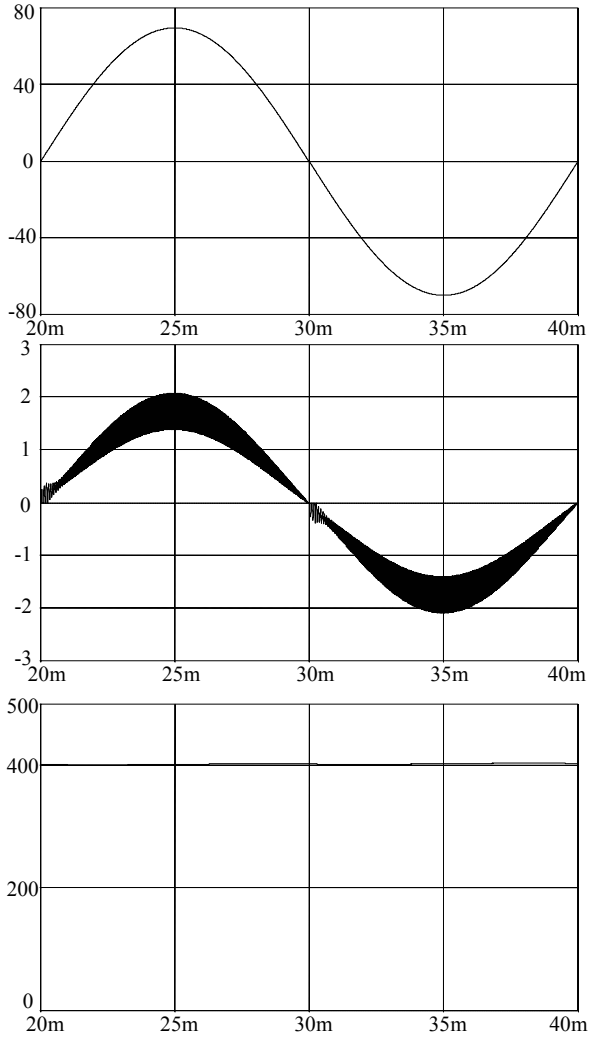

Fig. 8. PFC operation of the new converter in DICM mode. Input voltage, input current and output voltage (this up to down order).

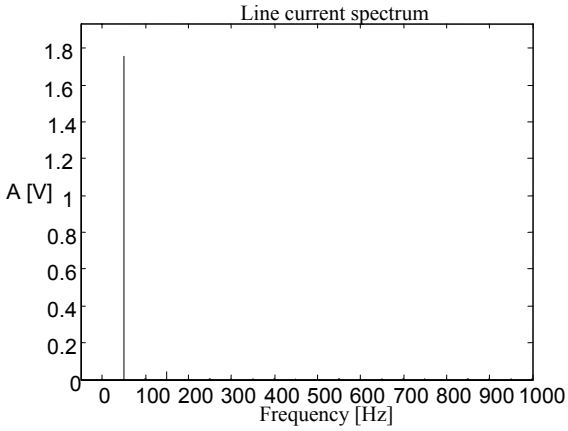

Fig. 9. Input current spectrum – first 20 harmonics.

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Active compensation in a low voltage network comprises power factor correction capacitor with harmonic current producing loads

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Abstract—**In this paper, a compensation strategy for a low-voltage network comprises a power factor correction capacitor and non- linear loads connected to the same load-buss is investigated. The loads in the low- voltage network can be classified, from the harmonics point of view, into harmonic current producing loads, harmonic voltage producing loads and harmonic sensitive loads. The compensation in the low -voltage side of a power network is more reliable, efficient, economic and straightforward. The idea here stems from the fact that when applying a pollution treatment for a river, it is not practical, in all cases, to establish a treatment unit across the river. The more reliable solution is to clean and purify those outlets discharging into the river individually. If this concept could be generalized in industry, it is logical that the cost of applying the proposed compensation strategy to an industrial unit would not be comparable either to the price of the production line or to the penalties paid to authority on the long run. In the next sections, the proposed strategy will be clarified through analysis, design and simulation using a shunt active power filter.**

I. Introduction

Non-linearities were brought to the utility network with the increasing use of power semi-conductor devices in industrial control. Using these devices in power control creates serious harmonics problems. Power converters have a significant contribution in generating harmonics during switching actions. Low order harmonics usually have considerable magnitudes and diversified phase angles [1]. These harmonics are responsible for the distortion of the line voltage and lead to several adverse effects including equipment overheating, the malfunction of solid-state devices and interference with communication systems [2]. Industrial loads are the massive part of the load of any utility network. These loads are responsible for most problems of power quality [3]. Power factor correction capacitors are connected mainly to a load-buss to control and improve the displacement factor due to linear loads. However, the idea of dealing with the problem of power quality partially on a limited scale is quite convenient. In this case, the load is assumed precisely identified and accordingly, both of current and voltage profiles are predictable at the different loading conditions. In a large multi-busses power system, the loads are changing randomly each moment. Therefore, besides the well-known problems of applying compensation to such systems, the control techniques discussed in the literature were suffering from the problem of that time delay between the moment of measuring the load voltage and /or current and that of injecting the compensating current [4]. What can be called "a time-racing problem" arises here because the proper compensating current for the passed moment would not be the same for now as the load surely changes.

II. System Description

An industrial load can be modeled by non-linear load connected to the mains as shown in Fig.1.

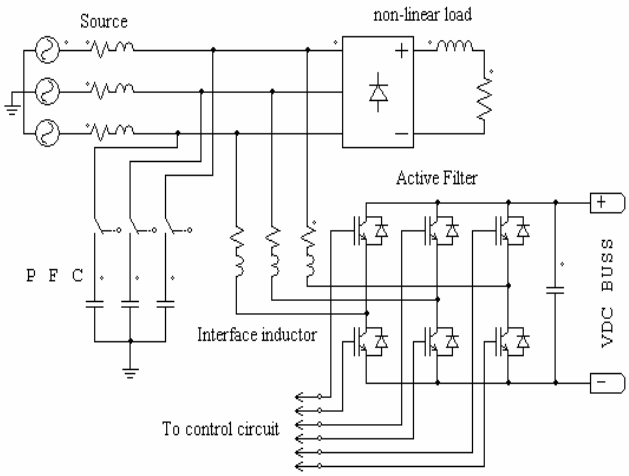

Fig. 1. System configuration.

The shunt active filter is mainly a voltage fed -inverter designed to pump a controllable reactive current into the point of common coupling via an interface inductor. The power factor correction capacitor is connected to the same buss with the shunt active filter. The non-linear load as shown is a harmonic current producing type. The bases of the IGBT power transistors are connected to the control circuit. This control circuit is a PWM modulator operates at a high frequency carrier to modulate the inverter current to track a reactive current reference signal. The idea of the current controller is based upon

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sensing the output- inverter current and comparing it to a desired reference. By a proper design of a PID controller, the inverter current can be forced to track its reference at steady state.

III. Analysis

A study for compensation in a low voltage network was introduced in [5]. Taking the interactions of circuit parameters into consideration, it was shown that the optimum compensation is achieved when the following two conditions are fulfilled,

$$I_f = k\, I_{L0}\ (\omega = \omega_h) \tag{1}$$

$$\left|\frac{Z_L}{1-k}\right|_{\omega=\omega_h} >> \left|Z_s\right|_{\omega=\omega_h} \tag{2}$$

Where, (I_{L0}) is the load current, (Z_L) is the equivalent load impedance, (I_f) is the reactive current injected by the shunt active filter, (Z_s) is the equivalent source impedance including the impedance of the feeder- cable to the load, (ω_h) is the frequency of the higher dominant harmonics and (k) is the active filter gain. The optimum theoretical value of (k) is unity when $\omega=\omega_h$ but practically and due to physical limitations, it swings around 0.9 for proper design [5].

The power factor correction capacitor creates a transient voltage magnification when switched into the power system [6]. These voltage surges are dangerous for the semi-conductor switches of the active filter. On the other hand, the capacitor bank itself constitutes an upstream low- impedance path for the reactive current at steady state. The result out of this is that the condition in (2) is no longer hold. As a consequence, the input DC voltage of the inverter fluctuates severely around its nominal value and the performance of the active filter becomes unsatisfactory. To solve this problem, it is necessary to shunt a capacitor (C_f) across the terminals of the DC supply. The DC voltage across this capacitor is regulated and controlled, in a way, to regain the power balance between the active filter and the mains. Moreover, the DC voltage across (C_f) must be kept constant to provide a stable operation for the shunt active filter [7].

IV. Reference Current Generation

The instantaneous active and reactive power theory, which referred to as p-q theory, is being used successfully to design and control the active filters. Starting with Park's vector definition for voltage and current and projecting these vectors in two orthogonal stationary frame coordinates α-β, the instantaneous values of active and reactive power can be easily measured. The instantaneous active power (p) and reactive power (q) can be also solved into their fundamental components $\bar{p}$ and $\bar{q}$ and their harmonic components $\tilde{p}$ and $\tilde{q}$ respectively. These $\tilde{p}$ and $\tilde{q}$ are responsible for what so-called "the harmonic distortion power".

There are several ways to derive the p-q algorithms. This entirely depends upon the compensation strategy and the optimum power flow of the system [8]. In this paper, the two components of the reactive reference current ($i_{\alpha q}$ and $i_{\beta q}$) are extracted by online calculations. Both of the load voltage and current in a-b-c reference frame are sensed and transformed into α-β orthogonal frame. The p-q algorithm used to calculate ($i_{\alpha q}$ and $i_{\beta q}$) is:

$$\begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} = \frac{1}{\left|v_\alpha{}^2 + v_\beta{}^2\right|} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} \hat{p} \\ \hat{q} \end{bmatrix} \tag{3}$$

Where,

$$\hat{p} = -\tilde{p} + p_{av} \tag{4}$$

$$\hat{q} = -\tilde{q} \tag{5}$$

The instantaneous active power (p) and reactive power (q) are defined in α-β orthogonal frame according to the p-q theory as:

$$p = i_\alpha v_\alpha + i_\beta v_\beta = \bar{p} + \tilde{p} \tag{6}$$

$$q = v_\beta i_\alpha - v_\alpha i_\beta = \bar{q} + \tilde{q} \tag{7}$$

Two high pass filters are required to extract both of $\tilde{p}$ and $\tilde{q}$ from (p) and (q) of (6) and (7) respectively. The still-missed term in (4) is (p_{av}). This term is obtained by regulating the DC voltage across the capacitor (C_f) at the input of the inverter. The actual capacitor voltage is compared to a reference value to obtain the error signal. This error signal contains a higher- frequency component due to the high frequency switching of the inverter. After filtering out this high frequency component using a low pass filter, the error signal is fed to a P-I controller, which is the heart of the voltage loop controller. The output of this controller represents the average active power (p_{av}) that passed back to the algorithm of (3). Fig.2 shows the voltage loop controller as simulated by PSIM ®.

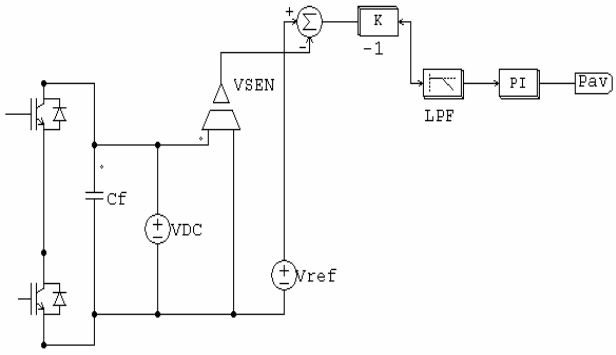

Fig. 2. The voltage loop controller.

IV. Design of Current Controller

It is convenient to design the current controllers in d-q synchronous frame. The design of a P-I controller in d-q frame eliminates the steady state error since it operates on D.C quantities and the integrator has infinite gain at zero frequency [9].

In Fig.1, assuming that the line voltages at the point of common coupling are e_a,e_b and e_c whereas the output

voltages of the inverter are v_a,v_b and v_c then, the voltage equations across the interface inductor are:

$$e_a - v_a = L\frac{d\,i_a}{d\,t} + R\,i_a \quad ;$$

$$e_b - v_b = L\frac{d\,i_b}{d\,t} + R\,i_b \quad ;$$

$$e_c - v_c = L\frac{d\,i_c}{d\,t} + R\,i_c \qquad (8)$$

Where, (L) and (R) are the inductance and the internal resistance of the interface inductor respectively. These equations in the stationary a-b-c frame are transformed into the synchronous rotating d-q frame as in [9]. The coupled voltage equations are:

$$\frac{di_d}{dt} = \frac{e_d}{L} - \frac{R}{L}i_d + \omega i_q - \frac{v_d}{L} \quad ;$$

$$\frac{di_q}{dt} = \frac{e_q}{L} - \frac{R}{L}i_q - \omega i_d - \frac{v_q}{L} \qquad (9)$$

A method for de-coupling these equations is described in [10]. Two control parameters h_d and h_q are introduced. The cross coupling terms are grouped into h_d and h_q as follows:

$$h_d = e_d - v_d + \omega L\,i_q \qquad (10)$$

$$h_q = e_q - v_q - \omega L\,i_d \qquad (11)$$

Substituting h_d and h_q into (9), the simplified de-coupled state equations are:

$$L\frac{di_d}{dt} = h_d - R\,i_d \qquad (12)$$

$$L\frac{di_q}{dt} = h_q - R\,i_q \qquad (13)$$

Taking Laplace transform for both sides of (12) and (13) and rearranging, the transfer functions that relate the output parameters (i_d and i_q) to the new input parameters (h_d and h_q) can be obtained.

The components of reference reactive current in the d-q synchronous rotating frame are obtained by transforming ($i_{\alpha q}$ and $i_{\beta q}$) from the α-β frame into the d-q frame. Assuming that α-axis coincides with the d-axis, then the components of the reference reactive current i_d^* and i_q^* in the d-q frame are:

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \qquad (14)$$

Where (ω) is the supply frequency. The complete closed loop current controller is shown in Fig.3.

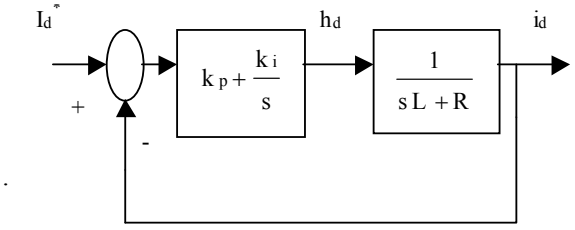

Fig. 3 The closed loop current controller.

It should be noted here that the closed loop current controller of i_q is identical to that of i_d. The design procedure of the P-I controller for a similar second order system is discussed in more details in [10]. Accordingly, the parameters of the P-I controller are found to be:

$$k_p = 2\xi\omega_n L - R$$

$$k_i = L\,\omega_n^2$$

A control criteria to select the proper values of the damping ratio (ξ), the natural frequency (ω_n) and the cutoff frequency of the interface filter, which filters out the unwanted higher harmonics of the inverter current and for simplicity is not shown in Fig.1, is also discussed in the same reference.

V. Design of the Voltage Controller

The state equation describes the current balance in the capacitor circuit is:

$$\frac{dV_{dc}}{dt} = \frac{1}{C_f}(S_a i_a + S_b i_b + S_c i_c) \qquad (15)$$

Where S_a , S_b and S_c are the switching functions of the inverter switches. For a PWM controlled inverter, these switching functions are non-linear in their nature. The output voltages of the inverter v_a, v_b and v_c can be expressed in terms of these switching functions as follows:

$$v_a = S_a V_{dc} \quad ;$$

$$v_b = S_b V_{dc} \quad ;$$

$$v_c = S_c V_{dc} \qquad (16)$$

Taking only the fundamental components of these switching functions into consideration, S_a, S_b and S_c can be written in a-b-c reference frame as [10]:

$$S_a = \frac{M}{\sqrt{3}}\cos(\omega t + \delta);$$

$$S_b = \frac{M}{\sqrt{3}}\cos(\omega t + \delta + \frac{2\pi}{3});$$

$$S_c = \frac{M}{\sqrt{3}} \cos(\omega t + \delta - \frac{2\pi}{3}) \quad (17)$$

Where (M) is the modulation index and (δ) is the power angle. The transformation of the equations set (17) into d-q synchronous rotating frame gives:

$$S_d = \frac{M}{\sqrt{2}} \cos(\delta);$$

$$S_q = \frac{M}{\sqrt{2}} \sin(\delta) \quad (18)$$

Applying the same transformation to the equations set of (16) gives:

$$v_d = S_d V_{dc};$$

$$v_q = S_q V_{dc} \quad (19)$$

Substituting (v_d) and (v_q) into (10) and (11), then (15) can be rewritten in terms of the control parameters (h_d) and (h_q) as follows:

$$\frac{dV_{dc}}{dt} = \frac{e_d - h_d}{C_f V_{dc}} i_d + \frac{e_q - h_q}{C_f V_{dc}} i_q \quad (20)$$

However, for more clarity, (20) can be written in terms of the cross-coupled parameters as:

$$\frac{dV_{dc}}{dt} = \frac{S_d V_{dc} - \omega L i_q}{C_f V_{dc}} i_d + \frac{S_q V_{dc} + \omega L i_d}{C_f V_{dc}} i_q \quad (21)$$

As the dynamics of the current controller is much faster than the dynamics of the voltage controller and the inductance of the interface inductor (L) is normally << 1, then, (21) can be simplified to:

$$\frac{dV_{dc}}{dt} = \frac{1}{C_f} (S_d i_d + S_q i_q) \quad (22)$$

Applying linearization to (22), the linearized- voltage state equation becomes:

$$C_f \frac{dV_{dc}}{dt} = \bar{S}_d \Delta i_d + \bar{S}_q \Delta i_q + \bar{i}_d \Delta S_d + \bar{i}_q \Delta S_q \quad (23)$$

Neglecting the dependency of i_d and i_q on the input variables S_d and S_q and taking into consideration that the voltage controller must act on the direct component of the current i.e. i_d hence, (23) is simplified to:

$$\frac{dV_{dc}}{dt} = \frac{\bar{S}_d}{C_f} \Delta i_d \quad (24)$$

The intermediate value of (S_d) which denoted ($\bar{S}_d$) in (24), is hold when the inverter output voltage and the mains voltage are equal i.e. when ($e_d = v_d$). In other words, this occurs only when δ= 0. Substituting for both of (δ) and the modulation index (M) by its definition in Eq.(18), then ($\bar{S}_d$) can be expressed as:

$$\bar{S}_d = \sqrt{\frac{3}{2}} \frac{V_1}{V_{dc}} \quad (25)$$

Where, (V_1) is the line r.m.s value of the inverter output voltage [11].

The closed loop voltage controller is shown in Fig.4.

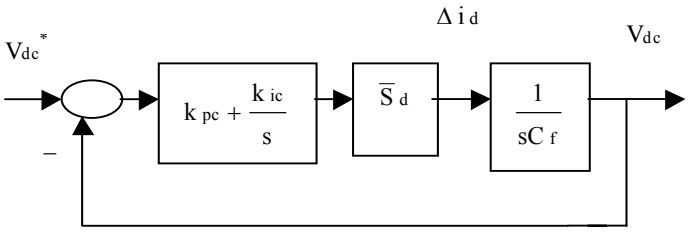

Fig. 4. The closed loop voltage controller.

The overall transfer function of this controller can be written as:

$$G_c(s) = \frac{1}{C_f} \frac{k_{pc} \bar{S}_d (s + \frac{k_{ic}}{k_{pc}})}{s^2 + \frac{k_{pc} \bar{S}_d}{C_f} s + \frac{k_{ic} \bar{S}_d}{C_f}} \quad (26)$$

Comparing the transfer function of (26) to the standard well-known transfer function of the second order system, the parameters of the P-I controller of the voltage loop can be obtained as follows:

$$k_{pc} = \frac{2 C_f \xi_c \omega_{nc}}{\bar{S}_d};$$

$$k_{ic} = \frac{C_f \omega^2_{nc}}{\bar{S}_d} \quad (27)$$

As the dynamics of voltage controller is supposed to be much slower than that of the current controller, the value of (C_f) is chosen to be 1000μF. The voltage of the D.C buss is set to be 600V. The natural frequency (f_{nc}) should be much less than 50Hz. It is selected to be (10Hz) in this paper. The low pass filter in the voltage loop controller, shown in Fig.2, is tuned to have a cutoff frequency of (70Hz). Finally, the value of the damping ratio (ξ_c) is selected to be $\frac{1}{\sqrt{2}}$ to ensures a good margin of stability and minimum percentage overshoot.

VI. Simulation Results

The system was fully simulated using PSIM6. PSIM6 depends upon ready-made modules to imitate the performance of real circuits with high accuracy [12]. The system includes a model for 20KVA non-linear load and power factor correction capacitor (120μF,1000V) per phase. Fig.5 shows the non-linear load current, which is the supply current when providing no compensation.

Fig.6 shows the supply current and the supply voltage for phase-A after providing compensation. It is clear that the

supply current became sinusoidal, smooth and in phase with the supply voltage. The system shows excellent transient response. As expected, a current was slightly high when the power switched on but it was damped rapidly and the supply current started to follow the supply voltage within the first half-cycle.

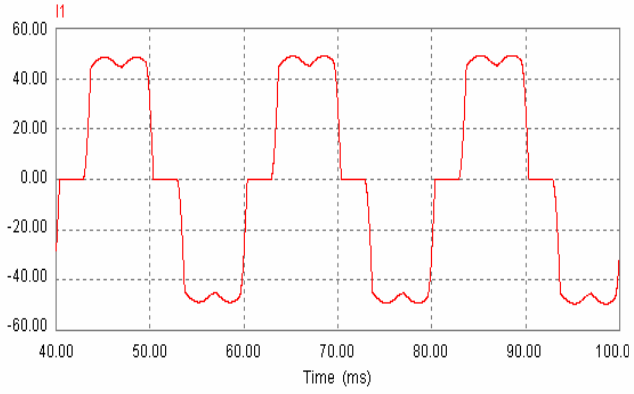

Fig. 5. The supply current without compensation.

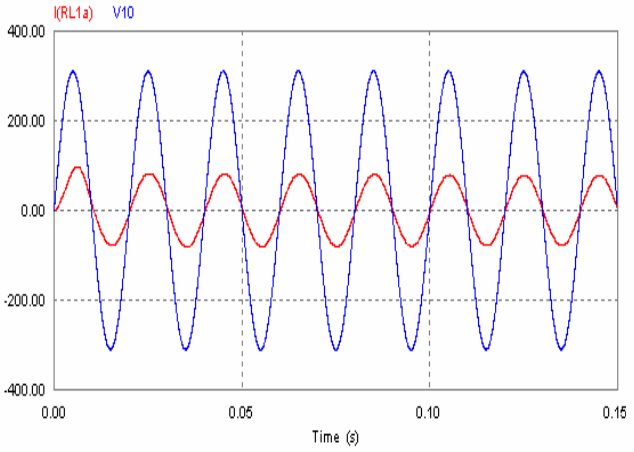

Fig.6. The supply current and voltage after compensation for phase-A.

The reactive current of the shunt active filter is shown in Fig.7. The current spikes are clear due to the effect of the P.F capacitor.

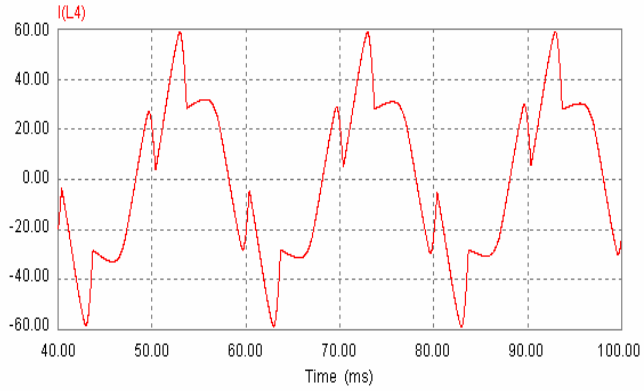

Fig. 7. The reactive current of the active filter.

The power regulated by the voltage controller (P_{av}) is shown in Fig. 8. This regulated power is a measure of the instantaneous active power exchanged between the active filter and the mains to achieve the power balance of the system.

Finally, the frequency spectrum of the supply current after compensation for phase-B, is shown in Fig.9. It is obvious that the supply current is represented by its fundamental component while all the higher dominant harmonics in the current spectrum were successfully rejected.

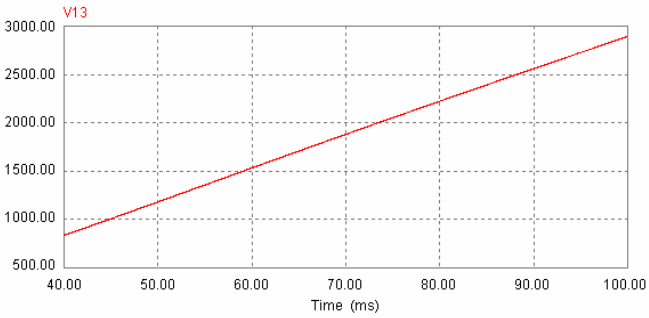

Fig. 8 The regulated average power (P_{av}).

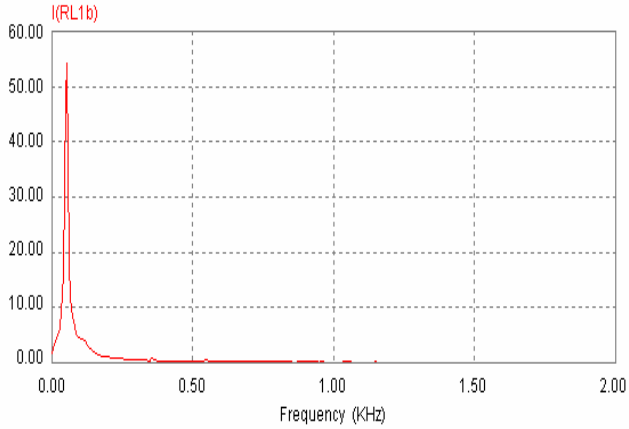

Fig.9 The frequency spectrum of the supply current after compensation for phase-B.

VII. Conclusions

Active compensation for a low voltage network comprises a non-linear industrial load and power factor correction capacitor, was investigated. The problems caused by these capacitors when they switched into the power network such as creating high voltage spikes and a low impedance path for higher dominant harmonics up-stream were overcome. The design of both the current and the voltage controllers, according to the proposed strategy, provides a clean power, a safe operation for the shunt active filter and a balanced exchange of instantaneous power between the active filter and the mains. The strategy also fits well the controlled- drives as they are mainly classified as harmonic current producing loads. Moreover, activating the policy of load identification, according to the harmonic type, can lead to an excellent compensation and solve what is called the "time- racing problem" plus the other well-known problems arise when providing on-line compensation

using power active filters. Finally, the cost of applying such compensation strategy in industry can not be comparable either to the price of a production line or to the penalties that would be paid to authority on the long run.

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AMR Gas Meters System by Radio - A New Trend in Natural Gas Metering Technology in Romania

Monica Sabina Crainic[1]

Abstract – Natural gas is a non-regenerable energy source. For this motive it must be managed properly to protect it for future generation. Proper management of natural gas reserves requires submetering. Submetering of natural gas consumption and revenue collection is traditionally accomplished using diaphragm gas meter. To resolve some problem of revenue collection new technologies liken automatic meter reading is implemented. In this context we at AEM Luxten Lighting Co produce a radio module for automatic gas meters reading and the reading system for this gas meters.

Keywords: flowmeters, diaphragm gas meter, natural gas submetering, radio module for gas meters reading

I. INTRODUCTION

Revenue collection is one of the core activities of any utility inclusive natural gas distribution company. This has traditionally been accomplished using conventional credit meters like diaphragm gas meter, with regular meter reading, extension of credit to customers and normal credit collection mechanisms.
This process is costly, with numerous inherent problems for both utility and customers. To solve some of these problems new technologies like automatic meter reading (AMR) [1-4] is implemented which offer benefits to both parties.
AMR was first tested 45 years ago when trials were conducted by AT &T in cooperation with a group of utilities and Westinghouse After those successful experiments AT & T offered to provide phone system-based AMR services at $ 2 per meter. The price was four times more than the monthly cost of a person to read the meter-50 cents. Thus the program was considered economically unfeasible.
The modern era of AMR began in 1985, when several major full-scale projects were implemented. AMR systems have been available to the utility industry for more than 20 years. However few natural gas utilities [1, 4] have chosen to implemented large scale AMR systems to replace manual meter reading. Despite the fact that AMR does not fundamental change the traditional way of collecting it does open up a communications channel between the utility and the consumer.

II. THE LEVELS OF AMR METERING SYSTEM

AMR systems operate on three levels [1]. At the lowest level are the mechanical gas meters with pulse output and an interface module, which allows data to be transmitted from this remote device to a central location. These meters are installed at the consumer's home. In many instances this communication interface is bidirectional and allows central office signal to be received by the remote unit as well. The next level is the communications systems used for the transmission or telemetry of data and control send signals between the meter interface units and the central office. At the top level is the central office system equipment including receivers, data concentrators, controllers, host upload links and host or central computer with the data base for the collection of the metered gas consumption.

2.1. *Mechanical gas meter with pulse output*

These are volumetric dry, diaphragms gas meters [5-6] meant for measuring domestic natural gases consumption. They have internal chambers with rubber walls that alternately fill and empty with the flowing gas. The mechanical motion thus generated is linked to a gear mechanism that moves the dials on the meter index (display) showing the volume of gas that has passed through the meter. Instantaneous flow rate is typically not measured. The diaphragm dry gas meters comply with OIML R6, R31 and to SR 6681-98 provisions. Some technical characteristics are presented in Table 1.

Table 1 [11 a]

	G 1,6	G 2,5	G 4
Cyclic volume V (dm^3)	1,2	1,2	1,2
Maximum flow Q_{max} (m^3/h)	2,5	4	6
Minimum flow Q_{min} (m^3/h)	0,016	0,025	0,040
Maximum pressure P_m (bar)	0,5		
Environmental and gas temperature range	- 20 … +50 ° C		
One pulse value (on request)	0,002 m^3		
Counter range	99999,999		

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Connections	G1 or G1 ¼”
Maximum admissible errors	± 3% for $Q_{min} \leq Q < Q_{max}$ ± 1,5% for $0,1Q_{min} \leq Q \leq Q_{max}$
Weight (kg)	2,5
Overall dimensions (mm)	243 × 228 × 172

Their cases are cupped steel bodies with electrostatic spray paint with epoxipolyesteric powder. The rotation of gear is transferred via a magnetic coupling.

The gas meter with pulse output converts the data obtained from mechanical meter into an electrical signal by means of a reed switch group that is activated by a permanent magnet. It makes a sensitive reading and gives 2 pulses per one liter.

2.2. *Interface module*

Volumetric dry, diaphragms gas meters with pulse output has an interface module with power supply, meter sensors, controlling electronics and a communications interface that allows data to be transmitted from this remote device to a central location. In many instances this communication interface is bi-directional and allows central office signals to be received by the remote unit as well.

Every gas meter must have such interface unit to be remotely read.

The AMR system starts at the meter. Some means of translating reading from rotating meter dials intro digital form is necessary in order to send digital metering data from the customer site to a central point.

2.3. *Communications systems*

Communications systems are used for the transmission or telemetry of data and control send signals between the meter interface units and the central office. Typically such communications take the form of telephone [1, 7-9], powerline carrier (PLC) [1,10], radiofrequency (RF) [1, 11b-11c , 12],or cable television [1]. The system components in the communications systems depend on the communication media used.

Radio is used in 90 % of the AMR meters installed around the world, making reading meters by radio the fastest growing segment of the AMR industry. It involves retrofitting an existing mechanical gas meter with pulse output with a radio AMR module [11b] that contains a radio transmitter and some times also a radio receiver. AMR modules work by sensing the mechanical motion that drives the mechanical register.

Radio AMR meter modules operate by transmitting periodically, or by responding to a radio interrogation. Periodic transmitting relies on either a fixed receiver being present nearby, or a mobile radio in a handled computer or mounted in a vehicle coming with range when meter data is required.

The operation of radio AMR meter modules falls within the regulatory agencies of each country. These regulations determine the radio frequency, the transmission power levels and other technical characteristics (see table 2) of radio operation [11c].

Table 2 [11 b]
Communication channel frequency: 868 MHz;
Modulation: RF-FSK;
Radiated power: max. 3mW (5dBm);
Transmission mode: bi-directional communication;
The communication protocol: M-bus;
The communication distance in open field:
up to 200 m;
Supply: Li battery - 3.6V (10 years life-time);
Protection degree: IP 54;
Operating temperature: -40 C...+60 C;
Standards: according to R&TTE Directive;

The radio module for gas meters reading (see fig.1) is an instrument intended for the remote reading of the consumption recorded by a gas meter.

The module attached to gas meter meters pulses whose number is proportional to the gas volume measured by the meter. At the receipt of a radio message following a reading request, the module transmits by radio the value of the pulse counters.

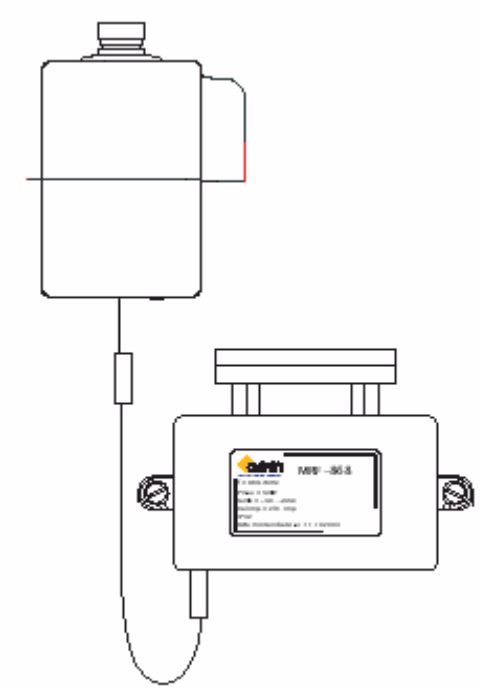

Fig. 1 Radio module for gas meter reading

The radio module is made up of the following:

- a pulse generator which takes over the pulses from the gas meter (the pulse has the weight of a certain gas volume);

• the printed board which contai ns a microcontroller with metering and communication functions, the radio circuit and the
• radio aerial;
• the battery for the electronic circuits supply;
• the case fixed on the gas meter, which contains the printed board and the battery.

2.4. *Central office systems equipment*

At the top level is the central office system equipment including receivers, data concentrators, controllers, host upload links and host or central computer.

There are three major building block functions that the meter interface and related electronics must perform.

First, an electro-optical interface according to EN61107 (IEC 62056-21); must be incorporated into or attached to the meter. This converts informations conveyed by the meter's mechanical register indexes, into electronic signals which may be processed, manipulated, stored and transmitted.

The second functional building block is a controller unit consisting of a low-voltage power supply, signal processing electronics, microcomputer, random access memory and program memory used to store the real-time run or operating system program. The controller unit is used to process the signal originating from the meter's electro-optical interface devices. In effect, the controller unit converts the meter's electromechanical interface device signals into computer type converts key pad entries into numbers appearing on the display. The controller's RAM memory maintains an up-to-the-minute mirror image of the meter's dials and as the dials increment, so do the numerical representations stored in RAM.

The third functional building block is the communication scheme and its associated electronics transmit/receive electronics.

III. REMOTE READING SYSTEM

Reading system is intended for the remote data collection concerning the consumption registered by gas meters equipped with radio module.
The system is made up of the following:
• gas meter equipped with radio module for remote reading (see pct. 2.1 - 2.3);
• PSIONWorkabout hand-held terminal equipped with radio interface;
• central computer with the database for the collection of the metered gas consumption (see pct 2.4).
On site data collection concerning gas consumption is carried out by means of PSION hand-held terminal provided with radio communication interface, and data storage is achieved on a PC. For these functions carrying out GazRadio_PSION software application is used. This application is made up of two modules:

• GazMP, for hand-held terminals of PsionWorkabout type
and
• Gaz MBD, for Purchase.
The GazMP module communicates with the gas meter through RS232 serial interface of Psion Workabout hand-held terminal by means of the radio module, and the communication with the PC is made by means of a RS232 cable. The application user interface is represented by a menus and dialog boxes system. The application starts working only after entering the user password. After the password checking, the user can use a menu comprising the following:
• configuration operations in the communication mode,
• addresses list loading,
• operations of current data reading and
• operations of current data transfer on a PC.
The configuration operations in the communication mode consist of the following:
a) Communication mode,
The program allows the use of the following external devices for the communication processes:
1. RS232;
2. Dock-Station;
b) The choice of the address list,
There can be loaded addresses lists, which contain information about the gas consumers (name, domicile and meter series).
These lists can be subsequently used in turn for the gas meters reading.
The lists are created by means of GazMBDprogram.
The selected list can be viewed entirely or there can be viewed only the consumers those have not been read.
c) List deleting
Consumer's lists can be deleted, as needed.

The reading operations consist of the following:

a) Current data reading
The program allows current data reading through the radio module. By operating this control, the following dialog box is displayed:
****
Gas meter reading
Address: <-Manual->
All meters: <-No->
GIVE UP GO ON
ESC ENTER
****
After pressing "Tab" key, the options for the address selection will displayed:
****
Manual
Name 1 l Domicile 1 l Address 1 l
Name 2 l Domicile 2 l Address 2 l
.....
****
In case there is no current list, only “Manual” option is displayed.

The meter can be read in turn, by selecting an address from the list or by entering the address with the keyboard, if <manual> option is selected.
If "All meters" is set up on "Yes", there will be read all the previously loaded meters, or only the meters that have not been read, as function of the chosen option.

****

Multiple readings
Select: <-All meters-> <-Unread meters->

GO ON
ENTER

****

The data thus read are grouped in a directory, and the file names are created on the basis of the serial information (identifier). The hand-held terminal will display the following data:

- the identifier (address)
- the measured volume (m3)
- current time
- current date

b) Manual data entering

The program also enables the manual entering of the following data:

- the identifier (address)
- the measured volume (m3)
- current time
- current date

GazMBDsoftware module has been intended to run under Windows 95, 98 and carry out the following:
The transfer of the current data stored in PSION hand-held terminal, and the deleting of the records from PSION hand-held terminal can be carried out by operating the controls of menu:

- Current data
- PSION data deleting

These functions are correlated with the similar functions of GazMBDprogram on PsionWorkabout hand-held terminal.
Data display in the view zone and their deleting by operating the controls of menu:

- View zone deleting
- Current data view

Viewing certain information from the data base by operating the controls of menu

- Search
- The first
- The preceding one
- The following
- The last

The users, passwords and consumers lists configuration by operating the controls of menu:

- Consumers
- PSION password
- Consumers list

The database can also be used by other specific applications: analysis, forecasting, billing etc.
Technical characteristics of remote reading system for gas meters are:

- The maximum number of consumers stored by the HHU (2M memory): 10,000 consumers;
- HHU autonomy: 24h;
- Data about the radio interface:

~ - it uses the free frequency band (no license required);
~ - communication channel frequency: 868 MHz;
~ - radiated power: max. 3mW (5dBm);
~ - the antenna: internally executed;
~ - DB9 connector for RS232;
~ - supply: Li battery, 3.6V (25 000 readings).

- One meter reading time length: 5 seconds.

IV. ABOUT REFERENCES

Submetering of natural gas consumption after a long time of relative stagnation is moving ahead rapidly to day based on new technologies: electronics based meters and advances in communications.
AMR metering replace not only the classical meters but also:

- the billing system,
- the reading of the meters and
- the administration of revenue collection.

The AMR capability could subsequently be an added in an evolutionary manner, in order to offer advantages over and above the simple payment function like added

- value service,
- fraud control,
- tariffs incentives and
- unattended dwelling

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An Analog Computing Circuit for SVM classifiers

Lelia Feştilă[1], Lorant Andras Szolga[2], Mihaela Cîrlugea[3], Mihaela Gordan[4]

Abstract – We propose an analog nonlinear current-mode circuit for computing the decision function in a SVM classifier based on radial basis kernels. The validity of design and operation was proved by simulations.

Keywords: SVM, Euclidian distance, analog computing, classifier

I. INTRODUCTION

Support vector machines (SVM) combine many approaches of artificial intelligence and neural networks. Mathematically they are based on statistical learning theory and are especially suited for adaptive object detection and identification with sparse training data [1]. The SVM classification goal is to assign an object to a class that contain similar objects. The SVM is trained with a set of positive and negative labeled examples. Relevant object features are extracted and retained in a set of support vectors.
The automata's response is a decision function that is expressed by a linear combination of kernels whose argument depends on both support and test vectors. The most kernels are based on internal products for polynomial classifications and for the multilayer perceptions [1] [8].

Other categories of classifiers are based on the radial basis functions that depend on the Euclidian distance (ED) between two vectors $\mathbf{X_m}$ and $\mathbf{X}$:

$$D_m\left(X, X_m\right) = \left\|X_m - X\right\| = \left(\sum_{i=1}^{N}\left|X_{mi} - X_i\right|^2\right)^{1/2} \qquad (1)$$

The kernel **K(•,•)** of such a classifier [7] can be linear (proportioal to D_m), a smooth limiter or a Gaussian function:

$$K\left(\left\|X - X_m\right\|, c\right) = ke^{\left(-\frac{\|X - X_m\|^2}{c}\right)} \qquad (2)$$

$\mathbf{X}$ is the input vector and $\mathbf{X_m}$ the reference vector which in SVMs, is called support vector SV. Coefficient **c** is the width of the kernel. The classifier computes the decision function :

$$y = sign\left[\sum y_m \alpha_m K\left(\left\|X - X_m\right\|, c\right) - b\right] \qquad (3)$$

where α_m are synaptic weights and $\mathbf{y_m}$, the labels +1 and –1 for positive and negative SVMs respectively and **b** is the bias term.
The vector X belongs to the class represented by positive defined SVs if its resulted label $y \geq 0$.
Although the number of SVs is usually much smaller than the number of training examples because of large dimensions and large degree of variability in the object class, an excessive amount of computation can appear in both learning and classifying process. The computational time is dominated by the calculation of kernels, so that computing time of large dimension nonlinear functions is needed. Therefore implementing such classifiers in hardware becomes a good alternative to software implementations especially in the case of real-time operation. Analog devices are recommended in such cases because of their run-time performance. They can perform very fast linear and nonlinear mathematical operations that are expensive in digital domain (multiplication, division, square-root, squaring, geometric mean). Current-mode CMOS transliniar circuits have also many other advantages like low voltage, low power aned simple cell structures requiering a small area.
In order to be able to study, analyze and develop different VLSI structures for analog computing with applications in SVM classifiers we created a Pspice environment containing a basic cell library and also some computing blocks for nonlinear functions like ED or different types of kernels.
We designed and simulated an analog computing circuit for parallel SVM image classifiers. The analog hardware is used only to classify unknown images.

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Training is performed separately using a dedicated software [8].

The presented circuit is destined to SVM classifiers based on radial basis kernels. As we know, the existing hardware implementations are mainly based on polynomial kernels. Radial basis kernels could only be approximately implemented with these types of structures or need extra look-up tables. The proposed circuit computes the ED, the nonlinear kernel and multiplies it by label and weight.

The ED calculator is simpler as the one found in literature [3] containing only 2N+1 cells/template not 3N+1 cells/template as in [3]. Using an extra multiplier for the weight α we could extend the multiplier linearity domain over the one obtained by bias controling of a smooth limiter as in [6].

By simulations we proved the feasability and validity of the algorithm and design and set appropriate parameters for a good functionality of each component and also for the whole operating chain. Chapter 2 describes the algorithm for ED calculation and determination of the decision function while in chapter 3 we present the circuit. Simulation results are given. The circuit functionality was checked on a small dimension image detection problem, presented in chapter 4.

II. ALGORITHM OF THE PROPOSED CLASSIFIER

A radial basis classifier circuit compares an unknown pattern **X** with a given set of **M** predefined patterns $\mathbf{X_m}$ (m= 1,...,M), called support vectors SVs and calculates distance ED denoted $D(X,X_m)$ between **X** and each VS prototype ($\mathbf{X_m}$). The distance (1) is:

$$D_m(X, X_m) = \sqrt{(X_1 - X_{m1})^2 + ... + (X_N - X_{mN})^2} \quad (4)$$

where m=1÷M is the number of SVs,
$X=\{X_1,X_2,...,X_N\}$, $X_m=\{X_{m1},X_{m2},...,X_{mN}\}$, N is the number of features, in our examples, the number of pixels.

The classifier based on ED implements (4) by doing the difference between X and X_m, squaring each result, summing the terms and finally applying the square root. In our circuit kernel K is an inverting smooth limiter with controllable gain and limits. Finally function f is calculated to obtain the decision y:

$$f(\|X - X_m\|) = \sum y_m \alpha_m K_m(\|X - X_m\|) \quad (5)$$

$$y = sign[(\|X - X_m\|) - b] \quad (6)$$

III. ANALOG PARALLEL ARCHITECTURE AND BUILDING BLOCKS CELLS

Fig.1 shows the general block diagram of a classifier with parallel architecture.

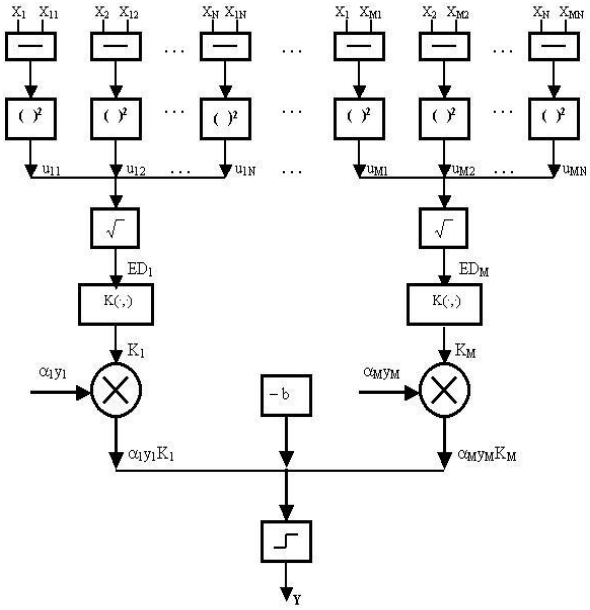


Figure 1. General block diagram of the classifier

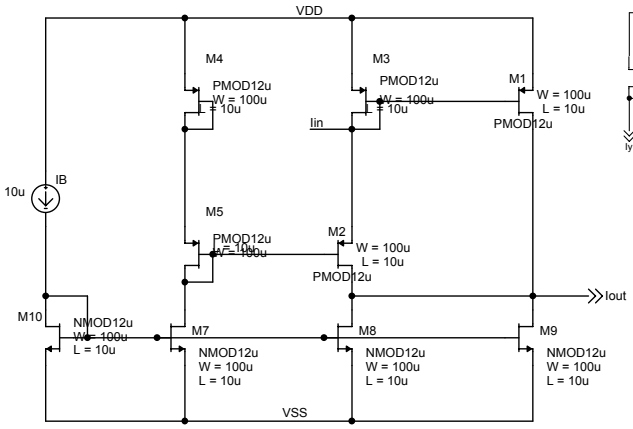
Each path permits the calculation of one term $y_m\alpha_m K_m(||X-X_m||)$ in the sum (5). For parallel current mode architectures these terms are currents and can be simply summed by a direct connection as Fig.1 shows.

The ED calculator contains N substractors, N squarers and a square-rooter/template. The substractors make simply current differences by directly connecting outputs of current mirrors and inverting current mirrors [2].

Fig.2.a shows the circuit used for realizing the square of a bidirectional current [10]. Its output is of the form:

$$I_{out} = \frac{i_{in}^2}{8I_B} \quad (7)$$

By simulations we proved the validity of the circuit, determined the optimal biasing current I_B and checked the theoretical conditions [2] $\|i_{in}\| \le 4I_B$. Figures 2.b and 2.c show examples of simulation.



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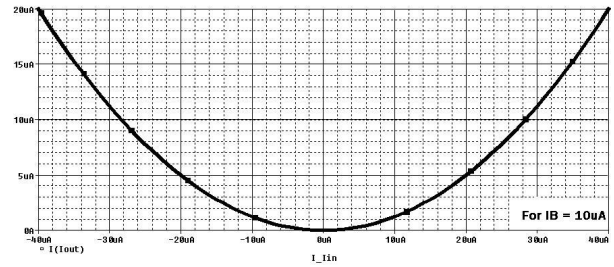

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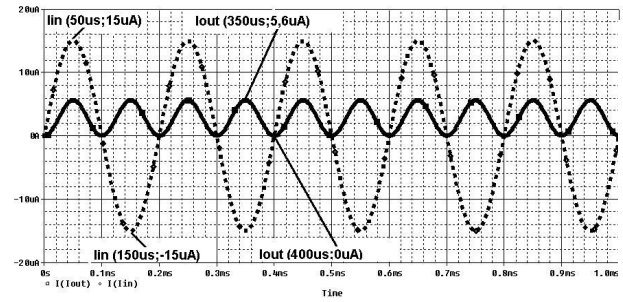
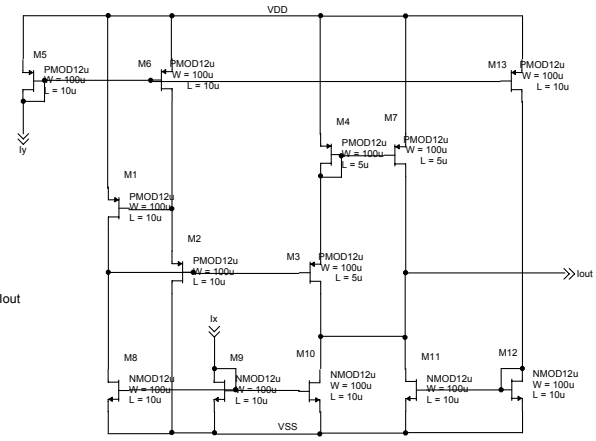


c)

Figure 2. Squaring block
- a) circuit schematic;
- b) in/out transfer characteristic;
- c) time diagram.



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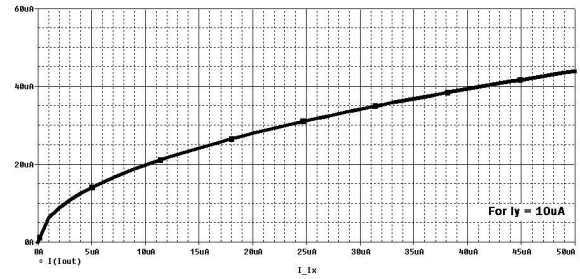

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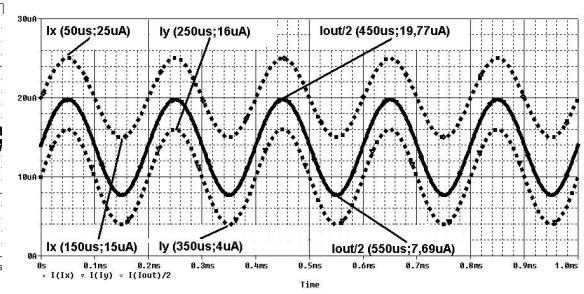


c)

Figure 3. Geometric mean block
- a) circuit schematic;
- b) in/out transfer characteristic;
- c) time diagram.

Fig.3.a represents the schematic of a geometric mean circuit [3]. One can calculate [2] and prove by simulations that the output current of this circuit is:

$$I_{out} = 2\sqrt{I_x I_y} \qquad (10)$$

The simulations are shown in Figures 3.b and 3.c for input currents I_X, I_Y(dots) and $I_{out}/2$ the half of output current that is the geometric mean of I_X and I_Y. In the classifier schematic we use this block for square-rooting the sum of squares and set $I_x = I_B$.

The smooth limiter function close to a sigmoidal form is realized with a differential CMOS inverting amplifier (DA).

Fig.4.a and Fig.4.b shows the input-output characteristics for different biasing currents I_B. Because input signals supplied by the square-rooter are positive only the fourth quadrant will be used.

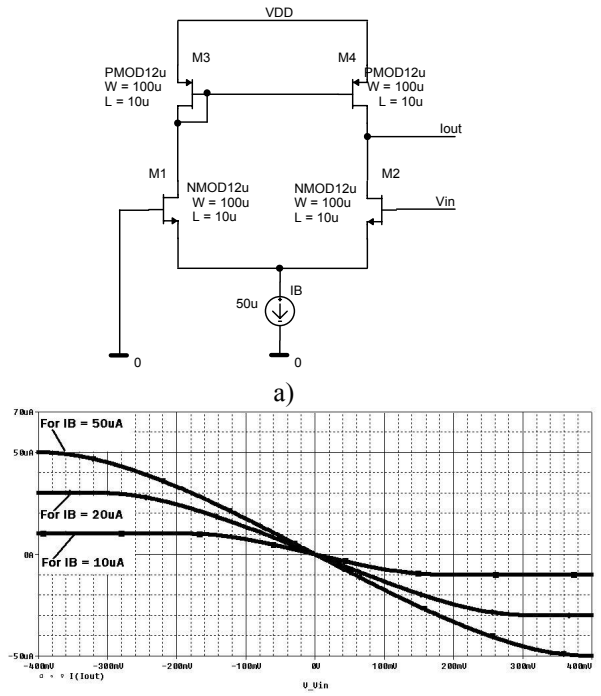


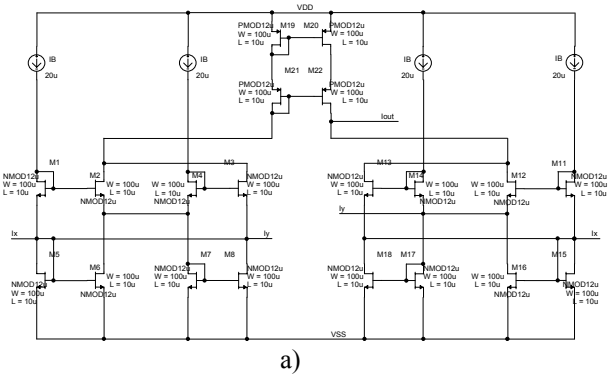
Figure 4. Differential amplifier
a) circuit schematic;
b) in/out transfer characteristic.

The multiplication by $\pm\alpha$, resulted from a software training, is performed by a multiplier shown in Fig.5. It is a four quadrant multiplier used to realize product $\boldsymbol{\alpha}_m \mathbf{y}_m \mathbf{K}$. One can calculate that the output is [2]:

$$I_{out} = \frac{I_x I_y}{2I_B} \qquad (11)$$

The performed simulations in Fig.5.b and c proved this result.

We chosed this variant with a separate multiplying block instead to simply control or set the biasing current of the DA beacause for certain applications the weights $\boldsymbol{\alpha}$ can vary in a large domain and labels and $\boldsymbol{y}$ can be positive or negative. By using a multiplier the domain of permitted $\boldsymbol{\alpha}$ values was considerable increased because of the good linearity domain of the multiplier (Fig.6.b)



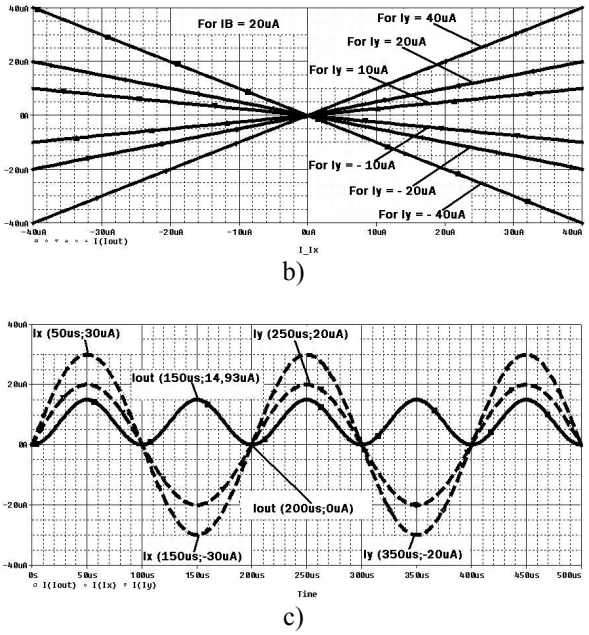


Figure 5. Four-quadrant current multiplier
a) circuit schematic;
b) in/out transfer characteristic;
c) time diagram.

If the distances $\|X-X_m\|$ are calculated in parallel as Fig.1 shows, the circuit is fast and does not need a sumator accumulator. For area reasons euclidian distances can be also sequentially calculated, but with a lower run-time.[4]

Four paths of the whole simulated structure of the classifier are shown in Fig.6.

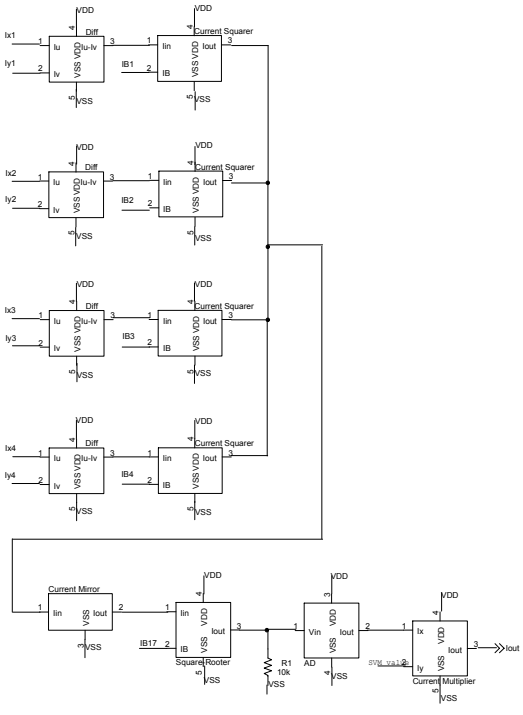


Figure 6. A part of the simulated circuit

IV. EXPERIMENTAL RESULTS

We took an example of a binary pattern classifier. Each template is a 4x4 black and white image. For a black quadrant, the input current is 25μA and for a white one 15μA. For each pair **(X,X_m)** we used 16 circuit paths, each of them containing modules for difference and power. The 16 output currents are summed and enter the square-root-circuit (Fig.6). A current mirror is also needed for adapting impedances. The SVM was trained separately by soft for identifying a diagonal in a 4x4 image. Some experiences needed to determine the proper number of positive and negative training vectors. The best result was obtained for 28 positive and 29 negative examples. The learning process resulted in 22 support vectors, their labels and weights Fig.7 and Table I.

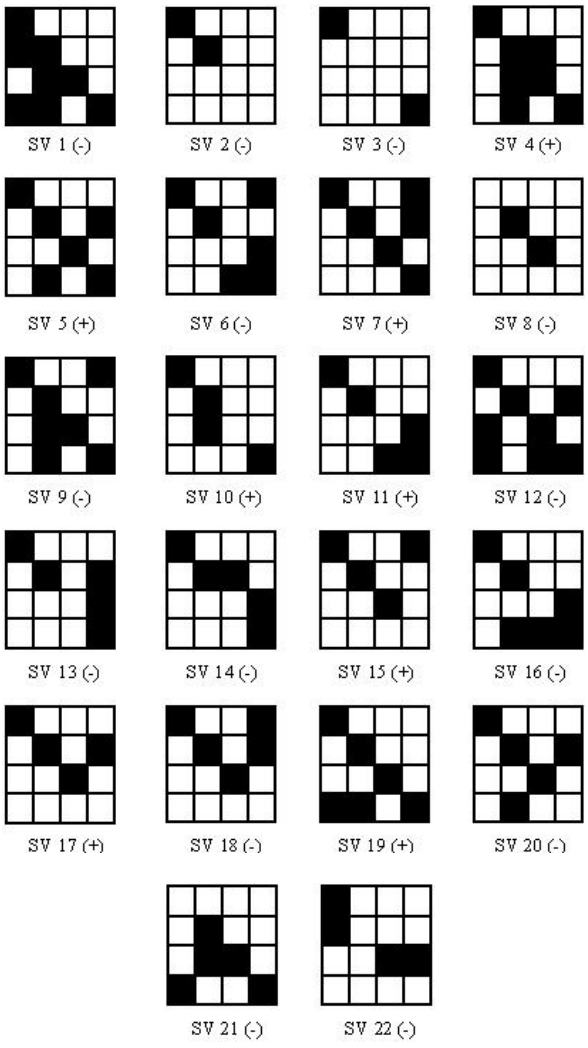


Figure 7. Predefined pattern class (SVs)

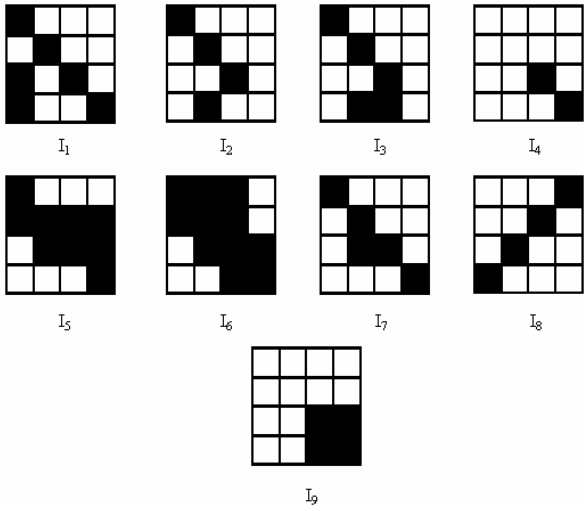


Figure 8. Patterns to be classified

As example nine images $I_1 \ldots I_9$ to be classified are given in Fig.8.

TABLE I
TRAINING WEIGHTS AND LABELS

SV	$\alpha_i y_i$	SV	$\alpha_i y_i$
SV1	- 3,57	SV12	- 8,78
SV2	- 17,79	SV13	- 6,28
SV3	- 8,18	SV14	- 9,08
SV4	8,15	SV15	37,97
SV5	4,83	SV16	- 5,81
SV6	- 11,17	SV17	32,86
SV7	19,62	SV18	- 42,89
SV8	- 12,56	SV19	9,23
SV9	- 16,11	SV20	- 8,53
SV10	13,7	SV21	- 3,58
SV11	28,11	SV22	- 0,12

TABLE II
"ED" AND "DA" OUTPUT CURRENTS

Difference	ED [μA]	DA [μA]
1	12,97	- 22,42
2	15,48	- 26,43
3	17,74	- 29,91
4	20,02	- 33,24
5	22,33	- 36,41
6	24,42	- 39,09
7	26,34	- 41,37
8	28,42	- 43,3
9	29,82	- 44,94
10	31,41	- 46,32

Table II shows the measured currents at the outputs of the ED and DA blocks in function of the number of differences between colours of template pixels.
We had to use a current multiplier to obtain $\alpha_i y_i \mathbf{I}_k (y_i = \pm 1)$. The two inputs are current $\mathbf{I}_k$ from the DA output and a current $\mathbf{I}_\alpha$ proportional to $\alpha_i y_i$. To

choose the right current multiplier, first of all we observed and analyzed the limits of these currents obtained for SVM coefficients $\alpha_i y_i$ and from the AD output I_k.

From TABLE I and TABLE II one can observe that:

$I_\alpha \sim \alpha_i y_i \in [-45,14; 46,15]$ and

$I_K \in [-43,3\mu A; -22,42\mu A]$, so a current multiplier which can accept both negative and positive currents for the input is needed. The four-quadrant current multiplier from Fig.5.a was ideal for us and established the best working conditions for this circuit in our implementation. For a good evaluation of this conditions we considered current domains:

$I_\alpha \in [-50\mu A; 50\mu A]$ and $I_K \in [-50\mu A; 0\mu A]$.

With a simple correlation between the input currents of the multiplier and the above currents, we set:

$I_x = I_K$ and $I_y = I_\alpha$.

One can prove that the proper operating conditions for this multiplier circuit are:

$(I_x + I_y) \in [-4I_B; 4I_B]$ and $(I_x - I_y) \in [-4I_B; 4I_B]$.

In our case $(I_K + I_\alpha), (I_K - I_\alpha) \in [-100\mu A; 50\mu A]$. With this last condition we can set the minimum value for I_B so that the circuit should work properly, value which was set to $I_B = 25\mu A$.

The threshold **b**, depends on the scale factor, different scale factors have been analyzed, by considering different reference currents I_B of multiplier.

TABLE III
EXPERIMENTAL RESULTS

Image	I_{out} [µA]		Classified	Diff	Threshold b [µA]
	for I_B= 25µA	for I_B= 50µA			
I_1	5,78	2,98	+	2	3,2 for I_B=25µA
I_2	3,93	1,96	+	2	
I_3	4,19	2,09	+	3	
I_4	1,533	0,76	–	2	
I_5	3,01	1,5	–	5	
I_6	3,22	1,61	+	7	
I_7	7,18	3,59	+	1	
I_8	- 1,56	- 0,78	–	8	
I_9	3,16	1,58	–	4	

Table III shows two final results: we used two values for the I_B currents. The output currents $\mathbf{I_{out}}$ corresponds to function ***f***, relation (5), for each image to be classified. With I_B=50µA we can choose the threshold value much better, because the interval between the smallest score for a positive classified image and the bigger one for a negative image is smaller than for I_B=25µA. So we set the threshold b=1,6µA, for the circuit having I_B=50µA. To have a bigger threshold current we are going to use the I_B=25µA case, multiplying the previously obtained threshold by 2. The final threshold value in this case is b=3,2µA.

In order to have a comparative view over the SVM classifiers and a classifier based only on ED, the circuit has also been used for calculating ED between each input vector under test and the pattern corresponding to a pure diagonal image. The decision in the ED method is only based on the minimum distance that in fact corresponds to the minimum number of different pixels in the compared images.

Therefore the ED could be the same for two images that belong to different classes. As example $\mathbf{I_1,I_2,I_4}$ have the same ED and are classified in the same class by an ED classifier. SVM classifier takes better decisions, as example, although $\mathbf{I_1,I_2,I_4}$ have the same ED, $\mathbf{I_4}$ is negative classified and $\mathbf{I_1,I_2}$ positive being closer to the diagonal. One can see in Table III that the decision functions of the SVM classifier for these images are very different. The image can be detected correctly by a well trained SVM classifier even if dots or other spots exists.

V. CONCLUSION

We have designed a current-mode analog computing CMOS circuit for SVM parallel classifiers based on radial basis functions. It consists of an ED computing stage and a circuit for realizing the kernel required by the nonlinear transformation with controllable weights. Simulations proved the validity of this circuit and of the SVM classifying application.

Using the SVM algorithm, the classifying task is by far improved in comparison to the method based only by appreciating the ED between two patterns [5][6].

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Automatic System for the Wheat Grind Process

Vintilă Florin Filipescu[1]

Abstract - This paper intends to present a new constructive, modern and reliable variant, of an automatic system that controls the electrovalves of the filter with aspiration in the technological process of wheat grinding; this variant implies a low cost price and an easy upkeep.
Keywords: technological process, automatic system, lapses of time, electrovalves, microcontroller, program.

I. INTRODUCTION

The aspiration filter, figure 1, is a device placed in the final zone of the technological flux of wheat grinding and has the role of separates and eliminates the particles of dust from the flour. It is made up of a metallic cylinder (1) through which a powerful ventilator aspirates the air and a great number of filterable bags (2) closed at the lower part and open at the upper one. To ensure aerodynamicity and efficiency of the filter, the lower parts of the bags are conical and elastically coupled through springs (6) to the fastening bars (7). The surface between the walls of the cylinder and the open muzzles (3) of the filterable bags is completely obturated, so that the air absorbed by the ventilator cannot circulate through the cylinder (1) unless it crosses the walls of the bags.
The flour, imbued with the partials of dust resulted from the process of decortication of the wheat beans, is stored in the cylinder through the pipe (4) and evacuated through the pipe (5). While crossing the cylinder, the thin and light particles of dust from the flour are driven upwards by the filterable bags, these particles are evacuated outside, in the atmosphere. At the same time, the thinnest flour particles are also driven, and stocking on the outward walls of the bags, obturate them, rendering more difficult or even blocking the process of filtration.
The only way of clearing the aspiration filter without stopping the technological process, is the periodical and successive cleaning of the filterable bags by shaking them with the help of some powerful air jets, injected downwards from the top through the open muzzles of the bags, by some spouts assembled on the distribution pipes (8) connected to the electrovalves (9), coupled, in their turn, to a pressure pipe.

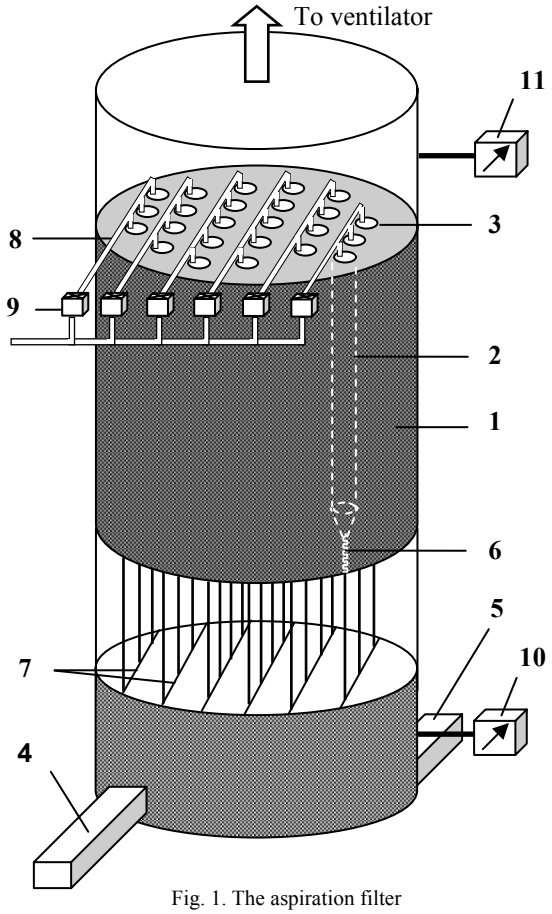

Fig. 1. The aspiration filter

The action of an electrovalve starts the process of cleaning the battery of filterable bags set under the spouts of the respective distribution pipe.
The electrovalves are controlled by an electronic device with microcontroller, according to the fitting cleaning cycle presented in the figure 2.
The adjustable lapses of time that should be considered are:
t_i = (0,1 ÷ 1) sec. - the duration of action of an electrovalve is the same with the duration of the cleaning air jets of a battery of filterable bags;
t_p = (6 ÷ 36) sec. – the duration of the pause between the moment of "fall" of an electrovalve and that of coupling of the next electrovalve is the same with the

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duration between the cleaning of two adjacent batteries of filterable bags;

t_c = (36 ÷ 360) sec. – the duration of pause between two successive cycles of action of electrovalves is the same with the duration between two successive cycles of cleaning.

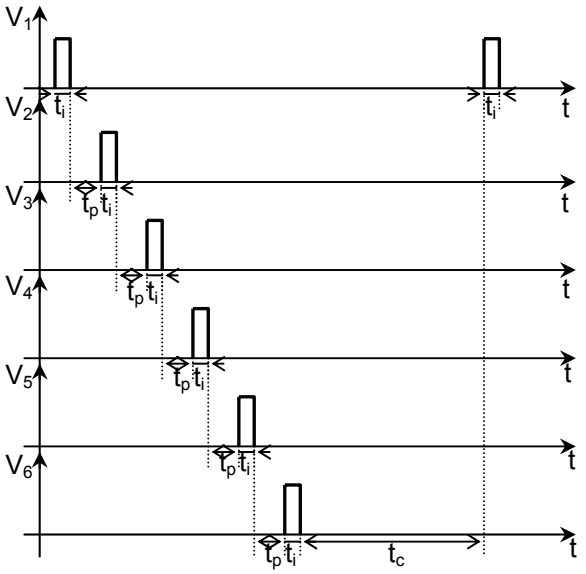

Fig. 2. The control of electrovalves

The adjustment of the three lapses of time is done depending on the flour amount and the differential pressure that has been measured between the entrance and the emergence of the filter by using pressure gauges (10) and (11). The differential pressure gives clear clues about the silting degree of the filterable bags from the aspiration filter, thus allowing the taking of the most propitious decisions regarding the 3 durations mentioned above.

The electrovalves (9) work at a tension of $220V_{DC}$ and consumes a power of 8W each

II. THE AUTOMATIC SYSTEM OF THE CONTROL OF ELECTROVALVES

The block scheme of the automatic system of the control of electrovalves is present in figure 3 and is made up of the following constitutive parts:

- The control block;
- The execution block;
- The display block;
- The supply block.

A. The control block

With a view to eliminating all the disadvantages of the similar existent systems, which use variants of analogical or digital control schemes less competitive from the point of view of accuracy, reliability and display systems, a simple control system was chosen, which is based on the microcontroller AT89C52, a component part which administrates both the control part of the electrovalves and the one of selection and display of the parameters of the working cycle of the electrovalves.

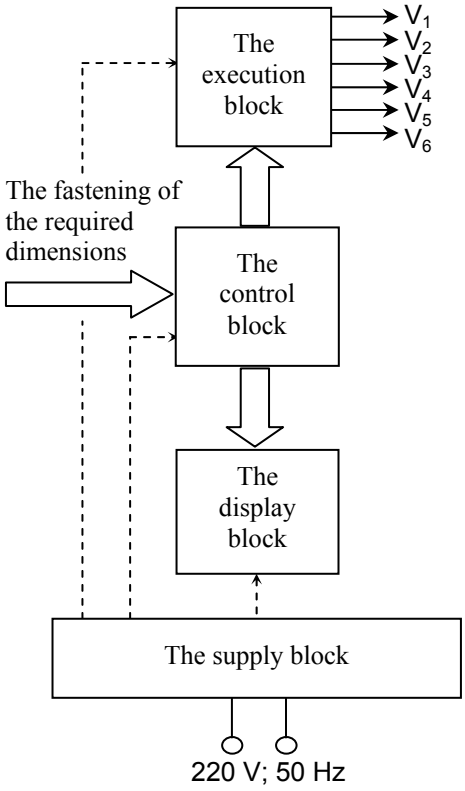

Fig. 3. The block scheme of the automatic system

More precisely, the microcontroller controls the span of the six electrovalves, considering the lapses of time presented in the diagram from the figure 2.

Thus, on initiation, the three lapses of time will be given the minimum values from the working areas (t_i = 0,1 s; t_p = 6 s; t_c = 36 s), following that depending on the development in the technological process, the values of the 3 lapses of time will be altered by the operator with the help of two keys SELection and INCrementation. These two keys represent for the system 2 external interruptions INT0 and INT1. Clap SEL performs the selection of one of the three lapses of time, and INC allows the increase of duration of the selected lapse of time.

The established values are saved into an EEPROM of type 24C02. The communication between microcontroller and EEPROM is made through the serial bus I^2C. The interface with the control unity is made through four special registers: S1CON (control register), S1STA (state register), S1DAT (data register), S1ADR (address register).

The control emergences of the electrovalves OUT1, …, OUT6, are directed by the port P0, port I/O bidirectional of eight bits, having the drainpipe emergences idly.

The microcontroller generates signals for the display block, to SEGM A, …, SEGM G and ANODE 1, …, ANODE 7, making a multiplexed display of seven digits. The signals ANODE 1, …, ANODE 7, select a

digit with the common anode, and SEGM A, …, SEGM G, generate the figure on that digit.

The general electric scheme of the control block is presented in figure 4.

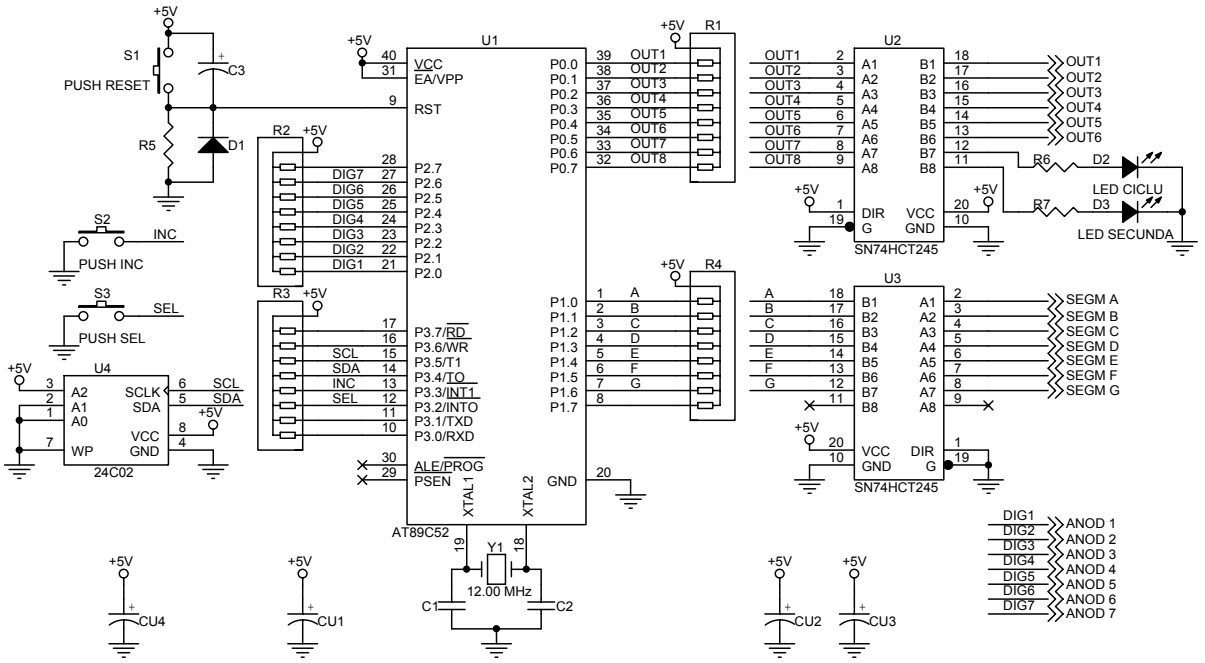

Fig. 4. The control block

B. The execution block

The execution block is formed of six identical sections, one for the action of each electrovalve. The electrical scheme of a section i, with i = 1, 2, …, 6 is presented in figure 5.

At the level of each section of the execution block a very good galvanic isolation is made between the control part and the power part through the optocoupler ISO1 – PC817, whose transistor has the collector polarized by the parametrical stabilizer DZ_i, R_{10i},.

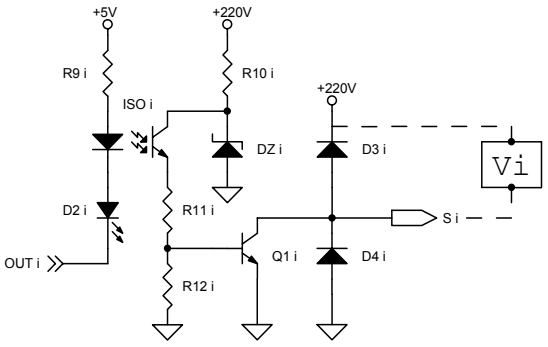

Fig. 5. The electric control scheme of one of the six sections of the execution block

For the entire duration of the control impulse, signalized by the LED D_{2i}, through the transistor of the optocoupler will circulate a current which will generate a tension fall on the resistor R_{12i} sufficient for the saturation of the transistor Q_{1i}. As a result, the electrovalve V_i will couple, allowing the transmission of a powerful air jet in the corresponding battery of filterable bags.

Transistor Q_{1i} is of the type BUT 11 AF, allows a collector-emitter tension of V_{CEmax} > 450V and a maximum collector current of Ic_{max} = 5A.

Diodes D_{3i} and D_{4i}, of the type 1N 4007, have the role of protecting the transistor Q_{1i} in the moment of shutting off.

C. The display block

The display block is formed of seven identical sections, one each seven-segment digit used. The electric scheme of a section i, with i = 1, 2, …, 7, is presented in figure 6.

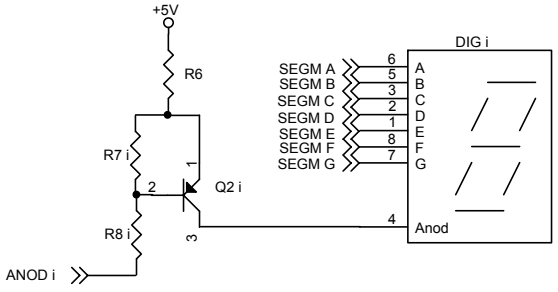

Fig.6. The electric control scheme of one of the seven sections of the display block

The use of seven display digits is justified by the total number of the figures used in the display of durations of the three lapses of time from the control cycle of the electrovalves, presented in figure 2.

Thus, the duration t_i of action of an electrovalve, may vary between 0,1 sec. and 1 sec., so it will need two display digits which will indicate the values 0.1, 0.2, …, 0.9, 1.0, the point being permanently activated, without control.
For displaying duration t_p = 6, ..., 36 sec. another two digits are necessary, and for t_c = 36, ..., 360 sec., another three digits are needed.
These seven digits are parallel connected, segment by segment, and successively activated by the emergences of the port P2 of the microcontroller. The activation of a digit coincides with the appearance at the emergence of the buffer SN74HCT245 of a logical combination corresponding to the figure that must be displayed on the respective digit.
Thus, a display cycle of the seven figures will be formed of seven steps; within each step the buffer releases just one logical combination, and the microcontroller activates only the digit that must display it.
The activation of a digit is done by transmitting a lower potential at the entrance of the scheme from figure 6, having as a result the saturation of the transistor Q_{2i} and the supply of the respective digit anode.
In conclusion, the display block works multiplexed, the frequency of work being chosen so that the figures periodically visualized on the seven digits persist on the retina, as if it were a continuous display, without flickers.

D. The supply block

The electrical scheme of the supply block, figure 7, contains a circuit for the supply of the execution part and one for the supply of the control part.
The supply circuit of the execution part, formed of the bridge rectifier P_1 and the filtering condenser C_1, generates a tension of 220 V_{DC} needed for the supply of the electrovalves.

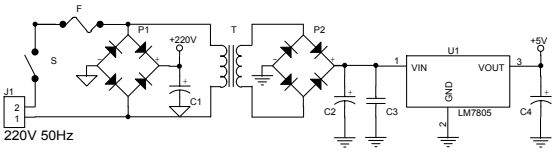

Fig. 7. The electrical scheme of the supply block

The supply circuit of the control part consists of a bridge rectifier P_2, a filtering circuit formed of the condensers C_2 and C_3 and a stabilizer U_1 of a type LM7805, which generates a tension of 5 V_{DC} needed for the supply of the control circuit.

III. THE PROGRAMMING OF THE MICROCONTROLLER

The programming of the microcontroller is achieved in assembly language as in C language.

The code source resulted from the compilation of the created program is taken down in microcontroller AT89C52 memory of program with the help of a specialized developer. The program was created after the algorithm presented in figure 8.
In order to control the electrovalve as in diagrams presented in figure 2, are necessary the many more step of associative programming.

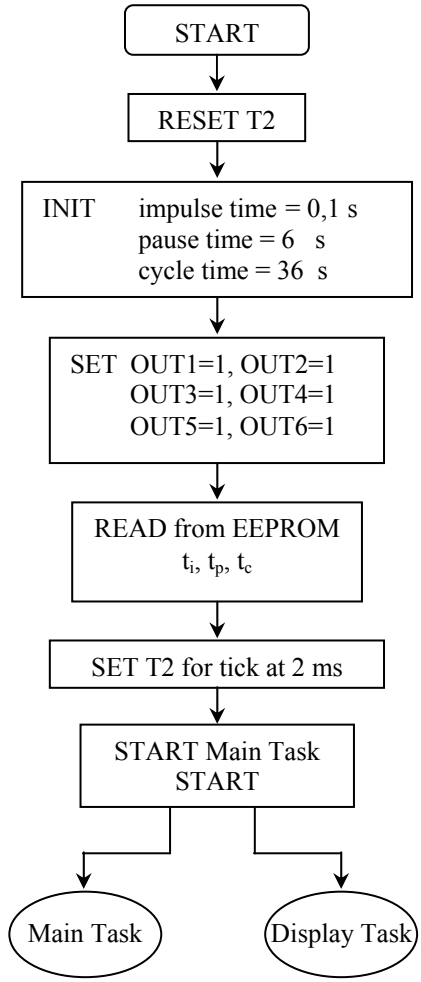

Fig. 8. The algorhythm of program

First, the T2 timer of microcontoller is reset, it is utilized for generating the tick of 2 ms used to establish times of command and for their multiplexed display these on the screen. The two registers T2H and T2L at the T2 timer are initialized with the value 0000h.
The three lapses of time are initialized to the minimum values (time_impuls = 0,1 sec., time_pauza = 6 sec., time_ciclu = 36 sec.) and the outs are set so that no valve could be commanded (OUT1 = … = OUT6 = 1), and so avoiding an abnormal function of the command system and of the filter with aspiration in the moment of coupling the supply power and of starting the process of production.

The microcontroller reads from EEPROM the values previously saved, for the three lapses of time.
Therefore, the bus serial I2C is activated between the microcontroller and EEPROM, the signal of the clock on bus, SCL is established and the saved dates, SDA are received.

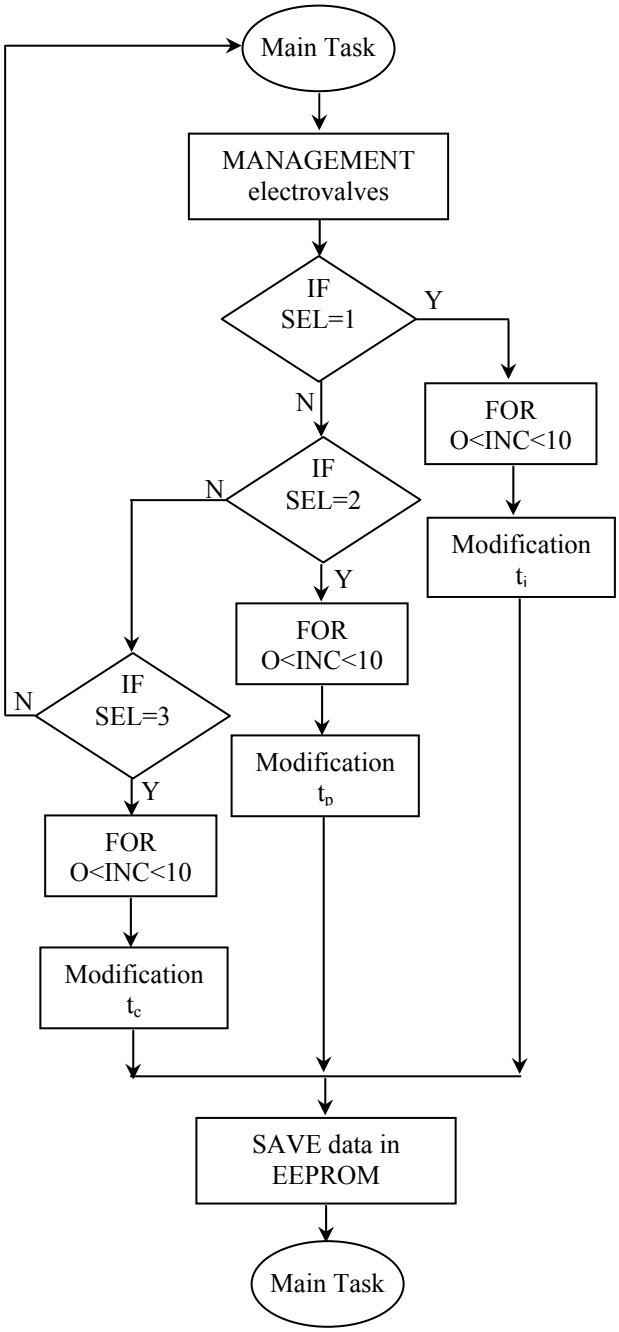

Fig. 9. The algorhythm for Main Task

The microcontroller allocates for the three lapses of time a number of seven bytes. For t_i are allocate two bytes, to addresses 0 and 1; for t_p, a number of two bytes to addresses 2 and 3; for t_c a number of three bytes to addresses 4, 5 and 6 from the data memory.

The T2 timer is set, by loading the two registers with the values T2H = 0F8H and T2L = 30H, to generate the tick of 2 ms, starting thus the T2 timer.

The two tasks of the program Main Task and Display Task are started.
In Main Task there are the order instructions for electrovalves, for examining the two external interruptions INT0 and INT1, if they were highlighted or not for modifying the intervals of time t_i, t_p and t_c, if the keyboard is acting (that is if one or both interruptions INT0, INT1 are activated) and the dates saved in EEPROM. The algorithm for Main Task is presented in figure 9.
The procedure for the control of electrovalves is described in the next sequence; and it is written in language C.

```
void management_electrovalve(void)
{  switch(status_cmd)
   { case 0x00:
        if(counter_command>=impulse time)
        { OUT1=1;   counter_command=0;
          status_cmd++; }
        else
        { OUT1=0;   counter_command++; }
        break;
     case 0x01:
        if(counter_command>=pause time)
        { OUT2=0;   counter_command=0;
          status_cmd++; }
        else
        { counter_command++; }
        break;
     case 0x02:
        if(counter_command>=impulse time)
        { OUT2=1;   counter_command=0;
          status_cmd++; }
        else
        { OUT2=0;   counter_command++; }
        break;
     case 0x03:
        if(counter_command>=pause time)
        { OUT3=0;   counter_command=0;
          status_cmd++; }
        else
        { counter_command++; }
        break;
     case 0x04:
        if(counter_command>=impulse time)
        { OUT3=1;   counter_command=0;
          status_cmd++; }
        else
        { OUT3=0;   counter_command++;  }
        break;
     case 0x05:
        if(counter_command>=pause time)
        { OUT4=0;   counter_command=0;
          status_cmd++; }
        else
        { counter_command++; }
        break;
     case 0x06:
        if(counter_command>=impulse time)
        { OUT4=1;   counter_command=0;
```

```
        status_cmd++; }
      else
      { OUT4=0;   counter_command++; }
      break;
    case 0x07:
      if(counter_command>=pause time)
      { OUT5=0;   counter_command=0;
        status_cmd++; }
      else
      { counter_command++; }
      break;
    case 0x08:
      if(counter_command>=impulse time)
      { OUT5=1;   counter_command=0;
        status_cmd++; }
      else
      { OUT5=0;   counter_command++; }
      break;
    case 0x09:
      if(counter_command>=pause time)
      { OUT6=0;   counter_command=0;
        status_cmd++; }
      else
      { counter_command++; }
      break;
    case 0x0A:
      if(counter_command>=impulse time)
      { OUT6=1;   counter_command=0;
        status_cmd++; }
      else
      { OUT6=0;   counter_command++; }
      break;
    case 0x0B:
      if(counter_command>=cycle time)
      { OUT1=0;   counter_command=0;
        status_cmd=0;
        set_led_cycle(); }
      else
      { reset_led_cycle();
        counter_command++;}
      break;
} }   }
```

The modification of the lapses of the command time is achieved as follows.

Once to 2 ms, the two external interruptions INT0 and INT1, connected to two keys SEL and INC are interrogated. The selection of the time lapses duration is done by pressing consecutively the keys SEL: SEL = 1 for t_i, SEL = 2 for t_p and SEL = 3 for t_c. The modification of the duration of the selected time lapse is done by pressing the key INC. Thus, for one pressure, the new time value will be: $t_i = t_i +$ time_impuls or $t_p = t_p +$ time_pauza or $t_c = t_c +$ time_ciclu.

If one of the three durations has touched the maximum value, then, at a new pressure of the keys INC, the duration will receive the initial value. The process is repeated in a curle till no key is pressed.

The dates thus modified are saved in EEPROM through bus I^2C.

In Display Task there are the activating instructions for the screen and for the multiplexed display of seven digits, with the value saved in each of the seven bytes of the addresses 0 to 6 from the data memory. The algorhythm for Display Task is presented in the figure 10.

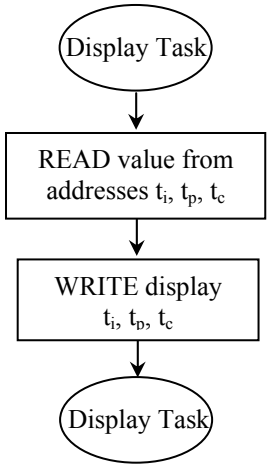

Fig. 10. The algorhythm of Display Task

IV. CONCLUSIONS

The utilization of the microcontroller in this present application represents a solution which substantially reduced the number of electronics component parts, and also the cost of projecting and developing the product. Nevertheless, however advanced the microcontroller were, some external component parts could not be excluded. These are the component parts of interface with the outside environment, which, in out case, are represented by optocouplers, transistors of power, display elements, etc.

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Broadband measurement of the refractive index using microstrip lines

Ladislau Matekovits[1] Aldo De Sabata[2] Paola Pirinoli[1] Mario Orefice[1]

Abstract – Measurement methods based on Vector Network Analyzer, for the determination of the refractive index of a medium, are described. The refractive index is obtained from the phase velocity of the radiofrequency signal along a microstrip line embedded in the considered medium. Simple structures are used for this purpose and advantages and disadvantages of different methods are discussed.

Keywords: microstrip lines, effective dielectric constant, Network Analyzer, education, microwaves

I. INTRODUCTION

Teaching electromagnetic course is usually an arduous task because of the new concepts to be transferred to the students. Description of the phenomena requires a good mathematical background and also, in the case when students understand the theoretical formulation, some of the concepts are not fully clarified from a practical point of view.

In such a context, this work has the aim to present some simple methods, well adapted as laboratory exercise for graduate courses, for the determination of the refractive index (RI) of a medium by means of a vector network analyzer (VNA).

The knowledge of the value of the RI n for a medium is important in different applications such as design of matching networks, phase shifters, etc.

For this purpose, we will consider a microstrip line embedded in the medium for which we want to evaluate the RI, and measurements on the phase of the reflection/transmission coefficients will allow us to determine the effective value of the dielectric constant ε_{eff} . The RI is related to this latter by:

$$n = \sqrt{\varepsilon_{eff}}$$

since it is defined as the ratio of the velocity of light in free space and the phase velocity in the considered medium.

Although the characteristic impedance of a microstrip line depends on ε_{eff} and on the ratio between the width of the line and heigth of the dielectric substrate

$$Z_\infty = Z_\infty(\varepsilon_{eff}, w/h)$$

in a relatively large frequency range, the effect of frequency on the characteristic impedance can be neglected.

Because of this dependence, in the following we will consider the general case when the microstrip line impedance does not match to the reference impedance of the VNA port. The effect of this mismatching is a non linear variation of the phase of the reflection coefficient versus frequency. From the maximum deviation with respect to a linear variation, one can compute the value of the line impedance as well.

II. DESCRIPTION OF THE MEASUREMENT METHODS

In this section we will describe various methods for the determination of the RI of a medium with the microstrip line. The described methods can be applied for single layer structures as well as multilayer ones. In this latter case, the value of the RI is different from layer to layer.

Since this work is essentially an educational one, we will start with the description of a simple but less accurate method based on an absolute measurement. It will be followed by different schemes, where using relative measurements some of the effects that contribute to the inaccuracy can be eliminated.

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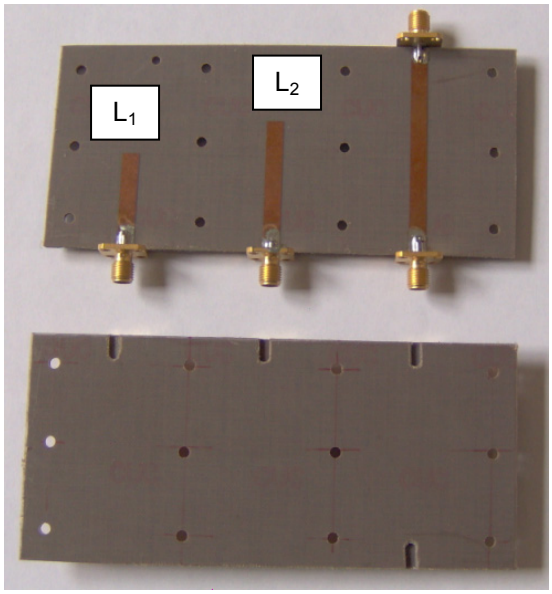
We note, that for the case of a single dielectric layer, an approximate expression for the effective value of the dielectric constant is [2]:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 10\frac{h}{w}\right)^{-0.5}$$

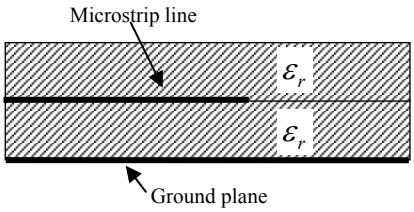
Measurements results can be compared with this value.

The structure used for all the reported measurements is presented in Fig.1. The microstrip line lies between two Arlon Cuclad™ dielectric sheets with ε_r=2.3, both of a height h=1/16" (1.6 mm). The lengths of the two open end lines (measured from the edge of the dielectric board) are L_1=26 mm and L_2=36 mm respectively.

In the figure also a thru is present. A second one, of different length, was built separately.



a)



b)

Figure 1 Photograph (a) and sketch b) of the considered structure

In Fig. 2 a photograph of the microstrip line in the experimental setup is presented. For all cases, it is supposed that the VNA has been calibrated before starting the measurements. In particular, we considered 1601 points in the 200 MHz-5 GHz frequency range.

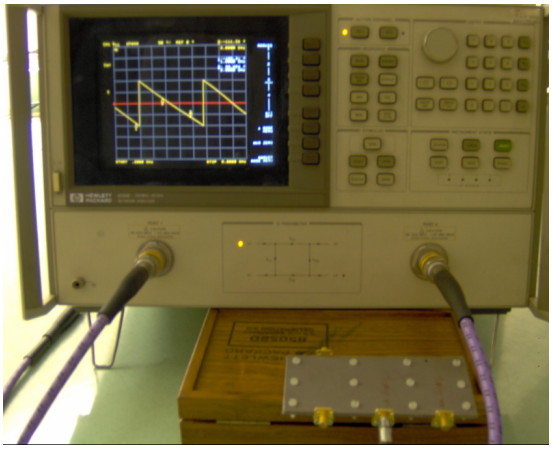


Figure 2 Photograph of the measurement setup

A. *Direct method*

The simplest method consists in measuring the phase of the reflection coefficient of an open-ended microstrip line, and introducing a shift of the reference plane, which is a feature of the VNA.

The considered circuit is depicted in Fig.3. The open ended microstrip line, of length ℓ, is fed by a coaxial-microstrip transition. The reference plane, defined during the calibration is somewhere inside the connector/transition.

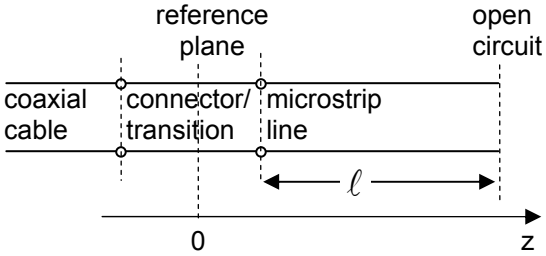


Figure 3 Sketch of the circuit for the direct method

An ideal open circuit has the phase of the reflection coefficients equal to 0°, but it is difficult to build due to radiation of the truncation and the fringing capacity. Moreover, we are interested in the fact that the *phase* at the terminal end is *constant* in a relatively wide frequency range.

Using the electrical delay option of the VNA, it is possible to shift the reference plane according to:

$$\Gamma(\ell_0) = \Gamma(0)e^{\pm 2jk_0\ell_0}$$

where k_0 is the *free space* propagation constant and ℓ_0 is the distance between the reference plane and the new section where the reflection coefficient is evaluated.

The + sign corresponds to a shift from the reference plane toward the load, while the – sign allows to move in the opposite direction.

Since the open circuit we are interested in is away from the reference plane, we will consider a *positive* phase shift.

By introducing the phase shift, we expect that, for a certain value of this electrical delay, the resulting phase to be constant in a certain frequency range. It is convenient to use a phase or Smith chart format for representing the measurements.

The resulting reflection coefficient is:

$$\Gamma(\ell_0, f) = \Gamma(0, f)e^{+2jk_0(f)\ell_0} = \left|\Gamma(0, f)\right|e^{+2jk_0(f)\ell_0 + j\Phi(0,f)}$$

where $\Phi(0, f)$ represents the phase of the measured reflection coefficient at the reference plane (z=0). The value of the electric delay that corresponds to this refers to a delay in free space. Denoting by ℓ_0 the value for which

$$2k_0(f)\ell_0 + \Phi(0, f) = const.$$

and by taking into account the definition of the RI, we can compute it as the ratio of this distance and the length ℓ of the line.

$$n = \frac{\ell_0}{\ell}$$

The main disadvantage of this method is that it requires the knowledge of the line length. Actually, ℓ includes the length of the line, the effect of the fringing field, and the distance inside the connector/transition from the reference plane to the beginning of the line. This latter distance is not known. To reduce the inaccuracy of the method, it is convenient to consider a relatively long line.

In Fig. 4, the phase of the reflection coefficient is reported for the line L_2. On the top, the electrical delay is equal to zero and a linear phase variation can be noticed. In the lower photograph, the uniform phase is obtained for an electrical delay equal to 438.12 ps. It corresponds to ℓ_0=131.34 mm. It is clear from the Smith chart, that it corresponds to an open circuit.

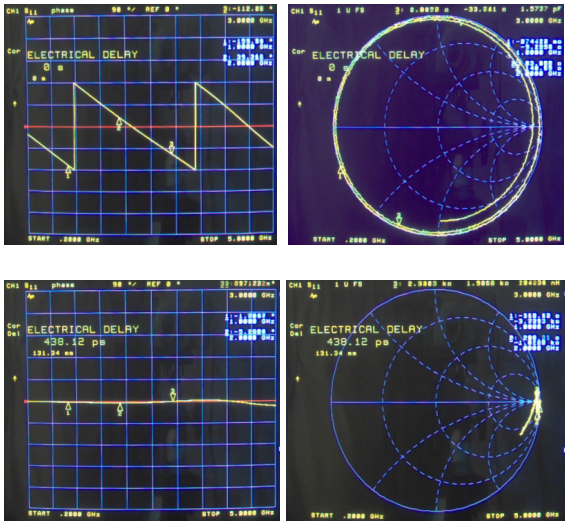


Figure 4 Zero electrical delay (top) and constant phase (bottom)

B. *Method based on the variation of the frequency*

Another fast method is based on the measurement of the phase of the reflection coefficient at two different frequencies. Denoting by 1 the reference frequency and by 2 a second value of the frequency, we have:

$$\Gamma_1 = \Gamma(0)e^{-2jk_1\ell} = \Gamma(0)e^{-j\Phi_1}$$
$$\Gamma_2 = \Gamma(0)e^{-2jk_2\ell} = \Gamma(0)e^{-j\Phi_2} \quad (1)$$

where Γ_1 and Γ_2 represent the reflection coefficients at the input of the line for the two frequencies f_1 and f_2. The phase difference is:

$$-\Delta\Phi = -\Phi_1 + \Phi_2 = 2k_2\ell - 2k_1\ell = 2\ell(k_2 - k_1) = \frac{4\pi}{c}n\ell\Delta f \quad (2)$$

In the equation above we considered a lossless line $\left(k = \frac{2\pi}{\lambda}\right)$, and made use of the relations $n = \frac{c}{v_f}$ and $\lambda = \frac{v_f}{f}$ From eq. 2 it is therefore possible to obtain:

$$n = -\frac{c}{\ell}\frac{\Delta\Phi}{4\pi}\frac{1}{\Delta f}$$

It has to be noted, that in eq. (2), the phase difference is the total (unwrapped) one, and not only the value reported on the VNA: one has to consider a 2π additional term at each "jump", due to the representation within the interval $[-\pi, \pi]$.

As in the previous method, in this case we have an inconvenient due to the length of the line too. Actually, the equation makes use of the distance between the open end and the reference plane defined during the calibration. Since the line has to be connected by a connector, the length of the connector and the transition is not known in a precise way. This length can be quantified, or its effect can be eliminated by employing a relative measurement, as it will be described in the following paragraph.

C. *Method based on the variation of the length of the microstrip line*

Instead of varying the frequency, as in the previous paragraph, we can imagine a scheme with two microstrip lines of different lengths (see Fig. 5). In this case, the phase difference will originate from the difference between the two lines lengths at the same frequency:

$$n = -\frac{c}{\Delta\ell}\frac{\Delta\Phi}{4\pi}\frac{1}{f} \qquad (3)$$

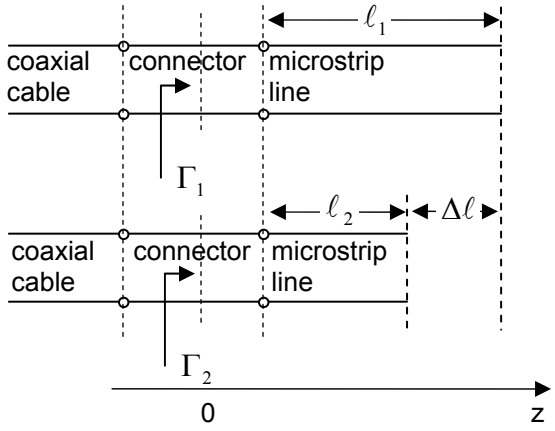


Figure 5 Sketch of the circuit for the method II. C

In Fig. 6, the behavior of two traces corresponding to two different line lengths (L1 and L2 in Fig. 1) for different values of the electrical delays are presented. The first photograph (top) refers to the absence of the electrical delay. The active trace, with the markers on it, corresponds to the shorter line. The second trace represents the phase of the longer line. It is clear from the photo that the longer line presents a higher variation of the phase for the same frequency range.

Introducing an electric delay and increasing its value up to ED_1 =349.88 ps (center photograph), the phase corresponding to line L1 presents azero mean value. The amplitude of the oscillations correspond to the mismatching between the 50 Ω reference impedance and the line impedance. By reporting this value of the reflection coefficient on a Smith chart, and by considering a circle with center in the center of the Smith chart and tangent to this line, the modulus of the reflection coefficient can be obtained. Since line impedance and reference impedance are real, the intersection of this circle with the real axis will represent the ratio between the two impedances.

Further increasing the electric delay, the phase corresponding to the L1 line will move from the zero mean value. We will find the same behavior for the L2 line for an electric delay of ED_2 =446.45 ps (bottom photograph).

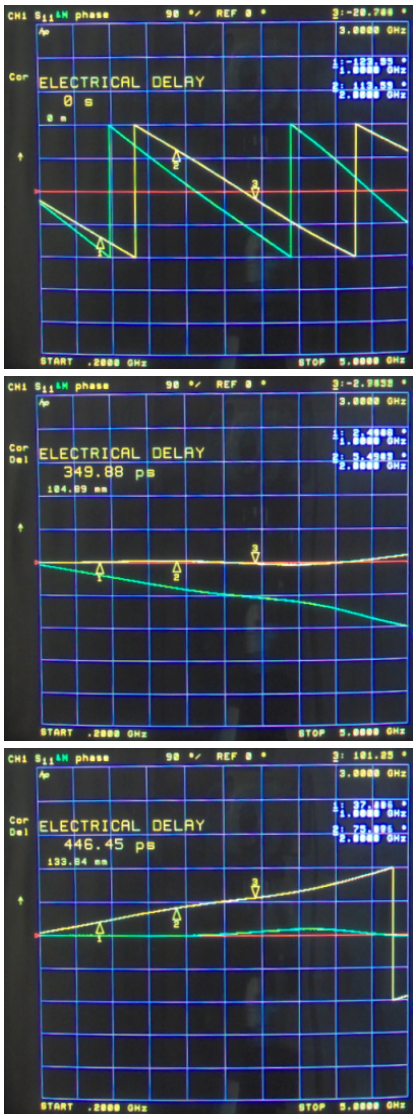


Figure 6 Phase value of the electrical delay corresponding to the reference plane shift to the open end for the two lines (active trace line L_1, memory trace line L_2)

The phase difference at different values of the frequency can be read directly from the VNA. Inserting it in eq. 3, we can find the value of *n*.

This method has the advantage of eliminating the inaccuracy on the line length, since in the determination of *n* only the difference between the two line lengths is present.

Furthermore, it allows to characterize the value of the RI vs. frequency, since measurements are made at single frequency points.

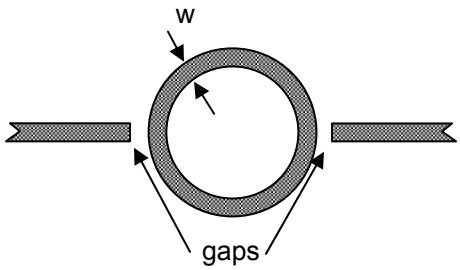
Regarding the measurement in transmission, two lines of different lengths are used. The measured phase difference corresponds to the product between the phase velocity and the difference in lengths. By inverting this expression, the value of n can be obtained.

D. Ring resonator

The method proposed in [3] eliminates completely the inaccuracy due to the position of the reference plane. It makes use of a printed resonant structure by electromagnetic coupling. Referring to the geometry of Fig. 2, the value of the RI is given by:

$$n = \frac{pc}{2f\ell}$$

Where p denotes the order of the resonance, c the speed of light in free space, f the ring resonant frequency and ℓ the principal circumference of the ring resonator.



Measurements can be done both in transmission and in reflection.

The advantage of the method is due to the fact that no phase measurement is needed and, consequently, the VNA can be disposed of.

The values of f and p are determined with the scalar network analyzer (NA). Resonant frequencyies can be defined in different ways: on one hand, they correspond to the frequencies where the imaginary part of the reflection coefficient vanishes. On the other hand, they are given by the minimum value of the reflection coefficient. The two values are slightly different (0.02-0.03 %)

The disadvantage is represented by the fact that the resonant frequencies are influenced by the dimension of the gaps.

III. CONCLUSIONS

Methods for the determination of the refractive index of media were presented. They are based on the measurement of the phase velocity of an RF signal on a microstrip line immersed in the considered media. The circuits required for the proposed measurements are relatively easy to realize in laboratory.

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Building A Transient Disturbances Generator With Graphical User Interface in Matlab

Gabriel Găşpăresc[1], Ciprian Dughir [1]

Abstract – This paper describes an implementation method of a transient disturbances generator with graphical user interface in Matlab environment, using an integrated codec or a sound card, the advantages and the disadvantages of this solution, in the actual context of increasing of the interest for ensure power quality and disturbances study which can affect it.
Keywords: transient disturbances, sound card, graphical user interface, power supply quality, electromagnetic compatibility.

I. INTRODUCTION

Transient disturbances represent an important category of disturbances which may affect the quality of electrical energy supply; the last decades were marked by an unprecedented development of electronics and telecommunications, there appeared devices and equipments more sensible to the power quality disturbances and there have increased the electromagnetic compatibility problems [3].

Signal generators are used in the field of electromagnetic compatibility at the immunity/susceptibility equipment tests. The signals of biexponential impulse and amortized sinus are obtained using RC or RLC circuits. The parameters of the test signals are standardized by regulation, for impulses the rise time can be under 1 ns and the required amplitudes are in the range of KV/KA, values hard to obtain [3].

At present most of computer mainboards have integrated codecs or sound card which contain analog-to-digital converters (ADC), respectively digital-to-analog converters (DAC), these operate at maximal sampling frequencies of 44100 Hz or 96000 Hz. These may be used as a cheaper alternative (probably the cheapest) at the acquisition boards used at the numeric processing of signals; the disadvantages are regarding the sampling frequency and the dynamical range of the more reduced input and output signals, but may be used successfully for didactic purposes, inclusively for the generating of transient disturbances with the help of a software application.

The Matlab environment, dedicated to the performing of numeric calculations, graphic representations and the programming in technique grants the access to and the configuring of the resources of the sound codec of the sound card or of the codec integrated on the computer mainboard. These may be used as an acquisition board, and by the building of a friendly interactive graphic interface with the user can be achieved an interactive control of the program execution, depending upon the data registered by the user, using the object oriented programming.

II. TRANSIENT DISTURBANCES

The transient disturbances represent quick variations of the voltage, current or of both and may be of two kinds, impulsive and oscillatory transient. The first category has exponential rise and falling fronts and is characterized by amplitude, rise time (the period in which the signal varies from 10% to 90% from its amplitude) and duration (time period for which the signal is greater than ½ from its amplitude) [3], and in order to generate a biexponential impulse (fig. 1a) there may be used a formula of the kind of the one shown below

$$s(t) = at^b e^{-ct} \tag{1}$$

where the parameters a, b and c allow the regulating of the amplitude, of the rise time and the impulse duration. The second category is characterized by the rise time according to the first peak and frequency, and further we have a division into 4 sub-categories: high frequency (>500 KHz), average frequency (5-500 KHz), low frequency (0,3-5 KHz) and very low frequency (<300 Hz) [1], and such a signal may be obtained by multiplying a biexponential impulse (obtained by using the formula (1)) with a sinusoidal signal (fig. 1b) described by the formula (2)

$$s_s(t) = A\sin(2\pi ft + phase_i) \tag{2}$$

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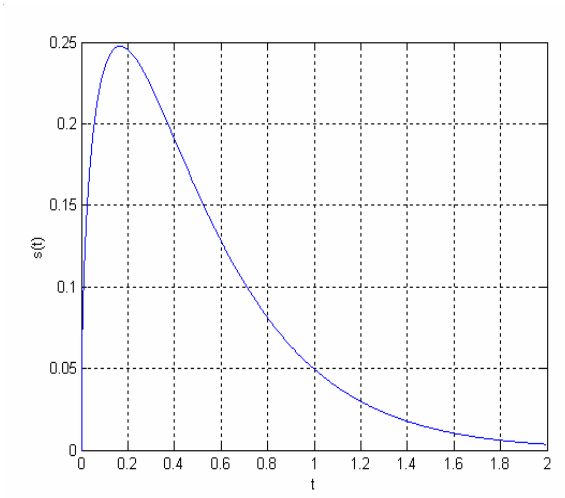
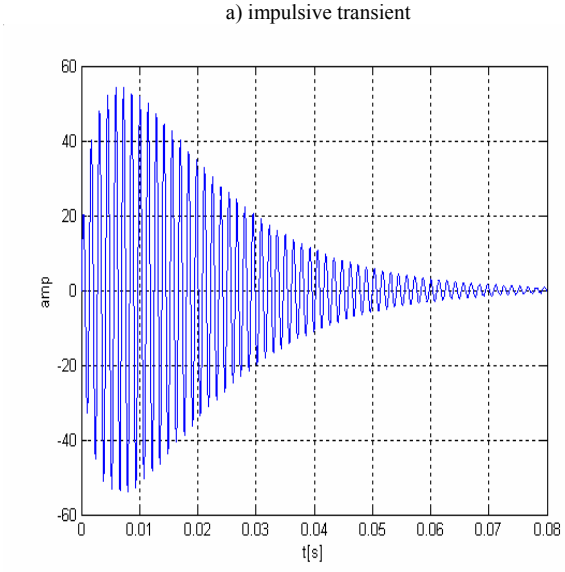
where A is the amplitude, f the frequency and $phase_i$ the initial phase.

Typical causes that lead to the producing of the transient disturbances are: thunder and lightning, short-circuits, burning of fuses, connecting and disconnecting of some consumers, connecting of the condenser batteries.



a) impulsive transient



b) oscillatory transient

Fig. 1. Transient disturbances

III. INTERFACE TO THE USER AND EXPERIMENTAL RESULTS

The control of the program running is achieved by an interactive graphical interface (GUI – Graphical User Interface) based on programming object oriented, where the running of the commands chosen by the user is achieved by the selecting of the meant interface elements with the mouse. For an easy using it is important that at the GUI design, to be considered some principles: simplicity (using of the strict necessary elements), coherence (for various applications to use the same moods of placing the interface elements facilitates the passing from one to the other) and familiarity (the use of some suggestive elements grants a more quicker learning of the using) [5].

The right part of the interface (fig. 2) has five areas with suggestive labels, the first in the upper part for inserting the parameters of the sinusoidal signal (amplitude, frequency, sampling frequency, whose maximum value is of 44100 Hz, number of desired periods), over which may be overlapped a transient disturbance, the second for transient impulse (characterized by the constants a, b, c from the formula (1)), the third for oscillatory transient (where the amplitude and frequency are specified), the fourth for selecting the desired output signal (undisturbed sinusoidal, disturbed sinusoidal with impulsive or oscillatory transient), where if the signal amplitude is higher than in module than 1, a normalization is achieved, the range of the output voltages at the sound card being of [-1V, 1V]. The last zone allows the starting/stopping of the sound card and the closing of the program. The left side allows the visualizing of the output signal wave shape.

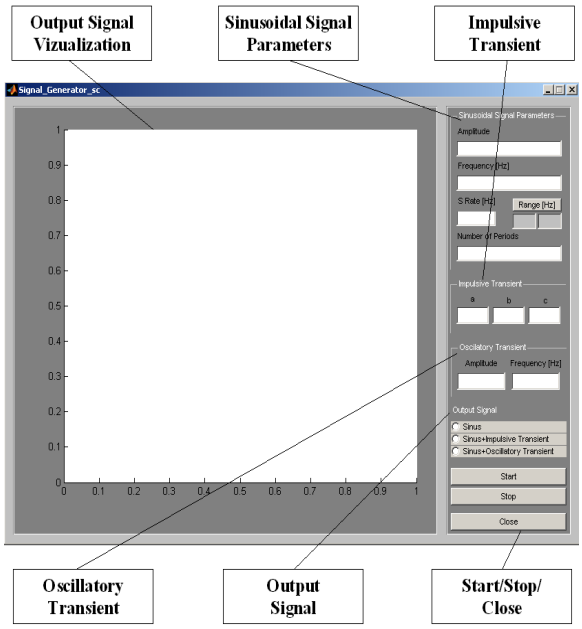


FIG. 2 Graphical user interface

The application structure is modular, between the functions corresponding to the elements of the graphic interface are transmitted the parameters inserted by the user for the generating of the desired output signal, at the activating of the sound board after setting the sampling frequency of the codec. Its value is chosen in the interval supported by the hardware, the minimum value being of 8000 Hz for most of the sound boards, and the maximum value of 44100 Hz or 96000 Hz at the more recent performance boards. Using the Range button of the interface, the minimal and maximal value of the supported sampling frequency will be displayed. At the choosing of this value there must be also considered the frequency of the generated sinusoidal signal, in order to observe the

sampling theorem [4], and to be able to rebuilt the signal from its samples (3)

$$T \le \frac{1}{2 f_m} \tag{3}$$

where T is the sampling period, and f_m the maximum frequency from the range of the signal spectrum to be sampled.

If we choose a value of 44100 Hz for the sampling frequency, that means that each second at the output are produced 44100 samples, meaning an important amount of samples that need a suitable memory volume, so that in order to use less memory, it is more convenient to choose a reduced amount of periods for the output signal, that are generated and produced repeatedly at the audio output in the desired time period (using the Start and Stop buttons), than to generate a signal of desired duration with a high amount of periods to be memorized and afterwards to be produced at the output.

The next table presents the necessary memory volume (*Memory*) in order to produce a signal of a frequency of 50 Hz at the audio output, regarding the sampling frequency (F_S) and the number of signal periods (*NP*). We can see that at the growing of the sampling frequency from 8000 Hz to 44100 Hz, when NP=2, the used memory volume grows 2.5 times, and for F_S=44100 and NP=100 in comparison with F_S=8000 and NP=2 the growth is 5.5 times. Continuing the remark from the previous paragraph, regarding the choosing of a lower amount of signal periods, for the reducing of the necessary memory volume, there may be also used a lower sampling frequency.

Table 1

Fs [Hz]	NP	Memory [B]
8000	2	16384
8000	100	32768
16000	2	20480
16000	100	65536
32000	2	40960
32000	100	131072
44100	2	40960
44100	100	180224

The experiments have been performed using a PC computer with a mainboard having an integrated audio codec, an analogical oscilloscope for visualizing the signals and a probe to link the audio output and the oscilloscope input (fig. 3).

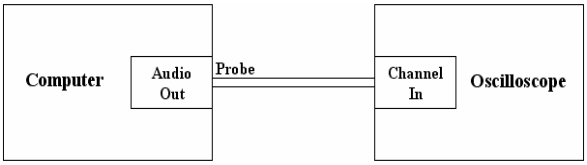
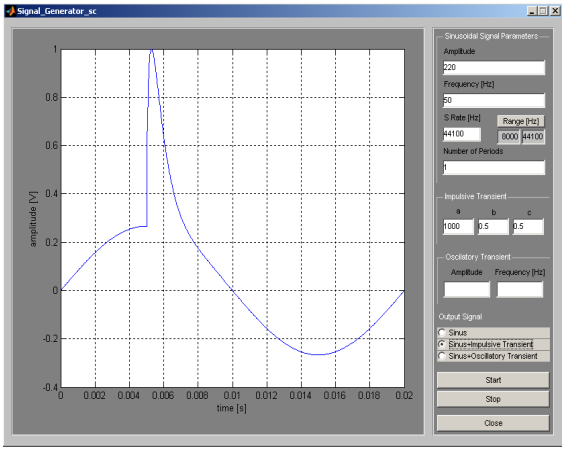
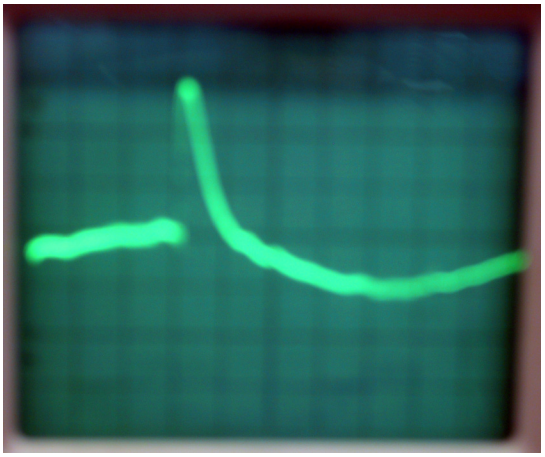


FIG. 3 Connection computer – oscilloscope

The signal from fig. 4 a) is obtained introducing for the sinusoidal signal the parameters amplitude, frequency, sampling frequency, number of periods with values of 220, 50, 44100, 1. The parameters a, b, c of the biexponential impulse have the values 1000, 0.5, 0.5. Fig. 4 b) shows the signal obtained at the audio codec output after selecting a time base suitable for the visualization only of a period of the output signal, in order to distinguish the details of the wave shape.



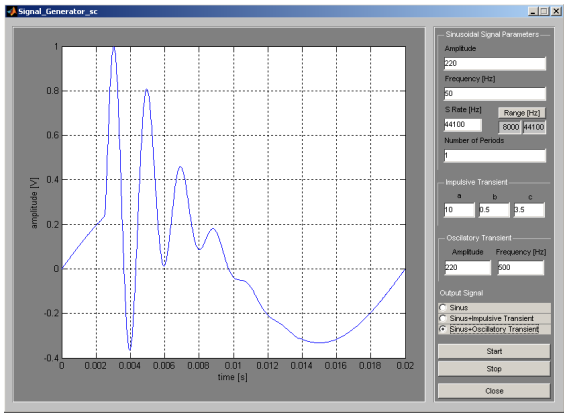
a)



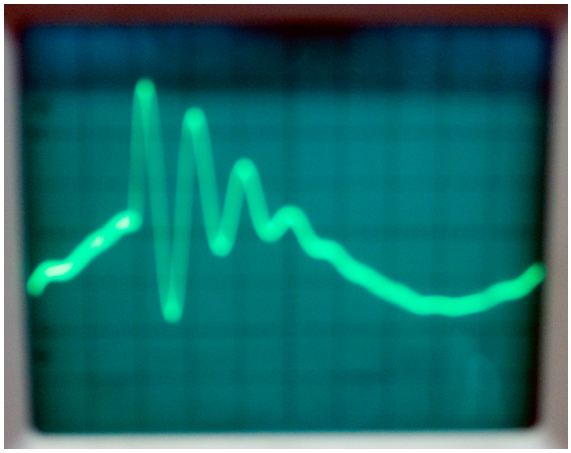
b)

FIG. 4 Generating of a disturbed sinusoidal signal with impulsive transient

Further, in order to obtain the signal from fig. 5 a), the parameters amplitude, frequency, sampling frequency, number of periods of the sinusoidal signal, upon which is overlapped the transitory disturbance, have the same values as at the previous output signal, the amortized sinus has the amplitude and the frequency with the values 220, 500, and the biexponential impulse has the parameters a, b, c with the values 10, 0.5, 3.5 and the signal obtained at the output of the audio codec is shown in fig. 5 b).



a)



b)

FIG. 5 Generating of a disturbed sinusoidal signal with oscillatory transient

IV. CONCLUSIONS

Using the Matlab environment and an audio codec integrated on the main board of a computer or a sound card, there may be achieved a transient disturbances generator, which allows the visualizing of the sinusoidal signals affected by such disturbances, at very low costs, that may be used at their study. The friendly interactive graphic interface allows the easy selecting of the parameters for the desired output signal, the selecting flexibility being restricted only by the input/output range limited at [-1V, 1V] and by the maximum sampling frequency. In order to obtain signals with higher amplitudes there may be used an amplification circuit.

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Chaos in Switching Power Converters

Corina M. Ivan[1], and Viorel Popescu[2]

Abstract - This paper presents an overview of the complex behaviour of the switching power converters. The power electronics circuits, due to their nonlinearity, exhibits a variety of complex behaviour, such as: sudden change of operating regime, subharmonic and chaotic operation, etc. This behaviour can occur when some parameters of the circuit are varied.
Keywords: switching power converters, nonlinear behaviour, chaos

I. INTRODUCTION

Power electronics circuits can be described as piecewise-switched circuits, which assume different topologies at different times. Toggling between these topologies is done in a cyclic manner. The result is nonlinear time-varying operation.

Power electronics circuits, being nonlinear, exhibit a variety of complex behaviour such as sudden change of operating regime, chaotic operation, occasional instability (depending on the circuit parameters), intermittent subharmonic or chaotic operation, etc.

Both the circuit topology and the control method determine the dynamical behaviour of a power electronics circuit. Chaos is a common phenomenon in power converters when they are operated under feedback control. Chaotic systems are sensitively dependent on the initial conditions, which makes long-term prediction of their behaviour impossible.

In analysing power electronics circuits much effort has been spent in developing linear models of dc-dc converters. One of the most popular of these models is the state-space averaging. Although it has many advantages, it is approximate [1]. Also, it doesn't predict some instabilities in the circuit, such as the subharmonic instability associated with the current-mode control [2].

An overview of the nonlinear behaviour in dynamic systems ("chaos theory"), the switching power converters models and their application for nonlinear behaviour analysis, and some techniques used for the study of nonlinear and chaotic behaviour are presented in Section II. The nonlinear behaviour in various switching power converters is examined in Section III. Some conclusions are presented in Section IV.

II. METHODS OF STUDYING NONLINEAR BEHAVIOUR IN SWITCHING POWER CONVERTERS

A. *Nonlinear behaviour in dynamic systems*

Even simple systems can behave in a chaotic fashion. The main cause of this behaviour has been identified as nonlinearity.

Chaos is a particular qualitative behaviour of nonlinear systems, which is characterized by an aperiodic and apparently random trajectory [4].

The behaviour of the dynamical systems varies as a function of time. A dynamical system can be described by the following equation:

$$\frac{dx(t)}{dt} = f(x(t), \mu, t) \qquad (1)$$

where x is the state variables vector, and μ is the parameters vector. If f depends on time, the system is called *non-autonomous*, and if f doesn't depend on time, the system is called *autonomous*.

The solution of the system is known as the *trajectory*. The equilibrium solution to which the system converges is called an attracting equilibrium solution (*attractor*). A dynamical system can have multiple equilibrium solutions, depending on the system parameters. When a parameter is varied, the behaviour of the system can suddenly change. This phenomenon is called *bifurcation*. Some commonly observed bifurcations are [2], [5]:

- *saddle-node bifurcation* – it is characterized by a sudden loss of a stable equilibrium solution, when a parameter goes beyond a critical value;
- *transcritical bifurcation* – it is characterized by an exchange of stability status between two equilibrium solutions;
- *supercritical pitchfork bifurcation* – the stable equilibrium solution splits into two stable

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equilibrium solutions, at a critical parameter value;

- *subcritical pitchfork bifurcation* – it is characterized by a sudden explosion of a stable equilibrium solution as a parameter goes beyond a critical value;
- *period-doubling bifurcation* – it is characterized by a sudden doubling of the period of a stable periodic orbit when a certain parameter is varied; this doubling of the period may continue to occur when the parameter is varied in the same direction;
- *Hopf bifurcation* – it is characterized by a sudden expansion of a stable fixed point to a stable limit cycle;
- *border collision* – it is an abrupt change in behaviour when a parameter is varied across the boundary of two structurally different systems. In switching converters it is a result of a change of topological sequence.

B. *Switching power converters modelling*

The nonlinear and time-varying operation of the switching power converters demands nonlinear methods for analysis.

The switching power converters modelling has two basic approaches: averaging approach and discrete-time approach.

Suppose the switching converter toggles between N circuit topologies, d_i being the fraction of the period in which the circuit stays in the i-th topology, A_i and B_i the system matrices, V_g the input voltage and T_s the switching period. Obviously, $d_1 + d_2 + \cdots + d_N = 1$. The state equations for the system are the following:

$$\dot{x} = \begin{cases} A_1 x + B_1 V_g, & t_n \le t < t_n + d_1 T_s \\ A_2 x + B_2 V_g, & t_n + d_1 T_s \le t < t_n + (d_1 + d_2) T_s \\ \quad \cdots & \\ A_N x + B_N V_g, & t_n + (1 - d_N) T_s \le t < t_{n+1} \end{cases} \quad (2)$$

The averaging approach [6] removes the time-varying dependence from the original time-varying model.

The averaged model is the weighted average of all the state equations, written for all possible circuit topologies. The typical form of the averaged model is the following:

$$\frac{dx}{dt} = \left(\sum_{i=1}^{N} d_1 A_i \right) x + \left(\sum_{i=1}^{N} d_1 B_i \right) V_g \quad (3)$$

The control law is given as a set of equations defining d_i. The general form of this set of equations is:

$$\begin{cases} G_1(d_1, d_2, \ldots, V_g, x) = 0 \\ G_2(d_1, d_2, \ldots, V_g, x) = 0 \\ \quad \cdots \end{cases} \quad (4)$$

The averaging approach is widely used and well known, and it is relative easy to derive the continuous averaged equation. Usually, the validity of averaged models is restricted to the low-frequency range, up to an order of magnitude below the switching frequency. For this reason, averaged models become inadequate when the aim is to explore nonlinear phenomena that may appear across a wide spectrum of frequencies. Nevertheless, averaging techniques can be useful to analyze low-frequency bifurcation phenomena.

Another modelling approach is the discrete-time iterative approach. Its aim is to derive an iterative function that expresses the state variables at one sampling instant in terms of those at an earlier sampling instant:

$$x_{n+1} = f(x_n, d, V_g) \quad (5)$$

where x_n is the state vector at $t = nT_s$, d is the vector of the duty cycles: $d = [d_1\ d_2\ \ldots\ d_N]^T$. Eqn (5), the discrete-time state equation, assumes that the sampling period is equal to the switching period. Therefore, the model can be used up to the switching frequency. Since most power electronics circuits are non-autonomous systems driven by fixed-period clock signals, the study of the dynamics can be effectively carried out using appropriate discrete-time maps. The disadvantage of the model is that the derivation of the iterative map is more complicated compared to the continuous-time averaged equation.

C. *Analysis of standard bifurcations*

The analysis begins with the system model.

If the averaged model is used, first the set of continuous averaged state equations are derived. Then, the eigenvalues (characteristic multipliers) of the Jacobian, $J(X_Q)$ and are found, using the following equation:

$$\det[\lambda I - J(X_Q)] = 0 \quad (6)$$

The next step is to identify the condition for the eigenvalue(s) to move across the imaginary axis in the complex plane (as for instance, a pair of complex eigenvalues moving across the imaginary axis implies a Hopf bifurcation).

If the discrete time approach is used, first is derived the discrete-time state equation (also called iterative map, iterative function or Poincaré map). Next, the Jacobian, $J(X_Q)$ is examined to find eigenvalues. Then, the condition for the eigenvalue(s) to move out the unit circle in the complex plane is identified.

The discrete-time and averaged models treat the duty cycle as an input. In practice, the duty cycle is controlled through some feedback mechanisms. Thus, to complete the model, we need to state the control law. For instance, in the usual pulse-width modulation control, a control signal (deriving from the state variables) and a ramp signal are compared, their

intersection defining the switching instant. Thus, the control law can be:

$$V_{ramp}(dT_s) = v_{con}(x(dT_s)) \tag{7}$$

where $V_{ramp}(t)$ is a ramp voltage and v_{con} is the control signal. From this equation, we can find d for each switching period. For the voltage-mode control, considering a proportional feedback, the control law is the following:

$$d_n = H\left(D - \kappa\left(v_o - V_{ref}\right)\right) \tag{8}$$

where D is the steady-state duty cycle, κ is the small-signal feedback gain, V_{ref} is the reference output voltage, and H limits the range of the duty cycle between 0 and 1:

$$H(x) = \begin{cases} 0, & for \quad x < 0 \\ 1, & for \quad x > 1 \\ x, & for\ 0 \le x \le 1 \end{cases} \tag{9}$$

For the current-mode control, the control law is given by:

$$i_{ref} = I_{ref} - \kappa(v_o(t) - V_{ref}) \tag{10}$$

where I_{ref} is the steady-state reference current.

D. *Techniques for studying nonlinear and chaotic behaviour*

Poincaré sections – are graphical representations of the behaviour of a high-order system. They are planes that intersects the trajectory of the system. If the Poincaré section contains a finite number of points, the steady-state operation is periodic. If the Poincaré section contains a closed loop, the operation is quasi-periodic. If the Poincaré section is irregular, the operation is chaotic.

Bifurcation diagrams – are graphical representations of the behaviour exhibited by a system when some parameters are varied.

Lyapunov exponents – they measure the exponential convergence or divergence of neighbouring orbits of a dynamical system. Considering two trajectories that initially are separated by a distance ε_0, if this distance increases or decreases exponentially in time, it can be expressed as:

$$\varepsilon(t) = \varepsilon_0 e^{\lambda t} \tag{11}$$

If $\lambda > 0$, the two trajectories diverge exponentially in time and the behaviour of the system is chaotic.

III. NONLINEAR BEHAVIOUR IN SWITCHING POWER CONVERTERS

Switching power converters, due to their nonlinearity exhibits a variety of complex and chaotic behaviour. The behaviour of a dc-dc converter is greatly influenced by the operating mode and the control technique. Most dc-dc converters are designed to deliver a regulated output voltage. The control of dc-dc converters usually takes on two approaches: *voltage feedback control (voltage-mode control)* and *current-programmed control (current-mode control)*.

In voltage feedback control, the output voltage is compared with a reference to generate a control signal which drives the pulse-width modulator.

For current-programmed control, an inner current loop is used in addition to the voltage feedback loop, to force the peak inductor current to follow a reference signal which is derived from the output voltage feedback loop.

From what has been reported so far in the literature, the following observations regarding the nonlinear behaviour of the switching power converters can be made:

- converters under fixed-frequency current-mode control generally lose stability via a period-doubling type of bifurcation;
- in switching power converters border collision can occur due to a change of operating mode or due to saturating nonlinearity– caused by the inherent limitation of the range of some control parameters (as for instance, as a result of saturating the duty cycle [2]);
- voltage-mode controlled BUCK converters typically exhibit period-doubling bifurcations [12, 13], whereas BOOST converters typically exhibit Hopf bifurcation [10, 14];
- period-doubling is common in BUCK or BOOST converters operating in Discontinuous Inductor Current Mode (DICM) [15, 16] and current-mode controlled converters [11, 17].

Further on, we analyse the nonlinear behaviour of some switching power systems.

A. *BUCK converter, voltage-mode control, CCM operation*

For the BUCK converter, shown in Fig. 1, the state-equations when the converter is operating in Continuous Conduction Mode (CCM), are the following:

$$\begin{aligned} \dot{x} &= A_1 x + B_1 V_g, \quad t_n \le t < t_n + dt \\ \dot{x} &= A_2 x + B_2 V_g, \quad t_n + dt \le t < t_{n+1} \end{aligned} \tag{12}$$

where x is the state vector $[v_o \ i_L]^T$, d is the duty cycle.

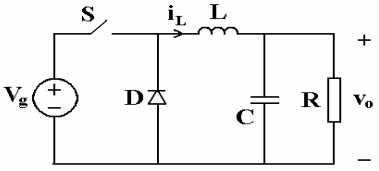

Fig. 1. The BUCK converter.

By solving the state equations, the discrete-time equation can be obtained:

where:

$$f(x,d)=\begin{bmatrix} f_{11} & f_{12} \\ f_{21} & f_{22} \end{bmatrix} x+\begin{bmatrix} g_1 \\ g_2 \end{bmatrix} V_g \qquad (14)$$

The approximate expressions for *f(x,d),* determined in [2] are given by:

$$f_{11}=1-\frac{T_s}{\tau_C}+\frac{T_s^2}{2\tau_C^2}-\frac{T_s^2}{2\tau_C\tau_L} \qquad (15)$$

$$f_{12}=\frac{RT_s}{\tau_C}-\frac{RT_s^2}{2\tau_C^2} \qquad (16)$$

$$f_{21}=-\frac{T_s}{R\tau_L}+\frac{T_s^2}{2R\tau_C\tau_L} \qquad (17)$$

$$f_{22}=1-\frac{T_s^2}{2\tau_C\tau_L} \qquad (18)$$

$$g_1=\left(1-\frac{d}{2}\right)\frac{dT_s^2}{\tau_C\tau_L} \qquad (19)$$

$$g_2=\frac{dT_s}{R\tau_L} \qquad (20)$$

where $\tau_C = CR,\ \tau_L = L/R$.

For voltage-mode controlled BUCK converter, operating in CCM [2], in order to investigate the bifurcation phenomena, the following parameters are used: V_g = 22-33V, L = 20mH, f_s = 2.5kHz, R = 22Ω, C = 47μF, V_{ref} = 11V.

In Fig. 2, 3, 4 are presented the output voltage and inductor current waveforms and the phase portraits in various operating regimes: fundamental periodic operation (period-1), period-2 subharmonic operation and chaos, as a result of the border collision, obtained by computer simulation, using CASPOC.

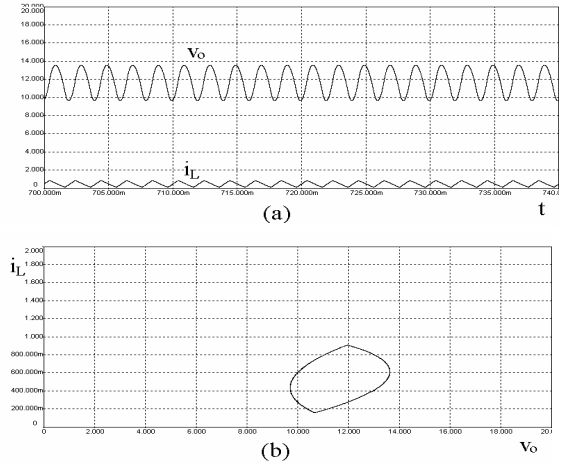

Fig. 2. (a) Fundamental waveforms (simulation results) for BUCK converter operating in CCM, V_g=23V; (b) phase portrait.

B. *BUCK converter, voltage-mode control, DICM operation*

In a similar way to CCM, the state equation for DICM can be derived:

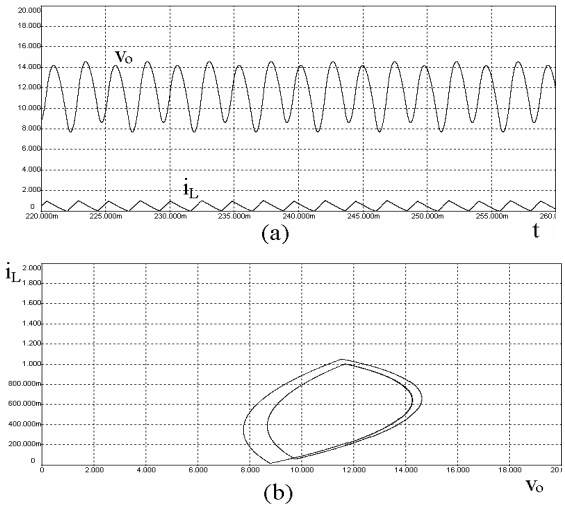

Fig. 3. (a) Period-2 subharmonic waveforms (simulation results) for BUCK converter operating in CCM, V_g=28V; (b) phase portrait.

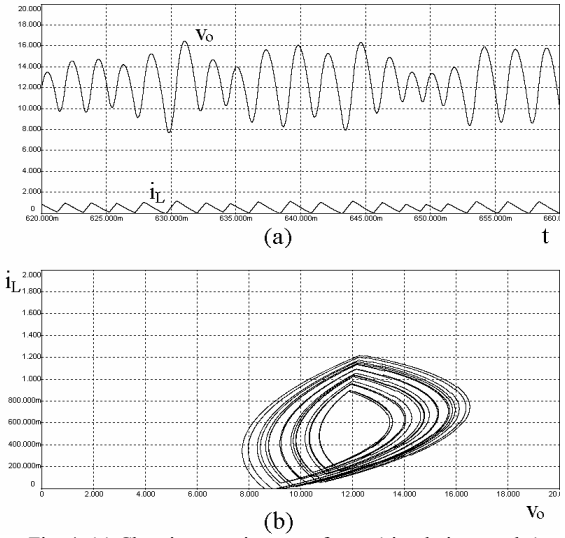

Fig. 4. (a) Chaotic operation waveforms (simulation results) for BUCK converter operating in CCM, V_g=33V; (b) phase portrait.

$$v_o(t_{n+1})=f(v_o(t_n),d_n)=\alpha v_o(t_n)+\frac{d_n^2V_g(V_g-v_o(t_n))}{v_o(t_n)} \qquad (21)$$

where:

$$\alpha=1-\frac{T_s}{\tau_C}+\frac{T_s^2}{2\tau_C^2} \qquad (22)$$

$$\beta=\frac{T_s^2}{2LC} \qquad (23)$$

For voltage-mode controlled BUCK converter, operating in DICM, in order to investigate the bifurcation phenomena, the following component values are used: V_g = 33V, L = 194μH, f_s = 3kHz, R = 12.5Ω, C = 222μF, V_{ref} = 25V, D = 0.47. Assuming that in the neighbourhood of the steady-state the duty

cycle does not saturate, the characteristic multiplier can be computed from Eqn. (21):

$$\lambda = \left.\frac{\partial f(v_o)}{\partial v_o}\right|_{v_0=V_o} = \alpha - \frac{\beta V_g D[2\kappa V_o(V_g - V_o) + DV_g]}{V_o^2} \tag{24}$$

The system is fundamentally stable if $|\lambda| < 1$. The critical value of the small-signal feedback gain, κ, can be found by setting the characteristic multiplier to -1:

$$\kappa_c = \frac{(1+\alpha)V_o^2 - \beta V_g^2 D^2}{2\beta V_g D V_o (V_g - V_o)} \tag{25}$$

For the studied circuit, κ_c=0.115.

In Fig. 5 and 6 are presented the waveforms and the phase portraits in two operating regimes: fundamental periodic operation (period-1) and chaos, obtained by computer simulation.

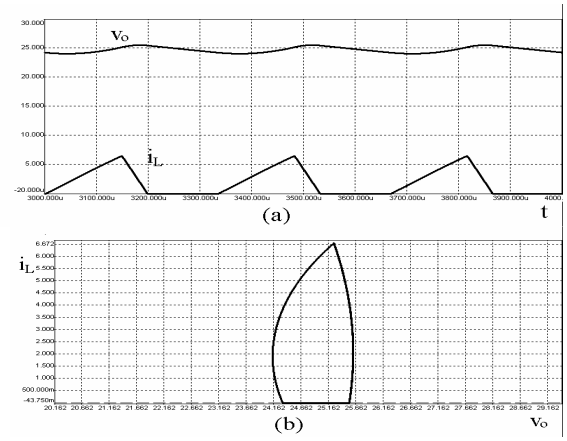

Fig. 5. (a) Fundamental waveforms (simulation results) for BUCK converter operating in DICM ,κ=0.1; (b) phase portrait.

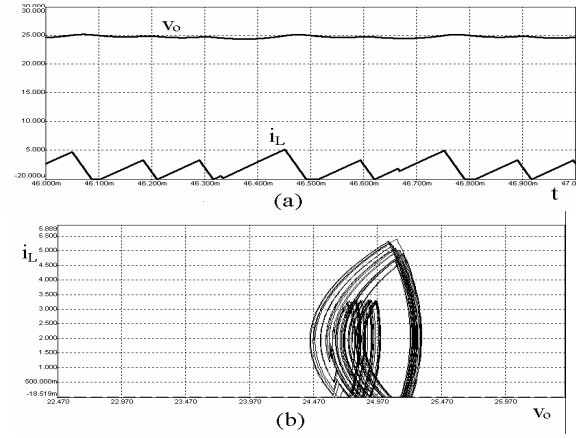

Fig. 6. (a) Chaotic operation waveforms (simulation results) for BUCK converter operating in DICM, κ=0.185; (b) phase portrait.

In Fig. 7 the analytical iterative map, given by Eqn. (21) is used to show the bifurcations of the converter. It can be observed that the system looses stability by period-doubling, and becomes chaotic when κ becomes larger that about 0.17.

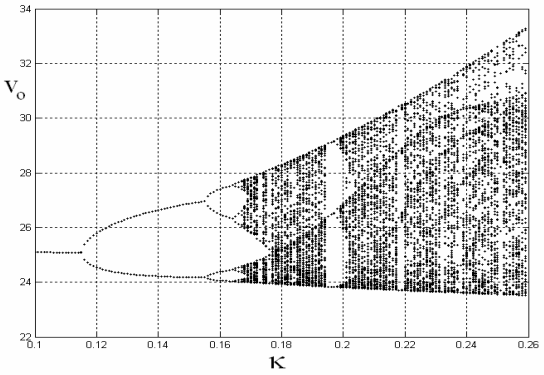

Fig. 7. Bifurcation diagram of the voltage-mode controlled BUCK converter operating in DICM.

The voltage-mode controlled BOOST converter, operating in DICM presents the same nonlinear behaviour [15].

C. *BUCK converter, current-mode control*

In this case, the control law is given by Eqn. (10). For current-mode controlled BUCK converter, in order to investigate the bifurcation phenomena, the following parameters are used: V_g = 5V, L = 2mH, f_s = 10kHz, R = 40Ω, C = 34μF, V_{ref} = 1.89V, I_{ref} = 0.2185A. In Fig. 8, 9, 10 are presented: the inductor current waveforms and the phase portraits in various operating regimes: fundamental periodic operation, period-2 subharmonic operation and chaos, obtained by computer simulation.

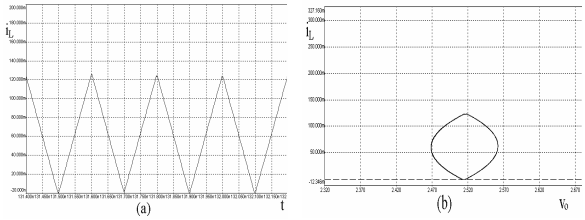

Fig. 8. (a) Fundamental waveform (simulation results) for current-mode controlled BUCK converter, κ=0.15; (b) phase portrait.

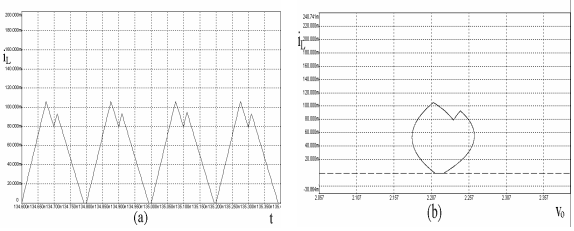

Fig. 9. (a) Period-2 subharmonic waveform (simulation results) for current-mode BUCK converter , κ=0.35; (b) phase portrait.

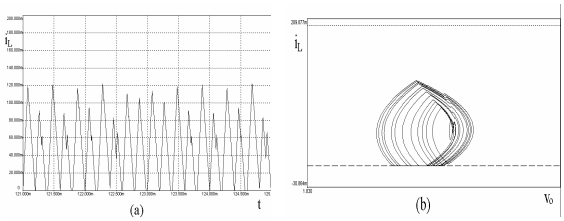

Fig. 10. (a) Chaos operation waveform (simulation results) for current-mode BUCK converter , κ=1.15; (b) phase portrait.

It can be observed that the circuit goes through 1-period operation, 2-period operation, and eventually exhibits chaos. A similar behaviour can be observed at the BOOST converter [2], [11].

D. *ĆUK converter, Discontinuous Capacitor Voltage Mode (DCVM) operation, voltage-mode control*

In this paper, the ĆUK converter (Fig. 11), operating in DCVM is studied. In order to investigate the occurence of the Hopf bifurcation, the following parameters are used: V_g = 15V, L_1=L_2 = 2.4mH, R = 10Ω, C_1=56.8μF C_2 = 47μF, f_s=20kHz.

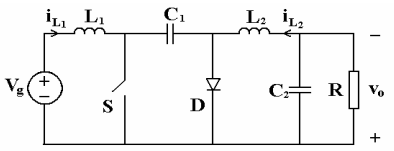

Fig. 11. The ĆUK converter.

The control law is given by (8). For this circuit parameters it is found that the critical value of the feedback gain, κ, is 0.816.

Computer simulations of the circuits show the bifurcation from fixed point (Fig. 12,a), through limit cycle (Fig. 12,b) and eventually to chaos (Fig. 12,c).

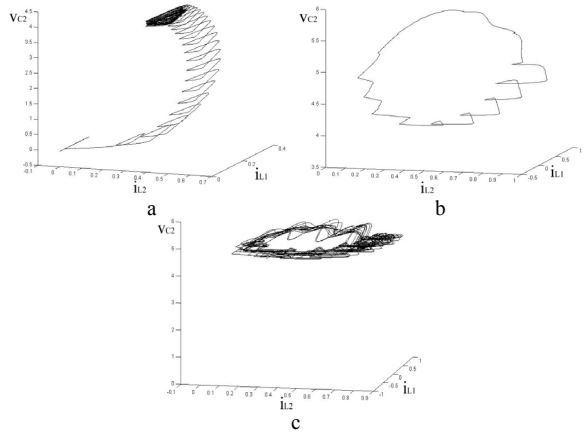

Fig. 12. The 3-d plots of the local trajectory for the DCVM ĆUK converter: a- the stable local trajectory for κ=0.1; b- the limit cycle (κ=0.816); c-chaotic orbit (κ=10).

In [2], [10] the Hopf bifurcation in the free-running ĆUK converter, operating in CCM, the boost converter with PWM voltage-mode control, and parallel boost converters is studied.

IV. CONCLUSIONS

The power electronics circuits, due to their nonlinearity, exhibits a variety of complex behaviour, such as: sudden change of operating regime, subharmonic and chaotic operation, etc. This behaviour can occur when some parameters of the circuit are varied. There are two reasons for studying nonlinear dynamics in the context of power electronics: to understand better the nonlinear behaviour of the power converters, and thereby avoid undesirable effects, or to deliberately use these effects, as shown in [19].

The nonlinear behaviour of some switching power converters is analysed in this paper.

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Comparison of LDA and RBF-NN in EEG Features Classification for Motor Imagery

Ştefan Cososchi[1], Rodica Strungaru[1], G. Mihaela Ungureanu[1]

Abstract – This paper presents an approach that uses self-organizing fuzzy neural network based time series prediction to extract the EEG features in time domain. EEG signals from two electrodes placed on the scalp over the motor cortex are predicted by a single fuzzy neural network. Features derived from the mean squared error of the predictions and from the mean squared of the predicted signals are extracted from EEG data within a sliding window using two auto-organizing fuzzy neural networks with multi inputs and a single output. The features are classified by linear discriminant analysis and radial-basis function neural network.
Keywords: EEG, neurofuzzy network, prediction, auto adaptation, LDA, RBF-NN

I. INTRODUCTION

Motor imagery is the mental simulation of a motor act that includes preparation for movement, passive observations of action and mental operations of motor representations implicitly or explicitly. Motor imagery as preparation for immediate movement likely involves the motor executive brain regions. Implicit mental operations of motor representations are considered to underlie cognitive functions. Another problem concerning neuro - imaging studies on motor imagery is that the performance of imagination is very difficult to control. The ability of an individual to control its EEG may enable him to communicate without being able to control their voluntary muscles. Communication based on EEG signals does not require neuromuscular control and the individuals who have neuromuscular disorders and who may have no more control over any of their conventional communication abilities may still be able to communicate through a direct brain-computer interface. A brain-computer interface replaces the use of nerves and muscles and the movements they produce with electrophysiological signals and is coupled with the hardware and software that translate those signals into physical actions. One of the most important components of a brain-computer interface is the EEG feature extraction procedure.

The Motor imagery is by far the commonest methodology employed by majority of BCI research groups. This can be attributed primarily to the 'purely cognitive' nature of these methods (as opposed to the requirement for a stimulus in BCIs based on P300 and steady state (SS) visually evoked EEG-potentials (VEP)). Motor imagery (like motor action) has been reported to produce an Event Related Desynchronization (ERD) [1]. This is characterized by a transient reduction in the power of the alpha and beta bands of the EEG. By cleverly employing different strategies for motor imagery, one can generate ERDs in different spatial locations overlying the bilateral motor homunculus. With proper training and motivation, majority of subjects can learn to control the intensities (and spatial location) of specific frequency bands in their EEG, which can then be used as a communication and control signal. A Canadian research group has studied the effect of mental imagery at the corticospinal level when hand movements are performed [2]. In their study, the influence of imitation of hand actions on the cortical level was analyzed. The hand movements were studied by an American research group which established that the specific cortical pattern associated with the variation of the motor control parameters during execution and imagery are the same [3]. Recently, the researchers have studied the interference between action observation and action execution [4], in order to contribute to the analysis of the observation, trying to explain the process by which the representation of an observed movement is converted into the representation of a goal-directed action. To analyze the EEG signals different methods have been proposed in the literature: autoregressive model [5], [6], neural networks [7], mixture of densities approach [8], independent component analysis [9], time-frequency analysis [10] and statistical methods [11]. The processing of the EEG within the motor imagery shows still opened directions. This year, the researchers have tried to elucidate the difference in processing the biological and non-biological movements in man [4], to detect the cognitive abilities of the unresponsive patients [12] and to improve the EEG analysis in the framework of motor imagery application [13]. Most studies have relied on subjective evaluation and not objective confirmation, of task performance. Motor

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imagery is a dynamic state in which a subject mentally simulates a given action. Our work presents a procedure for extracting features from the electroencephalogram (EEG) recorded from subjects involving motor imagery. Two auto-organizing fuzzy neural networks are used to perform prediction tasks for the EEG data, as proposed by Coyle and his coworkers [6]. Features are taken from the mean squared error in prediction and from the mean squared of the predicted signals. Linear analysis is used for classification of signals. This extraction procedure is tested offline on two subjects leading to classification accuracy rates near 83% with information transfer rates near 8 bits/min. This approach shows good potential for online feature extraction and autonomous system adaptation. The architecture of the two auto-organizing fuzzy neural networks is a network with multi inputs and single output. The use of auto-organizing fuzzy neural networks is convenient for applications because the auto-organizing fuzzy neural network can adapt itself to each individual's EEG signals so that very little subject specific knowledge or parameter selection is required. It can perform online learning thus has potential for continous learning and continuous adaptation to the dynamics of each individual's EEG signals. Chapter II of the paper presents the data configuration. Chapter III gives the results and some conclusions.

II. DATA CONFIGURATION

A. *Acquisition of EEG data*

The data is recorded from two subjects in a timed experimental recording procedure where the subject is instructed to imagine moving the left and right hand in accordance to a directional cue displayed on a monitor. In each recording session a number of EEG patterns correlated to the imagined right or left arm movement are produced by a subject over a number of trials. Recorded EEG signals are filtered between 0.5 and 30Hz and then are sampled at 120Hz [14].

B. *Configuration of EEG data*

The EEG data recorded from each electrode is configured so that the measurements from time instants t - 5 to t - 1 are used to make a prediction of the measurement at time t. Each training data input exemplar contains five measurements from the data recorded from either the C3 or C4 electrode. The training data output contains every subsequent measurement t from each of the input data vectors. The extracted input-output data vector for the time series at the electrodes C3 and C4 are in (1) and (2).

$$[c_3(t-5); c_3(t-4); c_3(t-3); c_3(t-2); c_3(t-1); c_3(t)] \quad (1)$$

$$[c_4(t-5); c_4(t-4); c_4(t-3); c_4(t-2); c_4(t-1); c_4(t)] \quad (2)$$

Every trial has 5 seconds of task related data. The data is recorded from two subjects, S1 and S2. There were 300 trials recorded for subject S1 and 300 trials recorded for subject S2, an equal number of trials for each type of movement imagery. Each trial consists of 600 samples (5 s x 120 Hz = 600). There are 595 training data pairs for each trial, samples 595 to 599 are used to predict the sample 600.

C. *Neurofuzzy architecture*

Two auto-organizing fuzzy neural networks are used to perform prediction. One auto-organizing fuzzy neural network is trained for the left EEG data and the other one auto-organizing fuzzy neural network for right EEG data. By using separate auto-organizing fuzzy neural networks for each type of data, it is desired that each trained auto-organizing fuzzy neural networks develop certain uniqueness, in that it is more apposite to each type of time series data [14].

The advantage of using a self-organizing structure, like that of the auto-organizing fuzzy neural networks, is that the problem of specifying the network's architecture does not have to be considered [15].

For the neural networks, finding the optimum architecture for a particular task can be very problematic and does have a significant effect on the performances. Auto-organizing fuzzy neural networks are hybrid systems that combine the theories of fuzzy logic and neural networks. In hybrid systems like the self-organizing fuzzy neural networks, the fuzzy techniques are used to create or improve certain aspects of the neural network's performance. An important advantage of the auto-organizing fuzzy neural network is the generation of a model from observations of complex systems where little insufficient expert knowledge is available to describe the behavior, as is the case for EEG data [16].

The auto-organizing fuzzy neural networks can deal with characteristics of EEG such as large dimensions and noise to provide a model that can be used for interpretation of the EEG. This is another advantage of using an auto-organizing fuzzy neural network for EEG analysis. The auto-organizing fuzzy neural network is designed to approximate a fuzzy process of fuzzy inference through the structure of neural network and thus create an interpretable hybrid model of neural network using the superior learning ability of neural networks and easy interpretability of fuzzy systems.

The dynamic adaptation of the structure of the hybrid network captures the underlying behavior of a nonlinear time-varying complex system more easily and accurately. The online learning algorithm, based on a hybrid recursive least squares estimator, and an autonomous neuron adding and pruning structure based on the optimal brain surgeon technique, provide a truly online learning algorithm for modeling/predicting the highly non-stationary EEG signal [14].

D. *EEG features extraction procedure*

Each self-organizing fuzzy neural network is a multi-input-single-output (MISO) network so only EEG data recorded from a single electrode can be predicted. The system is configured in three stages [14]. The first stage involves training of the two auto-organizing fuzzy neural networks separately to perform one-step-ahead prediction, using five previous measurements of each time series. The two auto-organizing fuzzy neural networks are named *L* for the left data-electrode C3 and *R* for right data electrode C4 corresponding to the type of EEG data on which they are trained, either left or right motor imagery. The second stage implies input of each type of training data, the same data used to train the auto-organizing fuzzy neural networks into each of the auto-organizing fuzzy neural networks. All the *L* training data is input to both the *L* and *R* networks, then all the *R* training data is input to both *L* and *R* network in a similar manner. Each auto-organizing fuzzy neural network provides a one-step-ahead prediction for the data in for each trial. When a trial is input to all of the two auto-organizing fuzzy neural networks, features are extracted by calculating the mean square error (MSE) of the prediction for a portion of the trial and the mean squared of the actual prediction (MSA). As these calculations gives predictions over a segment to a scalar value, EEG features based on the error and on predicted signal can be obtained as in (3).

$$f_k = \frac{1}{M}\left(\sum_{t=1}^{M} \left(y(t) - \hat{y}_k(t) \right)^2 + \sum_{t=1}^{M} \left(\hat{y}_k(t) \right)^2 \right) \qquad (3)$$

Equation (3) is used for obtaining each feature, where $y(t)$ is the actual signal and $\hat{y}_k$ (t) is the predicted signal. The *k* index is used to show whether the signal is from left *l* or right *r* auto-organizing fuzzy neural network. *M* is the number of prediction samples used. The extracted features are in vector form, the feature vector f_v, is shown in Fig. 1.

For each trial a two elements feature vector is obtained and classes of features for right and left data can be obtained by entering all trials of training data into the auto-organizing fuzzy neural networks in Fig. 1. Normalizing the features (i.e. dividing each feature vector by the sum of the components within the vector) can reduce the intra class variance – a fundamental goal of any feature extraction procedure. Features can be extracted for every time point in a trial using a sliding window approach. To extract a new set of features for every time point in a trial using the sliding window approach, *t* ranges from *t* = *s* to *M* where *s* and *M* are incremented before the next set of features is extracted (initially *s* = 1 and *M* = window size). This means that data at the beginning of a trial is forgotten as the window slides away from the start of the trial. The advantage of using the sliding window for feature extraction is that the feature extraction procedure does not require knowledge about the point at which communication is initiated by the user and so online feature extraction can be realized [14].

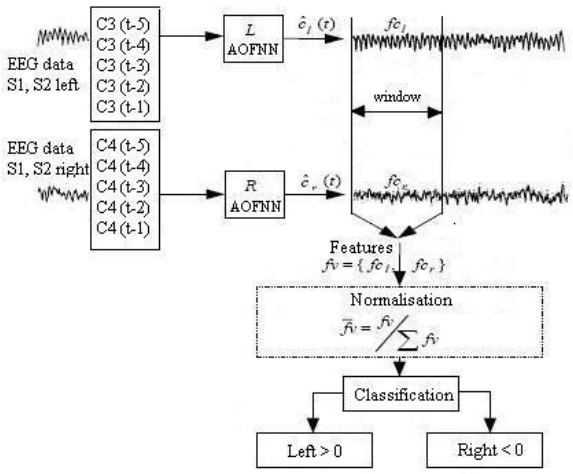

Fig. 1. EEG feature extraction procedure

III. DATA CLASSIFICATION

The last step is the data classification performed using linear discriminant analysis (LDA), a classifier that works on the assumption that different classes of features can be separated linearly and alternatively using radial basis function network (RBF-NN) that uses a nonlinear function to map the input data into high-dimension space so that they are more likely to be linearly separable than in the low-dimension space.

A. *Linear discriminant analysis*

The principle of LDA is to seek a vector *w* so that two projected clusters of *R* and *L* feature vectors can be well separated from each other while keeping small variance of each cluster. This can be done by maximizing the Fisher's criterion. After *w* is obtained by means of the training data, we project the test samples on it, and then classify the projected points by the k-nearest-neighbor decision rule [17]. Linear classifiers are more reliable than the nonlinear ones because they have limited flexibility.

The idea of LDA is to seek a vector $\vec{w}$ so that two projected clusters of *R* and *L* feature vectors on $\vec{w}$ can be well separated from each other while keeping small variance of each cluster. This can be done by maximizing the Fisher's criterion

$$J(w) = \frac{w' S_b w}{w S_w w} \qquad (4)$$

where S_b is the scatter matrix between classes:

$$S_b = (m_R - m_L)(m_R - m_L)^{\mathrm{T}} \qquad (5)$$

and S_w is the scatter matrix within the class:

$$S_w = \sum_{\vec{x}\in \mathrm{R}} (\vec{x} - m_R)(\vec{x} - m_R)^{\mathrm{T}} + \\ + \sum_{\vec{x}\in \mathrm{L}} (\vec{x} - m_L)(\vec{x} - m_L)^{\mathrm{T}} \quad (6)$$

in which two summations run over all the training samples of classes R and L , respectively, and m_R and m_L represent the group mean of classes R and L, respectively. The optimal $\vec{w}$ is the eigenvector corresponding to the largest eigenvalue of $S_w^{-1} S_b$. After $\vec{w}$ is obtained by means of the training data. Experimentation involved extraction and classification of features at every time point in a trial, allowing selection of the optimum time points to perform feature extraction and classification for more effective deployment of the system. This approach allows features to be extracted at the rate of the sampling interval [14].

B. *Radial - basis function neural networks*

The radial - basis function neural network (RBF-NN) uses a nonlinear function to map the input data into high-dimension space so that they are more likely to be linearly separable than in the low-dimension space, as depicted in Fig. 2.

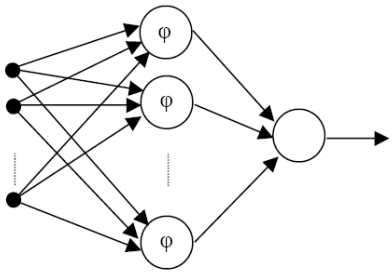

Fig. 2. RBF-NN architecture

The hierarchy of RBF-NN consists of one input layer, one hidden layer, and one output layer. Each RBF-NN is designed to have a nonlinear transformation from the input layer to the hidden layer, followed by a linear mapping from the hidden layer to the output layer. The mapping between the input and output space is expressed by:

$$F(\vec{x}) = \sum w_i \varphi(\|\vec{x} - \vec{x}_i\|) \quad (7)$$

where $\varphi(\|\vec{x} - \vec{x}_i\|) = e^{-\|\vec{x}-\vec{x}_i\|^2}$ and w_i is the weighting from the *i*-th hidden neuron to output neuron and $\vec{x}_i$ represents the *i*-th known feature vector with dimension *N*.

Compared with other neural networks which uses gradient-based optimization process to estimate the weightings, for example, the back-propagation recurrent neural network, the RBF-NN solve for a set of linear equations to avoid trapping in a local minimum and greatly reduce the training time [17].

IV. RESULTS AND CONCLUSIONS

A. *Results*

The system was tested on 150 for subject S1 and 150 for subject S2. The obtained results are shown in Table 1 and Table 2.

The first column specifies the subject. The second column specifies whether normalized features where used. Column three specifies the sliding window size. Column four indicates classification accuracy rate for LDA in Table 1 and respectively for RBF-NN in Table 2. Column five shows the time elapsed for classification and column six shows the information transfer (IT) rates.

All results in bold specify the best results obtained for each type of performance quantifier. All IT rates were calculated using the time interval between communication start meaning the second 4 of timing scheme and the point that maximum classification accuracy was obtained. This provides good indication about the maximum IT rate a system can achieve whilst system accuracy is optimal. IT rates can be much higher if calculated in the first second of a trial, even if classification accuracy is lower.

Irregular transients in the signals, caused by noise or artifacts did not have as much affect on the features because the auto-organizing fuzzy neural networks did not predict irregular transients in the signal that indicates that the auto-organizing fuzzy neural networks aided to the removal of artifacts and noise for subjects S1 and S2. Normalizing the features produces higher classification accuracy and IT rates that is because normalization reduces the intra-class variability. The number of neurons in each auto-organizing fuzzy neural network was different from its counterparts due to variations in the types of signals on which each auto-organizing fuzzy neural network was trained.

Table 1

Sub	Norm	Wind Size	Classif Acc [%] LDA	Time [s]	Rate [bpm]
S1	No	310	76.34	3.43	6.89
	Yes	320	**82.68**	3.62	7.27
S2	No	300	70.63	**3.24**	6.43
	Yes	340	79.87	4.13	**7.68**

Table 2

Sub	Norm	Wind Size	Classif Acc [%] RBF-NN	Time [s]	Rate [bpm]
S1	No	310	73.54	3.46	6.56
	Yes	320	**84.21**	3.57	7.75
S2	No	300	68.67	**3.28**	6.32
	Yes	340	81.28	3.98	**8.12**

B. *Conclusions*

No artifact removal or noise reduction was carried out on the raw EEG data from subjects. This indicates the robustness of the proposed approach. However, the number of neurons in each auto-organizing fuzzy neural network increases when noise is increased. This approach shows good potential for online EEG feature extraction and can be further developed by implementing a multiple-step-ahead prediction technique. The system can perform online adaptation because it can autonomously add neurons to accommodate to the variations in the EEG data.

RBF-NN performs a better classification of the extracted features in comparison with LDA, due to the nonlinear function used for the hidden layer.

Further studies will investigate the success of the proposed algorithms on different motor imagery tasks and will look for other methods to improve the classification of the extracted features.

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Data structures for industrial laser range sensors

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Abstract – This paper describes the implementation of data structures based on data acquisition of active optical range sensors. At first, three available industrial laser sensors are introduced and compared exemplarily. Based on the raw data structure of these sensors an abstract data structure and the possibility of the evaluation of depth information are presented. Finally industrial applications are presented which are using the introduced data structure.
Keywords: laser range sensors, 3D models, data representations

I. INTRODUCTION

The evaluation of depth information from different sources is a very popular field of research in the data processing. Many lines of business and sciences, such as the automobile industry, medicine and physics are interested and involved in it. The difficulty consists in transferring point data sets to a reliable order so that it is possible to make evaluations over created surfaces.
Such datasets have a number of different sources: they range from a simple distance measuring system to complex 3D scanners for any-sized objects. These data structures could be used starting with simple counting tasks up to complex 3D registration and reconstruction algorithms of modern image processing [1][2].
This paper describes laser sensors in industrial environments which exist in different types of constructions. Especially laser sensors are introduced in detail in the following chapter. With the help of practically proven sensors a data structure for the representation in the computer is defined. It is easy to understand that these sensors are generating different types of information depending on manufacturer and on the functional principle. The next chapter describes usual operation modes of contactless optical sensors. Various laser sensors from industrial component suppliers will be evaluated to generate an abstract data model from their data acquisition methods.

II. Industrial Laser range sensors

Many different 3D Scanning sensors are presently existing in the market [3]. This selection consists of sensor devices usually used in the automation and robotic industry.

A. SICK LMS 400

The company Sick [4] is one of the world's leading producers of sensors for all sorts of industrial applications. The measuring principle of the LMS400 is based on the so called Time of Flight method with an additional phase difference analysis. The propagation time of the light and the used wavelength result in a phase shift between the beam sent and the beam received. This phase difference is converted into a frequency. The system determines the distance between the object and the zero point based on this frequency. The sensor is a 2D measuring system sending out and receiving laser beams in an angle of 70°.

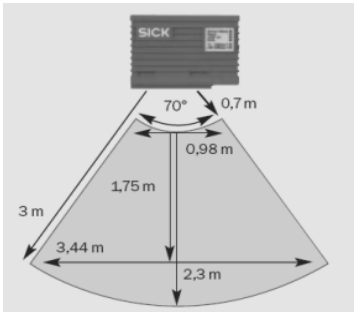

Figure 1 Sick LMS200 measurement range [4]

The laser measuring system LMS 400 is based on the LMS 200 and was developed for close ranges up to 3 meters. The LMS 400 has a distance resolution of 1 millimeters at a maximum measuring distance of 3 meters. Additional remission values are also transmitted. The measured sensor data is provided to a PC via Ethernet.

Table 1 Sick LMS400 Technical Specifications [4]

Measurement range (Z)	700-3000	mm
Accuracy (Z)	1	mm
Measurement range (X)	< 70	°
Sample Frequency	250 Hz	1/s

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The typical angular resolution at 250 Hz is 0.1°. Lower sample frequencies slow down the measurement process. The measurement range starts with at 700 millimeters and has a constant resolution of 1 millimeters over the complete measurement range [5]. At a maximum usage of the angular range of 70° the lowest angular resolution of 0.1° yields an area of 700 values (in X).

B. MEL M2D 75/30

The M2D from MEL [6] works according to the principle of triangulation. A pulsed laser diode and the line optics produce a laser line. The diffused reflecting light of the object is detected by a Charge-coupled Device array (CCD).

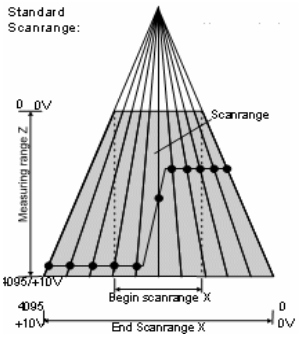

Figure 2 scan range of MEL M2D 75/30

The object's different height contours cause a deviation of the laser line which is evaluated trigonometrically. The distance of the Z axis is allocated to the respective X position of the sampling point. The profile of the sensor profile can be achieved as a representation of Z(X).

Table 2 MEL M2D 75/30 [6]

Measurement range (Z)	90-165	mm
Accuracy (Z)	0.16	mm
Measurement range (X)	30	mm
Sample Frequency	110	1/s

At a measurement range of 30 millimeters (in X) the sensor 75/30 has a resolution of 0.1 millimeters. In the measurement range of 75-90 millimeters the resolution is 0.16 millimeters. The sensor works with a sample frequency of 55Hz in the full screen mode (566 lines) and 110Hz in the half resolution mode (283 lines).

C. MicroEpsilon ScanCONTROL 2800

The laser sensor ScanCONTROL 2800 from MicroEpsilon [7] uses the triangulation principle for the two-dimensional recording of profiles. A laser line is projected onto the object. High-quality optics maps the light of this diffusely reflected laser line to a Complementary Metal Oxide Semiconductor (CMOS) matrix. The controller calculates the distance information (Z axis) along the laser line (x-axis) and distributes both in a two-dimensional coordinate system. ScanCONTROL 2800 consists of a compact sensor and an intelligent controller which distributes the two-dimensional profile information and sends it via FireWire interface to the PC.

Table 3 MicroEpsilon ScanCONTROL 2800 25X [7]

Measurement range (Z)	62.5 – 87.5	mm
Accuracy (Z)	0,01	mm
Measurement range (X)	1000	Points
Sample Frequency	< 1000	1/s

Like other sensors the ScanCONTROL 2800 is able to work with higher speed and higher precision at a measurement range of 25 millimeters. The sensor resolution of 0.01 millimeters depends on the scan frequency. Test scans were taken with a resolution of 1000 points and 95Hz.

III. Sensor data acquisition

Depending on an industrial application of the sensors different measurement ranges have to be selected. Therefore a direct comparison of the properties is hardly possible. The choice of the measurement range rather plays a subordinate role for the data representation described in this paper. Distance sensors produce simple distance values representing the z coordinate of a Cartesian coordinate system in a fixed relation to the sensor. For a 2D laser range sensor the results are represented in the X Z plane.
The laser triangulation sensor M2D 75/30 of MEL delivers linearized data in x and z with values between 0 and 4095 (figure 2). The intensity value ranges from 0 to 254. These values have to be scaled depending on the sensor measurement range. The measurement range for MEL M2D 75/30 is defined for x values between -20 and 20 millimeters (end scan range is 40 millimeters) and for z values between 90 and 165 millimeters. The values are transferred directly into a coordinate system, which is shown in figure 3 based for X and Z in millimeters.

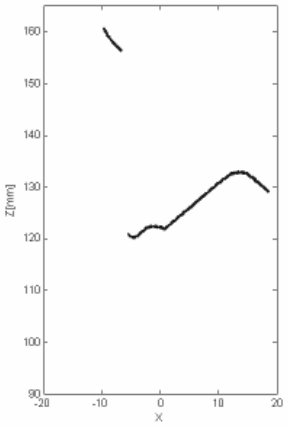

Figure 3 MEL M2D 75/30 laser scan

The Sick LMS400 uses the principle of phase shift (continuous wave). The packages with the measured values are transferred in an Ethernet telegram to a PC. The most important values of this telegram are the start angle (4 bytes) and 2 bytes for the angle step width. For every angle step the distance is encoded in 2 bytes. These distances have to be multiplied by the transferred scaling factor to scale the value to millimeter range. The remission values are transferred for every angle step to values between 0 and 255. The value of 255 correlates with a full reflection.
The linearized distance d is a result of this relation:

$$\mathrm{d} = d'\cos(\varphi_{Start} + \Delta\varphi) \qquad (4)$$

In this way the test scans can be compared to other scans. A height profile of the Sick LMS400 is presented in figure 4.

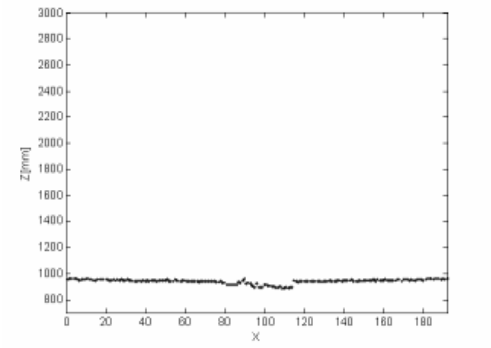

Figure 4 Sick LMS400 laser scan

This profile was produced with an angular resolution of 0.125° for a scanning part of 24°. The distance measuring range starts at 0.7 meters and goes up to 3 meters. In this case the surface of a slightly deformed object has been scanned in a distance of approximately 1 meter.
Concerning the format of the data transmission the ScanCONTROL 2800 is not fundamentally different from the other sensors. A special byte array is transferred by Firewire and can be stored with a driver function. This byte array is predefined by a certain data structure (PURE_PROFILE). The data structure consists of 4 bytes per scan value. The first 2 bytes contain the X value and the next 2 bytes the corresponding Z value (distance to X). This very similar order of the data can be visualized in an X-Z plane. In the figure 5 a laser scan of 1000 Points was scaled to the measurement range of 40 millimeters in order to compare it with the MEL M2D 75/30 scan.

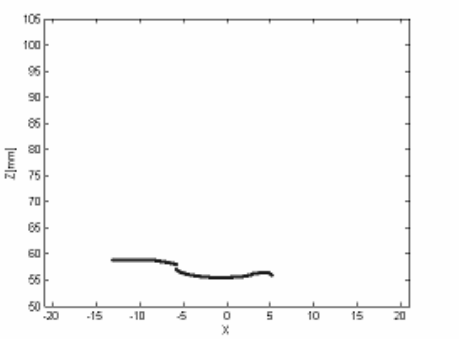

Figure 5 MicroEpsilon ScanControll 2800 25X laser scan

All these sensors provide a scan profile in the X Z plane. With the help of a linear movement of the sensor in Y direction over an object three-dimensional data can be generated. Besides local information of the single scan points the intensity values could possibly help to identify properties of the surface. The intensity values of the points are often used for filtration of the point clouds and for the detection of faulty points. To increase the accuracy of the scans the measurement rates often have to be decreased. If possible, the distance between the object and the sensor has to be reduced.

IV. Data representation

A general range image consists of a simple net of points. The smallest part of a 3D scan is a scan point. This abstraction has the advantage that the representation of the sensor data is completely independent of the selected laser sensor. The most important advantage of laser range sensors is that the values of the Z axis can be directly equated with the distance (e.g. in millimeters). Additionally an intensity value can be assigned to every point of most sensors scaled between 0 an 1. Concerning the introduced 2D sensors the X values are given by the resolution and the provided measurement range. Results for every point in a height profile are defined in the following way:

$$\mathrm{P} = (\mathrm{X}, \mathrm{Y}, \mathrm{Z}, \mathrm{I}) . \qquad (5)$$

A scan point differs from a height profile only due to the missing Y coordinate. The missing information for the Y coordinate of a laser line can only be assigned with the help external sources like robot axis and incremental encoders. The intensity value of the unordered point clouds is often not included in the point representation (computer graphics). All introduced sensors always take complete height profiles. In the data structure this is reflected by a point list.

$$\mathrm{L} = \{\mathrm{P1}, \mathrm{P2}, ...\mathrm{Pn}\} . \qquad (6)$$

The list of points sorted by X coordinate includes exactly the number of entries n according to the resolution of the sensor. It is possible to assign an Y value independently to every point. In the simplest case Y will increment if the sensor is orthogonally moved to the X Z plane. The movement in the Y-direction is possible with an independent resolution. In this case the Y coordinate is equal in the data structure for each laser line. A 3D range image is constructed with a sequential storage of laser lines. The range image

$$H = \{L1, L2, ...Ln\} \quad (7)$$

consists of a list of laser stripes ordered by the Y coordinate. Every range image is a list of laser lines, in which the number of laser lines is different. The data structure of a range image will contain an ordered point list, if the sensor is moved orthogonally in Y- direction.

There are well known data structures in the computer graphics sciences for 3d range images. The most general and often used data structure is the storage of unordered point clouds. The main goal of many algorithms in computer graphics is the reconstruction of surfaces from given point clouds. The data structure described above is a specialization of the generally used point cloud definition. For further interpretations also methods for unstructured point clouds can be used.

The data structures are implemented in object-oriented C++ classes. An Unified Modeling Language (UML) notation for this data structure is shown in diagram 6.

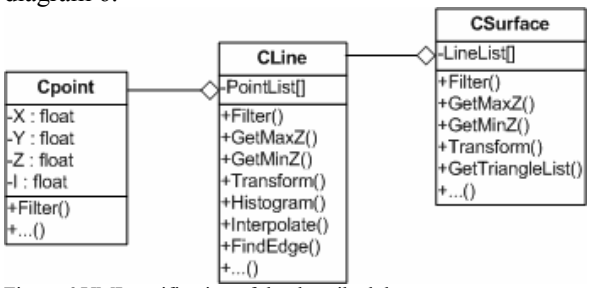

Figure 6 UML notification of the described data structure

Besides the described properties of a scan point it is for example possible to implement a filter function. With the help this filter function the point values can be checked with a threshold analysis in order to determine if this point is valid. Apart from this functions element operators are provided for comparisons between points, lines and surfaces (not included in the diagram). The laser lines contain a list of the points represented in the class "CLine". General functions are filtration, histogram creation, transformations, min/max and regression functions. Depending on application the class has the possibility to implement other methods. Concerning the parameterization of the laser line different interpolation methods can be implemented [16]. The implementation of the range images in the class "CSurface" also contains usual methods for the transformation and filtration mentioned above. The most common use cases are methods for surface reconstruction. There are several approaches like Delaunay triangulation [8], spline based algorithms which are used in different fields of application [16][10]. Also registration methods like the iterative closest points (ICP) algorithms [9] could be easily implemented.

V. Industrial Applications

The data representations for laser scans have the advantage that there are already ordered data structures existing which can be evaluated. Due to the stored intensity a point can be validated and verified with the help of a class method.

It is possible to develop different evaluations on a laser line. These line interpretations strongly depends on the application. Some applications in the industrial image processing were shown in this section. Many of them profit from the introduced data structure.

In the automobile industry robots are often used in the production lines. The precision of robots is mostly sufficient. But if the work piece has an alternating position, the process can not be permanently repeated. Usually the position of the work piece related to the robot position has to be determined very exactly. In order to solve this problem it is possible to use distance sensors providing characteristic points of the work piece. The line sensors recognize a laser line contour. With the help of this contour an edge point has to be extracted. This edge can be used to determine the position and orientation of the robot tool later on. The calculation of the edge coordinates based on regressions and contour extraction. In different range image applications many further methods belong to 2D Template Matching [11][12] [13]. Data structures for 3D surfaces arise from moving 2D sensors but also from 3D distance sensors [14]. Most applications [15] are using line sensors which are moved on external axes. An classic industrial application for laser range sensors is the measuring of volumes and geometries of (endless) production lines. In the automobile industry the geometry and volume of the sealing mass of car windows is checked with the help of laser range sensors, directly after they have been applied by the corresponding device. One example which uses the introduced data structure is shown in figure 7.

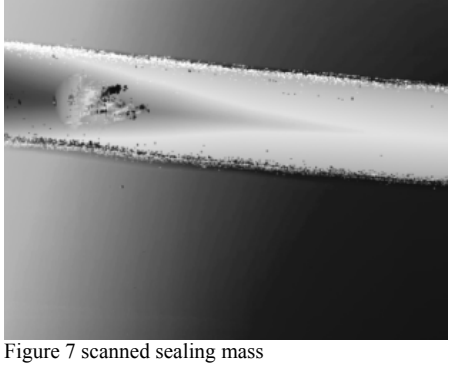

Figure 7 scanned sealing mass

During the scan the complete applied sealing mass is evaluated. With the help of a simple integration the volume of the applied mass is determined. A further application can be seen in figure 8.

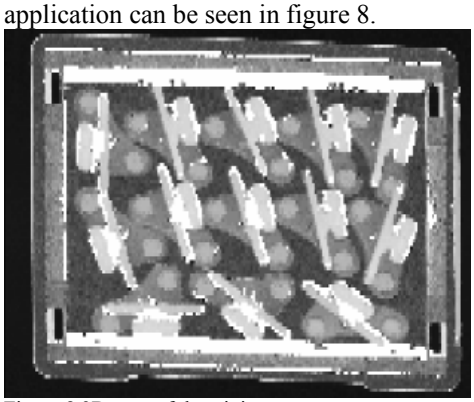

Figure 8 3D scan of door joints

Single door joints are represented in a box. In this picture the grey value always corresponds to the direct distance between the objects and the sensor. In order to achieve this, the Sick LMS 400 was moved linearly with a robot. Based on this distance information the positions of the parts are determined by 3D matching with CAD models.
Another application for the ScanControl2800 can be seen in figure 9.

Figure 9 3D profile of tire identification

With the help of a three dimensional scan the identifications on a car tire shall be verified with character recognition. Due to the different illuminations and low height of the identification the reconnaissance is very difficult for a conventional image processing. The ScanControl2800 is suitable for this task, because high resolution is needed. For the evaluation the height information is converted to grey values comparable to figure 9. The grey scaled pictures are transmitted to known optical character recognition systems (OCR).

VI. Conclusion

Common laser range sensors as described above provide metric calibrated sensor data in a two dimensional measurement field. The introduced data structures in this paper were defined by this sensor data. The data structures are implemented hierarchically as classes in C++. It is important for industrial applications to make implementations of different evaluations very simple and useable; therefore the data representation has to be efficient too.

The described data structures are used successfully in many applications and are more and more improved continuously.

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DEIC: Web-Based Materials to Teach Digital Electronics

Gabriel Oltean[1], Ioana Oltean[2], and Sorin Hintea[1]

Abstract – The paper describes a Web-based Digital Electronics Interactive Course (DEIC). DEIC transmits knowledge to the students by means of static text, figures, tables, and by interactive simulation of some digital circuits. It also offers different kinds of interactive tests with prompt feedback for self-assessment. Students' surveys show that they found the software easy to use and felt it helped them improve their skills and understanding.

Keywords: computer-based learning, digital electronics, self-assessment, interactive simulation

I. INTRODUCTION

In our days, technology is everywhere. Since the early days of computers, learning through computer-based environments has dramatically increased [1]. Students and teachers now expect their educational experience to include the use of current Web technologies and engaging learning interactivity. Web-based simulations, Web-based classrooms, and Web-based tools can provide a dramatic benefit for teaching and learning.

All this activities are possible since we have ubiquitous personal computers with Web access and Web browsers. We will be able to do better things, to provide students with deep learning; we will be able to move beyond the limitations of a traditional classroom since we have now access to learning opportunities such as:

- interactive course materials;
- simulations, multimedia, visualization;
- homework and quizzes.

In addition we can access this features any time and any place, since they involve site-independent learning (distance education) – through courses that are delivered largely or entirely online.

Deep learning may be facilitated by interactive simulation; static text-based information may serve as enrichment or preclass assignment; and a video-on-demand presentation could be a postclass reinforcement activity.

As this development becomes more of a reality, we will need to redefine existing educational pedagogy, commonly accepted learning theories, and the role of the professor, which have all driven our traditional education delivery system. These changes will involve, among other things, a major shift in pedagogy from a teacher-lectured-centered environment to a learner-centered/learning-style environment [2].

In recent years, there have been important changes in education, both in terms of curriculum content (what is taught) and in the delivery of material (how it is taught) [1].

The prestigious IEEE Transactions on Education magazine devoted in 2005 a special issue on Web-Based Instruction containing no less than 25 papers.

A Web-based educational tool for digital signal processing tools is described in [1]. In addition, the paper presents an exploratory study about the improvement and validation of this tool. An adaptive testing system that generates tests for assessment that are tailored to each student appears in [3]. A discussion of the author's use of WebCT environment to deliver a sophomore Electric Circuit Theory Course to undergraduate students at the Texas A&M University, College Station campus is presented in [4]. The OASIS tool containing a large question database and server-side program that delivers questions, marks student responses provides prompt feedback, and records students' activities was developed and implemented in the University of Auckland, New Zeeland [5].

Textbooks had traditionally been the fundamental tools for the Digital Electronics course, so the learning process was somehow static and inefficient. The need was great for developing and delivering quality, up-to-date educational material based on new technology and associated pedagogical advantages, such as interactivity, enjoinment and instantaneous feedback.

The result of a collaborative work between the Bases of Electronics Department of the Technical University of Cluj-Napoca and the "Edmond Nicolau" Electrotehnic Group School of Cluj-Napoca, consists of a Web-based Digital Electronics Interactive Course – DEIC. DEIC transmits knowledge by means of static text, figures, tables and data sheets and by the possibility to simulate the operation principles of digital circuits. It also offers the self-assessment

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possibility; different types of tests that provide prompt feedback to the learners being available.

II. DEIC – DIGITAL ELECTRONICS INTERACTIVE COURSE

The Digital Electronics Interactive Course (DEIC) has been designed using the HTML language and Java and JavaScript languages (Fig. 1). It can be run in an internet browser being adequate for use in traditional classrooms or in asynchronous and non-eyewitness active self learning courses to engage students in active reinforcement of the concepts acquired in class.

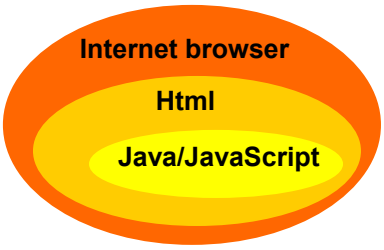

Fig. 1. The DEIC structure

A. *The DEIC content*

The course deals with active and interactive study of logic gates, combinational circuits, and sequential circuits. The course Web page allows the instructor to make available all course-related materials in a very accessible way. Table 1 shows a synthesis of all materials and their available format. Some material is in .pdf format for easy downloading and printing.

In general, for each topic the learner can access the following materials: theoretical aspects, experiment, data sheets of the discussed integrated circuits, a number of proposed problems as assignment, test for knowledge reinforcement and/or self assessment, and working sheets.

The chapter of logic gates contains the following types of gates: OR, AND, NOT, NOR, NAND, and XOR. The decoders, multiplexers, demultiplexers, adders, and magnitude comparators are presented in the chapter of combinational circuits. The sequential circuits chapter treats the flip-flops (RS, JK, and D), counters, and registers.

Table 1

The theoretical aspects are introduced through the medium of static text, circuit symbols, truth tables, waveforms, and datasheets. The learners are welcome to run attractive experiments by simulation. To facilitate the comprehension of the circuits operation, these experiments highlight the operating principle of the studied devices eliminating the details and second order effects. They are interactive applications: the mouse action on graphical element leads to modification in color of some graphical elements or in the appearance of new graphical elements.

A very useful tool in the learning process is the interactive assessment test. This kind of test is primarily appreciated for its prompt response on the correctness of the answers provided by the learner. The waiting time and the involvement of a teacher to check the answers, specific to traditional tests on paper are fully eliminated.

DEIC proposes a diversified spectrum of tests:

- closed evaluative questions and answers tests, specific to computer-based assessment [6]:
  - tests with multiple choosing items where the learner chooses a correct answer from the proposed ones for each question or utterance. Two versions are implemented in DEIC: 1) all items of the test are available scrolling the display, with the possibility to return to a previously solved item to change the initial answer, and 2) each item of the test is individually presented with no possibility to return to a previous item;
  - tests with alternating answers items containing statements that have to be appreciated as being true of false, with no possibility to return to a previous item;
- opened evaluative questions and answers tests:
  - filling gap tests; that kind of test being among the very few kind of tests that admits a quick and objective control.

B. *The graphical user interface*

The graphical user interfaces of DEIC look like the one presented in Fig. 2. The title window allows the user to browse all the DEIC content, the window being present in all the application screens. For instance, the user can select one chapter to be studied. According to the selected chapter, the corresponding hyperlinks are displayed in the content window: sub-chapters, interactive tests, proposed exercises and problems, respectively working sheets (last ones only

	Theoretical aspects		Experiment	Test		Proposed problems		Data sheet		Working sheet
	pdf	html	java	pdf	Java/JS	pdf	html	pdf	html	pdf
Logic gates	X	X	X	X	X	X	X	X	X	X
Combinational circuits	X	X	X							X
Sequential circuits	X	X	X							X

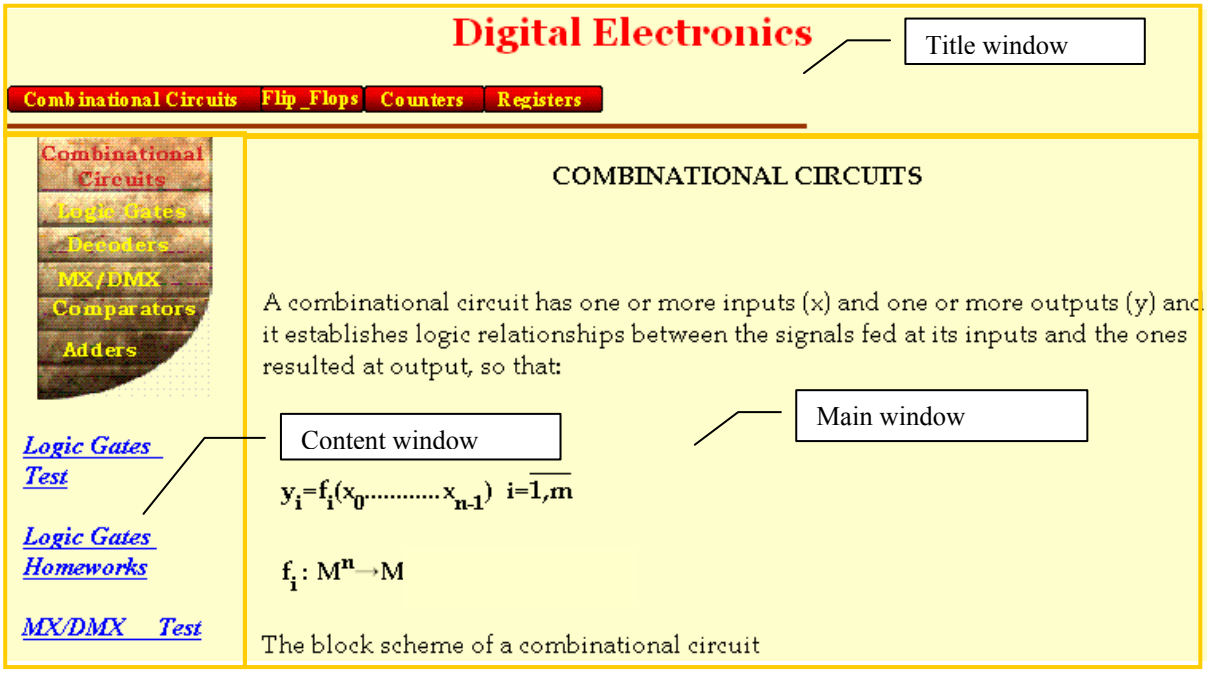

Fig.2. The graphical user interface of DEIC

in .pdf format). The experiments, tests, and theoretical aspects are displayed in the main window.

C. *A lesson in DEIC*

For the illustration purpose we will present in the following the *RS* flip-flop lesson in the flip-flops chapter.

The lesson can be efficiently learned using its associated working sheet. In the case of *RS* flip-flop the learner is invited as a first step to study the theoretical aspects (circuit symbol, description of the operation, truth table), as one can see in Fig. 3.

At the second step, the learner has to fill in the working sheet with experimental results, obtained by simulating the behavior of a *RS* flip-flop. Fig. 4 shows

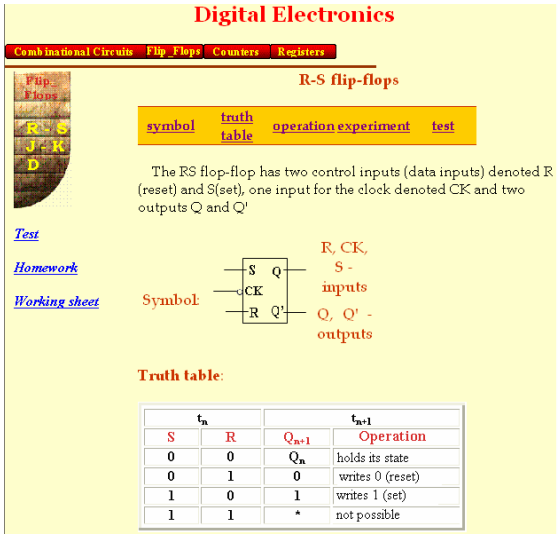

Fig. 3. The screen of the RS flip-flop lesson

the Java applet used for simulation. The *R*, *S* and *T* (clock) inputs are sensitive to the mouse action. The logic state of any input can be altered by a mouse click on the corresponding green circle. The current logic state is written inside of that circle. For an efficient graphical communication, the yellow color is used to represent the *logic 0* state, while the red color is used to represent the *logic 1* state at the output. As a special case we used the mauve color at the output in the case when the forbidden state is present at the input (*R*=*S*=1).

According to the combination of logic states presented at the input, the output of the flip-flop keeps its previous logic state or changes its logic states (and implicitly the color of the graphical components representing the outputs) by clicking the *T* input. Simultaneously, some waveforms representing the time evolution of the inputs and output will be drawn

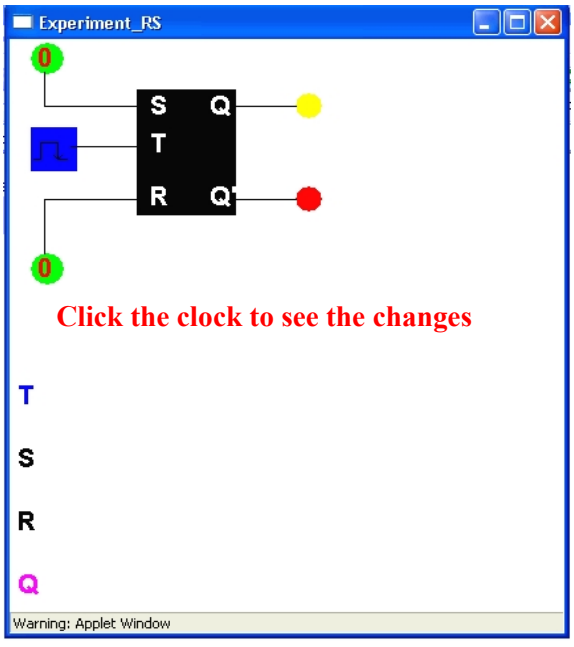

Fig.4. The window to simulate the *RS* flip-flop

in the same window (see Fig. 5). All these events happen synchronous with the action of a mouse click on the clock input (*T*), signifying the apparition of a

falling active edge of the clock signal. Each action on the *T* input is equivalent with a clock period.

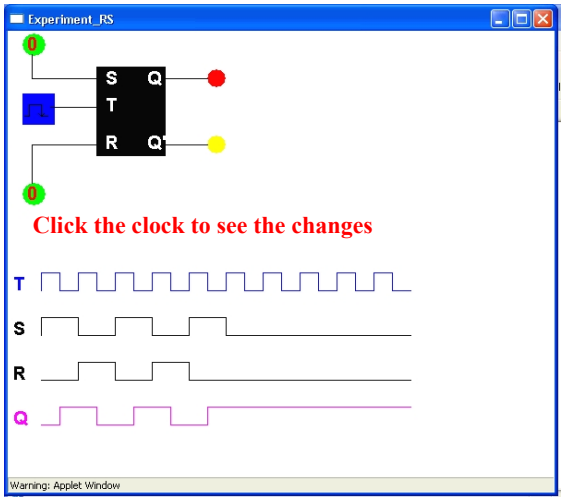

Fig. 5. Operation of the *RS* flip-flop. Waveforms.

The third step in the working sheet requires running the simulation and completing the waveforms at the *Q* output for specified inputs waveforms. The final step in the working sheet asks the learner for a text description of the *RS* flip-flop operation.

The features, the absolute maximum rating, the electrical characteristics, and the connection diagrams of the integrated circuits complete the picture on the real behavior of the circuits.

One proposed test for consolidation and deepening the knowledge is the one with multiple choosing items, containing 10 items. This test was implemented as a Java application. One single question is displayed on a certain time (Fig. 6.), the learner having the possibility to choose the correct answer. Once a question is solved and one passes to the next one there is no possibility to return to a previous question. To the end of the test, the number of correct answers is displayed. At every new running of the same test the

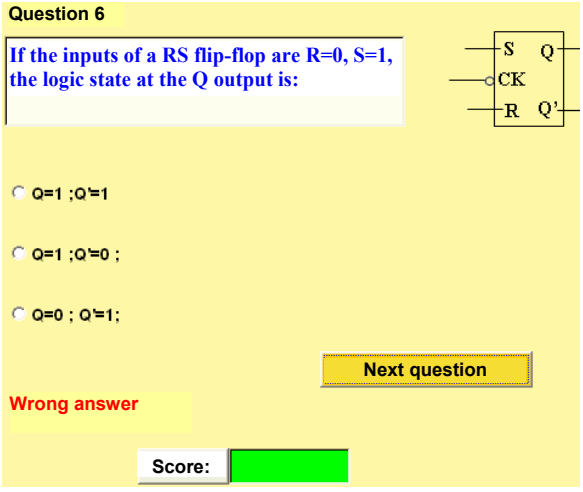

Fig. 6. Test containing multiple choosing items

questions appears in a new random order.

Table 2

The DEIC proposes problems for the learners to be solved as homework in the traditional way, on paper. The proposed problems consist in closed and open answer tests [6]. Some items used for the closed answer test are similar with the items of the interactive tests and other ones are associative items. The open answer test contains primarily problems to be fully solved.

The knowledge accumulated by the learner by covering the available learning materials give to he or she the ability to solve practical applications.

III. EVALUATION OF THE DEIC

There is quite a short time since DEIC has been applied in the teaching activity to the "Edmond Nicolau" Electrotehnic Group School of Cluj-Napoca. Despite of this short period we were very interested in the opinion of the students about using DEIC in the instruction process. The survey results are encouraging. Table 2 presents the survey results. In addition, Fig. 7 shows a chart highlighting the agreement and disagreement for each item in the survey.

Most students (75%) found DEIC easy to use, while only 12% did not. The instant feedback was appreciated, with 50% agreeing or strongly agreeing with the statement "I like the instant performance feedback using DEIC". Furthermore, 56% agreed or strongly agreed with the statement "DEIC helped improve my skill level", while 69% agreed or strongly agreed with the statement "DEIC helps me to prepare for the assessments". The students appreciate (66%) the problems provided in DEIC as helping them to better understood the course material. The rate of using DEIC is not so high (34%), the reason being the short period since it is available for the teaching process. The survey results are also encouraging regarding the computer-based teaching style: 56% of the students consider that "It would be a good idea to have Web-based materials in other courses", while 26% disagree this teaching style. We are sure the appreciation of the students will strongly increase for the computer-based teaching style as they became more and more accustomed with it.

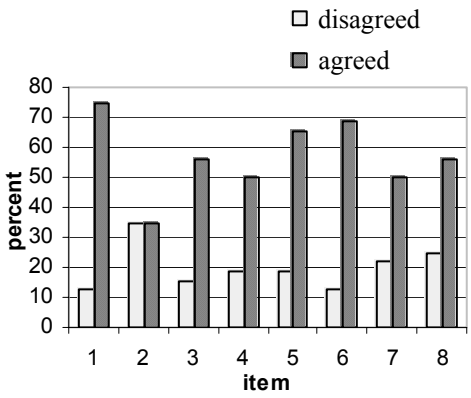

Fig.7. Graphical representation of the survey results

Student evaluation results for DEIC (Key: SD- Strongly Disagree, D-Disagree, N-Neutral, A-Agree, SA-Strongly Agree

No.	Item	SD (%)	D (%)	N (%)	A (%)	SA (%)
1	DEIC is easy to use	9	3	13	66	9
2	I often use DEIC	9	25	31	31	3
3	DEIC helped improve my skill level	3	13	28	31	25
4	I am more confident about my learning after using DEIC	9	9	31	38	13
5	The problems provided in DEIC helped me understand the course material better	6	13	16	50	16
6	DEIC helps me to prepare for the assessments	3	9	19	47	22
7	I like the instant performance feedback using DEIC	9	13	28	31	19
8	It would be a good idea to have Web-based materials in other courses	13	13	19	28	28

IV. CONCLUSIONS

A Web-based Interactive Course to teach digital electronics was presented in this paper. DEIC represents a computer-based, modern, and interactive didactical method. Through the means of theoretical aspects presentations, interactive simulations of digital circuits, and self-assessment tests this method assures the development and accumulation of the required competencies for the students.

DEIC benefits by a series of positive aspects. There is a high accessibility for all the course-related materials without any constraint regarding the time, place and staff. The cost for material dissemination is low in the conditions of existing infrastructure (computer network and internet access). The contents can be very easy and quickly updated at negligible costs. The method gives the students some pleasure for study, due to the opportunity to use the computer in all the learning stages. The self assessment tests are very well appreciated by the students for the opportunity to practice and learn from their mistakes without penalty or loss of face. Thus, students can practice each question until satisfied that they have mastered the particular skill, situation, or concept.

Another strong point is the possibility to simulate the behavior of the circuit individually, once and again, if it is the case. There is no need to be in the laboratory or to use expensive experimental setups and instrumentations. Let us remember here that the experiments are very important in the learning process, taking into consideration that we tend to remember up to 90% of what we are doing in an active manner.

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Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 51(65), Fascicola 1, 2006

Determination of Error Probability Concerning the Study of Vibrations at the Rotary Knitting Machine with two Cylinders, of MATEC Type

Adriana Balta[1], Horia Balta[2], Adrian Chiriac[1]

Abstract – In the normal working of a knitting machine, defects appear in the fabric because of the uninterception of the yarn by the needle. Their causes, excluding the irreversible defects, are the mechanical or electrical shocks, vibrations etc.
In this paper it is presented a study about mechanical vibrations produced by the knitting machine Matec, with the purpose to estimate the probability of uninterception of the yarn by the knitting needle. There were considered a few of the main normal working regimes of the machine.
Keywords: knitting machine, mechanical vibrations, statistical analyze, error probability.

I. INTRODUCTION

In the working of the knitting machines, it appears defects, which have an unknown or a random cause, difficult to prognosticate [1]. So, the necessity of repairing appears which means time consuming and sometimes, fabrication defects. The systems based on the detection of fabrication defects, basically consist in photoelectric cells, located close to the fabric, inside or at one side of the machine cylinder. With the help of a conveniently orientated lamp, these systems detect holes and dropped stitches. The systems used for the surveillance of defective knitting elements are normally optical or capacitive sensors, respectively, the shadow produced by the knitting element or the electric field variation produced by the elements, looking for broken needles, closed latches and broken sinkers. These systems are very effective and capable to detect, with high accuracy, the position of the defect, stopping immediately the knitting machine, thus reducing loss. Unfortunately, they do not give further information related to the knitting process and the cause of the defect. Furthermore, some abnormalities pass undetected [1].

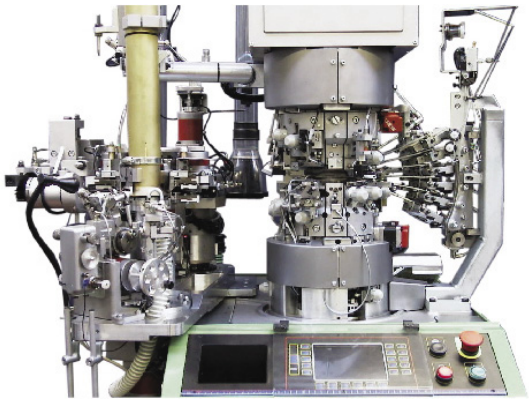

Fig.1 Knitting machine MATEC-1 Silver

The aim of the paper is to estimate error probability, starting from the study of the machine vibrations. On the basis of the vibration statistics, it was estimated the chance of flaw appearance.
The equipment used was a circular knitting machine „MATEC-1 Silver", Fig.1, with a 3.75" cylinder diameter, gauge 18 (corresponding to a set of 216 needles) and one single feeder [2]. The machine is equipped with a roller type positive feeding system and the yarn speed can be adjusted by the means of a worm screw. A speed inverter, connected to the knitting machine motor, allows the adjustment of the cylinder speed with a coefficient of variation of 0.5 %. The most important pieces which work to obtain the fabric are presented in Fig.2. The knit needle (1) and slider (not presented for simplicity) pair is located in the channels of the two vertical cylinders (2), along their generatrix. The cylinders are rotated in trigonometric direction, with a speed which depends on the quality of the machine, fabric type, and quality of the yarn and stage in execution.

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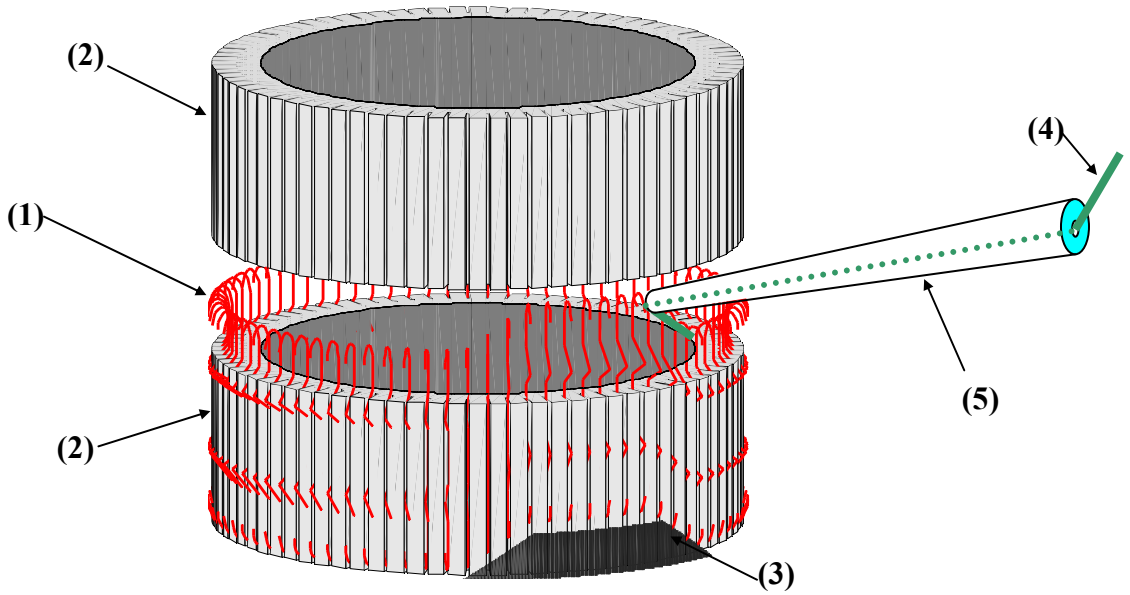


Fig.2 The main elements which realize fabric

For the toes and hells of the sock fabric, the motion of cylinders is of swinging type. The stages of stitched forming are specific to the knitting with final loop. When the needles, due to the cylinder rotation, reach the cam level, these ones give to the needles a vertical motion, through the needle slider (Fig. 2). Through this vertical motion, the needles release the old loop and through yarn retention (4), form the new loop. The yarn of trick is delivered by the yarn roller (5).

A fabric defect appears when the needle, in its reverse motion, does not catch the yarn. The probable cause that was supposed is the moving off of the yarn roller, because of the mechanical vibrations of the machine [3].

In this paper it is proposed to estimate the chances that this moving-off between the yarn trajectory and the delivered yarn, to exceed the *d* needle opening, which is of 1.3 mm, Fig.3. The mechanical vibrations were measured on the slider, through the acquisition system – Fig.4 [4]. Using these values and supposition that the needle and the cylinder have not vibrations, namely the needle trajectory is rigorously correct, in the III^{-th} paragraph, it was determinate the statistics of the yarn moving-off, due to the mechanical vibrations. Through that statistics, in the IV^{-th} paragraph, it was determinate the error probability. In the paragraph V, some concluding remarks are made.

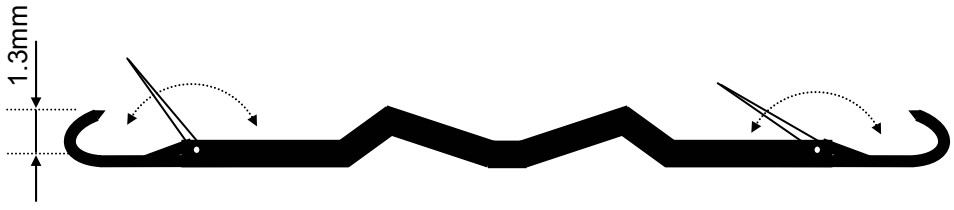


Fig.3 Knitting needle of the machine MATEC-1

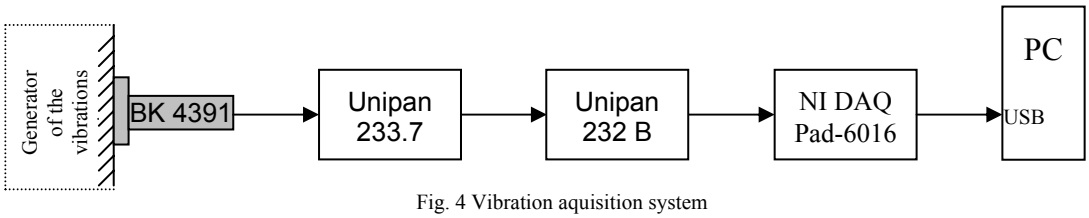


Fig. 4 Vibration aquisition system

II. VIBRATION MEASURING SYSTEM

In Fig.4, it is presented the draft chart of the acquisition system [4]. It was used a piezoelectric accelerometer „Brüel&Kjaer 4391" which has a frequency band 5 Hz – 10 kHz and a sensitivity of 1pC/(m/s^2) for a proper capacity, C=1100pF. The positioning of the accelerometer on the yarn roller is made with a magnet. The signal, generated by the accelerometer is amplified with the preamplifier "Unipan 233-7" and the selective nanovoltmeter „Unipan 232-B" with amplifier role. The amplified signal is taken by PC through an acquisition board from National Instruments, type NI DAQ – 6016 [4]. The utilized sampling rate was of 10000 samples per second. The preamplifier "Unipan 233-7" has input impedance composed by a resistance of 100 MΩ and a capacity of 1.5 pF and the amplification is of 20 dB, equal to the nano-voltmeter amplification.

III. EXPERIMENTAL DETERMINATIONS

There were taken the vibrations values of the yarn roller (Fig.2), during the fabrication of a shock (welt, leg–zone, hell, foot, toe, set up, press off) [5].

In Fig. 5a and b, there is presented the acquired signal, corresponding to a block (10000 samples), during the welt fabric.

In its spectrum (Fig.5b), it distinguishes the spectral components. The dominant component has a frequency of 900Hz and is due to the impact between needles and cams. For example, considering a normal number of rotations of the cylinders, of 250 rot/min and 216 needles, it results a needle frequency of 900Hz. If the model imposes a rib fabric, than the periodicity is of 2 needles and it is obtained a frequency of 450Hz.

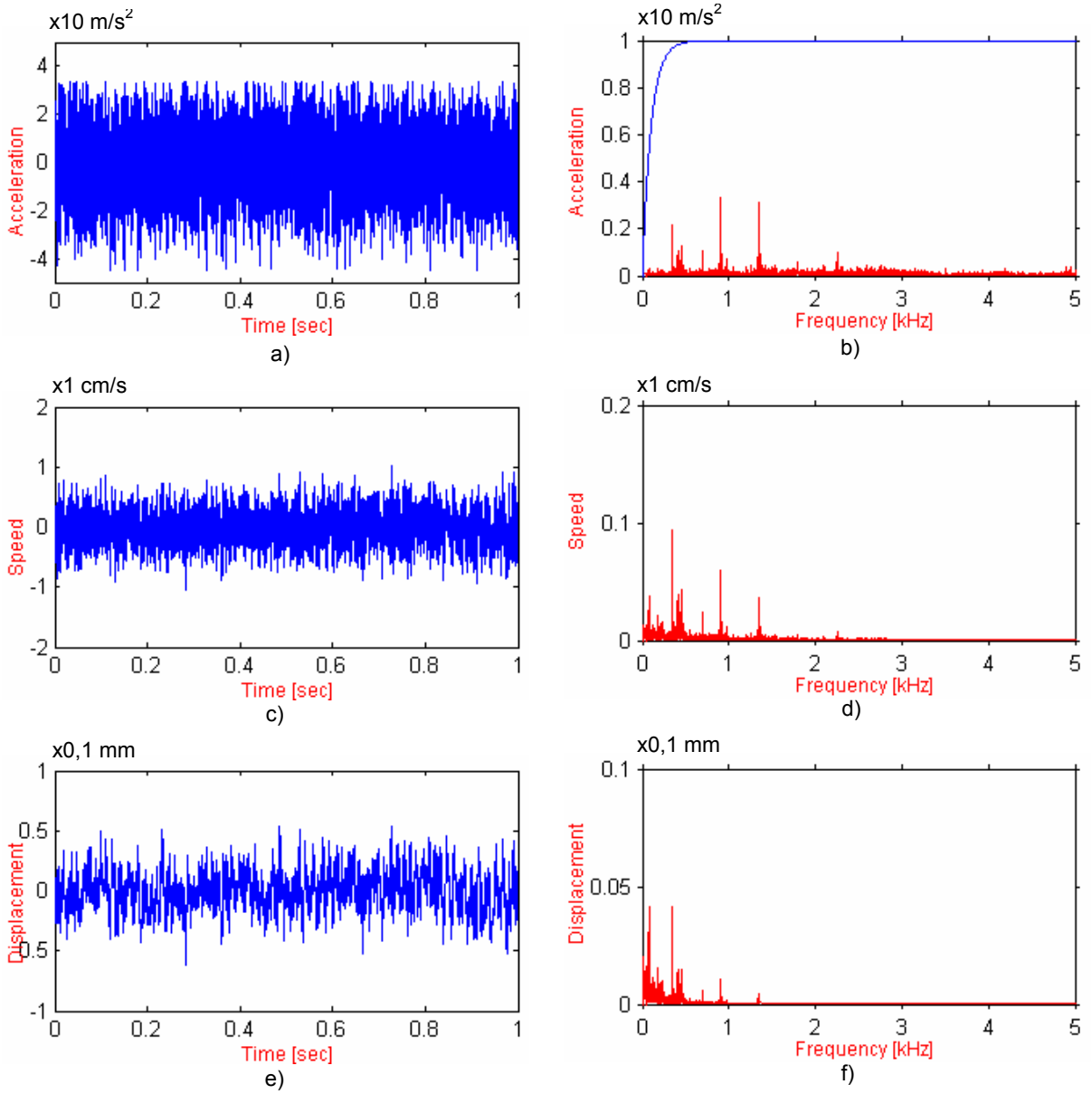


Fig.5 Example of measurement results

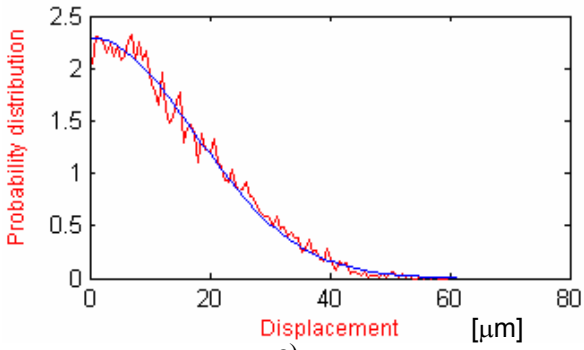
The diagrams c, d, e, f present a speed signal and its spectrum, respectively, the displacement signal and its spectrum [6].
To obtain the speed and displacement spectrum, it is utilized a high pass filter, in order to eliminate the very low parasite frequency components (because of some vices of the acquisition system).

IV. CALCULATION OF ERROR PROBABILITY

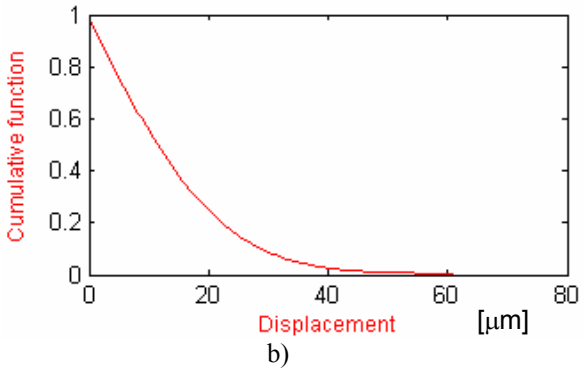
For the determination of the error probability, it was constructed the distribution of the displacement values of the yarn roller, in relation to the cylinders with needles, which were considered unvibrating [7]. In Fig.6a, it is presented the obtained distribution on the basis of the signal of Fig.5, as well as its approximation by a normal distribution (Gaussian) with a null average. It was considerate the appearance probability of a defect, if the yarn is not intercepted by the needle, in the case when the yarn displacement exceeds the d value, defined in the paragraph 1.
In Fig.6b, it is represented the function

$$F(z) = 1\text{-}2\int_0^z p(x)dx = erfc\left(\frac{z}{\sqrt{2\cdot\sigma^2}}\right), \qquad (1)$$

where $p(x)$ represents the normal distribution, previously determined, $F(z)$ represents the probability that, because of the yarn roller vibrations, to be positioned at the z distance to the rest position; than



a)



b)

Fig.6 Displacement statistic

Table 1

Working regime	Dispersion $\sigma^2[mm^2]$	$F(z)$
Starting moment for the knitting welt	0.0505	$7.2545\cdot10^{-9}$
Stop of machine by the operator	0.1192	$1.6632\cdot10^{-4}$
Continuous working of machine (Fig.5)	0.0330	$8.2905\cdot10^{-13}$

$F(d)$ represents the probability that $z>d$, i.e. the appearance of a defect; σ^2 is the dispersion of the values of displacement signal and $erfc(\ )$ is the error function.
In Table 1 there are presented, fore some phases from the working process of the knitting machine, the determined values of the dispersion σ^2 and, respectively, the resulted values for the probability that a dropped sinker to exist.

V. REMARKS

In this paper it was determined the probability of appearance of the defect of "dropped sinker" type, in the normal working of the knitting machine Silver Matec -1, due to the mechanical vibrations. In the determination of this probability, it was supposed that the needle trajectories are rigorously correct, the vibrating element being vibrating the yarn roller. It was supposed that the defect is exclusively due to the moving-off of the yarn and yarn roller in relation to the needle trajectory, so that the needle does not hold the yarn.
All measurements were made on the yarn roller with a piezoelectric accelerometer B&K4591. From the measured signal of acceleration, there were obtained, by calculus, the speed and displacement signals-Fig.5. By the statistic analysis of the displacement signal, it was determined the probability that the yarn to moving-off from the needle trajectory with a distance, bigger than the needle opening, fact which is considered as the apparition of a defect of "droppe stich" type.
The measurements were made in the normal regimes of working of the knitting machine (excluding the damage cases). The resulted probabilities are presented in Table 1. Apparently, the presented values are negligible. It must make some remarks. Firstly, these probabilities are giving for *a single sinker*. But, if this one appears at a product, the whole product is defect. So, the probability to appear to a product (in this case, a sock) is of N times bigger, where N represents the number of sliders for the whole product. For an ordinary sock, N has a value of 10^5-10^6 order, depending on the thinness of the knitting machine and the product type and there is the possibility that these values to be bigger.
Another observation consist in the fact that in the determination of the displacement signal, it was utilized a filtration of high pass type, to remove the low frequency components. This filtration was necessary because, due to the imperfection of the

acquisition system, the displacement signal, in the absence of this filtration, presents abnormally deviations. But, because of this way of processing of signal, it was also lost the information about the very low frequency components, which normally lead to much bigger values in displacement. (If a, v and s are the acceleration, speed and, respectively, displacement signals, harmonic of f frequency, than between their amplitude values, it exist the relation: $A=2\cdot\pi\cdot f\cdot V$, $V=2\cdot\pi\cdot f\cdot S$.). The determined values of the defect probability in Table 1 correspond to the average and high frequency spectrum, being able to be bigger in reality. It results that these ones are minimal values for the defect probability.

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Embedded system for remote temperature sensor's net

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Abstract – This paper describe solution of remote temperature measurement problem in two areas. First area is remote temperature measurement in prospecting holes on mine dumps to prevent risk of fire. Second area is remote temperature measurement in heat pump to prevent freeze of earth. The measuring system is using battery powered embedded system ensuring service time up to 12 months. Due good covering by signal in normal and demanding terrain the GSM communication system is used. The system has three options of sensor depending on temperature range and depth of boreholes.

Keywords: sensor's net, control technology, microprocessor control, remote control, monitoring

I. INTRODUCTION

This time requirements of security and cost reducing involve observing some parameters of earth. The measurement has to be done on different places without power net. Each station has to be equipped with own power source. In case of battery using service time should more than one year. In this reason good power management should be used. In such large distributed measurement systems the wireless communication with remote objects which are the integral part of these systems should be used. In the large systems we can utilize, with advantage, the communication which will be provided by the GSM technique. Good covering by signal in case of GSM enables the building up of measuring and control systems where the communication can run also in the demanding terrain. For wireless data transmission the whole series of producers offer the sets of radio-modems enabling the wireless data transmission in mobile telephone networks which, in addition, enable the interconnection with Internet. In these networks the short message service SMS can be used where the short message contains the data being measured or the data service GPRS. The data transmission in the GPRS networks is paid according to the data volume transmitted and not according to the number or time of connection what is suitable especially for applications of remote distributed measurements or safety systems, in both cases in connection with the central dispatching. In case of the whole series of systems the often transmission of small data volumes is required.

Compared with the usual communication technologies this technology has the following advantages:

- The costs for the data transmission in the GPRS network or SMS are very low.
- Time for transmission of 500 Bytes including setting the connection makes 2 sec.
- Mobility, possibility to realize the application anywhere in the sphere covered by the GSM signal.

II. SENSOR'S NET

The measurement data has to be collected from different places on the world or given area. Measurement places are often without any power source and with close or far distance from data destination. We can obtain large net of sensors – SENSOR'S NET. The sensor's net is configured from 1 to several measurement station (MS1… MSx) and one base station BS1. Each station is equipped with GSM modem. Maximal number of measurement station is limited by given GSM operator only.

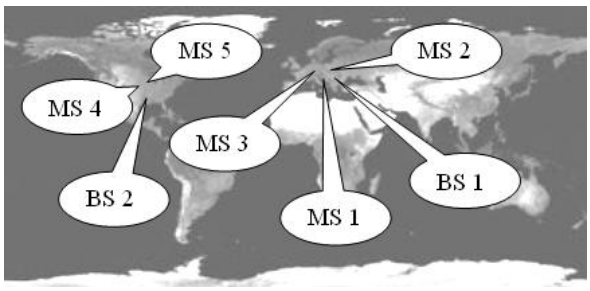

Fig. 1. Example of two sensor's nets

II. MEASURING SYSTEM

The embedded measuring system is composed of two main parts. The first part is the control one which is universal and, at the same time, it includes the power supply. The second part is the measuring one which depends on the application. This part can be changed in dependence on each application. At this time are developed three different measurement parts. Each variant differs with temperature range, distance from

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control part and maximum number of measuring points. For application "Measuring of temperatures in the prospecting holes" two different variants were developed, given in the flow sheet. Third variant was developed for the application "Temperature measurement in heat pump". Realized electronic control board supports all variants of measuring. The simple configuration of the embedded measuring system consists of the group of the temperature sensors, micro-controller, feeding part, GSM module and antenna as illustrated in the flow-sheet in the Figure 2.

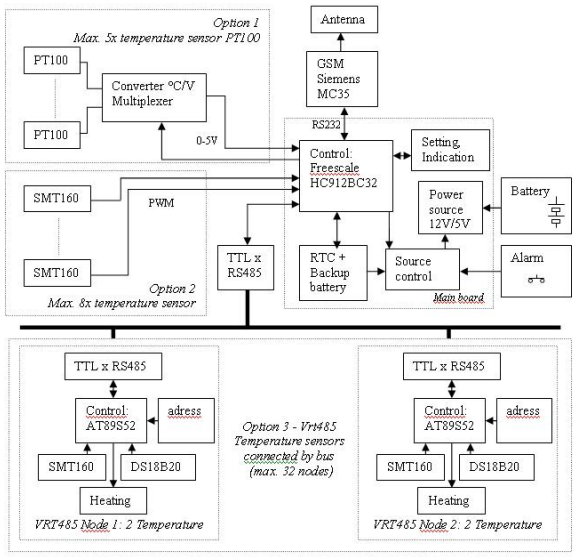

Fig. 2. Flow-sheet of embedded measuring system with three types of sensing option

III. CONTROL PART

The core of the control part is the 16-bits micro-controller Freescale HC12 (Kotzian and Srovnal, 2002a) which controls the GSM modem Siemens MC 35 with the help of the AT commands. The communication runs on the serial line RS 232. The specially adjusted antenna for horizontal location on the probe surface is connected to the GSM module. For ensuring of the universal character of the measuring system utilization anywhere in terrain the supply from 12 V accumulator of the type WP26-12 (12V/26Ah) was selected. For ensuring of low electrical power consumption and so the long-term service life of measuring system the following system of the feeding control was proposed. The system contains the back-up lithium battery which feeds the control of the source being connected and the RTC circuit for generation of the real time and alarms. The micro-controller controls the RTC circuit through the bus I2C. After programming of the next starting up of the embedded system, the micro-controller will interrupt supply of measuring part, GSM modem and itself. On this interrupt is cooperating the of the switched power supply control circuit. Herewith, the consumption of the whole system will be significantly reduced to several micro-amperes. The control part contains also the safety input which monitors the unauthorized handling with the probe, e.g. by opening the lid of the probe covering. The safety input is also bound on the circuit of the supply control enabling the immediate transition from the mode of the reduced supply.

Algorithm of the control part behaviour ensures the following functions:

- The regular activation of the microprocessor and GSM module in the selected measuring intervals and services.
- The measuring itself with the data transmission through GSM.
- Reception of control and configuration data from the dispatcher's working place.
- Immediate reporting of the alarm input.
- Immediate reporting of the decrease of the accumulator capacity and the back-up battery under the limit selected.

The programming of the embedded system for measuring and transmission of the data measured can be carried out either by the SMS service or GPRS. The microcontroller is programmed using CodeWarrior for Embedded Systems environment from Metrowerks. (Kotzian and Srovnal, 2002c)

The whole control system was proposed universally in such a way so that it with connection to microcontroller could be possible to utilize it also for other applications than the temperatures measuring in the application selected.

IV. MEASURING PART

The electronics measuring station has three possible solutions. The solutions differ by the limit of the maximally achieved operating temperature which is influenced by technological principle of sensing elements.

A. *Variant 1. Semiconductor sensor*

This variant respects the economic requirements. The low cost variant of the prospecting holes using semiconductor sensor SMT 160-30. The limit working range is up to 175ºC (optimum limit of the working temperature makes 135ºC). The financial saving is reflected in simplifying of the circuit solution of circuits for processing of the signal linked up on the implemented microcontroller Freescale HC12.

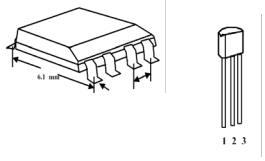

Fig. 3. Semiconductor sensor SMT 160-30

Thanks to the selection of intelligent (programmable) sensors with the output with the coded measuring values into the width modulation of the outgoing voltage signal this version is simplified by the circuits of the signal adjustment – filters, amplifiers, multiplexers, current sources. The outputs of single sensors are led directly on the digital inputs of microcontroller and the value of single sensors, thanks to the internal counters and program means of the microcontroller, is converted on the digit and, subsequently together with other data according to the selected program of values distribution, sent by the SMS service or GPRS for processing in the dispatching working place.

B. *Variant 2. PT1000 sensor*

The more economically demanding variant of measuring part, fully meeting the required range of temperatures measured, works with the sensors Pt1000 "Fig.4." The sensors are executed in the encasing in stainless steel tanks and silicon insulation line. This configuration resists the increased temperatures for a long time and respectively also the aggressive environment. The outputs of single sensors are led to the analogue multiplexer. The connection of multiplexer measuring channels is controlled by digital outputs of the micro-controller Freescale HC12. The single sensors are supplied by the current source. Thanks to the implemented circuit connection the affects of lines and connected circuits on measuring accuracy are removed. The signal from the multiplexer is amplified by the operating amplifier and connected to the internal A/D converter of the micro-controller. The program will convert the analogue value on digit and, subsequently together with other data according to the selected program of the value distribution, is sent by the SMS service or GPRS for processing into the dispatching working place.

Fig. 4. PT1000 Sensor

C. *Variant 3. Distributed sensors VRT485*

This variant is suitable for temperature measurement in deep boreholes. Variant A and B are suitable for distance more than several meters or hundreds of meters. For measuring temperatures in deeps more than hundreds of meters it is necessary to process sensors data locally. Processed data are sending to control part using industrial bus. Variant 3 is collection of nodes connected to industrial bus standard RS485. Each node is equipped with two different semiconductor temperature sensors, heating resistor for temperature jump, microcontroller, communication interface, and power supply monitor. Maximal number of nodes is 32. Node is programmed using ISP (In system programming) connector. Block diagram is shown of figure 5.

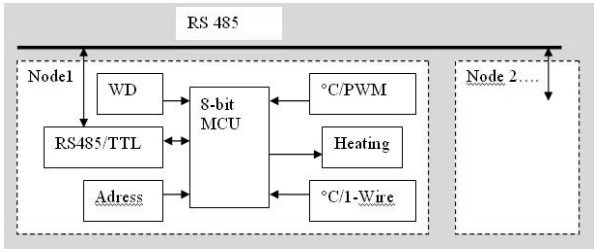

Fig. 5. VRT485 Node with Sensors and heating

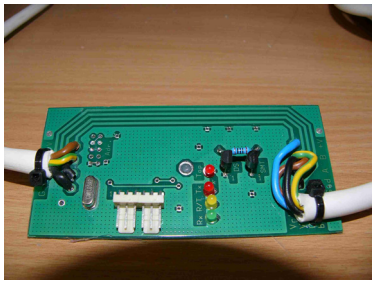

Fig. 6. Implementation of VRT485 Node

V. BASE STATION

The program equipment of the dispatching in the function of visualization working place was developed. The working place of dispatching is equipped with the computer PC and terminal Siemens MC35. The visualization application was carried out in the SCADA system Promotic. The majority of the GSM modules can communicate with the environment with the help of the RS232 interface. The module functions are controlled with the help of the AT commands, which can be entered directly in the text form, for instance with the help of HyperTerminal, which is an integral part of the accessories of the operating system Windows 95 and higher.

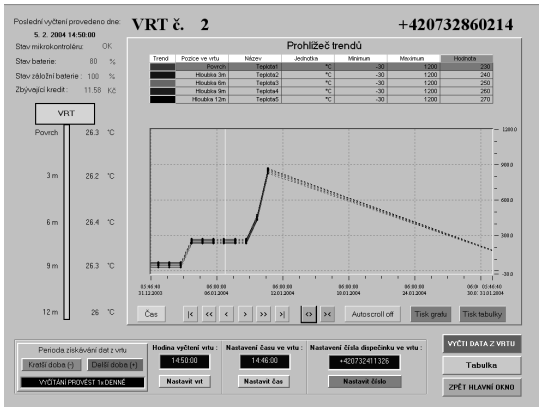

Fig. 7. User interface of Base station

VI. APPLICATIONS AND RESULTS

This project has two main utilizations. First area is remote temperature measurement in prospecting holes on mine dumps to prevent risk of fire. Two systems with semiconductor sensor silicon was created and delivered to the customer. The customer was installed them in Ostrava region. Second type was installed on VŠB-TU University. This application makes remote temperature measurement in heat pump o prevent freeze of earth of new university hall. The test station of this type is on the figure 8. Pictures from installation are on figures 9 and 10.

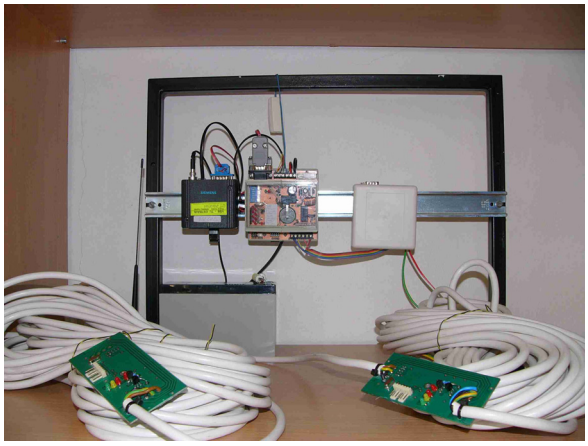

Fig. 8. Test setup of Measuring station.

Fig. 9. Real installation of VRT485 bus of sensor

Fig. 10. Real VRT485 placing

VIII. CONCLUSION

This project solves the problem of remote measurement with battery supply with long service time. Within the project the embedded system for measuring station was developed. Base station and three variant of measuring part are supported now. Variants differ by the operating temperatures and measuring distance. Developed system was realised with all three measuring variants. Two variants of measuring were practically applied. Two systems with VRT485 measuring nodes were tested on university and two systems with semiconductors sensors were used by personal company in the Czech Republic.

VII. AKNOWLEDGEMENT

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Experimental results regarding the using of the UC3854 circuit for power factor correction in the drives with asynchronous motors

Adrian Şchiop[1], Viorel Popescu[2]

Abstract – In this paper are presented experimental results obtained by simulation, using PSpice model of the UC3854 circuit and the average model of the boost converter, and by measurements on experimental stand, regarding the manner in which the capacitor from voltage control loop affects the dynamic response of power factor circuit at voltage supply changes. Also, it was studied the manner in which the values of this capacitor affects the power factor and the total harmonic distortion factor. The efficiency of power factor circuit depending on output power and power factor modification depending on asynchronous motor speed were experimental determined.
Keywords: UC3854, boost converter, power factor

I. INTRODUCTION

The static frequency converters with dc voltage link used for asynchronous motors drives contain in their structure rectifiers for changing the ac voltage given by the utility grid into dc voltage. Once with the development and increasing the performances of the electronic equipments, new performances of rectifiers are required. As a result, modern rectifiers have many of the de-dc converters principle. The reason is the low power factor and unexpected current harmonics that appear in classical rectifiers.
In the first part of the paper is developed an average model for boost converter available both in continuous conduction mode CCM and in discontinuous conduction mode DCM, model which will be used for modeling and simulating the circuit for power factor correction using UC3854 as command circuit.
In the second part it is presented the way of modeling and simulating in PSpice for UC3854. To realize the power factor correction PFC circuit is necessary to simulate before with one of the programs for computer-aided design like Orcad, Protel, Caspoc etc. These programs must contain libraries with models for all the components that are in the electronic circuit that is simulated. So, to simulate the PFC circuit, to see how it works and its performances, is necessary to simulate the control circuit UC3854, as this is not in the libraries for simulation programs. In this part it was analyzed by simulation how the capacitor from voltage control loop influences: the dynamic response of PFC circuit to the modifying input voltage, power factor PF and total harmonic distortion THD factor.
In the third part there are presented the laboratory experimental results. It was experimental determined the efficiency to the PFC circuit regarding to output power and power factor regarding to the speed of asynchronous motor.

II. AVERAGE MODEL FOR BOOST CONVERTER

Because state-space averaging model for boost converter taking into account the working conditions, CCM or DCM, in the next will be developed an average model unchanging in time, valid regardless of working conditions.
For boost converter from Fig.1 the PWM switch formed by active switch S and the diode D changes his topology in time. In this way appears the idea to mediate only this element.

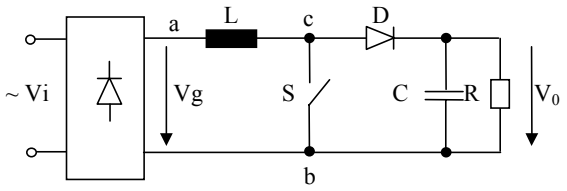

Fig.1. Circuit of the boost converter

In DCM, when S is open and through L passes current in time T_{off}, like in Fig.2, between points c and d is applying the output voltage V_0. When the current from L is breaking, D is blocking and between c and d is applying the rectified voltage V_g in time $T-T_{on}-T_{off}$. T_{on} is switch S conduction time. The average value of

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the voltage between c and d in time switching period T will be:

$$V_{cb,med} = V_0 D_{off} + V_g (1 - D_{on} - D_{off}), \quad (1)$$

where: $D_{on}=T_{on}/T$, and $D_{off}=T_{off}/T$.
In CCM the last term of (1) will de zero.
In Fig.2 is presented the wave shape of inductor current in DCM.

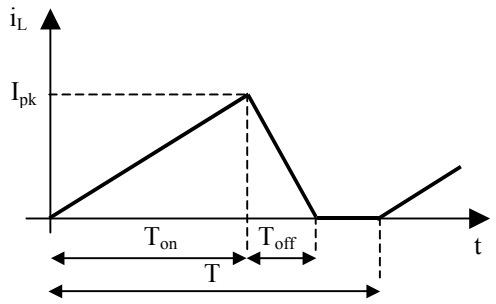

Fig. 2. Inductor current in discontinuous case

The average value of inductor current depending on peak current I_{pk} is [1]:

$$i_L = I_{pk}(D_{on}+D_{off})/2. \quad (2)$$

The average value of diode current is [1]:

$$i_D = I_{pk}D_{off}/2. \quad (3)$$

From (2) and (3) yields:

$$i_D = i_L D_{off}/(D_{on}+D_{off}). \quad (4)$$

Average model of the boost converter is obtained by (1) and (3). This model is presented in Fig.3 and it is valid regardless working mode CCM or DCM.

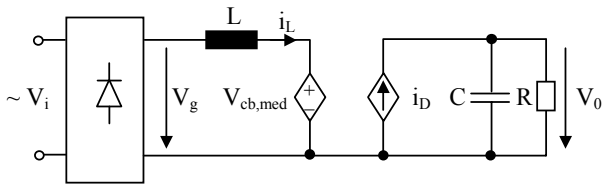

Fig. 3. Average model of boost converter

From [2], in DCM, i_d is:

$$i_D = V_g D_{on} D_{off} T/2L. \quad (5)$$

The last two equations give:

$$D_{off} = (2 i_L L/V_g D_{on} T) - D_{on}. \quad (6)$$

In CCM:

$$D_{off} = 1 - D_{on}. \quad (7)$$

Because the average model of boost converter must be valid in DCM and CCM, D_{off} is choosing:

$$D_{off} = \min\{(2 i_L L/V_g D_{on} T) - D_{on}, 1 - D_{on}\}. \quad (8)$$

This model was implemented in PSpice using voltage source voltage controlled and current source voltage controlled. The duty factors D_{on} and D_{off} appear like voltages accordingly nodes D_{on} and D_{off} as can be shown in Fig. 4.

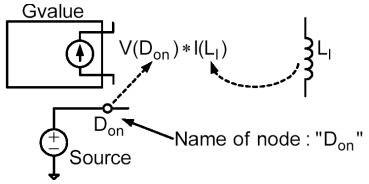

Fig. 4. PSpice representation of duty factor D_{on}

Pspice implementation of average model for boost converter is presented in Fig. 5.

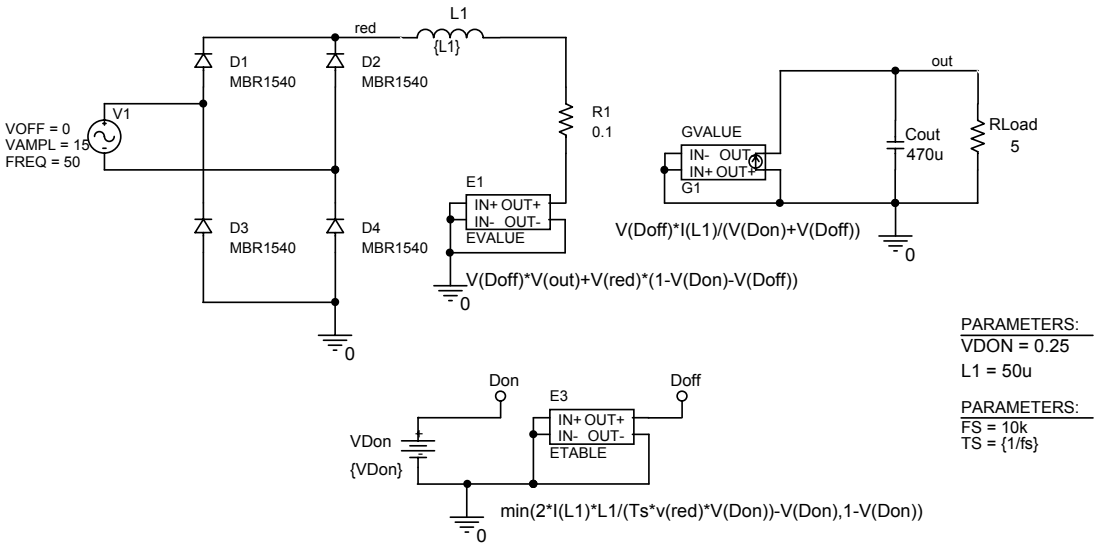

Fig. 5. PSpice implementation of average model for boost converter

In Fig. 6 are presented wave shapes for output voltage and current through inductance when is used average model and real model that contains the power transistor and the diode. As can we see, the wave shapes obtained using average model is mean values for real case. The simulation time for average model is ten times lower than for real case.

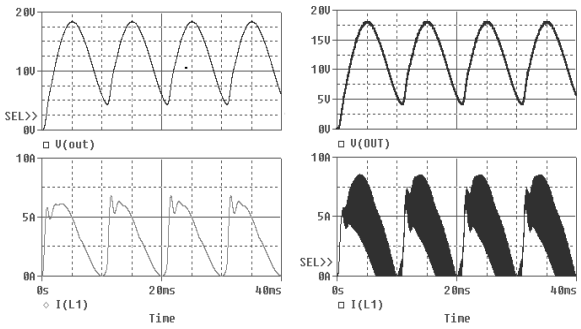

Fig. 6. Wave shapes for average model a) and for real model b)

III. PSPICE MODEL FOR UC3854

The UC3854 provides active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC3854 contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC3854 contains a power MOSFET compatible gate driver, 7.5V reference, load-enable comparator, low-supply detector, and over-current comparator. The UC3854 uses average current-mode control to accomplish fixed frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

For UC3854 will be implemented only principal blocks: multiplier-divider-square, current error amplifier, voltage error amplifier and PWM modulator.

PSpice model of multiplier, divider and squarer MDS is presented in Fig. 7.

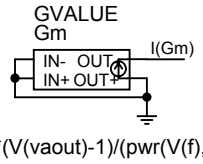

Fig. 7. PSpice implementation of multiplier-divider-square block

MDS block keep the current loop gain constant [3]. This circuitry makes it possible to operate a boost PFC stage over a 3:1 input voltage range and still get excellent voltage loop bandwidth and fast response to input voltage variations. The output of the voltage error amplifier V(vaout) is divided by the square of the average input voltage V(f) before it is multiplied by the rectified input signal I(V_Iac). I(Gm) is output quantity of the MDS and it is given by [4]:

$$I(Gm)=I(V\_ac)\cdot[V(vaout)-1]/V(f)^2 \qquad (9)$$

Equation (9) is modeled with part GVALUE from Analog Behavioral Model ABM library.

Current error amplifier is a large bandwidth amplifier. Feedback loop part has been designed like in [5]. PSpice implementation of current error amplifier and Bode plots obtained by simulation are presented in Fig. 8 and Fig. 9.

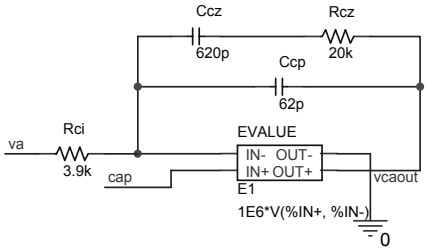

Fig. 8. Current error amplifier

In flat zone of frequency characteristic of current error the zero corresponds to 12,38 kHz, while the pole to 141,18 kHz. The crossover frequency is 15,7 kHz and it is in the flat zone. The phase margin is $46{,}2^0$, being an acceptable value.

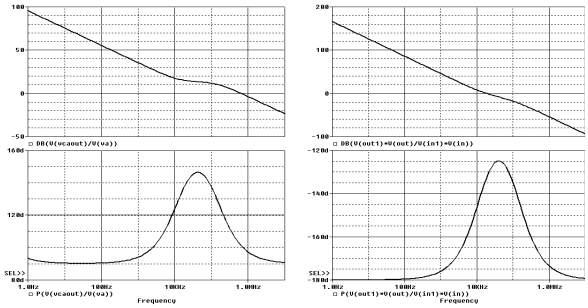

Fig. 9.a) Frequency characteristics for error amplifier b) transfer function in open loop

PSpice implementation of voltage error amplifier and its frequency characteristic are presented in Fig. 10 and Fig. 11.

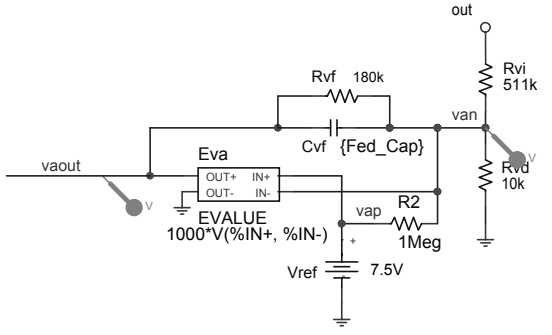

Fig. 10. PSpice model of voltage error amplifier

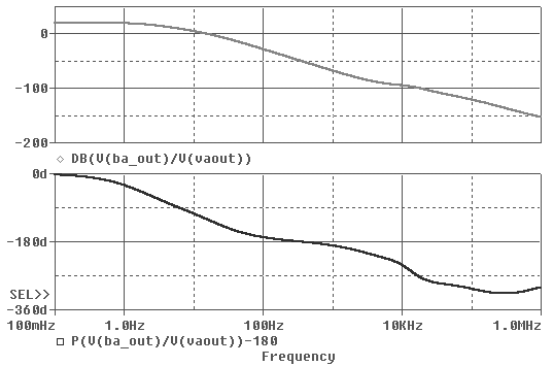

Fig 11 Voltage error amplifier

The voltage control loop must be compensated for stability but because the bandwidth of the voltage loop is so small compared to the switching frequency the requirements for the voltage control loop are really driven by the need to keep the input distortion to a minimum rather than by stability. The bandwidth of the voltage control loop is determined by the amount of input distortion to be contributed by the output ripple voltage. If the output capacitor is small and the distortion must be low then the bandwidth of the loop will be low so that the ripple voltage will be sufficiently attenuated by the error amplifier. Transient response is a function of the loop bandwidth and the lower the bandwidth the slower the transient response and the greater the overshoot. The output capacitor may need to be large to have both fast output transient response and low input current distortion.

Feedback loop part has been designed like in [3].

The crossover frequency is 19,14 Hz and phase margin is 61^0, being an acceptable value.

PSpice model of PWM is presented in Fig.12. The PWM signal is obtained by comparison between a triangular signal and output of current error amplifier. For UC3854, the triangular signal has a minimal value V_{PP}= 1,1V and a maximal value V_{PP}=5,2V [4]. The relationship between output signal of PWM block V_{cauot} and duty factor D_{on} is given by [6].

$$D_{on} = (V_{caout}\text{-}V_{min})/V_{pp} \qquad (10)$$

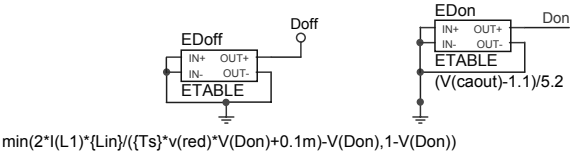

Fig.12. PWM modulator

PWM block was implemented in PSpice with voltage source ETABLE from ABM library. The voltage source EDoff is necessary because is work with average model of boost converter.

PSpice model of PFC circuit with UC3854 and average model of boost converter is presented in Fig.13.

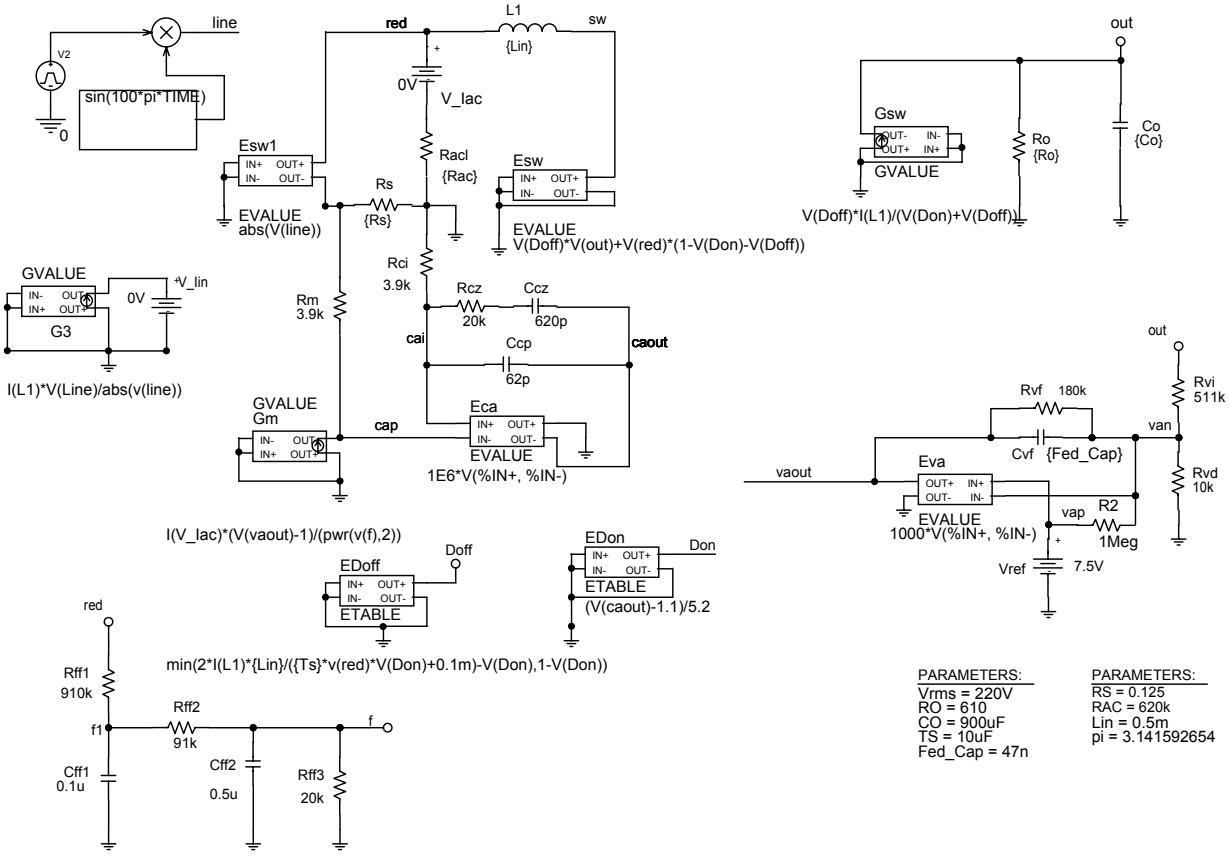

Fig. 13. PSpice model of PFC circuit

Have been supposed that at time t=0,5 seconds the utility grid was changed from115V rms at 220V rms. As can be seen from Fig. 14a, the average value of output voltage V(out) remain constant round about 400V and input current I(G3) is in phase with input voltage V(LINE). It was studied how C_{vf} from voltage control loop influences the step response at changes of utility grid and distortions introduced in input current. Were analyzed the situations when C_{vf} is0,1nF, 47nF and 300nF. Have been observed that when values of C_{vf} arise, the distortions of input current decrease, because the gain of error amplifier decreases but, the time response is slower.

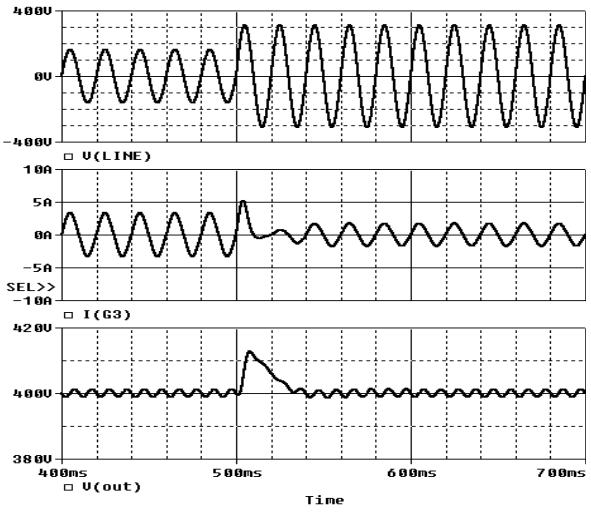

Fig.14a Simulation results obtained when input voltage changes from 155V at 220V rms for C_{vf}=47nF

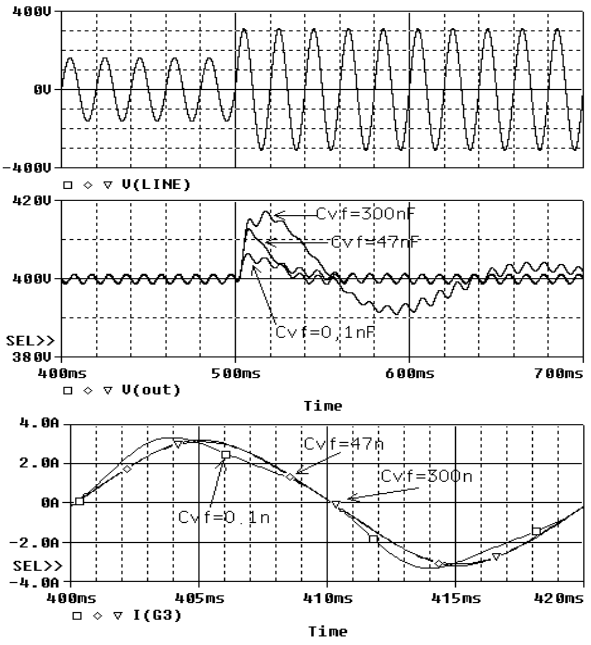

Fig 14b Dynamic response of PFC for 0,1nF, 47nF and 300nF

In Fig. 15 is presented THD and PF depending on C_{vf} values. A trade-off value of C_{vf} between small time response and high PF is C_{vf}=47nF.

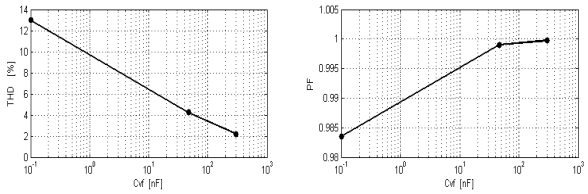

Fig. 15. THD and PF of PFC

IV. EXPERIMENTAL RESULTS

PFC circuit was designed for output power P_{out}=500W, input voltage V_{in}=220V and output voltage V_{out}=400V.

Wave shapes of acquisitioned signals and Fourier component depending on C_{vf} are presented in Fig. 16.

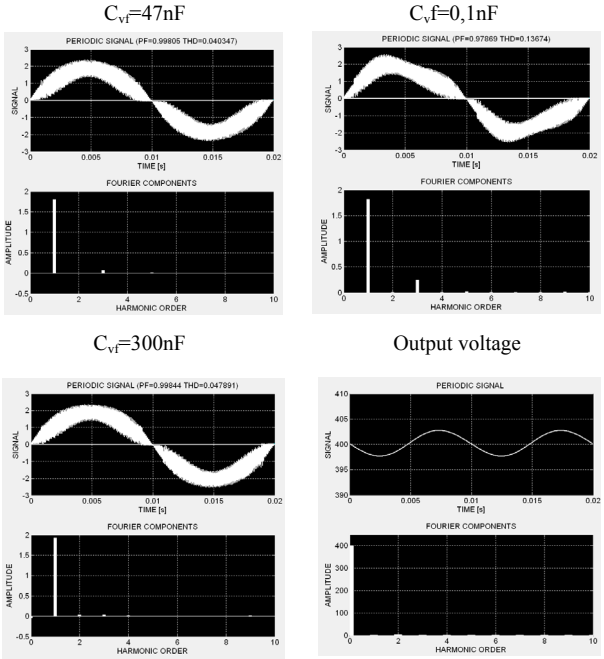

Fig. 16. Acquisition signal of input current and output voltage

Fourier components of input current obtained by acquisition and processed in Matlab are presented in Table1.

Table1 Fourier components of input current

C_{vf} harmonic no.	47nF	0,1nF	300nF
1	1,8295	1.7922	0.9174
2	0.0001	0.0001	0.0397
3	0.0289	0.2359	0.0464
4	0	0	0.0076
5	0.0476	0.0234	0.0053
6	0.0001	0	0.004
7	0.0191	0.007	0.0656
8	0.0001	0	0.0025
9	0.0136	0.0082	0.0067
10	0.0001	0	0.0016
PF	0.9980	0.9786	0.9984
THD	0.0403	0.1367	0.0478

The efficiency of PFC circuit depending on output power and PF depending on speed motor were experimental determined. The results are presented in Fig. 17 and Fig. 18.

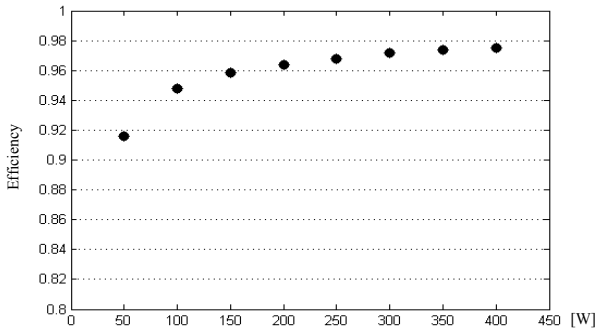

Fig. 17. Efficiency of PFC circuit

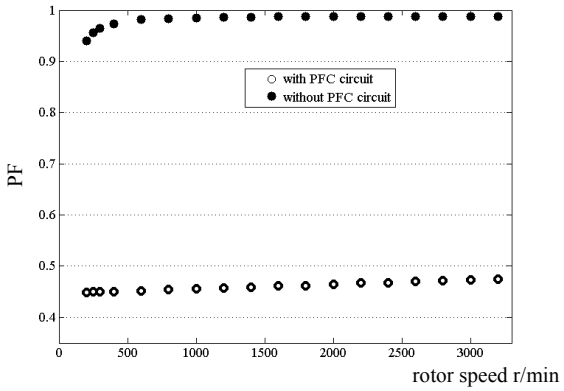

Fig. 18. Power factor with and without PFC circuit

By using PFC circuit PF rises from about 0,46 to 0,98. The speed motor was modified by 50 rotation/min between 200 and 400 r/min where was observed a more rising of PF, and by 200 r/min between 400 and 3200r/min. PF rises with motor speed. This fact is explicated by raising the input current, so, sinusoidal reference voltage of UC3854 is closely follows.

V. CONCLUSIONS

As we said at the beginning, the major disadvantages of rectifying circuits is it the low power factor and the harmonic problems that appear being necessary the usage of PFC circuits. The PFC circuit used in simulating and experiments uses the average current mode control and is realized with Unitrode part UC3854. Before the practical realization of the PFC circuit it is recommended to simulate it first. For simulating the PFC functioning it is necessary to do a model for the control circuit. Has been implemented the average model of boost converter in PSpice environment using voltage controlled voltage source and voltage controlled current source. The duty cycles D_{on} and D_{off} occur as voltage corresponding to the nods. The model shown has advantage, different than other models seen in the specific literature, that uses two controlled sources not four as the [1]. The wave shapes obtained with the average model represents the medium values of the wave shapes obtained in real model. As well, the simulation time when used the average model is ten times lower than when used real model.

It was made the PSpice model of control circuit for PFC. To realize UC3854 model it suggests a model which could be applied to a average model of boost converter. It will use parts from Analog Behavioral Model. In this case the simulation time will be lower.

It has been studied the way in which the values of capacitor in voltage regulation loop cause the modification of the PF and THD. The study was done through simulations and laboratory experiments, the results were very similar, confirming thus validity of the proposed and simulated model.

It has been determined the efficiency of PFC circuit and PF for different values of motor speed. The PF of asynchronous motor drives is substantially improved when using PFC circuit.

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Feedback control design for the image segmentation level in an image processing system

Danijela Ristić and Axel Gräser[1]

Abstract – Inclusion of closed-loop control to overcome the problems of traditional open-loop image processing is proposed. The basic principles and features of feedback control in image processing are illustrated by the example of the recognition of 3D characters on a metallic surface. The feedback control for improving the image segmentation and consequently the character recognition in an unevenly illuminated image is presented.

Keywords: image processing, character recognition, local thresholding, feedback control

I. INTRODUCTION

The improvement of robustness and reliability of vision algorithms is a key issue in computer vision. A number of methods for robust image processing have been developed over recent decades [1]. Their common characteristic is development of vision algorithms with adaptive parameters in order to find the optimal parameters that can cope with the challenges of a particular real-world application. Most of those methods are open-loop so that they are characterised by the significant disadvantage that the low- and high- components of a vision system do not interact, which often leads to nonrobust performance under changing environmental conditions. Recently, a few closed-loop robust image processing systems have been published [2]. The basic idea is to take the output of high level processing and to use it as a feedback to influence the performance of the lower level image processing. Some of those systems consist of optimization algorithms [3] while some are characterized by usage of control techniques [4]. In contrast to Active Vision and Visual Servoing systems, which use the image processing to provide visual feedback information for closed-loop control [5], there are only a few publications dealing with the usage of control techniques in image processing [4][6]. The intention of this paper is to give an additional contribution to the topic.

The authors that have used classical and modern control techniques to solve image processing problems used them for improving the reliability of applied processing techniques. E.g. in [4] control ideas were used to improve sub-pixel analysis in pattern matching. In those publications the image quality is taken for granted. The assumption is that the image at the high level of an image processing system, usually concerning the object recognition, is of a quality good enough for successful feature extraction. In contrast, in this paper as well as in [6] the closed-loop control of image quality at different levels of image processing, including image acquisition, is considered. Namely, due to numerous external disturbances the images at different stages of processing, which are arranged sequentially starting from original (not-processed) image, are often of bad quality so image information is lost during the sequence of processing stages. By inclusion of feedback image quality control the high processing level is supported by reliable data from the lower levels of image processing. The idea behind this is that feedback has natural robustness against system uncertainty and ability to provide disturbance rejection, which is a fundamental concept in control theory [13]. The paper treats the full process of designing a feedback control system that consists of the following steps:

1. the selection of actuator and controlled variable,
2. the selection of a control structure,
3. controller design.

The paper is organized as follows. The key principle of the inclusion of feedback structures in image processing is given in Section II. Specifics, as well as the benefit of the closed-loop control in image processing, are discussed more detailed in Sections III and IV through the demonstration of results achieved for recognition of characters on metallic surfaces. Our feedback mechanism treats the image acquisition as the essential image processing step bearing in mind the influence of the quality of original image on the subsequent processing, which is different from other published results on feedback structures in image processing [2][7]. Besides the image acquisition control, aiming at improvement of the quality of original image, the inclusion of feedback control at the segmentation level of image processing is considered. The full process of designing the threshold adjustment closed-loop is presented in Section IV. The method based on independent

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feedback control loops is suggested for the solution of the problem of character recognition in an unevenly illuminated image. The comparison of performance of proposed method of closed-loop parameter adjustment to the performance of traditional open-loop adaptive thresholding method is given in Section V.

II. CLOSED-LOOP CONTROL IN IMAGE PROCESSING

In a traditional image processing system, processing steps are arranged sequentially as shown in Fig. 1. This arrangement causes a lot of problems. Most important is the unreliability due to the high sensitivity to imaging conditions. That is, due to numerous external influences like illumination conditions, imaging system and imaged objects characteristics, the original image is often of bad quality. If its imperfections are introduced in the standard sequential processing steps then the results of the subsequent steps become unreliable. Nevertheless, in many real-world applications vision engineers will accept the images as given and use traditional preprocessing methods to improve the image quality. This is time-consuming and the results are of low accuracy due to the image information loss during the image acquisition. A further factor is that traditional image processing systems are not flexible since the processing algorithms are mostly *ad-hoc* suffering from the subjective tuning of parameters. Later, together with the fact that the processing at lower levels is performed regardless of the requirements of the following steps, leads to low-robustness of the overall system even in a case of reliable input image data. These problems of traditional open-loop image processing system can be overcome by the introduction of feedback structures at all levels of image processing as proposed in Fig. 1.

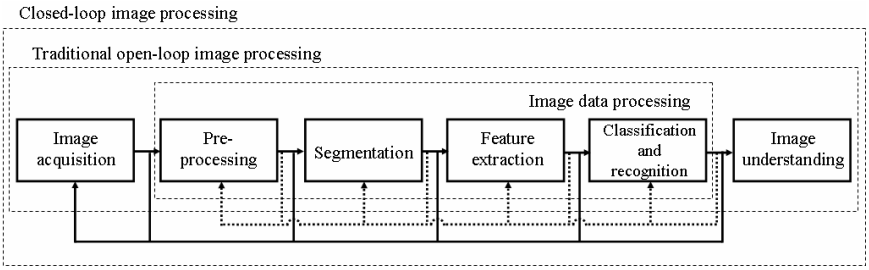


Fig. 1. Block-diagram of standard open-loop and closed-loop digital image processing

It is possible to include two types of closed-loops in a standard image processing system. The first one can be named *image acquisition closed-loop*. Here, the information from all subsequent stages of image processing may be used as feedback to control acquisition conditions (solid lines in Fig. 1). The aim is to provide a "good" image for the subsequent processing steps. The second type of closed-loop can be realized as the feedback between the quality of the image, representing the input of a higher processing level, and the parameters of image processing at lower level as represented with dashed lines in Fig. 1. This closed-loop adjusts parameters of the applied processing algorithm according to requirements of the subsequent image processing step and so can be named *parameters adjustment closed-loop*.

A. The choice of actuator and controlled variables

The closed-loop control in image processing differs significantly from the usual industrial control, especially concerning the choice of actuator and controlled variables. Generally, the actuator variables are those that directly influence image characteristics. Hence, for the image acquisition closed-loop, depending on the application, the actuator variables can be camera's parameters or the illumination condition. For the second type of closed-loop the actuator variables are the parameters of applied processing algorithms (e.g. coefficients and size of filter masks). However, the choice of controlled variable is not a trivial problem. This variable has to be appropriate from the control as well as from the image processing point of view. From the image processing point of view, a feedback variable must be an appropriate measure of image quality. A basic requirement of the control is that the quality of the image has to be measured so that the control variables can be changed to optimize it and it should be possible to calculate it easily from the image.

The problem of identifying which image data are good or bad has become a serious issue in the vision community [8]. To answer the question "what is the image of good quality?" is quite a difficult problem since the image quality depends on the interpretation of the image context. If the image of a "top fashion model" is considered, a good image may hide some details like e.g. imperfect skin. For a surgical endoscope a good image is one showing the organ of interest in all details clearly for human interpretation. Besides, in the computer vision context the way in which the computer "sees" is of importance. Since the correct image understanding highly depends on the result of object recognition as last step in the processing steps chain (Fig. 1), it turns out that *a "good" image is one on which the subsequent steps work well.* Hence, the original image is suitable for further processing if it is not saturated. The resulting image of the preprocessing step is "good" if it has good contrast. The output image at segmentation level is "good" if the image areas corresponding to objects of interest are correctly segmented, etc.

The selection of actuator and controlled variables, known also as *input/output selection*, as well as the selection of control structure highly depends on the application. In the following, these selections representing the typical steps in the process of designing a control system is presented for the case of character recognition in industrial environment. The authors are of opinion that despite of application dependence, once a input/output pair is found and control system is designed the framework for the inclusion of proven error based control techniques in different image processing applications is provided.

III. AN EXAMPLE: RECOGNITION OF CHARACTERS IN INDUSTRIAL ENVIRONMENT

Automated reading of human-readable characters, known as optical character recognition (OCR) [9], is one of the most difficult tasks for computer vision. Besides the common problems concerning the nature of text information to be recognized, in various industrial applications there are numerous specific challenges that should be met. In the automotive industry, that represents one of the most frequent and important application area of the OCR, there is a great variety of identification marks to be detected.

embossed characters scratched characters

Fig. 2. Different types of codes on metallic surfaces to be detected

Scratched or embossed (Fig. 2) marks of work pieces, representing surface deformations, are required in many production processes as durable markings, resistant to subsequent processing. Because of their 3D structure, it is often difficult to illuminate, to segment and, consequently, to detect them. Usage of directional front lighting is a good way to visualize surface deformations since the characters appear bright in contrast due to the reflection from the characters edges [11]. Depending on the quality of the marking process, the depth of the characters on differently colored and processed surfaces can vary demanding a variable illumination even for the same characters due to different reflection conditions. Hence, to find the optimal illumination is of major significance for characters detection. To cope with the need for illumination adaptation the inclusion of feedback control in standard open-loop OCR system is suggested as presented in the following. This inclusion has been investigated within the experiment of imaging differently colored metallic plates with scratched characters on them in variable illumination conditions [10].

A. *Feedback structures for improvement of character recognition on metallic surfaces*

We consider the classical structure of an OCR system [9] consisting of two sections: image acquisition and image data processing. Processing consists of usual steps: segmentation of characters, their binarization, classification and recognition. The novel difference between our configuration and other traditional systems lies in the extension with two control loops as shown in Fig. 3. The idea behind is to provide a basis for the classification to be supported by reliable data from the lower levels of image processing.

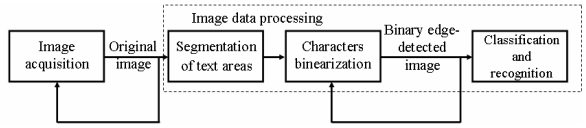


Fig. 3. OCR system with included feedback control

A sequential arrangement of control loops has been chosen since the image acquisition closed-loop is necessary to provide the optimal illumination which yields the original image of "good" quality suitable for the subsequent segmentation. This closed-loop, realized as feedback between the quality of the original image and the illumination condition, as a crucial factor for the image acquisition, is described in details in [12]. In this paper, the emphasis is only on the threshold adjustment closed-loop realized as the feedback between the quality of binary edge-detected image and the threshold as a parameter determining the success of characters binarization at image segmentation level. Its control goal is to give a "good" image input for the classifier, i.e. the binary image containing the "full" clearly separated characters that resemble the characters used for the training of the classifier so that all can be recognized. The second closed-loop is initialized once the image of good contrast is achieved by the image acquisition closed-loop.

IV. THRESHOLD ADJUSTMENT CLOSED-LOOP

As shown in Fig. 3, the segmentation of characters consists of two image processing operations: edge-detection and thresholding. Bearing in mind that the image acquisition closed-loop provides original image of good quality, the assumption that the edges of characters are correctly segmented by chosen Sobel filter [11] can be taken for granted. Hence, the eventual success or failure of subsequent characters classification highly depends on the thresholding step. Thresholding is an image point operation which produces a binary image from a gray scale image (in our system from the gray scale edge-detected image). Too high threshold yields a very small number of black pixels and so, in the case of white background and black characters, leads to loss of information on characters to be detected. In contrast, a low threshold yields a large number of black pixels giving noisy characters. That is why the adequate determination of the threshold and its adaptation to environmental changes is of major importance for character recognition. Since it is very difficult to estimate what is optimal threshold without any feedback information on the result of image binarization, thresholding in

standard open-loop image processing gives often poor results. To determine the threshold providing a binary image with maximum information on characters it is suggested to apply the proven error based control techniques by the closed-loop shown in Fig. 4.

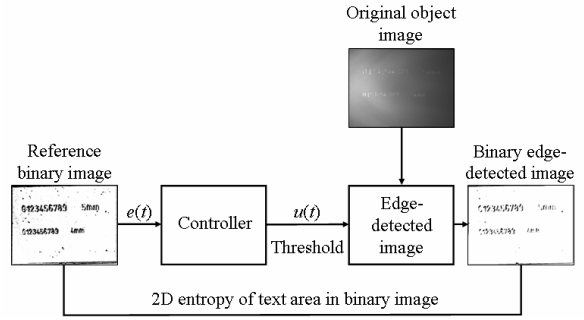


Fig. 4. Threshold adjustment closed-loop

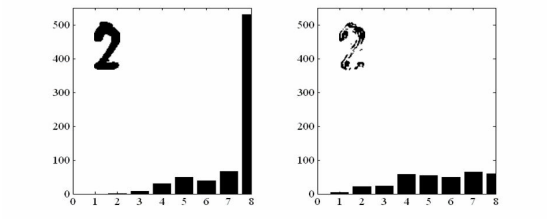
A. *The selection of actuator and controlled variable*

In the proposed closed-loop image segmentation system the threshold value, as parameter determining the quality of binary image, is considered as the actuator variable. The more compact are black pixels that form the characters to be recognized, the binary image is of better quality. Hence, the measure of connectivity of black pixels in text area is naturally imposed as controlled variable. We introduce the two-dimensional (2D) entropy as a connectivity measure:

$$S = -\sum_{i=0}^{8} p_{(0,i)} \log_2 p_{(0,i)} , \qquad (1)$$

where $p_{(0,i)}$ is the estimate of the probability of occurrence of a pair $(0,i)$ representing the black pixel surrounded with i black pixels ($i \in [0,8]$ for the 8-pixel neighbourhood).

Figures 5(a) and 5(b) show respectively the images of the "good" numerical character "2" and the "broken" one with the corresponding histograms of distribution of pairs $(0,i)$ found in the characters images.



(a) (b)

Fig. 5. "Full" (a) and "broken" (b) numerical character "2" with corresponding histograms of distribution of pairs $(0,i)$

Obviously, histogram of the "full" character is narrow in contrast to histogram of the "broken" one. This is an expected result since the number of different pairs $(0,i)$ in the image of "good" character is smaller than in the image of "noised" one, but the estimate $p_{(0,i)}$ is larger. Since a random variable X with a large probability of being observed has a very small degree of information $-\log p(X)$, according to (1) the 2D entropy of a "good" character is to be quite smaller than the 2D entropy of a "broken" character. The results 1.066 and 2.775, for shown "full" and "broken" character respectively, confirm the previous statement. This provides a basis for the use of 2D entropy as a measure of the quality of a binary image containing the characters to be detected.

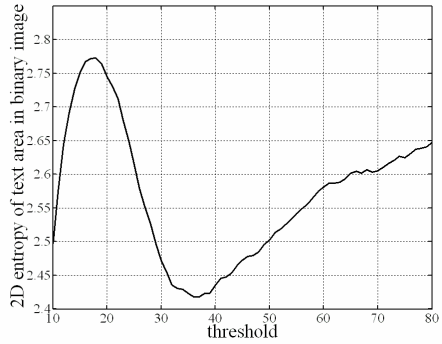


Fig. 6. 2D entropy of text area vs. threshold value

Fig. 6 shows the changing of 2D entropy of text area in binary image with changing of the threshold value. Evidently, 2D entropy of text area is *sensitive* to the chosen control variable across the available operating range. Also, it is obvious that there is *one-to-one steady state mapping* between these two variables and that it is possible to achieve the *global minimum* of S by changing the threshold. The satisfied prerequisites for successful control action prove the pair "threshold – 2D entropy of text in binary image" as a good pair "actuator variable - controlled variable". The idea behind is to drive the actual 2D entropy to the reference value and so to achieve a binary image suitable for recognition.

B. *Choice of the control structure*

Even though smaller 2D entropy means better quality of text to be recognized, the global threshold corresponding to minimal 2D entropy of whole text area will not yield good recognition result. As it was said in Section III, the considered metallic plates were illuminated using point lighting in order to detect the characters edges. The drawback is an unevenly illuminated image. Due to that, the regions of interest (ROIs) in image (in our case 4 text regions) are of different brightness. Hence, the global optimal threshold is not necessarily the optimal threshold for the particular region when consider the number of recognized characters. The 2D entropies of all ROIs in considered image of metallic plate, with 4 strings of scratched characters on it, that correspond to global i.e. to optimal local thresholds are shown in Table 1.

Table 1

	ROI1	ROI2	ROI3	ROI4
Global threshold	38	38	38	38
2D entropy	2.280	2.492	2.383	2.416
Optimal local threshold	38	20	34	26
2D entropy	2.280	2.284	2.339	2.156

The solution of the problem of global thresholding is to perform so-called local adaptive thresholding. The assumption behind this is that smaller image regions are more likely to have approximately uniform illumination, thus being more suitable for the thresholding. In the literature there are different local adaptive thresholding methods which basically divide an image into an array of subimages and then find the optimum threshold for each subimage by investigating its histogram [14]. Those methods are open-loop and so suffer from all problems of standard open-loop image processing mentioned in Section II. To overcome those problems we propose the feedback control structure consisting of four independent control loops as shown in Fig. 7. The idea behind is to drive separately the actual 2D entropy in each ROI (y_i, $i = 1,..,4$) to the given reference value (r_i, $i = 1,..,4$) and so to achieve a binary image with all text regions suitable for recognition.

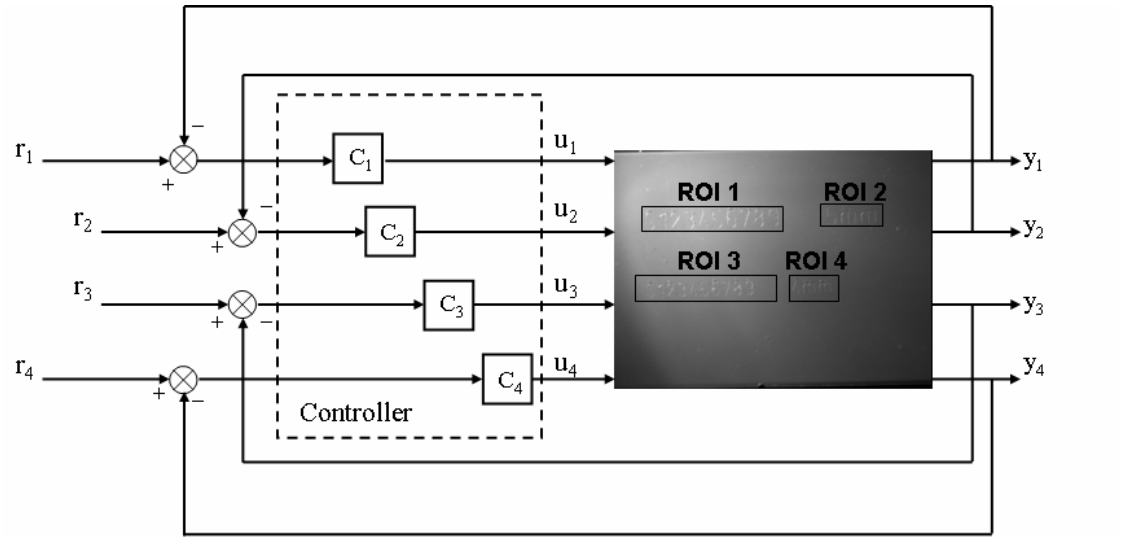


Fig. 7. Feedback control of local image thresholding

C. Controller design

The design of proposed control system involves two steps:

1. the choice of input/output pairings
2. the design (tuning) of each controller C_i.

In each individual loop the pair "threshold - 2D entropy of text in ROI" is chosen as appropriate "actuator variable u_i – controlled variable y_i" pair. The justification of this choice has been discussed in the previous section. In the following, the second step of feedback control system design is shortly presented.

The difficulty of suggested control system lies in the tuning of parameters of each controller C_i (here $i = 1,...,4$). This difficulty is emphasised in an image processing system bearing in mind that the main goal of inclusion of closed-loop control is to avoid "trial and error" tuning of many image processing parameters. Hence, the control design objective was to minimize the tuning problem subject to the achievement of accuracy and stability specifications in the face of uncertainty. Therefore the PI controllers with the same proportional Kp and integral Ki gain for each individual loop have been considered. The controller parameters $Kp = 10$ and $Ki = 40$ were chosen based on the closed-loop responses shown in Fig. 8. The control objective is to achieve as small as possible settling time subject to stability specification of all four individual control loops.

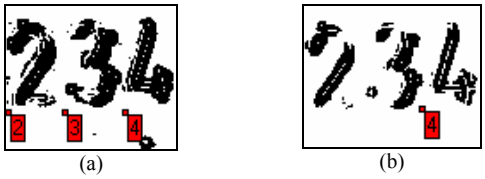
V. COMPARISON WITH THE TRADITIONAL OPEN-LOOP LOCAL THRESHOLDING

The result of comparison the performance of proposed closed-loop control based local thresholding method with the performances of a traditional adaptive thresholding method is given in Table 2. This traditional method is based on one-dimensional (1D) histogram entropy representing the measure of image information [15]. In contrast to our method, which uses feedback information on quality of ROI in binary image to adjust the local threshold, this method presents a "feedforward action". The 1D entropies of the background and foreground of the ROI in gray level image to be thresholded (in our system edge-detected image) are calculated. Then the threshold which corresponds to the maximum of the sum of background and foreground entropies is determined as the optimal threshold. The abbreviations T and 2DE in Table 2 are used for threshold and 2D entropy of text in individual ROI, respectively.

Table 2

Local Thresholding		ROI1	ROI2	ROI3	ROI4
Open-loop	T	70	50	73	55
	2DE	2.512	2.590	2.635	2.710
Closed-loop	T	38	20	34	26
	2DE	2.280	2.284	2.339	2.156

Obviously the value of 2D entropy of text in each ROI in binary image obtained by proposed closed-loop method is lower then one obtained by conventional open-loop thresholding. Moreover, as a result of PI control action, the achieved values using feedback control are given set points for 2D entropies of each ROI. Consequently, the result of character recognition using proposed method is better than the recognition result using open-loop local thresholding as shown in Fig. 9 for the case of numerical characters 2, 3 and 4.



(a) (b)

Fig. 9. Character recognition result achieved with the OCR system with closed-loop (a) open-loop (b) thresholding

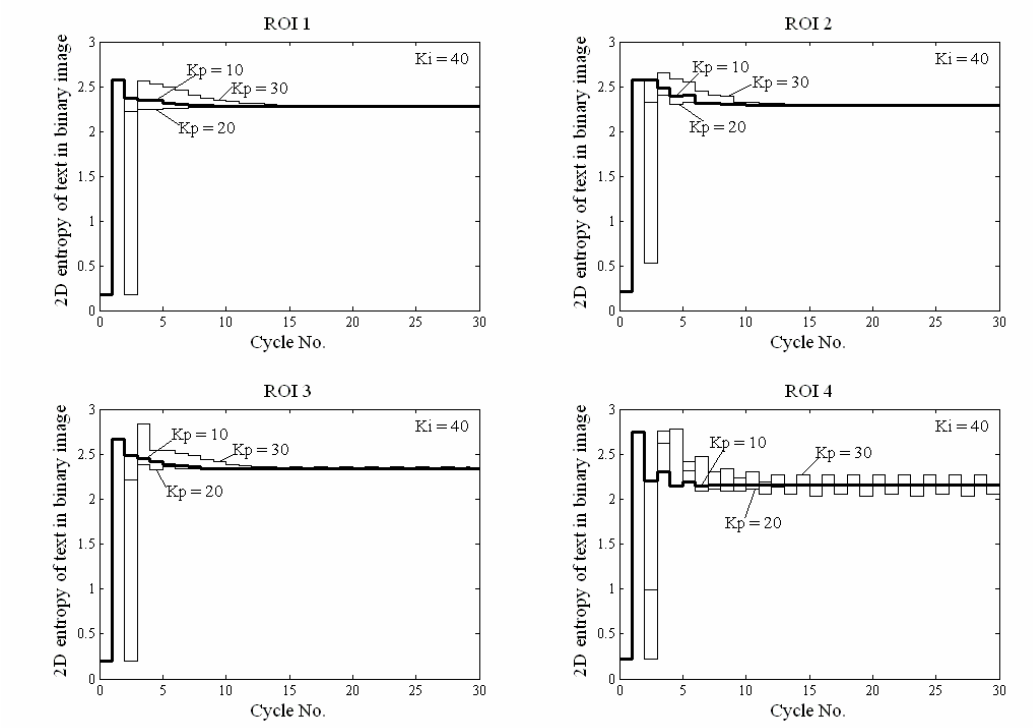


Fig. 8. Closed-loop responses of four ROIs in binary image

VI. CONCLUSIONS

In this paper the idea of inclusion of closed-loop control techniques to improve the robustness and reliability of image processing is discussed. Control of image quality at different processing levels with the emphasis on image segmentation level is considered. The full process of designing the feedback control for solving the problem of character recognition in an unevenly illuminated image is presented. Shown experimental results confirm benefit of the using of feedback information on the quality of binary image to adjust threshold yielding reliable character recognition.

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Fuzzy Sliding Mode Decoupling Controller Design Based on Indirect Field Orientation for Induction Motor Drive

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Abstract – In this paper, the design of a speed control scheme based on total fuzzy-sliding mode control for indirect field-orientated induction motor (IM) is proposed. In this scheme, the motor speed is controlled by fuzzy sliding mode controller, in which the fuzzy logic controller replaces the discontinuous part of the classical SMC law ($k \cdot sign(s)$). The proposed fuzzy sliding mode control operation can reduce the dependence on the motor parameters and disturbance uncertainties. The decoupling scheme uses two fuzzy sliding mode controllers to regulate the *d*-axis and q-*axis* stator currents respectively. This new current controller exhibits several advantages such as fast dynamic response, perfect decoupling and robustness to parameter variations. Finally, the effectiveness of the complete proposed control scheme is verified by numerical simulation. The numerical validation results of the proposed scheme have presented good performances compared to the classical sliding mode control.

Keywords: induction motor, vector control, decoupling, sliding mode control and fuzzy sliding mode.

I. INTRODUCTION

Nowadays, like a consequence of the important progress in the power electronics and of micro-computing, the control of the AC electric machines known a considerable development and a possibility of the real time implantation applications. AC motors, especially, the induction motor (IM), enjoy several inherent advantages, like simplicity, reliability, low cost, and almost maintenance-free electrical drives [1]. However, for high dynamic performance industrial applications, their control remains a challenging problem because they exhibit significant nonlinearities, and many of the parameters, mainly the rotor resistance, vary with the operating conditions. On the other hand and during numerous decades, the machine with direct current (DC) machine constituted the only electromechanical source of variable speed applications because of its ease of control, where torque and flux are naturally decoupled and can be controlled independently by the torque producing current and the flux producing current [1, 2, 3].

The field-oriented control technique has been widely used in industry for high-performance IM drive [2, 3], where the knowledge of synchronous angular velocity is often necessary in the phase transformation for achieving the favourable decoupling control between motor torque and rotor flux as for a separately excited DC machine. This control strategy can provide the same performance as achieved from a separately excited DC machine [3, 4]. This technique can be performed by two basic methods: direct vector control and indirect vector control. Both DFO and IFO solutions have been implemented in industrial drives demonstrating performances suitable for a wide spectrum of technological applications. This stimulated a significant research activity to develop IM vector control algorithms using nonlinear control theory in order to improve performances, achieving speed (or torque) and flux tracking, or to give a theoretical justification of the existing solutions [2, 3]. Sliding mode control theory, due to its order reduction, disturbance rejection, strong robustness and simple implementation by means of power converter, is one of the prospective control methodologies for electrical machines[5, 6]. The feature of sliding mode control system is that the controller is switched between tow distinct control structures. In general, the design of variable structure controller generally consists of two steps, which are hitting and sliding phases [5]. First, the system is directed towards a switching surface by a feedback control law, the sliding mode occurs. When the system states enter the sliding mode, the dynamic of the system are determined by the choice of sliding surface. The mentioned situations are independent of parametric uncertainties and load disturbances. Hence, SMC has been employed to the position and speed control of AC machines. But because of the non-continuous switch feature of SMC, the chattering can occur in the control system [5, 6]. In order to reduce or overcome the system chattering, researches have proposed the fuzzy control design methods based on the sliding-mode control scheme [7, 8, 9]. These controllers are referred to as fuzzy sliding-mode controllers (FSMC).

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Since only one variable is defined as the fuzzy input variable, the main advantage of the FSMC system is that the fuzzy rules can be reduced.

In this paper, a fuzzy sliding mode decoupling controller which combines the merits of the sliding mode control and the fuzzy inference mechanism is proposed. In addition, an outer-loop speed controller that employs fuzzy sliding mode control is derived. In this scheme, a fuzzy sliding mode controllers are investigated, in which the fuzzy logic system is used to replace the discontinuous control action ($k \cdot sign(s)$) of the classical SMC law. The reminder of this paper is organized as follows. Section II reviews the principle of the indirect field-oriented control (FOC) of induction motor. Section III shows the development of sliding mode controllers design for IM control. The proposed fuzzy sliding mode control scheme is presented in section IV. Section V gives some simulation results. Finally, some conclusions are drawn in section VI

II. INDIRECT FIELD-ORIENTED CONTROL OF THE IM

The dynamic model of three-phase, Y-connected induction motor can be expressed in the *d-q* synchronously rotating frame as [1, 2, 3]:

$$\begin{cases} \dfrac{di_{ds}}{dt} = \dfrac{1}{\sigma . L_s}\left(-\left(R_s + \left(\dfrac{L_m}{L_r}\right)^2 . R_r\right) i_{ds} + \sigma . L_s . \omega_e . i_{qs} + \dfrac{L_m . R_r}{L_r^2} . \phi_{dr} + \dfrac{L_m}{L_r} . \phi_{qr} . \omega_r + V_{ds}\right) \\ \dfrac{di_{qs}}{dt} = \dfrac{1}{\sigma . L_s}\left(-\sigma . L_s . \omega_e . i_{ds} - \left(R_s + \left(\dfrac{L_m}{L_r}\right)^2 . R_r\right) i_{qs} - \dfrac{L_m}{L_r} . \phi_{dr} . \omega_r + \dfrac{L_m . R_r}{L_r^2} . \phi_{qr} + V_{qs}\right) \\ \dfrac{d\phi_{dr}}{dt} = \dfrac{L_m . R_r}{L_r} i_{ds} - \dfrac{R_r}{L_r} . \phi_{dr} + (\omega_e - \omega_r)\phi_{dr} \\ \dfrac{d\phi_{qr}}{dt} = \dfrac{L_m . R_r}{L_r} i_{qs} - (\omega_e - \omega_r)\phi_{dr} - \dfrac{R_r}{L_r} . \phi_{qr} \\ \dfrac{d\omega_r}{dt} = \dfrac{3}{2}\dfrac{P^2 . L_m}{L_r . J}\left(i_{qs} . \phi_{dr} - i_{ds} . \phi_{qr}\right) - \dfrac{f_c}{J} . \omega_r - \dfrac{P}{J} . T_l \end{cases} \quad (1)$$

Where σ is the coefficient of dispersion and is given by (2):

$$\sigma = 1 - \frac{L_m^2}{L_s L_r} \quad (2)$$

L_s, L_r, L_m stator, rotor and mutual inductances;

R_s, R_r stator and rotor resistances;

ω_e, ω_r electrical and rotor angular frequency;

ω_{sl} slip frequency $(\omega_e - \omega_r)$;

τ_r rotor time constant (L_r / R_r);

P pole pairs

The main objective of the vector control of induction motors is, as in DC machines, to independently control the torque and the flux; this is done by using a *d-q* rotating reference frame synchronously with the rotor flux space vector [2, 3]. In ideally field-oriented control, the rotor flux linkage axis is forced to align with the *d*-axes, and it follows that [3, 4, 12]:

$$\phi_{rq} = \frac{d\phi_{rq}}{dt} = 0 \quad (3)$$

$$\phi_{rd} = \phi_r = cons\tan t \quad (4)$$

Applying the result of (3) and (4), namely field-oriented control, the torque equation become analogous to the DC machine and can be described as follows:

$$T_e = \frac{3}{2}\frac{p \cdot L_m}{L_r} \cdot \phi_r \cdot i_{qs} \quad (5)$$

And the slip frequency can be given as follow:

$$\omega_{sl} = \frac{1}{\tau_r}\frac{i_{qs}^*}{i_{ds}^*} \quad (6)$$

Consequently, the dynamic equations (1) yield:

$$\frac{di_{ds}}{dt} = -\left(\frac{R_s}{\sigma L_s} + \frac{1-\sigma}{\sigma \tau_r}\right) i_{ds} + \omega_e i_{qs} + \frac{L_m}{\sigma L_s L_r \tau_r}\phi_{rd} + \frac{1}{\sigma L_s} V_{ds} \quad (7)$$

$$\frac{di_{qs}}{dt} = -\left(\frac{R_s}{\sigma L_s} + \frac{1-\sigma}{\sigma \tau_r}\right) i_{qs} - \omega_e i_{ds} + \frac{L_m}{\sigma L_s L_r \tau_r}\phi_{rd} + \frac{1}{\sigma L_s} V_{ds} \quad (8)$$

$$\frac{d\phi_r}{dt} = \frac{L_m}{\tau_r} i_{ds} - \frac{1}{\tau_r}\phi_{rd} \quad (9)$$

$$\frac{d\omega_r}{dt} = \frac{3}{2}\frac{P^2 L_m}{J L_r} i_{qs}\phi_{rd} - \frac{f_c}{J}\omega_r - \frac{P}{J} T_l \quad (10)$$

The decoupling control method with compensation is to choose inverter output voltages such that [10]:

$$V_{ds}^* = \left(K_p + K_i \frac{1}{s}\right)\left(i_{ds}^* - i_{ds}\right) - \omega_e \sigma L_s i_{qs}^* \quad (11)$$

$$V_{qs}^* = \left(K_p + K_i \frac{1}{s}\right)\left(i_{qs}^* - i_{qs}\right) + \omega_e \sigma L_s i_{ds}^* + \omega_r \frac{L_m}{L_r}\phi_{rd} \quad (12)$$

According to the above analysis, the indirect field-oriented control (IFOC) [1, 4, 10] of induction motor with current-regulated PWM drive system can reasonably presented by the block diagram shown in the Fig. 1.

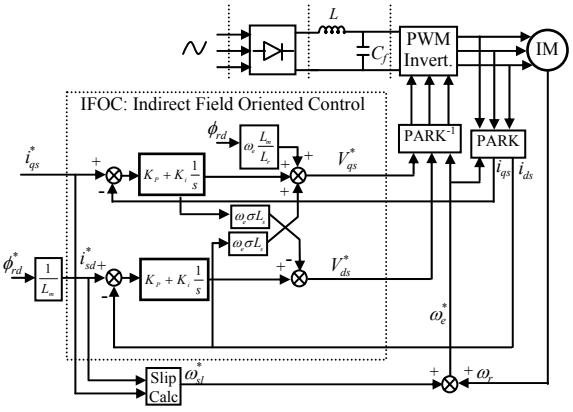


Fig. 1. Block diagram of IFOC for an induction motor.

III. SLIDING MODE CONTROL

A Sliding Mode Controller is a Variable Structure Controller (VSC). Basically, a VSC includes several different continuous functions that can map plant state to a control surface, and the switching among different functions is determined by plant state that is represented by a switching function [6, 7, 8].

Without lost of generality, consider the design of a sliding mode controller for the following second order system:

$$\ddot{x} = f(x, \dot{x}, t) + b \cdot u(t) \quad (13)$$

Here we assume $b > 0$. $u(t)$ is the input to the system. The following is a possible choice of the structure of a sliding mode controller [5, 11]:

$$u = u_{eq} + k \cdot sign(s) \quad (14)$$

Where u_{eq} is called equivalent control which dictates the motion of the state trajectory along the sliding surface [9]. is a constant, representing the maximum controller output. s is called switching function because the control action switches its sign on the two sides of the switching surface $s = 0$. For a second order system *S* is defined as [11, 12]:

$$s = \dot{e} + \lambda e \quad (15)$$

Where $e = x_d - x$ and x_d is the desired state. λ is a constant. $sign(s)$ is a *sign* function, which is defined as:

$$sign(s) = \begin{cases} -1 & s < 0 \\ 1 & s > 0 \end{cases} \quad (16)$$

The control strategy adopted here will guarantee the system trajectories move toward and stay on the sliding surface $s = 0$ from any initial condition if the following condition meets:

$$s\dot{s} \le -\eta \quad (17)$$

Where η is a positive constant that guarantees the system trajectories and hit the sliding surface in finite time [6, 9].

Using a *sign* function often causes chattering in practice. One solution is to introduce a boundary layer around the switch surface [9, 12, 13]:

$$u = u_s + u_{eq} \quad (18)$$

Where:

$$u_s = k \cdot sat\left(s/\xi\right) \quad (19)$$

Where the constant factor ξ defines the thickness of the boundary layer. $sat\left(s/\xi\right)$ is a saturation function that is defined as:

$$sat\left(s/\xi\right) = \begin{cases} sign\left(\dfrac{s}{\xi}\right) & \left|\dfrac{s}{\xi}\right| \ge 1 \\ \dfrac{s}{\xi} & \left|\dfrac{s}{\xi}\right| < 1 \end{cases} \quad (20)$$

The diagram of u_s versus s/ξ is shown in Fig. 2.

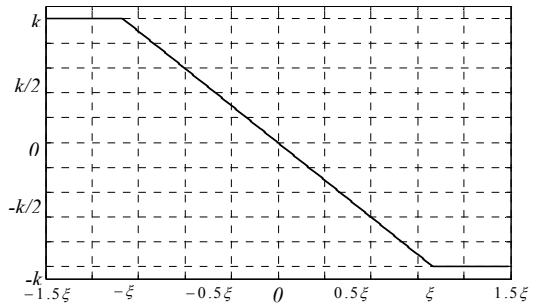


Fig. 2. The discontinuous control action of the SMC control law ($u_s = ksat(s/\xi)$)

III.1. *Design of sliding mode current controllers*

The currents loop is often the inner regulated loop in a field oriented controlled induction motor drive, and the overall performance of the drive depends strongly on the performance of current control. Therefore, a precise and fast current control is essential to achieve high static and dynamic performance for the FOC of induction motors. If the actual stator currents are not adjusted precisely and instantaneously to the reference values, cross coupling will be caused between the motor torque and rotor flux. Thus, the performance of the FOC degrades [2, 11].

In this paper, we propose a current control method based on sliding mode control design. The proposed control design uses two sliding mode controllers to regulate the *d*-axis and *q*-axis stator currents respectively. The design of the controllers consists of two steps.

Firstly, we define sliding surfaces $s = [s_1 \quad s_2] = 0$ as follows:

$$s_1 = i_{ds}^* - i_{ds} \quad (21)$$

$$s_2 = i_{qs}^* - i_{qs} \quad (22)$$

Where i_{ds}^* and i_{qs}^* are the reference values of the *d*-axis and *q*-axis stator currents, respectively. If the system stays stationary on the surface, then we can obtain $s_1 = s_2 = 0$. Substituting (21) and (22) into $s_1 = 0$ and $s_2 = 0$ yields

$$i_{ds} = i_{ds}^* \text{ and } i_{qs} = i_{qs}^* \quad (23)$$

Secondly, we design the voltage control law, which forces the system to move on the sliding surface in a finite time, as follows:

$$V_{ds}^* = V_{ds}^{equ} + k_1 \cdot sat(s_1/\xi_1) \quad (24)$$

$$V_{qs}^* = V_{qs}^{equ} + k_2 \cdot sat(s_2/\xi_2) \quad (26)$$

Where V_{ds}^{equ} and V_{qs}^{equ} are the equivalent control actions, and are defined as:

$$V_{ds}^{equ} = \sigma L_s \left(i_{ds}^* + \frac{1}{\sigma L_s}\left(R_S + R_r \left(\frac{L_m}{L_r}\right)^2 \right) i_{ds} - w_e . i_{qs} - \frac{L_m . R_r}{\sigma L_s L_r^2}\phi_r^* \right) \quad (27)$$

$$V_{qs}^{equ} = \sigma L_s . [i_{qs}^* + \omega_e . i_{ds} + \frac{1}{\sigma L_s}\left(R_s + R_r \left(\frac{L_m}{L_r}\right)^2 \right) i_{qs} + \frac{L_m}{\sigma L_s L_r}\phi_r^* \omega_r] \quad (28)$$

To verify the stability conditions, parameters k_1 and k_2 must be positives.

III.2. *Design of sliding mode speed controller*

To control the speed of the induction machine, the sliding surface is defined as follows:

$$s(\omega) = \omega_r^* - \omega_r \quad (29)$$

The derivative of the sliding surface can be given as:

$$\dot{s}(\omega_r) = \dot{\omega}_r^* - \dot{\omega}_r \quad (30)$$

Taking account the mechanical equation of the induction motor defined in the system of equations (1), the derivative of sliding surface becomes:

$$\dot{S}(\omega_r) = \dot{\omega}_r^{\,*} - \left(\frac{3}{2} \frac{P^2 L_m \phi_{dr}^{*}}{J L_r} . i_{qs} - \frac{f_c}{J} \dot{\omega}_r - \frac{P}{J} T_l \right) \quad (31)$$

We take

$$i_{qs} = i_{qs}^{equ} + i_{qs}^{n} \quad (32)$$

During the sliding mode and in permanent regime, we have $s(\omega_r) = 0$, $\dot{s}(\omega_r) = 0$, the equivalent control action can be defined as follows:

$$i_{qs}^{equ} = \frac{2}{3} \frac{J L_r}{P^2 L_m \phi_{dr}^{*}} \left(\dot{\omega}_r^{*} + \frac{f_c}{J} \omega_r + \frac{P}{J} T_l \right) \quad (33)$$

The discontinuous control action can be given as:

$$i_{qs}^{n} = k_{iqs} \cdot sat\left(s(\omega_r)/\xi_{\omega}\right) \quad (34)$$

To verify the system stability condition, the factor k_{iqs} must be positive.

IV. FUZZY SLIDING MODE CONTROL

The disadvantage of sliding mode controllers is that the discontinuous control signal produces chattering dynamics; chatter is aggravated by small time delays in the system. In order to eliminate the chattering phenomenon, different schemes have been proposed in the literature. However, this does not solve the problem completely. In this section, a fuzzy sliding surface is introduced to develop a sliding mode controller, where the expression $k \cdot sat(s/\xi)$ of all sliding mode controllers is replaced by a fuzzy system mechanism for reduce the chattering phenomenon. This approach shows that a particular fuzzy controller is an extension of an SMC with boundary layer [13].

Because the data manipulated in the fuzzy inference mechanism is based on fuzzy set theory, the associated fuzzy sets involved in the fuzzy control rules are defined as follows:

BN : Big Negative	**Bigger**
MN : Medium Negative	**Big**
ZE : Zero	**Medium**
MP : Medium Positive	**Small**
BP : Big Positive	**Smaller**

Since only five fuzzy subsets, BN, MN, ZE, MP and BP, are defined for s, the fuzzy inference mechanism contains five rules for the FLC output. The resulting fuzzy inference rules for the output variable u_n are as follows:

Rule 1: **IF** s is BN **THEN** u_n is Bigger

Rule 2: **IF** s is MN **THEN** u_n is Big

Rule 3: **IF** s is ZE **THEN** u_n is Medium

Rule 4: **IF** s is MP **THEN** u_n is Small

Rule 5: **IF** s is BP **THEN** u_n is Smaller

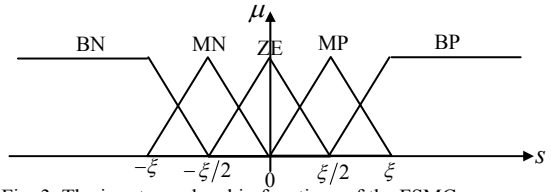


Fig. 3. The input membership functions of the FSMC

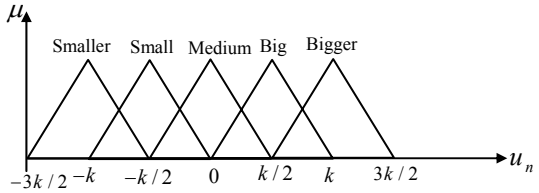


Fig. 4. The output membership function of the FSMC

Fig. 5 shows the result of a defuzzified output u_n for a fuzzy input s.

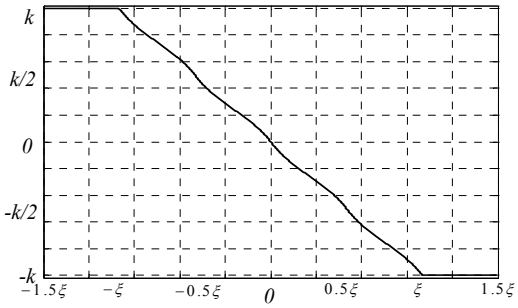


Fig. 5. The discontinuous control action of the fuzzy sliding mode controller

In order to control the speed and stator currents of the induction motor, the three discontinuous control actions of the outer- and inner-loops are replaced by fuzzy logic controllers.

The membership functions of input and output fuzzy sets are depicted in Figs. 6 and 7. In this study, the triangular membership functions and center average defuzzification method are adopted, as they are computationally simple, intuitively plausible, and most frequently used in the opening literatures

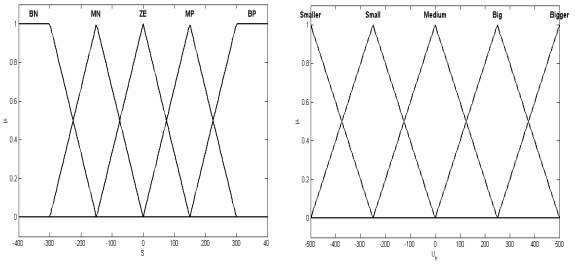


Fig. 6. Membership functions of the inputs s_1, s_2 and outputs V_{as}^{n}, V_{ds}^{n} of FSMC current controllers

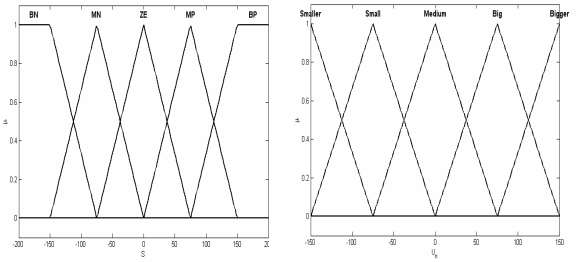


Fig. 7:.Membership functions of the input s and output i_{qs}^{n} FSMC speed controller.

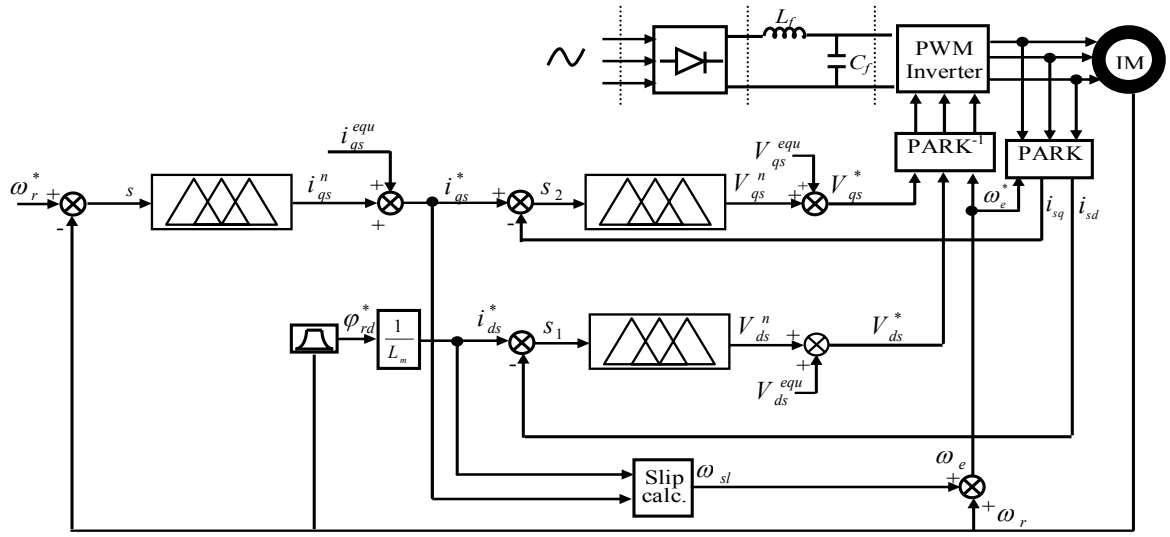


Fig. 8: The block diagram of proposed fuzzy sliding mode speed and currents control of induction motor

V. SIMULATION RESULTS

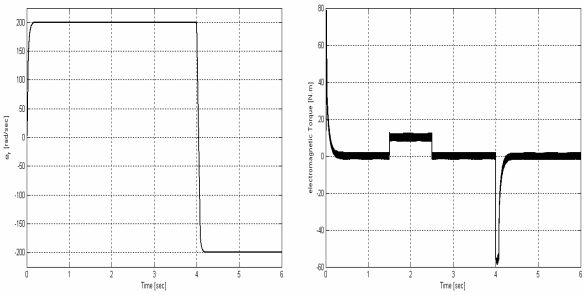
To prove the rightness and effectiveness of the proposed control scheme, we apply the designed controllers to the speed control of the induction motor. The induction motor is a three phase, *Y* connected, four pole, 1.5 kW, 1428min^{-1} 220/380V, 50Hz. The machine parameters are given in [14]. The configuration of the overall control system is shown in Fig. 08. It mainly consists of an induction motor, a ramp comparison current-controlled pulse width modulated (PWM) inverter, a slip angular speed estimator, an inverse park, indirect field oriented control bloc based on fuzzy sliding mode current controller, and an outer speed feedback control loop contains on a fuzzy sliding mode controller.

Fig. 9 shows the disturbance rejection of fuzzy sliding mode controller when the machine is operated at 200 [rad/sec] under no load and a nominal load disturbance torque (10 N.m) is suddenly applied and eliminated at 1.5sec, 2.5ec respectively, followed by a reversed reference (-200rad/sec) at 4sec. The fuzzy sliding mode controller rejects the load disturbance very rapidly with a negligible steady state error.

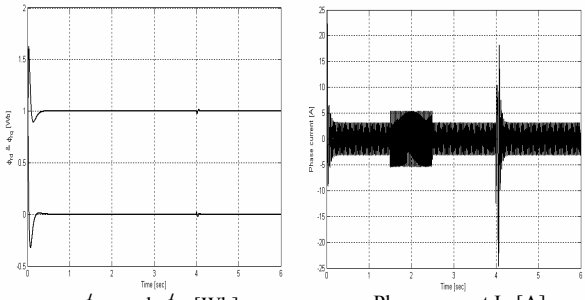
This controller rejects the load disturbance very rapidly with no overshoot and with a negligible steady state error more than the classical sliding mode controller and the PI controller which is shown clearly in fig. 12.

Fig. 10 and 11 show a comparison between the classical field oriented control using PI controllers, the sliding mode current controllers and which based on fuzzy sliding mode current regulators. It shows clearly that the decoupling control is more maintained for the fuzzy sliding mode design than which obtained by a classical sliding mode and PI currents controllers.

The simulation results show that the proposed scheme gave satisfactory performances thus judges that the controller is robust.



Rotor speed [rad/sec] Torque [N.m]



ϕ_{rd} and ϕ_{rq} [Wb] Phase current Ia [A]

Fig. 9. Simulated results of fuzzy sliding mode speed and currents control of induction motor

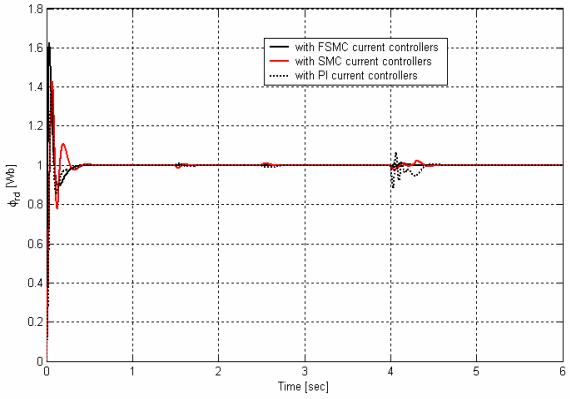


Fig. 10. Simulated results of the comparison between the decoupling obtained by PI, SMC and FSMC for IM.

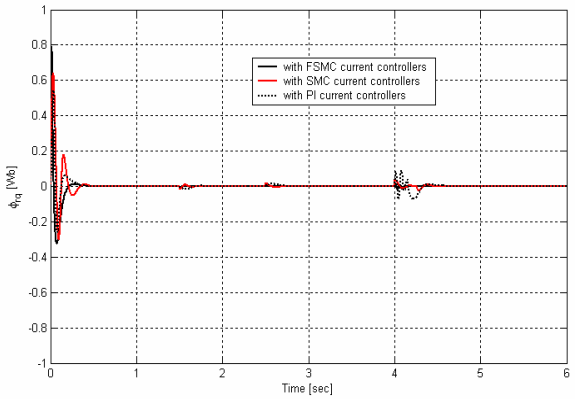


Fig. 11. Simulated results of the comparison between the decoupling obtained by PI, SMC and FSMC for IM.

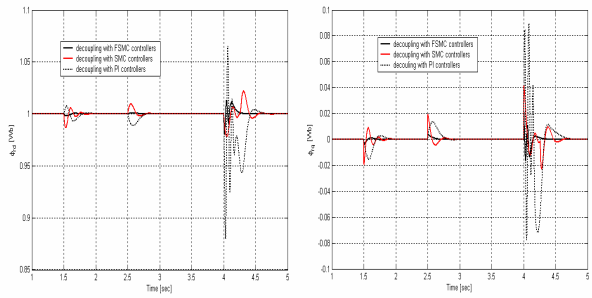


Fig. 12. Zoomed responses of decoupling obtained by PI, SMC and FSMC for IM.

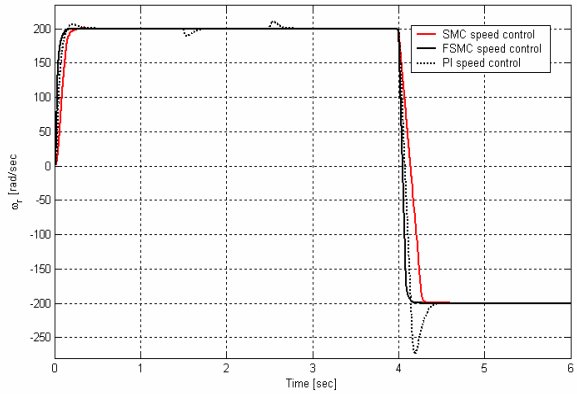


Fig. 13. Simulated results of the comparison between the PI, SMC and FSMC speed control of induction motor

VI. CONCLUSION

In this work, we have presented a fuzzy sliding mode controller for speed and currents control of induction motor. This study has successfully demonstrated the design of the fuzzy sliding mode for the speed control of an induction motor and the indirect field orientation control design based on fuzzy sliding mode control combination. The Proposed scheme has presented satisfactory performances (no overshoot, minimal rise time, best disturbance rejection) for time-varying external force disturbances. The simulation results obtained have confirmed the excellent decoupling maintain and the efficiency of the proposed scheme. Finally, the effectiveness of the PI, classical sliding mode with boundary layer controller and the fuzzy sliding mode controller has been verified through simulation.

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Improved Linearity Active Resistor with Negative Equivalent Resistance

Cosmin Popa[1]

Abstract - An original improved linearization technique for a CMOS active resistor will be further presented. The main advantages of the original proposed implementation are the improved linearity, the small area consumption and the improved frequency response. The new method for linearizing the $I(V)$ characteristic of the active resistor will be based on a parallel connection of two quasi-ideal circuits opposite excited and different biased, having the result of improving the circuit linearity with about an order of magnitude. Because of this original design technique, the circuit linearity is not affected by the second-order effects that alter the MOS transistor operation. The reduced complexity obtained by using a FGMOS transistor will be made maintaining the compatibility with classical technologies (the classical FGMOS device could be replaced by an original equivalent circuit using exclusively classical MOS devices). The frequency response of the circuit is very good as a result of operating all MOS transistors in the saturation region. In order to design a circuit having a negative equivalent resistance, an original method specific to the proposed implementation of the active resistor circuit will be presented. The circuit is implemented in $0.35\mu m$ CMOS technology, the SPICE simulation confirming the theoretical estimated results and showing a linearity error under a percent for an extended input range $(\pm 500mV)$ and for a small value of the supply voltage $(\pm 3V)$.

Keywords: active resistor circuit, linearity error, complementary functions, second-order effects

I. INTRODUCTION

CMOS active resistors are very important blocks in VLSI analog designs, mainly used for replacing the large value passive resistors, with the great advantage of a much smaller area occupied on silicon. Their utilisation domains includes amplitude control in low distortion oscillators, voltage controlled amplifiers and active RC filters. These important applications for programmable floating resistors have motivated a significant research effort for linearising their current-voltage characteristic.

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An important class of these circuits, referring to the active resistors with controllable negative equivalent resistance, covers a specific area of VLSI designs, finding very large domains of applications such as the cancelling of an operational amplifier load or the design of Deboo integrators with improved performances.

The first generation of MOS active resistors [1], [2] used MOS transistors working in the linear region. The main disadvantage is that the realised active resistor is inherently nonlinear and the distortion components were complex functions on MOS technological parameters.

A better design of CMOS active resistors is based on MOS transistors working in saturation [3], [4]. Because of the quadratic characteristic of the MOS transistor, some linearisation techniques were developed in order to minimize the nonlinear terms from the current-voltage characteristic of the active resistor. Usually, the resulting linearisation of the $I-V$ characteristic is obtained by a first-order analysis. However, the second-order effects which affect the MOS transistor operation (mobility degradation, bulk effect and short-channel effect) limits the circuit linearity introducing odd and even-order distortions, as shown in [4]. For this reason, an improved linearisation technique has to be design to compensate also the nonlinearities introduced by the second-order effects.

II. THEORETICAL ANALYSIS

The original idea for implementing a linear current-voltage characteristic of the active resistor, similar to the characteristic of a classical passive resistor is to use two complementary functions, the desired linearity being obtained by a mutual compensation of their nonlinearities. The proposed circuit presents the important advantage of a reduced silicon area with respect to classical implementations of an active resistors, based on symmetrical structures. Because of the requirements for a good frequency response, only MOS transistors working in saturation could be used. For this reason, the original choose is to use the quadratic and the square-root dependencies as complementary functions. So, square and square-root

circuits must be designed based exclusively on saturated MOS devices.

The application of a new method of inversing the current passing through the two pins of the active resistor allows to obtain a circuit having a controllable negative resistance.

In order to improve the circuit performances by using the FGMOS device and to maintain, also, the compatibility with classical CMOS technologies, an original equivalent FGMOS device will be proposed.

A. *The block diagram of the FGMOS active resistor*

The structure of the proposed active resistor is based on three important blocks:

- a voltage-current squarer X^2, implementing the function $I_{OUT} = K(V_X - V_Y)^2 / 4$;
- a current-pass circuit I;
- a current square-root circuit $\sqrt{\ }$, for obtaining $I_{XY} = 2\sqrt{I_{OUT} I_O}$;

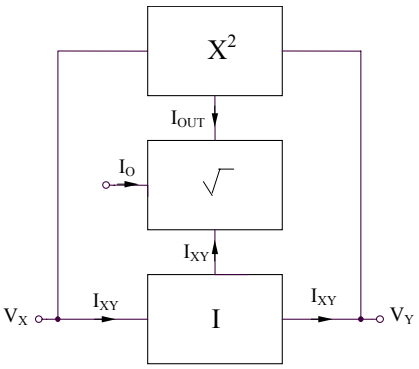

Fig. 1. The block diagram of the resistor

Because I_{XY} current is proportional to the square-root of I_{OUT} and I_O currents, while I_{OUT} current is proportional to the square of the differential input voltage $V_X - V_Y$, the result will be a linear relation between the differential voltage across the two pins, $V_X - V_Y$ of the active resistor and the current passing through it, I_{XY}. The great advantage of the proposed circuit is that, in a first-order analysis, no superior-order terms will appear in the $I(V)$ characteristic of the active resistor.

B. *The equivalent FGMOS transistor*

The FGMOS transistor is a MOS transistor whose gate is floating (Fig. 2a), while the symbolical representation of this device is shown in Fig. 2b. The first silicon layer over the channel represents the floating-gate and the second polysilicon layer, located over the floating-gate implements the multiple input gates. This floating-gate is capacitive coupled to the multiple input gates. The drain current of a FGMOS transistor with n-input gates in the saturation region is given by the following relation:

$$I_D = \frac{K}{2}\left[\sum_{i=1}^{n} k_i (V_i - V_S) - V_T\right]^2 \qquad (1)$$

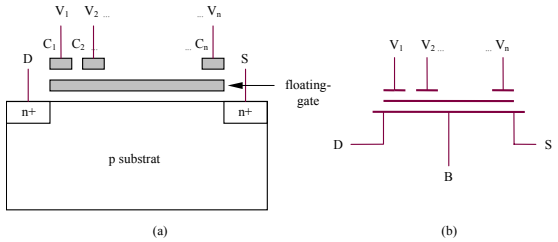

Fig. 2. (a) The basic structure of a n-channel FGMOS transistor; (b) symbolic representation

The great limitation of using FGMOS devices is that they are available only in few CMOS technologies, restricting the area of utilization of the circuits based on these transistors. The original idea for replacing the classical FGMOS device with two inputs by five MOS transistors is presented in Fig. 3.

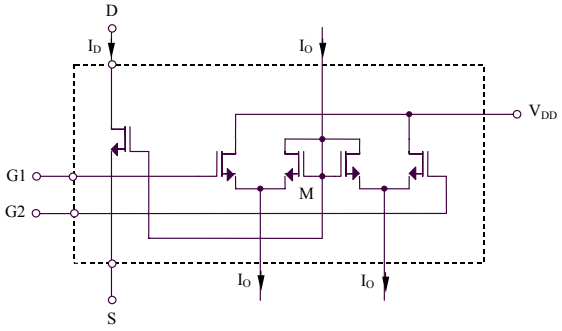

Fig. 3. The equivalent circuit of the FGMOST

The four pins of the equivalent FGMOS device are, respectively: D (drain), S (source), $G1$ and $G2$ (gates). Because of the connection of the four MOS transistors from the right part of the circuit, the M potential is equal to the arithmetic mean of the gates' potentials, $V_M = (V_{G1} + V_{G2})/2$. For this reason, the drain current of the entire equivalent FGMOS device from Fig. 3 will have the following expression:

$$I_D = \frac{K}{2}\left(\frac{V_{G1} + V_{G2}}{2} - V_S - V_T\right)^2 \qquad (2)$$

similar to the equation which characterizes the operation of the classical FGMOS transistor.

The original proposed implementation presents the great advantage of avoiding the utilization of any resistor for computing the arithmetic mean, with the result of reducing the circuit area and of improving the achieved accuracy. The circuit from Fig. 3 could replace, in the practical implementation, the FGMOS transistors, symbolic used in Figs 4 and 5.

C. *The voltage-current Squarer*

The new proposed squarer is based on the quasi - symmetrical structure from Fig. 4.

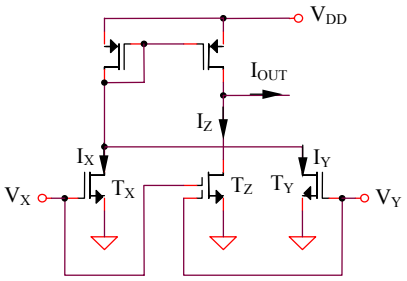

Fig. 4. The voltage-current squarer

The output current expression has a linear dependence on the drain currents of T_X, T_Y and T_Z transistors:

$$I_{OUT} = I_X + I_Y - I_Z \tag{3}$$

Considering a saturation operation of all MOS devices from Fig. 4 and supposing that the area of T_Z is twice that the T_X and T_Y areas, I_{OUT} will have the following dependence on the differential input voltage $V_X - V_Y$:

$$I_{OUT} = \frac{K}{4}(V_X - V_Y)^2 \tag{4}$$

D. *The square-root circuit*

The square-root circuit represents also a perfect symmetrical structure (Fig. 5), using MOS transistors and a FGMOS device (T) working in saturation for improving the circuit frequency response.

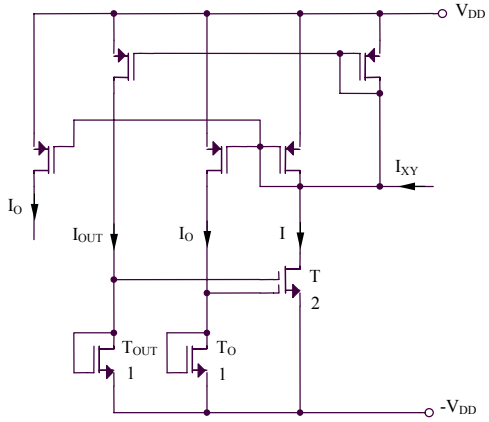

Fig. 5. The square-root circuit

Considering an aspect ratio of the FGMOS transistor fourth time greater than the aspect ratio of all the other devices from Fig. 5, the drain current I will have the following expression:

$$I = \frac{4K}{2}\left(\frac{V_{GS_{OUT}} + V_{GS_O}}{2} - V_T\right)^2 \tag{5}$$

where $V_{GS_{OUT}}$ and V_{GS_O} represent the gate-source voltages of T_{OUT} and T_O transistors. The output current expression is linearly dependending on the drain currents of T_{OUT}, T_O and T transistors:

$$I_{XY} = I - I_{OUT} - I_O \tag{6}$$

resulting a square-root dependence of the output current on the two input currents:

$$I_{XY} = 2\sqrt{I_{OUT} I_O} \tag{7}$$

E. *The current-pass circuit*

The necessity of designing this circuit is derived from the requirement that the same current to pass between the two output pins, X and Y. The implementation in CMOS technology of this circuit is very simple, consisting in a simple and a multiple current mirrors (Fig. 6).

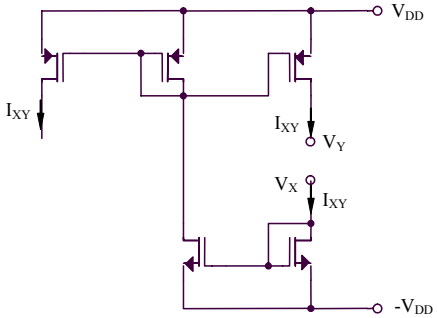

Fig. 6. The current-pass circuit

F. *The linear characteristic of the active resistor*

Because of the complementary characteristics (4) and (7) of the squaring and square-root circuits, the current-voltage characteristic $I_{XY}(V_X - V_Y)$ of the active resistor will be perfectly linear.

$$I_{XY} = \sqrt{KI_O}(V_X - V_Y) \tag{8}$$

being possible to define an equivalent resistance between X and Y pins as follows:

$$R_{ECH.} = \frac{V_X - V_Y}{I_{XY}} \tag{9}$$

It results $R_{ECH.} = 1/\sqrt{KI_O}$. The great advantage of the previous presented circuit is that the value of the equivalent active resistance could be very easily controlled by modifying the reference current I_O. For

usual values of K and I_O parameters, R_{ECH}. resistance covers about three decades $(1k\Omega - 1M\Omega)$, equivalent with an important reduction of the silicon occupied area, especially for large values of the active resistance simulated by the circuit from Fig. 1.

G. *The second-order effects*

The relation (8) of the current-voltage characteristic for the active resistor circuit having the block diagram presented in Fig. 1 is slightly modified by the second-order effects that affect the MOS transistor operation, modeled by the following relations: channel-length modulation (10) and mobility degradation (11)).

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{10}$$

$$K = \frac{K_0}{[1 + \theta_G(V_{GS} - V_T)](1 + \theta_D V_{DS})} \tag{11}$$

Taking into account these second-order effects and considering that the design condition $\lambda = \theta_D$ is fulfilled, the operation of the voltage-current squarer from Fig. 4 will be affected by a small error that will be quantitative evaluated by:

$$\varepsilon = -\frac{K\theta_G}{4}(V_X - V_Y)^2\left(\frac{V_{CM}}{2} - V_T\right) \tag{12}$$

V_{CM} being the common-mode input voltage of the current-voltage squarer. The great advantage of this implementation is that the additional error ε is proportional to the square of the differential input voltage $V_X - V_Y$, so no superior-order terms will appear in the $I - V$ characteristic of the CMOS active resistor as a result of the second-order effects. The only error introduced by these undesired effects will be a small changing of the equivalent resistance (no linearity degradation for the proposed circuit).

$$R_{ECH} = \frac{1}{\sqrt{KI_O}}\left[1 + \frac{\theta_G}{4}(V_{CM} - 2V_T)\right] \tag{13}$$

Small nonlinearities could be identified for large values of the active resistance, equivalent with small values of the reference current.

H. *The active resistor with controllable negative equivalent resistance*

The great advantage of the proposed implementation shown in Fig. 1 is that a circuit with a negative equivalent resistance could be very easily obtained by a minor change in the current-pass circuit presented in Fig. 6. The modified implementation of the current-pass circuit proposed for obtaining an active resistor with a negative equivalent resistance is presented in Fig. 7.

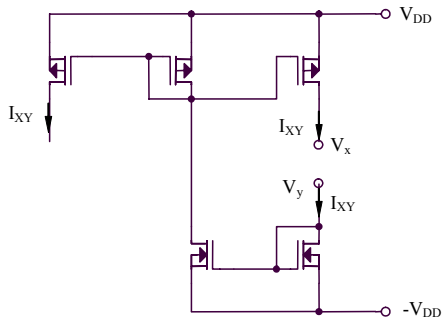

Fig. 7. The current-pass circuit for the active resistor with a negative equivalent resistance

The resulting expression of the active resistance will be $R'_{ECH} = -R_{ECH} = -1/\sqrt{KI_O}$. The advantage of the good controlability of R_{ECH} by the current I_O is still valuable, even for the negative resistance active resistor.

III. SIMULATED RESULTS

The low-power CMOS active resistor was implemented in $0.35\mu m$ CMOS technology. The SPICE simulation $I_{XY}(V_X - V_Y)$ of the active resistor is presented in Fig. 8. The maximum nonlinearity error of the active resistor for limited input voltage range ($|V_X - V_Y| \le 500mV$) is less than a percent.

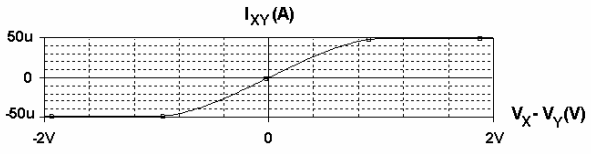

Fig. 8. The SPICE simulation $I_{XY}(V_X - V_Y)$

IV. CONCLUSIONS

A new active resistor circuit has been presented in this paper. The main advantages of the original proposed implementation are the improved linearity, the small area consumption and the improved frequency response. Because of an original design technique, the circuit linearity is not affected by the second-order effects that alter the MOS transistor operation. The reduced complexity obtained by using a FGMOS transistor was made maintaining the compatibility with classical technologies (the classical FGMOS device could be replaced by an original equivalent circuit using exclusively classical MOS devices). The frequency response of the circuit is very good as a result of operating all MOS transistors in the saturation region. The circuit was implemented in $0.35\mu m$ CMOS technology, the SPICE simulation confirming the theoretical estimated results and showing a linearity error under a percent for an

extended input range ($\pm 500mV$) and a small value of the supply voltage ($\pm 3V$). In order to design a circuit having a negative equivalent resistance, an original method specific to the proposed implementation of the active resistor circuit will be presented. In order to obtain a low-power operation of the proposed active resistors, the MOS active devices could be biased in weak inversion, while the complementary squaring/square-root functions must be replaced by logarithmical/exponential functions.

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Instability of Dc-Dc Converters at the Boundary Between CCM and Discontinuous Capacitor Voltage Mode

Corina M. Ivan[1], Dan Lascu[2] and Viorel Popescu[3]

Abstract – In this paper, the operating mode between Continuous Conduction Mode (CCM) and Discontinuous Capacitor Voltage Mode (DCVM) of dc-dc converters is investigated. A large-signal model for the switching network is obtained. The small-signal averaged model is derived, and it is used to obtain analytical expressions for the small-signal transfer functions, for the ĆUK, SEPIC and ZETA converters. It is shown that the transfer functions exhibit at least one right half-plane (RHP) pole. This pole cannot be eliminated by varying the circuit parameters. From this it is concluded that the operating mode between CCM and DCVM is unstable and unusable.

Keywords: boundary conduction mode, discontinuous capacitor voltage mode, averaged switch models.

I. INTRODUCTION

Occurrence of discontinuous modes in PWM dc-dc converters can be easily explained taking into account some topological aspects. In [1] it is shown that the transistor and the diode in every PWM converter form:

- a loop L, with possibly the supply voltage, V_g, and a (possibly empty) set of capacitors;
- a cut-set C, with a non-empty set of inductors.

In DCVM the small ripple assumption is invalid for at least one capacitor in the loop L. A necessary and sufficient condition for the occurrence of DCVM is the existence of at least one capacitor in the loop L, obviously different from the output filter capacitor. Therefore it is clear that DCVM cannot be related to BUCK, BOOST or BUCK-BOOST converters, as these converters contain a single capacitor for filtering the output voltage. On the other side, ĆUK, SEPIC and ZETA converters can enter DCVM mode when the small ripple assumption is removed from the energy storage capacitor contained in the loop L.

The large-signal averaged switch model of the switch network in pulse width modulated (PWM) dc-dc converters operating at the boundary between CCM and DCVM is derived in Section 2. In Section 3 the small-signal averaged switch model is derived and it is used to obtain analytical expressions for the small-signal transfer functions. A discution, based on the small-signal transfer functions, regarding the stability of this operating mode is also presented. In Section 4 the instability is verified through CASPOC simulation. Conclusions are presented in Section 5.

II. AVERAGED SWITCH MODEL FOR BOUNDARY CONDUCTION MODE BETWEEN CCM AND DCVM

Let us examine the operation at the Boundary Conduction Mode between CCM and DCVM of the ĆUK converter, and follow the averaged switch modelling approach [2] to derive an equivalent circuit that models the averaged (over one switching period, T_s) terminal variables of the switch network.

As it is known, for the inductor currents, i_{L1} and i_{L2} the negligible ripple assumption is still valid, and therefore, they can be admitted constant during one switching cycle. However, for the capacitor voltage, v_{C1} the small ripple assumption is not valid, while v_{C2} is assumed to be constant as it is in fact the output voltage.

The terminal variables of the switch network, i_1, i_2, v_1 and v_2 are defined in Fig. 1.

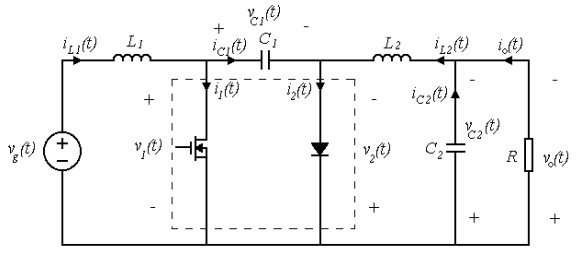

Fig. 1. The CUK converter, with the switch network identified.

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The switch network voltage and current waveforms are presented in Fig. 2.

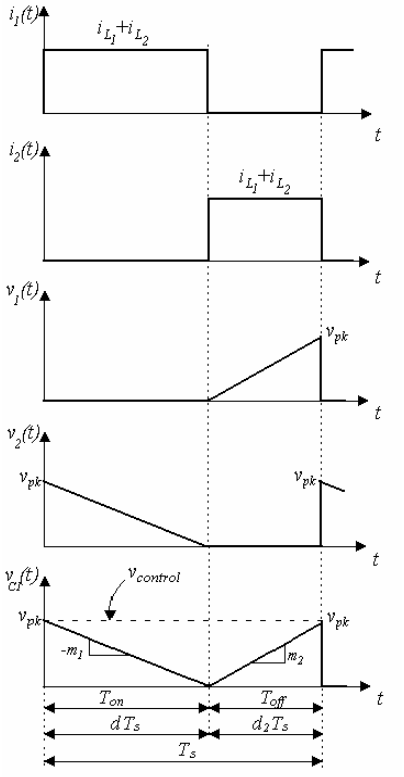

Fig. 2. The switch network and capacitor C_1 waveforms.

The peak value of the capacitor voltage, v_{pk} is equal to the control input, $v_{control}$. During the transistor on-time, in the first subinterval, the capacitor voltage decreases from the peak value with a slope $m_1 = \frac{i_{L2}}{C_1}$ until it reaches zero. At this time, the transistor is turned off, and the diode starts to conduct. In the second subinterval, during the diode on-time, the capacitor voltage increases from zero with a slope $m_2 = \frac{i_{L1}}{C_1}$ to the peak value. Therefore, the averaged value over one switching period, T_s, of the capacitor voltage, v_{C1} is given by:

$$< v_{C1} >= \frac{1}{2} < v_{pk} >= \frac{1}{2} < v_{control} > \qquad (1)$$

By averaging the waveforms in Fig. 2 over one switching period, T_s, and taking Eqn. (1) into account, the averaged switch network variables are found as:

$$< i_1(t) >= \frac{T_{on}}{T_s}(< i_{L1} > + < i_{L2} >) \qquad (2)$$

$$< i_2(t) >= \frac{T_{off}}{T_s}(< i_{L1} > + < i_{L2} >) \qquad (3)$$

$$< v_1(t) >= \frac{T_{off}}{T_s}\frac{< v_{control} >}{2} \qquad (4)$$

$$< v_2(t) >= \frac{T_{on}}{T_s}\frac{< v_{control} >}{2} \qquad (5)$$

From Eqns. (2)-(5) the relations between the switch network variables can be written as:

$$< v_1(t) >= \frac{T_{off}}{T_{on}} < v_2(t) > \qquad (6)$$

$$< i_2(t) >= \frac{T_{off}}{T_{on}} < i_1(t) > \qquad (7)$$

From Eqns. (6) and (7) it is obvious that:

$$< i_1(t) >< v_1(t) >=< i_2(t) >< v_2(t) >=< p(t) > \qquad (8)$$

which is expected, as we considered ideal and therefore lossless active and pasive switches. In fact, Eqn. (8) denotes instantaneous power conservation in the switch network.

Based on Eqn. \ref{av5} and \ref{av6} the averaged large-signal switch model can be constructed, as in Fig. 3.

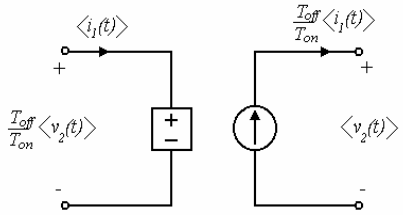

Fig. 3. The boundary mode averaged large-signal model.

The averaged switch models of the ĆUK, SEPIC and ZETA converters are shown in Fig. 4.

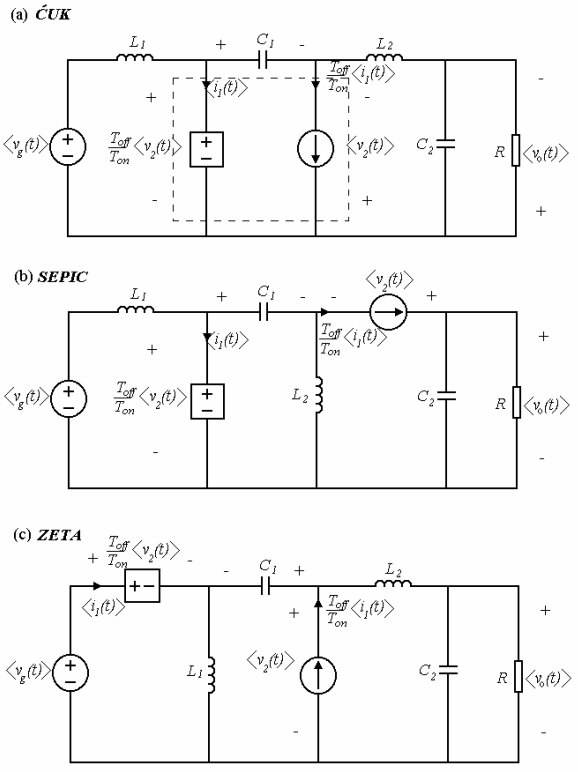

Fig. 4. Averaged large-signal equivalent circuits of the ĆUK, SEPIC and ZETA converters operating in boundary mode.

The steady-state average value for any converter are found by setting all averaged waveforms to their quiescent values and letting the inductors and capacitors become a short-circuit and an open circuit respectively. From Fig. 4 it can be observed that the dc conversion ratio, M, is equal to:

$$M = \frac{V_o}{V_g} = \frac{V_2}{V_1} = \frac{I_1}{I_2} \tag{9}$$

From Fig. 2 we have:

$$D = \frac{T_{on}}{T_s} \tag{10}$$

and

$$D_1 = 1 - D = \frac{T_{off}}{T_s} \tag{11}$$

where D is the steady-state duty cycle.

Using the Eqn. (6), (10) and (11), from Eqn. (9) we get:

$$M = \frac{D}{1-D} \tag{12}$$

III. SMALL-SIGNAL MODEL FOR BOUNDARY CONDUCTION MODE BETWEEN CCM AND DCVM

Small-signal models are constructed by perturbation and linearization of the large-signal averaged expressions. Let:

$$\begin{aligned} v_1(t) &= V_1 + \hat{v}_1 \\ i_1(t) &= I_1 + \hat{i}_1 \\ v_2(t) &= V_2 + \hat{v}_2 \\ i_2(t) &= I_2 + \hat{i}_2 \\ v_{control}(t) &= V_{control} + \hat{v}_{control} \end{aligned} \tag{13}$$

Perturbation of the Eqn. (8) leads to:

$$\left(I_1 + \hat{i}_1\right)\left(V_1 + \hat{v}_1\right) = \left(I_2 + \hat{i}_2\right)\left(V_2 + \hat{v}_2\right) \tag{14}$$

The dc terms of both sides of this equation are equal from the steady-state operation:

$$V_1 I_1 = V_2 I_2 \tag{15}$$

Taking Eqn. (11) into account and neglecting the product of two small perturbations, Eqn. (10) becomes:

$$I_1 \hat{v}_1 + \hat{i}_1 V_1 = I_2 \hat{v}_2 + \hat{i}_2 V_2 \tag{16}$$

From Eqn. (12) the solution for the small-signal switch network output voltage, $\hat{v}_2$, is given by:

$$\hat{v}_2 = \frac{I_1}{I_2}\hat{v}_1 + \frac{V_1}{I_2}\hat{i}_1 - \frac{V_2}{I_2}\hat{i}_2 \tag{17}$$

From the Eqn. (4) and (5) it can be observed that

$$< v_1(t) > + < v_2(t) > = \frac{1}{2} < v_{control} > \tag{18}$$

Perturbating Eqn. (18) we get:

$$\hat{v}_1 + \hat{v}_2 = \frac{1}{2}\hat{v}_{control} \tag{19}$$

In Eqn. (17) $\hat{v}_1$ is replaced from Eqn. (19), which gives:

$$\hat{v}_2 = \left(\frac{1}{1+\frac{I_1}{I_2}}\right)\left(\frac{I_1}{2I_2}\hat{v}_{control} + \frac{V_1}{I_2}\hat{i}_1 - \frac{V_2}{I_2}\hat{i}_2\right) \tag{20}$$

From Eqn. (19) and (20) the small-signal switch network input voltage $\hat{v}_1$ is given by:

$$\hat{v}_1 = \left(\frac{1}{1+\frac{I_1}{I_2}}\right)\left(\frac{1}{2}\hat{v}_{control} - \frac{V_1}{I_2}\hat{i}_1 + \frac{V_2}{I_2}\hat{i}_2\right) \tag{21}$$

By using the dc relations $V_2 = MV_1$, $I_1 = MI_2$, $I_2 = \frac{V_2}{R}$, Eqn. (20) and (21) become:

$$\begin{cases} \hat{v}_1 = \dfrac{1}{2(M+1)}\hat{v}_{control} - \dfrac{R}{M(M+1)}\hat{i}_1 + \dfrac{R}{M+1}\hat{i}_2 \\ \hat{v}_2 = \dfrac{M}{2(M+1)}\hat{v}_{control} + \dfrac{R}{M(M+1)}\hat{i}_1 - \dfrac{R}{M+1}\hat{i}_2 \end{cases} \tag{22}$$

Based on Eqn. (22) the small-signal switch model of the switch network can be constructed, as in Fig. 5.

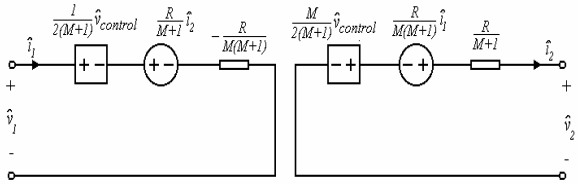

Fig. 5. The boundary mode small-signal model of the switch network.

The expressions of the small-signal model parameters are the same for both the ĆUK and for the SEPIC and ZETA converters.

The small-signal circuit model can be obtained by replacing the switch network with the two-port network described by Eqn. (22), as shown in Fig. 6, for the ĆUK, SEPIC and ZETA converters.

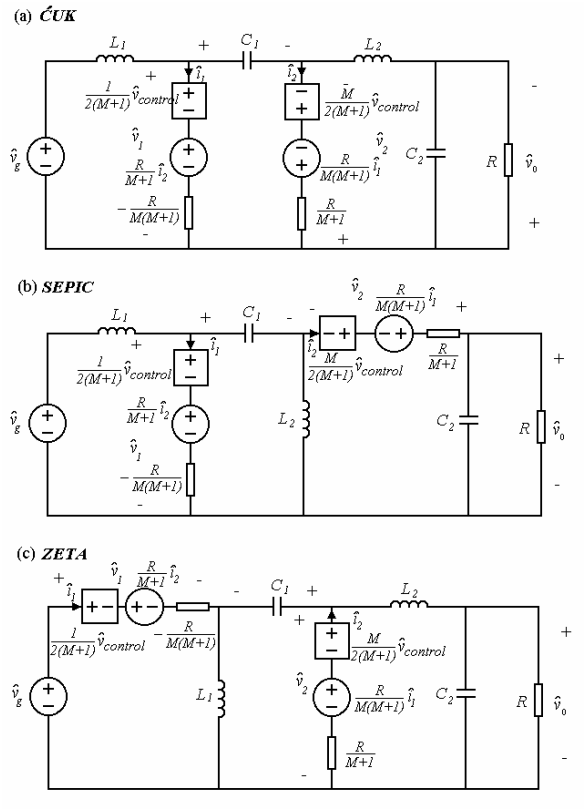

Fig. 6. Small-signal models of the ĆUK, SEPIC and ZETA converters.

By solving the small-signal equivalent circuits, the transfer functions can be found. For the ĆUK, SEPIC and ZETA converters, the transfer functions are given in Table 1.

It can be seen that the denominators of all transfer functions from Table 1 is a cubic polynomial. Its roots can be all three real, or one real and two compound numbers. In both cases, the free term is equal to the product of the roots, with the sign changed, which can be verified through a simple calculation. Therefore, if the free term has the opposite sign as against the s^3 term, as in the case of the transfer functions from Table 1, it results that all three roots are positive or the real root is positive respectively. It also can be observed that the sign of the free term does not depend on the circuit parameters. This means that the small-signal transfer functions exhibit at least one right half-plane (RHP) pole. This pole cannot be eliminated by varying the circuit parameters. From this it is concluded that the operating mode between CCM and DCVM is unstable, therefore unusable.

IV. SIMULATION RESULTS

In order to verify the results, a ĆUK converter and a SEPIC converter are examined. The component values are the following:

1. ĆUK converter: V_g = 20V, L_1 = 0,64mH, L_2 = 0,64m, R = 10Ω, C_1 = 90nF, C_2 = 800μF; V_o = 5V;
2. SEPIC converter: V_g = 15V, L_1 = 0,64mH, L_2 = 0,64m, R = 10Ω, C_1 = 56.8nF, C_2 = 100μF; V_o = 3.75V.

The poles of the transfer functions are, for the ĆUK converter: 37.517k, -71±1612i, and for the SEPIC converter: 37.633k, -566±4521i.

The capacitor voltage waveform for the ĆUK

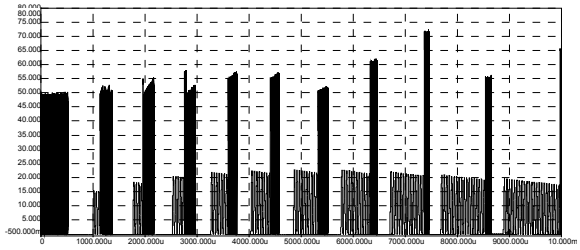

Fig. 7. The capacitor voltage waveform for the ĆUK converter.

The output voltage waveforms are shown in Fig. 8 (for the ĆUK converter) and in Fig. 9 (for the SEPIC converter). It can be observed the instability of this operating mode.

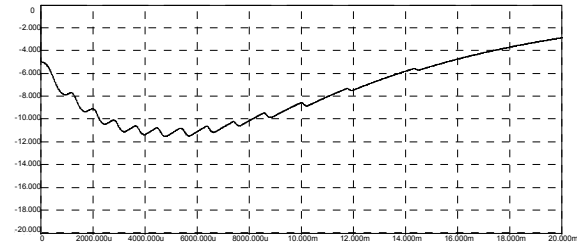

Fig. 8. The output voltage waveform for the ĆUK converter.

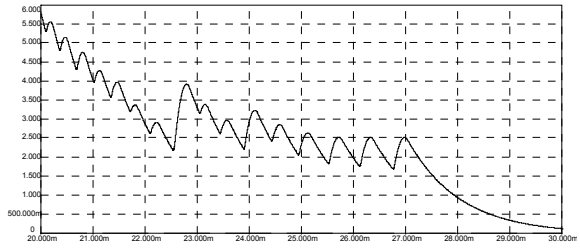

Fig. 9. The output voltage waveform for the SEPIC converter.

Table 1

Small-signal transfer functions
ĆUK
$G_{vc}(s)=\frac{\hat{v}_o}{\hat{v}_{control}}=\frac{\frac{1}{2}\left[1-sL_1\frac{M^2}{R}+s^2L_1C_1(M+1)\right]}{1-s\left[\frac{L_1M(M+2)}{R}-\frac{L_2}{R}\right]+s^2\left[-ML_1C_2+L_2C_2-\frac{L_1L_2M(M+1)}{R^2}\right]-s^3\frac{L_1L_2C_2M(M+1)}{R}}$
$G_{vg}(s)=\frac{\hat{v}_o}{\hat{v}_g}=\frac{1}{1-s\left[\frac{L_1M(M+2)}{R}-\frac{L_2}{R}\right]+s^2\left[-ML_1C_2+L_2C_2-\frac{L_1L_2M(M+1)}{R^2}\right]-s^3\frac{L_1L_2C_2M(M+1)}{R}}$
SEPIC
$G_{vc}(s)=\frac{\hat{v}_o}{\hat{v}_{control}}=\frac{\frac{1}{2}\left[1-sL_1\frac{M^2}{R}+s^2C_1(L_1+L_2)-s^3\frac{L_1L_2C_1M(M+1)}{R}\right]}{1-s\left[\frac{L_1M(M+2)}{R}-\frac{L_2}{R}\right]+s^2\left[-ML_1C_2+L_2(C_1+C_2)+L_2C_2-\frac{L_1L_2M(M+1)}{R^2}\right]-s^3\frac{L_1L_2(C_1+C_2)M(M+1)}{R}}$
$G_{vg}(s)=\frac{\hat{v}_o}{\hat{v}_g}=\frac{1}{1-s\left[\frac{L_1M(M+2)}{R}-\frac{L_2}{R}\right]+s^2\left[-ML_1C_2+L_2(C_1+C_2)+L_2C_2-\frac{L_1L_2M(M+1)}{R^2}\right]-s^3\frac{L_1L_2(C_1+C_2)M(M+1)}{R}}$
ZETA
$G_{vc}(s)=\frac{\hat{v}_o}{\hat{v}_{control}}=\frac{\frac{1}{2}\left[1-sL_1\frac{M^2}{R}+s^2L_1C_1(M+1)\right]}{1-s\left[\frac{L_1M(M+2)}{R}-\frac{L_2}{R}\right]+s^2\left[-ML_1C_2+L_2C_2-\frac{L_1L_2M(M+1)}{R^2}\right]-s^3\frac{L_1L_2C_2M(M+1)}{R}}$
$G_{vg}(s)=\frac{\hat{v}_o}{\hat{v}_g}=\frac{1+s^2L_1C_1(M+1)}{1-s\left[\frac{L_1M(M+2)}{R}-\frac{L_2}{R}\right]+s^2\left[-ML_1C_2+L_2C_2-\frac{L_1L_2M(M+1)}{R^2}\right]-s^3\frac{L_1L_2C_2M(M+1)}{R}}$

V. CONCLUSIONS

The operating mode between Continuous Conduction Mode (CCM) and Discontinuous Capacitor Voltage Mode (DCVM) of dc-dc converters is investigated. A large-signal model for the switching network of the pulse width modulated (PWM) dc-dc converters operating at the boundary CCM and DCVM is developed. The small-signal averaged model is derived, and it is used to obtain analytical expressions for the small-signal transfer functions, for the ĆUK, SEPIC and ZETA converters. It is shown that the transfer functions exhibit at least one right half-plane (RHP) pole. The RHP pole cannot be eliminated by varying the circuit parameters. From this it is concluded that the operating mode between CCM and DCVM is unstable and unusable. CASPOC simulations of the The ĆUK and the SEPIC converters are performed. The results confirm the instability of the operating mode between CCM and DCVM.

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Interpolation of linear track movements of modern industrial robots

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Abstract – Integration of linear track movements in the robot control is a significant part of the accuracy improvement process of modern robotics. For this, the linear track profile has to be analysed for getting a continous description of its inaccuracies for correcting the robot's end effector position for arbitrary points. This analysis bases in the first step on a discrete measurement of the linear track in special sampling points. In the second step an interpolation between the sampling points is done. In this article some of the possible interpolation methods for creating a continous description of the linear track were tested.
Keywords: industrial robot, accuracy, 7th axis, linear track, interpolation

I. INTRODUCTION

Modern robotics today deals with a great number of different applications. A great number of special functions or tasks are done by industrial robots. The field of using industrial robots ranges from picking or placing very small parts for electrical layouts to the painting or welding of jumbo jets. In each one of this varying types the demands on the robot are different and depending on single aspects like accuracy, time consumption or the costs.
One important fact is that in the past few years the demands of modern robotics have increased due to the ever growing demand for flexible automation. Flexible automation today expects highly accurate robotic systems. In this meaning not only the robot, but the complete system consisting of robot and its peripherals have to fulfill the extensive requirements. But against this demand for highly accurate robotic systems the requested flexibility in the used systems is increasing rapidly.
One example of the situation discussed in this document is the demand for manipulating very large workpieces which even the workspace for a huge robot is too small. To extend the workspace the robot is placed on a linear track, even called 7th axis, to move the robot linear in one determined direction. Using this extension practically any workpieces can be handled by robots suitable for the application without the necessity of using large robots which have a sufficient workspace.
On the one hand the usage of the linear tracks gives the opportunity to extend the robot's workspace, but on the other hand there is an additional error component in the robotic system which must not only be analysed but in the best case compensated.
The following document deals with a special task of analyzing of linear tracks for industrial robots. Dependent on an earlier article [15] there exists a method for a highly accurate integration of track profiles on the robot control. This is partly based on

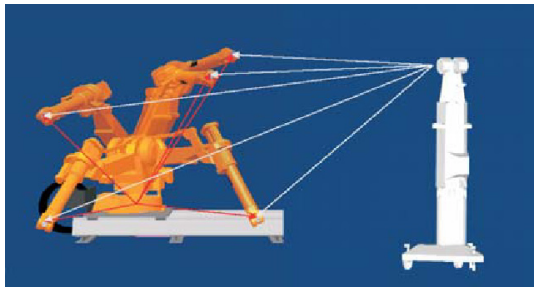

Fig. 1. Identifying of the robots base via 10 measured points

the interpolation of one, in single sampling positions measured, three-dimensional track profile to get a continous description of the linear track. For this the

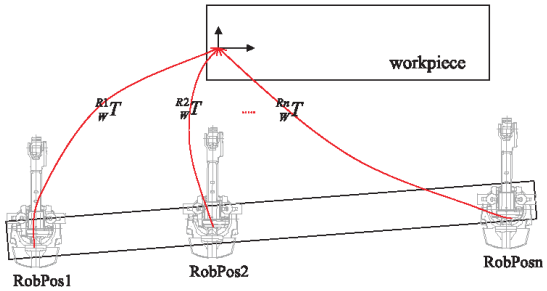

Fig. 2. Continous description of the linear track

robot's base frame is identified at several equidistant positions by measuring 10 different points with an external measurement system (Leica Laser Tracker

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LTD800), figure 1 illustrates this situation. After identifying the single track coordinate systems an interpolation between the sampling points creates a continous description of the track profile (figure 2).
Based on this interpolation further steps for the calculation of the correction values are done so that the error of the interpolation has an effect on the accuracy of the whole integration method.
The identification of the best interpolation method for getting the continous description of the track file is the basic topic of this document. Based on this, an experimental attempt was selected in which first a simulated interpolation on some test data was done using MATLAB. The next step was the creation of a test built up for measuring the real track profile. After getting the real measurement data, three different interpolation methods were tested and the dependent deviations calculated.

II. TESTED INTERPOLATION METHODS

For the interpolation of the 3-dimensional movement, each direction was seperately interpolated. Three different interpolation methods for the interpolation between the sampling points in one direction of the linear track were tested. The basic idea of all three methods was to find a continous function *g(x)* which approximates a given tabulated function *f(x)* so that

$$\left(f(x)-g(x)\right)^2 < \varepsilon, \quad \varepsilon > 0 \qquad (1)$$

The interpolation function *g(x)* is equal to the tabulated function *f(x)* in the *N* given tabulated points x_i:

$$f(x_i) = g(x_i), \quad i = 0,1,....N-1 \qquad (2)$$

A. *Polynomial interpolation*

Basing on the Weierstrass Theorem the task of the polynomial interpolation is to find a polynom $p_n(x)$ of degree *N* which agrees with a function *f(x)* given through *N* tabulated values, so

$$p_n(x) = a_n x^n + a_{n-1}x^{n-1} + ... + a_1 x + a_0 \qquad (3)$$

There are different methods for calculating this $p_n(x)$, such as Lagrange, Newton, Bessel, Stirling or many others. These methods are well-known in the literature and for the purposes of calculating one polynomial interpolation for $p_n(x)$ the least squares method was used in this paper.

B. *Trigonometric interpolation*

The second tested interpolation method is the trigonometric interpolation. Based on the Fast Fourier Transformation the interpolating function $t_n(x)$ which interpolates the function *f(x)* given in tabulated and equidistant sampling points (x_i, f_i) consist of an addition of trigonometric components:

$$t_n(x) = a_0 + \sum_{j=1}^{n} a_j \cos(jx) + \sum_{j=1}^{n} b_j \sin(jx) \qquad (4)$$

The coefficients of the trigonometric function $t_n(x)$ are calculated by the FFT-algorithm.

C. *Cubic spline interpolation*

Using this interpolation method, not one function with a large polynomial order, but several functions with degree of 3 are used to interpolate the given tabulated function *f(x)*. Between every two sampling points a different smooth and also smooth in the first derivate spline-function is defined:

$$S_i(x) = a_i + b_i(x-x_i) + c_i(x-x_i)^2 + d_i(x-x_i)^3 \qquad (5)$$

The concatenation of the spline-functions gives the interpolating function.

III. INTERPOLATION TEST ON NON-REAL MEASUREMENT DATA

The first step of the interpolation analysis was a simulation on artificial measurement data with MATLAB. For this a special MATLAB batch file was programmed, which created different interpolations on
a given set of values for the measurement function *f(x)*. The 3-dimensional movement of the robot's TCP was interpolated seperately for each axis x, y and z. After the successful simulation the real measurement data can be given into the system.
As can be seen, in the programmed MATLAB file the three different interpolation methods polynomial, trigonometric and cubic spline interpolation are used to create prediction how the different methods behave during interpolation.

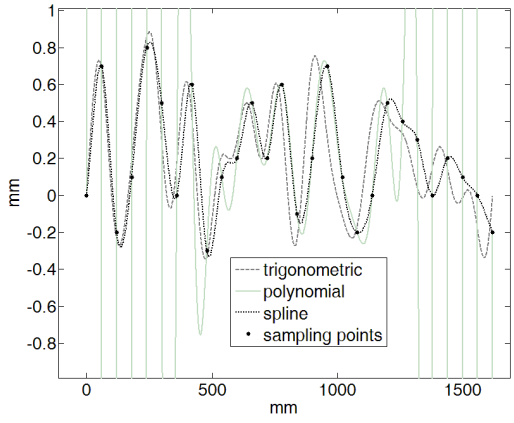

Fig. 4. Simulated interpolation

Figure 4 shows the results of the three interpolations with test values of 28 sampling positions. The differences between the single values caused by a simulated inaccuracy are 1 mm.

IV. MEASUREMENT OF THE REAL TRACK MOTION

A. *Measurement device*

The used measurement system for the needed measurement tasks like scanning the track motion, determining the particular track coordinate systems or identifying of the robots accuracy is represented by a Leica Laser Tracker LTD800 (figure 5). With this measurement device it is possible to do touchless measurements of 3-dimensional points in a range up to 80 meters. The measurement uncertainty of a coordinate is given by 10 µm + 5 µm/m (the accuracy is dependent on the measurement distance) with a possible maximum measurement rate of 3000 points per second.

Fig. 5. Leica laser tracker LTD800

Using the world's most accurate absolute distance meter for getting the distance between laser track and measuring point (25 µm within 40m) and two built-in precision encoders for horizontal and vertical angle measurements, it is a highly accurate measurement system and common in measurement tasks for aircraft and automobile industries.

B. *Robot accuracy*

For proving the measurements for identification of the linear track profile, the accuracy of the robot was tested dependent on an european standard (DIN EN ISO 9283). In this case interesting values were the positional accuracy (AP_p) and the repeating accuracy (RP_l), to show that the robot can be used as a rigid device when moving with its repeating accuracy. As described in the standard, the positional accuracy is calculated by:

$$AP_p = \sqrt{(\bar{x} - x_c)^2 + (\bar{y} - y_c)^2 + (\bar{z} - z_c)^2} \quad (6)$$

where $\bar{x}, \bar{y}, \bar{z}$ are the mean values of the coordinates form 30 different movements to one programmed point $p_c\,(x_c,y_c,z_c)$. The repeating accuracy then is:

$$RP_l = \bar{l} + 3S_l \quad (7)$$

$$\bar{l} = \frac{1}{n}\sum_{j=1}^{n}\sqrt{(x_j - \bar{x})^2 + (y_j + \bar{y})^2 + (z_j + \bar{z})^2} \quad (8)$$

$$S_l = \sqrt{\frac{\sum_{j=1}^{n}(l_j - \bar{l})^2}{n-1}} \quad (9)$$

where x_j,y_j,z_j are the coordinates of one measured point and S_l is the standard deviation. Figure 6 depicts the positional and repeating accuracy of the used robot.

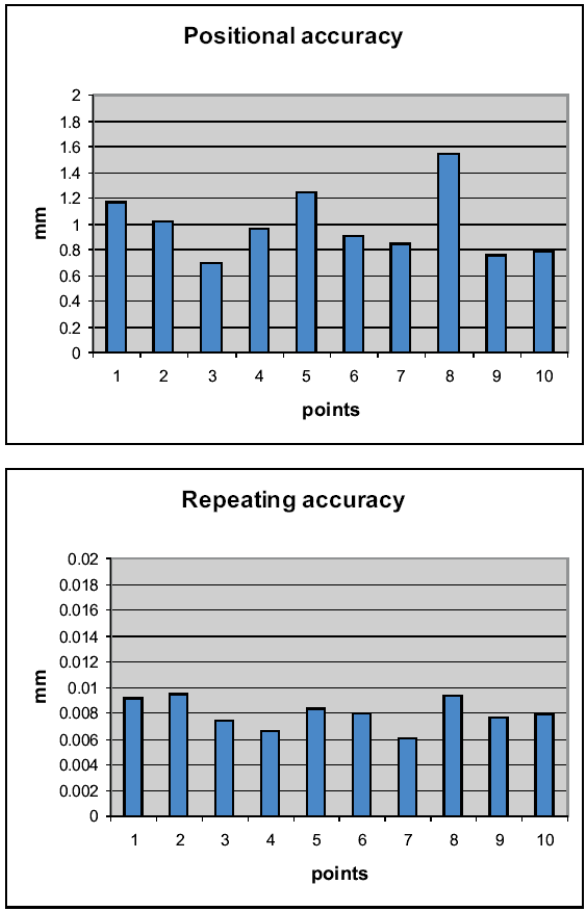

Fig. 6. Accuracy of the used robot

C. *Measurement system*

For analysing the track profile the robot can be used as a rigid device because of its high repeating accuracy. To get the sampling points for the interpolation, the robot was measured at 28 different equidistant linear track positions in one programmed control point (figure 7).

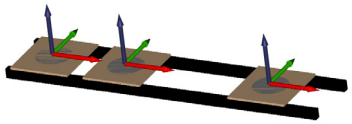

Fig. 7. Measurement at 28 sampling points

So the robot did not move but only the linear track caused potential positional errors. Figure 8 gives an overview about the whole measurement system setup. To compare the interpolating function with real

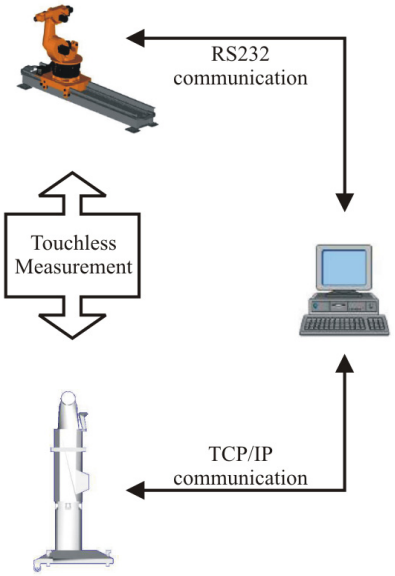

Fig. 8. Build up of the measurement system

measurement data, the robot was not only measured in the discrete sampling points, but also a quasi-continous scan of the robots TCP during a linear track movement was done. It is quasi-continous because the measurement rate was set to 1000 measurements per second, therefore the leftover discretisation error can be neglected.

V. ERROR CALCULATION BETWEEN REAL MOVEMENT AND INTERPOLATION

Comparing the interpolation functions with the real measured values the corresponding error between them decides the quality of the used interpolation method. To get this error the difference d_{error} between every measurement value p_i of the quasi-continous scan and the corresponding value of the interpolation function $f_{ipo}(x_i)$ is calculated by:

$$d_{error,i} = \left| p_i(\xi) - f_{ipo,\xi}(x_i) \right| \qquad (10)$$

where $p_i(\xi)$ is the x,y or z-coordinate of one measurement value of the quasi-continous scan. Figure 9 shows the robots TCP movement represented by the measured sampling points and the three different

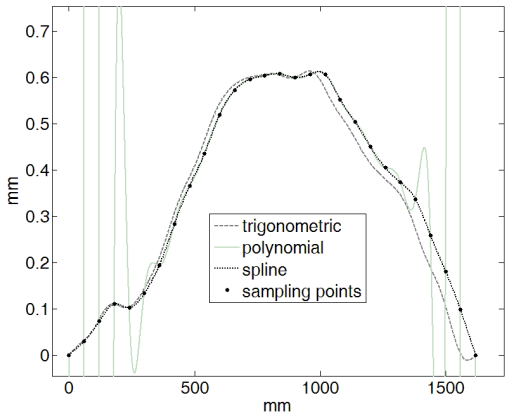

Fig. 9. Interpolation functions and robot movement scan

corresponding interpolation methods. The polynomial interpolation (solid line) confirms the results of section III. A swinging and non-exact interpolation is caused by a polynomial of a high order. In difference to this, the trigonometric interpolation (dashed line)

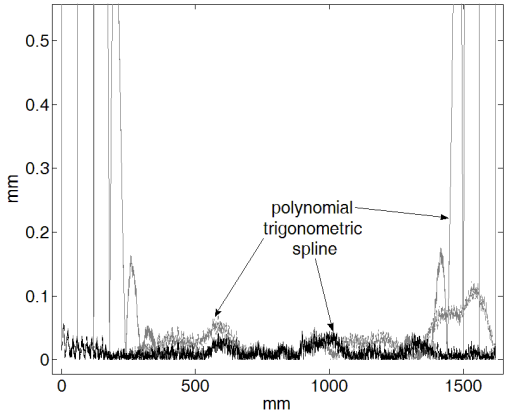

Fig. 10. Deviation between interpolation and real robot movement

and the cubic spline interpolation (dotted line) present a better approximation behaviour to the real TCP movement.

Figure 10 shows the differences $d_{error,i}$ between interpolation function and a continous measurement of the robot's TCP movement. Depending on the maximums of the error functions shown in figure 10, the cubic spline interpolation is the most accurate of the tested interpolation methods.

VI. CONCLUSIONS

Regarding to the lowest difference between the interpolation function and real TCP movement, the cubic spline interpolation was chosen to create the continous description of the track motion. Even the simple construction of the particular spline functions from one sampling point to another offers an efficient implementation in the robot control for further steps in the integration of track motions in the motion control of industrial robots.

The interpolation of the sampling points on the linear track is an important step in the achieving of highly accurate robotic systems. The quasi-continous scan of the robot's TCP position during a movement along the linear track could awake the impression, that due to this exact measurement of the TCP, no interpolation is needed. But it gives only information for one robot joint configuration. To get a general predicion about arbitrary robot positions, e.g. for correcting robot programs the base frame positions of the robot have to be interpolated. For this, the calculated base frame coordinates, given through the measurement of the robot in 10 different points on one linear track position are taken as sampling points for the interpolation and not the measured points. For comparing the results for this interpolation test it was neccessary to have one robot position and not the robot base interpolated.

A further step in this project will be the analysing of three-dimensional interpolation methods to avoid inaccuracies caused by the disjunction of the 3-dimensional movement to 3x1-dimensional movements.

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Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

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Linearity Considerations for Adaptively Biased Transconductors with Applications in Continuous Time Filters

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Abstract – This paper discuses the approach of increasing the linearity of transconductor cells using adaptive bias currents. Adaptive biasing proves to be a powerful technique that may be used to obtain a very linear voltage-to-current conversion. The advantages of this method are its simplicity and its applicability in designing current-mode circuits that can handle wide dynamic range signals without introducing significant (harmonic) distortions. In this paper a 6th order, gm-C, Chebyshev band-pass filter is designed to demonstrate the excellent linearity of adaptively-biased transconductors.

Keywords: transconductor, adaptive bias current

I. INTRODUCTION

Current mode signal processing techniques have been in the last years the first choice for hardware designers when designing high performance analog circuits. Current mode circuits offer significant advantages when compared with voltage mode circuits: simpler structures that often lead to higher operating frequencies, higher dynamic range and lower supply voltages. Transconductor-based circuits have found applications in designing filters for wireless applications, current-mode amplifiers and other circuits that claim simplicity and high linearity at moderate frequencies (of the order of tens of MHz). Design specifications for high performance transconductor circuits include: no internal dominant parasitic poles, high linearity and low bias currents. Programmability or tunability or are also at high prize, since there are numerous applications where the transconductor cell must feature a digital control over the value of g_m [17], [18] or a precise values of transconductance is needed.

Linearity and dynamic range are two closely related parameters that measure the performance of a transconductor in terms of large signal handling capabilities; for example, the linearity of the transconductor cells that are used to build filters for wireless applications plays an important role in the overall performance of a transceiver. Harmonics that are introduced by nonlinear circuits may be seen as distortion that disrupts the process of accurate demodulation.

In what follows, this paper analyses and discusses the technique of adaptive biasing to improve the linearity of MOS transconductance elements. Adaptive biasing refers to circuits which use signal dependent bias currents, in contrast to circuits that use current sources uncorrelated in magnitude to the input signal. Although other efficient techniques have been proposed for the linearization of transconductor circuits, among which current differencing, source degeneration and class AB configuration [3], adaptively biased transconductors offer simpler basic g_m cells at greater performance in terms of linearity.

II. THE PRINCIPLE OF ADAPTIVE BIASING

A. Simple differential pair transconductor

The simplest differential voltage-to-current converter circuit is shown in Fig. 1a. It consists of one pair of source-coupled MOS devices biased – at this point – with a constant current I_{bias}. The relationship between the differential input voltage and the two gate-source voltages is described by (1); this equation also shows the relationship between the two drain currents and the total bias current.

$$\begin{cases} v_{id} = v_{gs1} - v_{gs,2} \\ i_{d1} + i_{d2} = I_{bias} \end{cases} \quad (1)$$

Using the square law of a saturated transistor, we can write the drain currents for transistors M_1 and M_2 as:

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$$i_{di} = k\left(v_{gsi} - V_{th}\right)^2, i = \overline{1,2} \qquad (2)$$

where $k=0.5\mu_n C_{ox} W/L$ defines the transconductance of an n-type MOS transistor and μ_n, C_{ox}, and W/L stand for the surface mobility, capacitance per unit area and channel geometrical parameters, respectively; v_{gs} is the gate-source voltage and V_{th} is the threshold voltage. Replacing (2) in (1), after some simple computations we obtain that the differential output current is:

$$i_{out} = i_{d1} - i_{d2} = \pm v_{id}\sqrt{2I_{bias}k}\sqrt{1 - \frac{k}{2I_{bias}}v_{id}^2} \qquad (3)$$

under the condition:

$$\left|v_{id}\right| \le \sqrt{\frac{I_{bias}}{k}} \qquad (4)$$

Eq. (4) shows that the current-voltage conversion of the simple differential MOS pair is linear only over a limited domain of the differential input voltage. Also, the nonlinear term in (3) is a square function of v_{id}; as the signal level increases the function becomes more nonlinear. Therefore, large input signals will result in harmonic distortion, thus limiting the dynamic range of the circuit. Nonlinearity is understood in this paper as the percent deviation of (3) from the ideal (and linear) conversion shown in (5) due to harmonic components:

$$i_{out} = \pm v_{id}\sqrt{2I_{bias}k} = g_m v_{id} \qquad (5)$$

where g_m defines the transconductance of the differential pair. The harmonic components are computed from the MacLaurin[2] development of (3).

B. Adaptive biasing principle

A significant increase in the linearity domain of the circuit in Fig. 1a can be obtained by employing an adaptive bias current [1], [2], [12]. Referring again to Fig. 1a, if we replace the dc bias current I_{bias} with a voltage dependent bias current as shown bellow, we obtain that the voltage-current conversion of (3) becomes of the form given in (7).

$$I_{ad} = I_{bias} + a v_{id}^2 \qquad (6)$$

$$i_{out} = i_{d1} - i_{d2} = \pm v_{id}\sqrt{2I_{bias}k}\sqrt{1 - \frac{k-2a}{2I_{bias}}v_{id}^2} \qquad (7)$$

under the condition given by (8), and where a is a constant measured in $\mu A/V^2$. The previous equation results in a perfectly linear $i_{out}=f(v_{id})$ conversion, if we impose that $a=k/2$.

[2] Taylor development around the operating point where $v_{id}=0$.

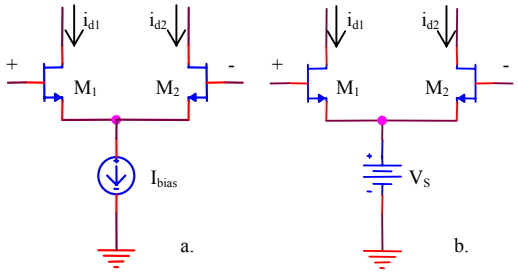

Fig. 1. Simple differential pair transconductor; current biased (a) and voltage biased (b)

$$\left|v_{id}\right| \le \sqrt{\frac{2I_{bias}}{k}} \qquad (8)$$

It must be noted from (8) that the range of the input voltage has increased by $\sqrt{2}$, in comparison to the circuit using non-adaptive current; this results in an increase of the large signal handling capability for 1% THD (Total Harmonic Distortion) of approximately 11dB [1].

C. Generation of adaptive bias current

The simplest way to generate a signal-dependent bias current proportional to the square of the input voltage signal as described by (6) is to use the square law model of MOS saturated transistors. This law was shown in (2); starting from the differential transistor pair in Fig. 1a in which we replace the bias current source at the common source node with a constant voltage source, we obtain the circuit shown in Fig. 1b. Writing the gate-source voltage as in (9) and assuming that the two transistors are perfectly matched and that the input signal is fully balanced around a common-mode voltage (V_{CM}), we derive that the sum of the two drain currents depends on the square of the input differential voltage; this relationship is shown in (10).

$$\begin{cases} v_{GS1} = V_{CM} + \dfrac{v_{id}}{2} - V_S \\ v_{GS2} = V_{CM} - \dfrac{v_{id}}{2} - V_S \end{cases} \qquad (9)$$

$$I_{sum} = I_{d1} + I_{d2} = 2K\left(V_{CM} - V_S - V_{th}\right)^2 + \frac{K}{2}v_{id}^2 \qquad (10)$$

By comparing (10) with (6), the two equations are equal provided that:

$$\begin{cases} I_{bias} = 2K\left(V_{CM} - V_S - V_{th}\right)^2 \\ a = \dfrac{K}{2} \end{cases} \qquad (11)$$

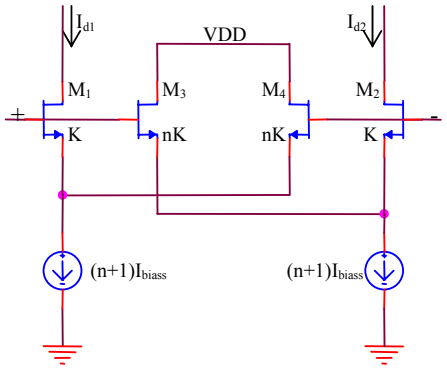

Fig. 2. Differential cross-coupled squarer

In (10) and (11), *K* stands for the transconductance parameter of the voltage pair in Fig. 1b. Another commonly used circuit for the generation of adaptive currents is shown in Fig. 2; it is based on two unbalanced differential pairs, with the inner pair transistors *n* times larger than the other transistors. In comparison to the previous circuit, this configuration increases the linearity of the quadratic equation by eliminating most of the third order harmonics of the adaptive current [1], [2], [3]. If we assume that all the transistors are operating in the saturation region, the sum of the two drain currents I_{d1} and I_{d2} is given by:

$$I_{d1} + I_{d2} = 2I_{bias} + 2K\frac{n(n-1)}{(n+1)^2}v_{id}^2 \quad (12)$$

under the condition that:

$$|v_{id}| \le \sqrt{\frac{n+1}{n}\frac{I_{bias}}{k}} \quad (13)$$

Comparing (12) to (10) we obtain that the following relationship must hold between the equation parameter *a* and the transconductance K of transistors M_1-M_4 from the circuit in Fig. 2:

$$a = 2K\frac{n(n-1)}{(n+1)^2} \quad (14)$$

In what follows the two methods described above are used for the generation of adaptive currents that are further applied as bias currents to differential pair transistors.

III. COMPLETE ADAPTIVELY BIASED TRANSCONDUCTOR CELLS

The complete transconductor circuit that is made of the two current and voltage-biased pairs shown in Fig. 1a and b is presented in Fig. 3; the transistor pair M_3M_4 generates the voltage dependent bias current that is applied at the common source node of the differential pair M_1M_2. Neglecting nonidealities of the square-law model of the transistors, from (11) we

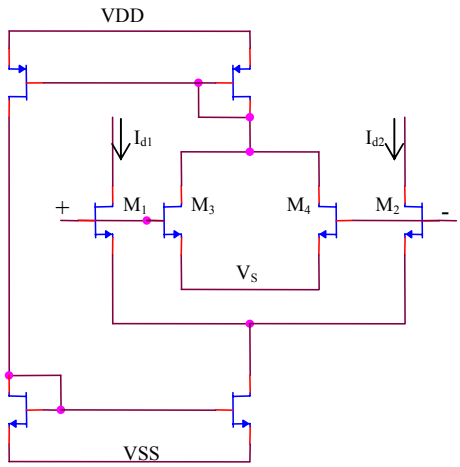

Fig. 3. Adaptively biased transconductor using the squarer circuit

obtain that the nonlinear term in equation (7) is cancelled when M_1-M_4 are matched. However, mobility reduction in the channel of transistors M_1-M_4 determines third order distortions that reduce the linearity of the circuit.

The effect of this mobility reduction can be modeled by:

$$\mu = \frac{\mu_0}{1+\theta(v_{GS}-V_{th})} \quad (15)$$

where μ defines the surface mobility, μ_0 is the zero-field carrier mobility and θ is the carrier mobility degradation factor. Including these effects, (7) becomes:

$$i_{out} = \pm v_{id}\sqrt{2I_{bias}k}\sqrt{1-\frac{k-2a}{2I_{bias}}v_{id}^2} - \\ -\theta v_{id}\left[I_{bias}-(K-a)v_{id}^2\right] \quad (16)$$

Writing the MacLaurin series of the previous equation (only the third harmonic is shown), we obtain the transfer function:

$$i_{out} = \left(\sqrt{2I_{bias}K}-\theta I_{bias}\right)v_{id} - \\ -\left[\sqrt{\frac{K}{8I_{bias}}}(K-2a)-\theta(K-a)\right]v_{id}^3 \quad (17)$$

This equation clearly indicates a deviation from the relationship given in (7) due to mobility degradation; we obtain that mobility reduction introduces third order harmonics and also a decrease of the small signal transconductance. Imposing that the third order term cancels, we compute that the optimum value for *a* is:

$$a = K\left(\left(\theta-\sqrt{\frac{K}{8I_{bias}}}\right)\Big/\left(\theta-\sqrt{\frac{K}{2I_{bias}}}\right)\right) \quad (18)$$

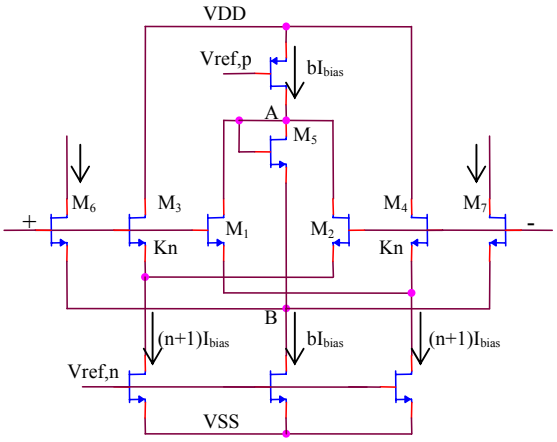

Fig. 4. Cross coupled adaptively biased transconductor

This new value for *a* is less than K/2 (see (11)); using level 7 SPICE transistor models, the previous equation provides a value of *a=K/2.32*, for a bias current of 200µA; V_S was chosen 400mV, the supply voltage is 1.8V with the common mode voltage 1.2V and the channel geometrical parameters for transistors M1-M4 are 10µm/1µm. Fig. 5 shows the measured performance of the complete transconductor cell; the percent nonlinearity measured as total harmonic distortion is plotted versus the differential input voltage (peak-to-peak). An important improvement in linearity may be observed in Fig. 6 (curves A and B) after taking into account the effects of mobility reduction with the value of *a* estimated by (18). The above analysis assumes that a perfect quadratic bias current can be generated, according to the expression predicted by (10). While good linearity performance can be obtained with the circuit described above, its main penalty is the frequency response [2]; this is caused by the current mirrors that are used to propagate the adaptive current to the common source node of M_1M_2.

An alternative to this implementation that makes use of the squarer circuit presented in Fig. 2 is discussed further. The complete transconductor cell is shown in Fig. 4. Instead of the current mirrors we used an additional transistor and two current sources to deliver the summed squared current of M_1 and M_2 from point A to point B. According to (11), if we choose a=K/2 we obtain from (14) that n=2.155. This is the optimum value for *n* in order to eliminate the nonlinear component from the differential output current. Mobility reduction has not been taken into account in this analysis. Instead of using current mirrors, this circuit uses an additional transistor (M_5) and the two current sources that generate the current bI_{bias}. It can be shown [1] that a value of b>4n/(n+1) is needed to maintain transistor $V_{ref,p}$ conducting over the input range given by (13). Replacing (12) in (7), with n=2.155 we obtain the transfer function of the circuit described above:

$$i_{out} = i_{d6} - i_{d7} = \pm 2\sqrt{KI_{bias}} \qquad (19)$$

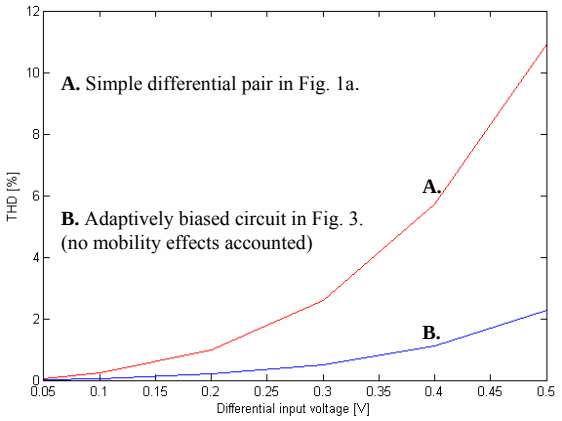

Fig. 5. THD versus differential input voltage

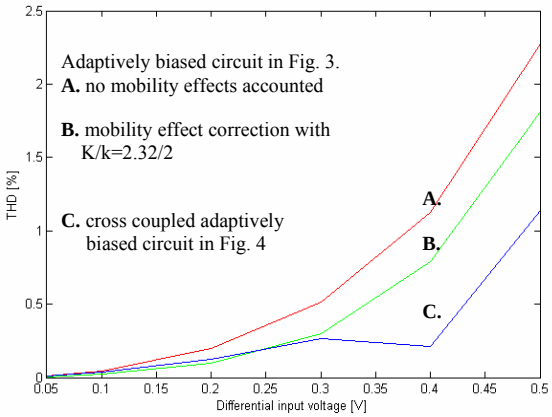

Fig. 6. THD versus differential input voltage

The small signal transconductance is now $\sqrt{2}$ times the value from the previous circuit, due to the DC bias current which is twice as much, as shown in (12). For *b* chosen equal to 4, the gate source voltages of transistors M_1-M_7 are equal. For this value of *b*, the circuit described in Fig. 4 was simulated and the THD versus differential input voltage is plotted in Fig. 6. Compared to the previous implementation, this circuit offers an improved voltage range over which the nonlinearity is maintained bellow 1%. Also, the frequency response is improved since no current mirrors are needed to propagate the adaptive current to the common source node of the differential pair.

IV. FILTER IMPLEMENTATION

The basic cell of the filter designed to demonstrate the high linearity of the transconductor cells discussed in the previous sections is shown in Fig. 7; the entire filter is constructed of three such g_m-C biquads in cascade, each biquad based on the g_m cell shown in Fig. 4. The adaptive biasing technique was used to linearize the transconductor cells. This filter is intended to be the IF (intermediate frequency) filter in a digital-IF wireless receiver with the IF stage at 50 MHz. A folded cascade was used as load to the basic cell in Fig. 4 as it ensures reasonably high output resistance; for an integrator constructed with one g_m

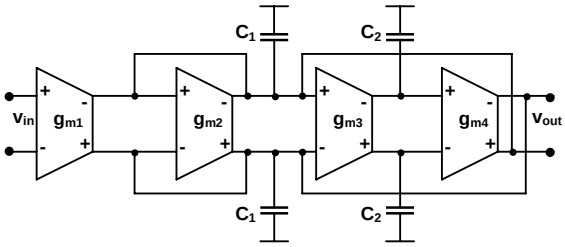

Fig. 7. Transconductor-based differential second-order section

cell loaded with this output stage and a load capacitor of 5 pF, the measured DC gain is of approximately 34 dB, while the phase shifts from -89° at 200 kHz and -91° at 420 MHz. Q-compensation techniques to boost the DC gain were not used, although negative resistor cells (g_m-based resistors) connected at the output of each transconductor cell may be used [5]. The gain of the 6th order, 0.1 dB, Chebyshev band-pass filter was set to 0 dB, the central frequency at 50 MHz, with a bandwidth of 5 MHz (Q=10). All the simulations were performed using SPICE, with Level 7, 130nm CMOS transistors. The filter draws 2.8 mA from a 3 V power supply. The linearity of the filter was determined using the „equivalent 3rd order input Intercept Point", IP_3; the measured value of the IIP_3 is of -6.5 dBm. Compared to other results (in [17] and in [18] the measured values are of -9.2 dBm and -8 dBm, respectively), this value indicates that the adaptive bias approach offers an improvement in terms of linearity.

V. CONCLUSIONS

The concept of adaptive biasing has been discussed in the context of increasing the linearity domain for transconductor cells. Two complete circuits have been presented and their performance in terms of linearity has been discussed and compared. The adaptive biasing method discussed was used to design a very linear CMOS filter using transconductor cells. The designed IF filter intended for use in the intermediary stage of a wireless receiver features high linearity (measured in terms of 3rd order Intercept Point), as required to implement high performance transceiver front-ends.

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TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 51(65), Fascicola 1, 2006

Log-Domain multipliers for VLSI architectures

Lelia Feştilă[1], Robert Groza[1], Lorand Szolga[1], Sorin Hintea[1]

Abstract – We propose new modular configurations for one-, two-, and four quadrant multipliers in order to be used in large dimension circuits, like analog support vector machines or neural networks. Some investigations on these structures are made taking into account the real configurations and parameters of transistors in BiCMOS technology. We also underline the advantage of using such modular structures for high frequency large dimension circuits.
Keywords: Log-Domain, analog multiplier, VLSI architecture

I. INTRODUCTION

In analog computation and signal processing there are many cellular architectures that have to perform weighted sums with controllable or adaptive weights or sums of products of signals. Such examples are artificial neural networks, cellular nonlinear networks or support vector machines whose decision function is based on vector products. All of these circuits have to perform a large amount of calculations, therefore demands in area, power and high frequency operations usually appear.
As example for a SVM classifier [6] a test vector

$$\mathbf{x} = [x_1, \ldots, x_N]^T \tag{1}$$

and M support vectors

$$\mathbf{x}_i = [x_{i1}, \ldots, x_{iN}]^T, i = 1 \ldots M \tag{2}$$

are given. Using kernels based on vector products a decision function has to be determined:

$$y = \operatorname{sgn}\left(\sum_1^M a_i y_i \left(\sum_1^N \mathbf{x}_{ij} \mathbf{x}_j \right) + b \right) \tag{3}$$

Coefficients a_i and the bias term b are known from the learning process and y_i are the positive or negative labels of SV's i. Resulted label y corresponds to the test vector of features, which is positive classified if $y \geq 0$. A possible structure of such a classifier is given in Fig. 1 [1].

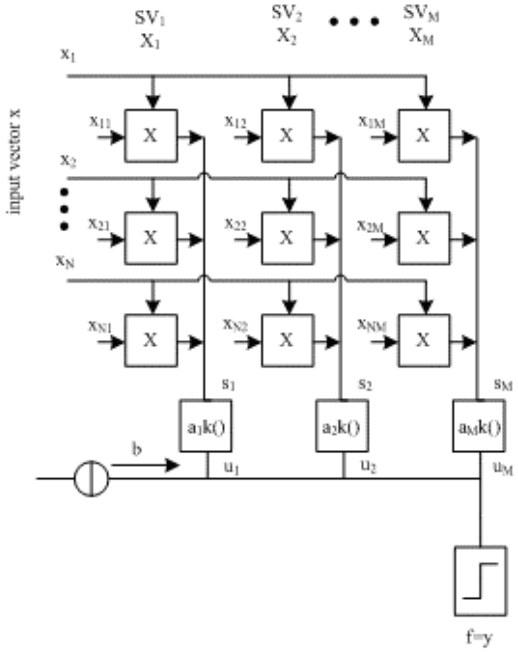

Fig. 1 Block diagram of a cellular SVM classifier with multiplying law: (x_k x_{kj})
k = 1,…,N; j = 1,…,M;
N – vector length M – SV number

The main cell in this schematic type is the multiplier. For summation we preferred to use current mode circuits and in the following we consider currents at input and output of multiplying cells.
Because the implementation of SVM classifiers needs high power, high speed, high densities, we thought to extend log-domain design [4] in this area because it is very appropriate for such requirements.
The very simple structure and the possibility of controlling their parameters are also very attractive for using this design.
Until now the log-domain was used for linear circuits [2] [3] [4] [5]. We have realized a modular nonlinear cell library for such tasks [4]. The principial architectures proposed in this paper for one-, two- and four quadrant multipliers were proved by simulations taking into account bipolar and BiCMOS technology. In this paper BiCMOS schematics are considered because they give the best results.

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II. ONE QUADRANT MULTIPLIER/DIVIDER

The function

$$i_{out} = \frac{i_x i_y}{i_{REF}} \tag{4}$$

can be simply obtained with a log-domain amplifier if the two signals are one-directional [4].

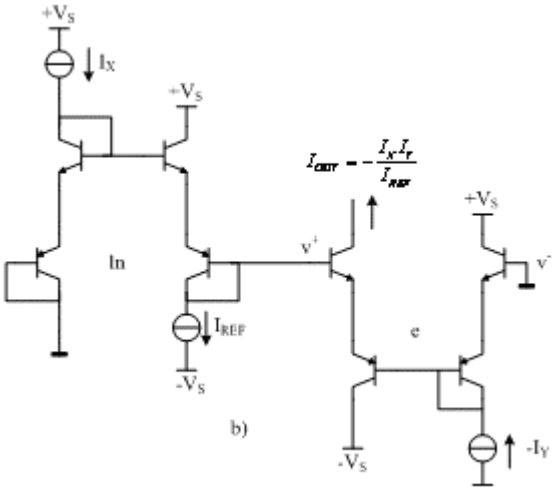


Fig. **2** a) and b) show such structures.

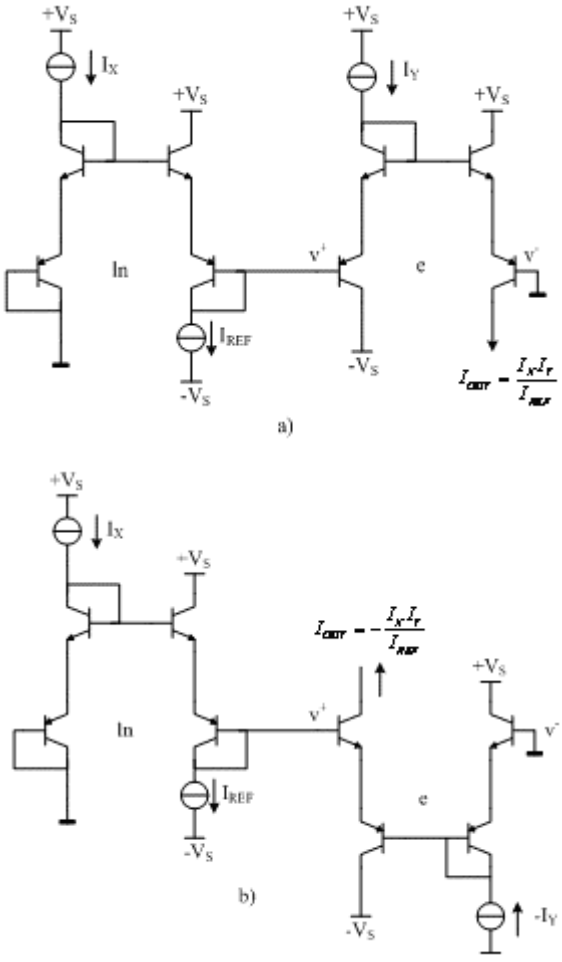


Fig. 2 One quadrant log-domain amplifiers: a), b) schematics

Modules **ln** in Fig. 2 accept a positive input I_X and a reference current I_{REF}. The inputs in the **e** cells can be either positive I_Y (Fig. 2, a) or negative ($-I_Y$) (Fig. 2, b). We took as reference the positive input and output directions as the arrow show in Fig. 2, a) and b). Multipliers operate in one quadrant. For Fig. 2, a) as an example we can write:

$$v^+ = V_A \ln \frac{I_X}{I_{REF}}; I_{out} = I_Y e^{\frac{v^+}{V_A}}; V_A = 2V_T \tag{5}$$

$$\Rightarrow I_{out} = \frac{I_X}{I_{REF}} I_Y \tag{6}$$

For Fig. 2 a) the simulated dc transfer characteristics and the time diagrams are shown in Fig. 3.

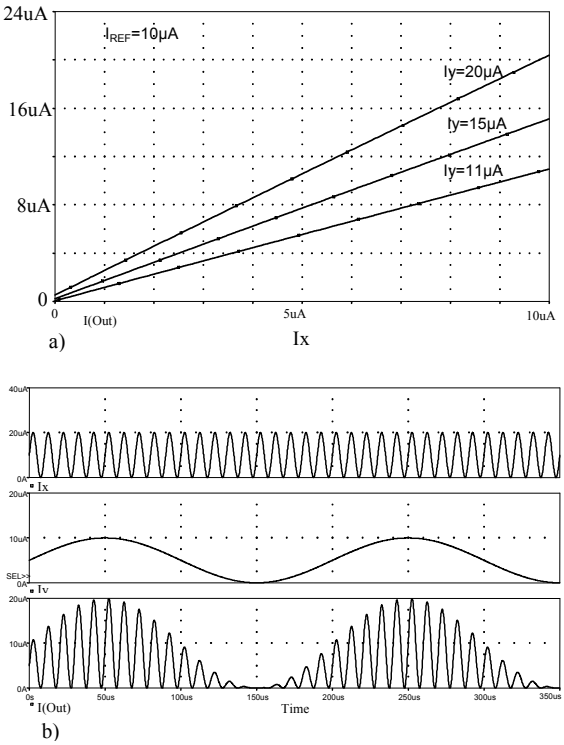


Fig. 3 a) DC transfer characteristic of one quadrant multiplier; b) time diagram for I_{REF}=10μA, I_X=(10+10sin2π100kt)μA, I_Y=(5+5sin2π5kt)μA

For Fig. 3 a), current I_X is positive [0,10uA], current I_Y is also positive and takes the values 11uA, 15uA, 20uA, I_{REF} is equal to 10uA.
Fig. 4 a) and b) show the symbols of each module **ln** and **e** respectively.

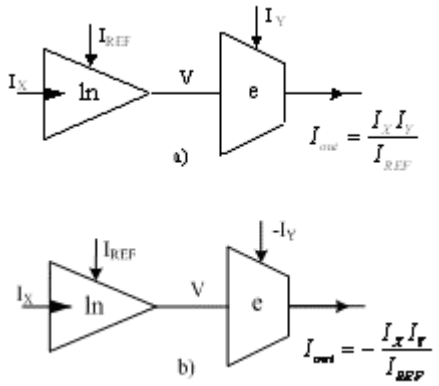


Fig. 4 One quadrant modular log-domain multiplier symbols: a) Ix>0, Iy>0; b) Ix>0, Iy<0

It is worth to put relation (6) in the form

$I_{out} = I_X \frac{I_Y}{I_{REF}} = A(I_Y) I_X$ so it can be seen why this circuit can also be considered as a current controlled current amplifier (Fig. 3, a).

III. TWO QUADRANT MULTIPLIERS

Fig. 5 shows the proposed two-quadrant multiplier. The input I_X is one-directional, the input i_y is bidirectional.

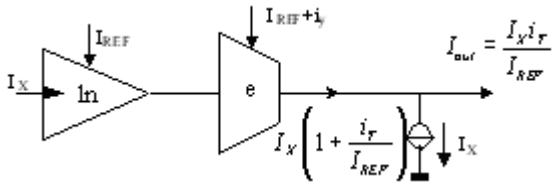


Fig. 5 Two quadrant multiplier

$$\left|i_y\right| < I_{REF}; I_{REF} > 0; A\left(i_y\right) = \frac{\left(I_{REF} + i_y\right)}{I_{REF}} \qquad (7)$$

$$I_{out} = A\left(i_y\right) I_X - I_X = \frac{I_X i_y}{I_{REF}} \qquad (8)$$

We simulated the circuit. The dc transfer characteristics of this multiplier is shown in Fig. 6 a) and a time diagram in Fig. 6 b):

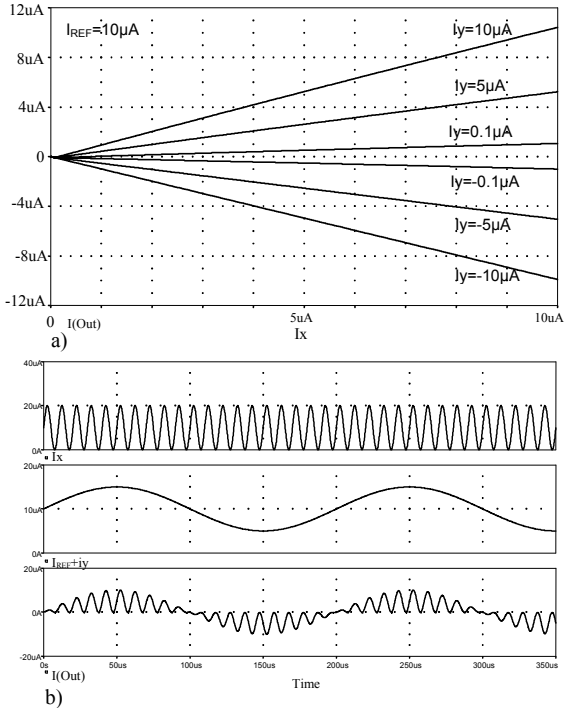


Fig. 6 a) DC transfer characteristics of the two-quadrant multiplier; b) time diagram for I_{REF}=10μA, I_X=(10+10sin2π100*10^{3}t)μA, i_Y=(5sin2π5*10^{3}t)μA

IV. FOUR QUADRANT MULTIPLIERS

For this type of multiplying cell we proposed the circuit given in Fig. 7.

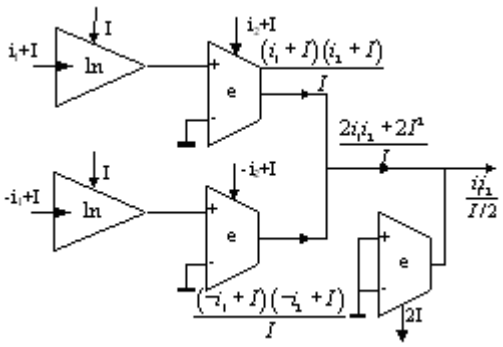


Fig. 7 Four-quadrant multiplier

The input signal i_1 is applied in opposite direction over a biasing current I at the input of two current amplifying paths, having the gains $(i_2+I)/I$ and $(-i_2+I)/I$ respectively. Current i_2 is the second bidirectional signal.

These currents, i_1+I and $-i_1+I$ (i_2+I, $-i_2+I$) were obtained by the circuit from Fig. 8:

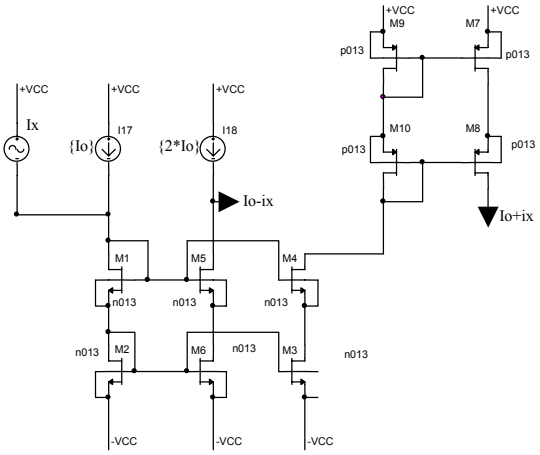


Fig. 8 Circuit for sum and difference

The input and output signals are presented in Fig. 9:

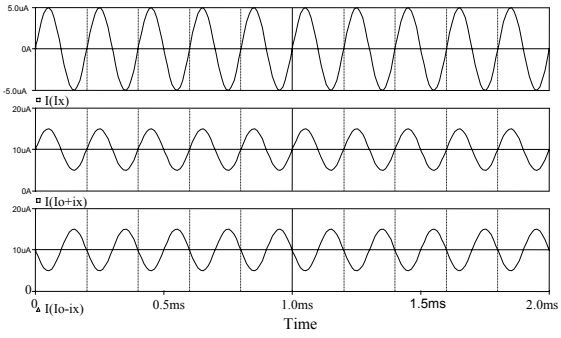


Fig. 9 Input and output signals from Fig. 8

The constant component of the sum of the output currents is cancelled by a current sink also realized with an **e** cell.

For proving the validity of the circuit some time diagrams resulted in simulations are given in Fig. 10. The simulated circuit is given in Fig. 15. Each input signal is a sinusoidal one, $i_1=(5\sin 2\pi 5*10^3 t)\mu A$ and $i_2=(5\sin 2\pi 100t)\mu A$, $I_{REF}=10\mu A$.

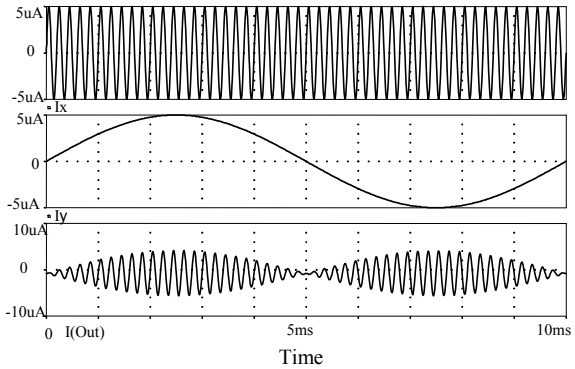


Fig. 10 Time diagrams for the four-quadrant multiplier

In Fig. 11 the magnitude spectrum of the output current signal for the proposed four-quadrant multiplier shown in Fig. 7 is presented.

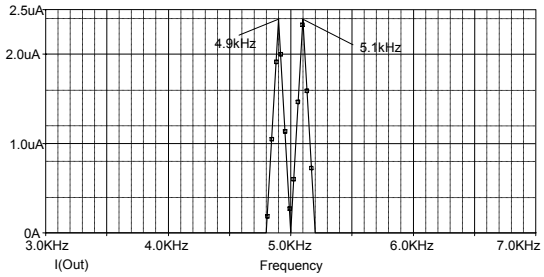


Fig. 11 Magnitude spectrum of the output current for the four-quadrant multiplier

The output current is of the form:

$$i_{out} = \frac{2i_x i_y}{I} \qquad (9)$$

Fig. 12 gives the dc transfer characteristic for: $i_x \in (-9\mu A, 9\mu A), I_{REF} = 10\mu A,$

$i_y \in \{-9\mu A, -5\mu A, -1\mu A, 1\mu A, 5\mu A, 9\mu A\}$

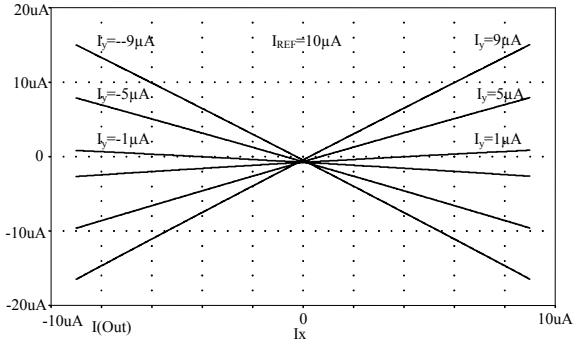
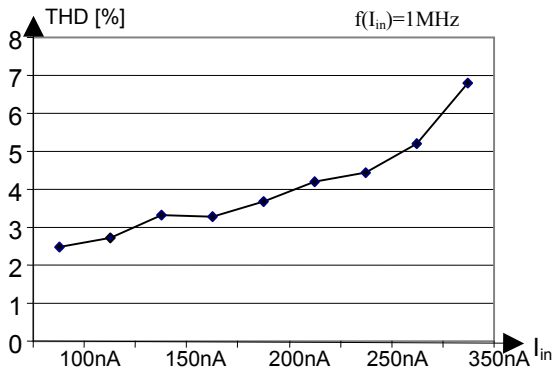


Fig. 12 DC transfer characteristics for the four-quadrant multiplier

We made also some THD computing and the results are shown in Fig. 13,a,b,c for different bias currents: 1μA (Fig. 13, a), 10μA (Fig. 13, b) and 100μA (Fig. 13, c). We compared the results with the THD results obtained for a classical Gillbert cell (Fig. 14, a). For the log-domain multiplier cell we consider three bias current values because for log-domain circuits the bias current is used for changing the cut-off frequency of the circuit. For higher bias current we have higher cut-off frequencies of the multiplier.



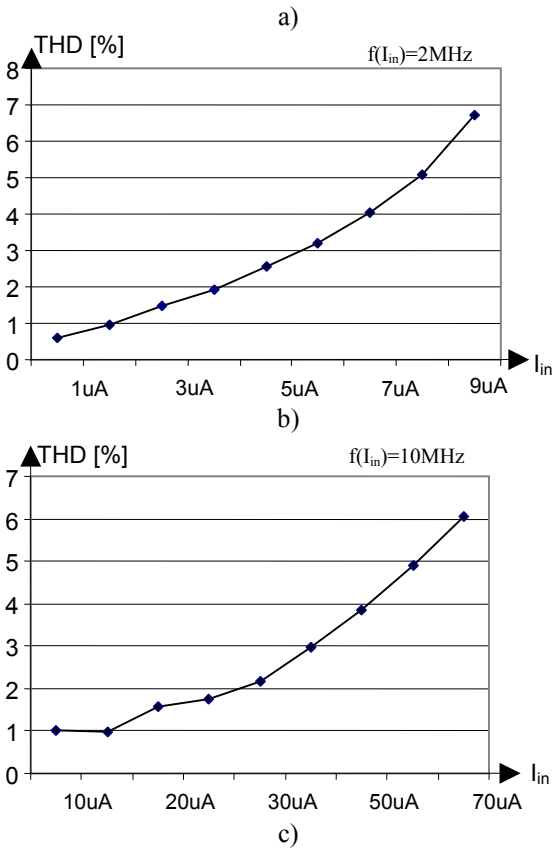
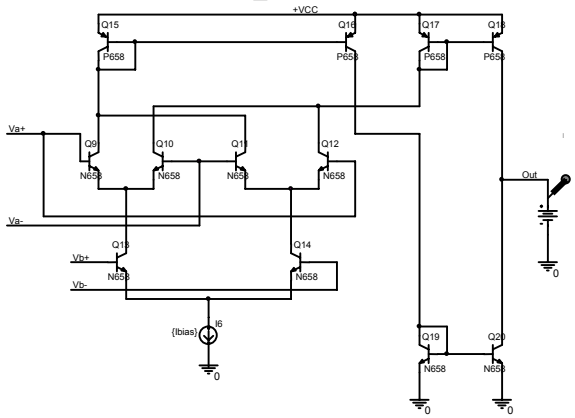


Fig. 13 THD characteristics for different bias currents: a) I_{REF}=1μA , b) I_{REF}=10μA, c) I_{REF}=100μA

The diagrams show that for a THD ≤ 5% we can increase the input current to about 30% I_{REF} if I_{REF}=1μA, 80% I_{REF} for I_{REF}=10μA and 60% I_{REF} for I_{REF}=100μA. In the case of Gillbert cell as Fig. 14, b shows the input voltage can reach only about 50% V_T in order to have a THD ≤ 5%.



a)

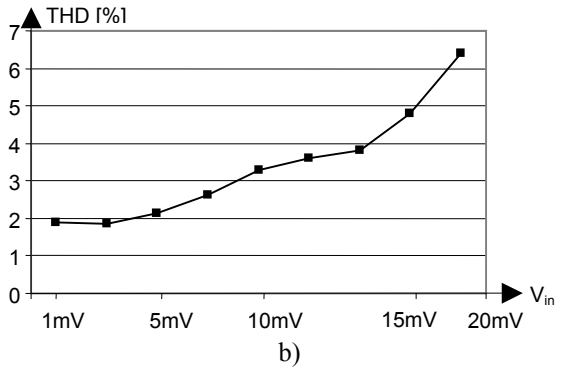


Fig. 14 Gillbert cell: a) Schematics b) THD characteristics

In Fig. 15 we have the simulated circuit in SPICE. All circuits were simulated in SPICE using BiCMOS transistor models from National Instruments.

V. REMARKS

The proposed multiplying cells open new directions of applications of log-domain design. We proposed this modular structure in order to be used in analog SVM classifiers and also in neural networks. This analog cells offer simplicity, low area, low voltage and high frequency and can be a good alternatives in VLSI analog modular design.

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Methodology of Algorithms Design and Methods Using in Predictive Diagnostic System

Zdenek Machacek[1],Vilem Srovnal[2]

Abstract – A paper deals with analysis and development of complex methods and algorithms for evaluation designed and measured signals of predictive diagnostic system. The design and the solution of system are original and an embedded system with a digital signal processor DSP is important control unit. The paper is composed of suitable algorithms design for measured signal processing. The developed system is designed for education and development at Department of measurement and control, VSB-TU Ostrava, further the system is available for a commercial industrial utilization. By described methods and algorithms implementation to the system, there is arisen unique instrument for predictive diagnostic of monitored mechanical devices.

Keywords: embedded system, predictive diagnostic system, signal analysis, digital signal processing

I. INTRODUCTION

Today, signal processing and signal analyses in embedded systems are a much evolved and interesting research area. There are many methods and possibilities for utilizing this theoretical and practical knowledge. Signal processing applications and development are affected by modern computers and electronics. A modern automated diagnostic and maintenance system is one of a sphere, where we can utilize new signal processing and computer possibilities. The modern automated diagnostic and maintenance system guarantees and increases stability and the economic efficiency of monitored devices.

II. SPECIFIC AUTOMATED DIAGNOSTIC SYSTEM DESIGN

Specific automated predictive diagnostic and maintenance system is developed for improvement of today's instruments for diagnostic of mechanical devices. This system manner is based on the data of the real states of monitored devices. So this allows the predicting of possible system events and problems. The diagnostic system executes signal measuring, diagnostic methods and signal analysis for the detection of real states of monitored devices or for the detection impending danger failures or device damage. The automated diagnostic system is composed of sensors, which scan mainly device vibrations and device noises, rotation speed, movement values, device temperatures, fluid states and other areas. These measured data and signals are analyzed by a user or automatically. Monitored devices are controlled pursuant to analysis results of system states. The predictive diagnostic system is composed of these basic function parts:

- Automated user system
- Embedded system
- Sensors
- Monitored mechanical devices

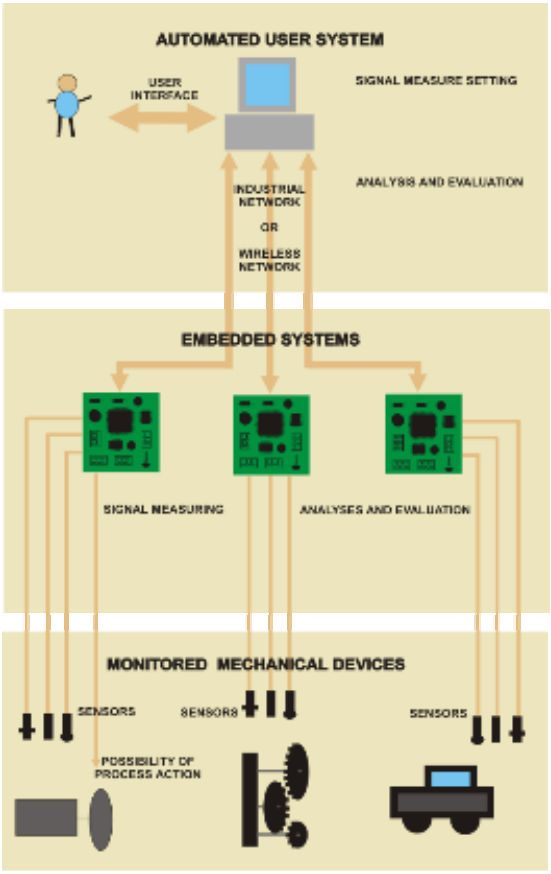

Fig.1. Automated system function blocks

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The automated user system is basically used for visualization, state monitoring, data transfer, the user interface, and connected embedded system control. This system is created in the programming environment Delphi 7. The program runs on the personal computer. This comfortable user environment of the developing system is designed for various embedded control systems. It enables selectable system parameter possibilities. The automated user system is created like a operating user program. This program is customized for comfortable user control and it is very well suited for data measuring and the analysis from embedded systems. The communication with embedded systems has to be fast enough and very safe. For real-time data computation communication is a very important and indispensable problem. This automated diagnostic system is customized for serial RS232 and wireless communication. The industrial communication can be very easily implemented to this automated user system, because communication protocol is able to edit and customized. The programs basic screen is composed of these easy common user components:

- **user menu** – is placed on the top of the program screen. There are selectable parameters of data measuring and analysis obtained from the embedded system. The selectable parameters appertain to peripheries, communication protocols, data sequences, sensors, limits and alarms, system reactions, signal analyses, computations, prediction, and files. Furthermore, there are program help and the finish item.

- **rapid icons** – are often used, and important data parameters settings. There are placed under the user menu. These icons make easier and faster user control.

- **graphical sheets** – are several sheets with one, two or three graphs. Inside of graphs are measured or computed data, which are sent from the embedded control system. They are placed in the middle of the program screen.

- **graphical setting items** – are for user data graph definitions. These items are placed on the right side of the program screen. The program user can define the name of the graph sheet, the number of the graph, data from the sensor, data computation, characteristic and analysis, the alarms and limits, the defined interconnection. So, all these user settings are determined for the displayed graph.

- **parameters of displayed data** – are placed under the graphical setting items. Information about just active graphical sheet is displayed. The information is about the graphs of the active sheet. There is information about the sensors, the data computations, the data characters, the alarms, the limits and prediction methods.

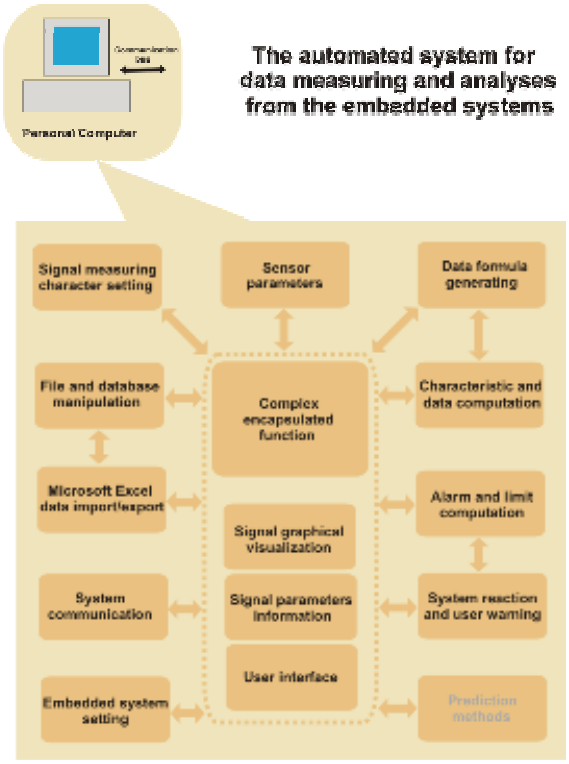

Fig.2. Automated user system function blocks

An embedded system is control system for fundamental calculations and algorithms execution. The embedded system is special purpose computer system, which is encapsulated and housed on a single microprocessor board. This system performs pre-defined tasks and it has specific requirements. It is of a contrary character to personal computers. The embedded systems often obtain a memory, a slower processor and needed interfaces. It guarantees lower cost and smaller power consumption. Programs often have to run with real-time and application-specific integrated circuit limits. Designers use assemblers, compilers, debuggers to develop the embedded system.

In developing a project, the embedded system contains a DSP digital signal processor for process and signal computation. This new improvement of the diagnostic system design is very powerful and it could control devices better and faster than the old ones. Thanks to this embedded system, we can automatically monitor values, execute, analyze, monitor the equipment state, and react to system operation. For modern applications, it is necessary to process complex computations in a very short time (RT - real time). So for processing, the digital signal processor DSP is mostly suitable.

DSP is a Harvard architecture processor with special features. The architecture enables using a more system buses for the data and instruction transfer inside processor. DSP is RISC (Reduce Instruction Set Computer) processor type. One of DSP special features is Pipe-lining. It means, they process more instructions in the one instruction cycle. It enables using special MAC instructions for filtering.

For this project is used the digital signal processor MOTOROLA DSP 56F805. Maximum core frequency is 80MHz, and 8MHz crystal. The program memory is internal FSRAM 64K x 16 bits and 64K x 16 bits is a data memory. It is 16 bit processor with a sufficient performance and a number of peripheries. For programming, there is the development software - Code Warrior - transparent and comfort programming in C and Assembler languages.

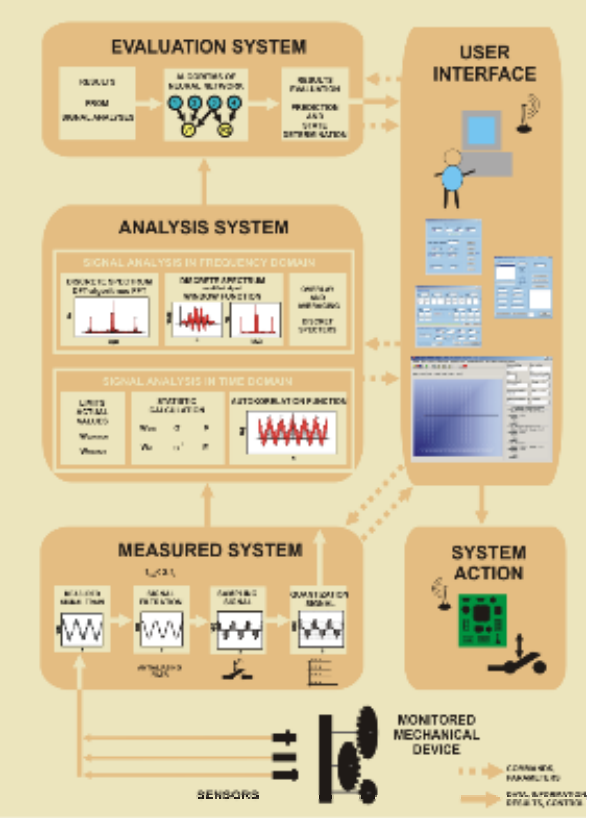

Fig.3. Diagnostic system structure of analysis and signal evaluation

III. ALGORITHMS AND ANALYSES FOR MEASURED SIGNAL DIAGNOSTIC

Algorithms and analysis methods are used for signal diagnostic. This signal is measured on the monitored mechanical device. Results from these analyses are used for mechanical device state detection and for prediction of impending failures. Analyses of signal are computed in time and frequency domain. Measured signals are scanned from the monitored devices in the real-time. These values can be processed by various analysis methods to the applicable results. There are used statistical analyses and computations, too. The analyses methods enable the performance these basic functions in the developing diagnostic system:

- determine impending failures
- detect part of a device, where is failure
- estimate the average time of failure starting
- inform about real system states
- predict device states problems

The measured continuous-time signal is filtering by an Antialising filter for a correct data conversion. Modified signal is sampled to discrete-time signal *w[n]* for following computer processing. The last operation with signal is quantization. The data from signal are moved to the embedded system after the signal modification.

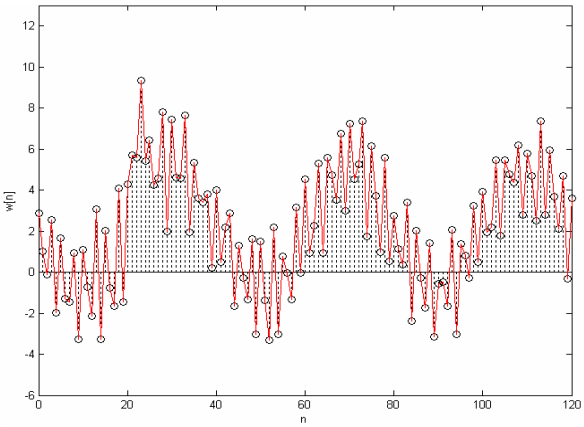

Fig. 4. Example of the measured signal in time domain

The data representing measured signal are processing by algorithms and analysis methodology in the embedded system. The analyses methods usable for this developing automated diagnostic and maintenance system are:

- **time domain signal analyses**
  This analyses type depends on the whole signal bandwidth in a time domain. The time signal analyses are much easer then frequency signal analyses. A results evaluation is almost based on specified critical values, which have not to be exceeded. The time signal analyses are:

  - **immediate signal value** – detection of maximal or minimal values in a signal *w[n]* train. Limit transcendence can detect the monitored device states.

$$w_{MINIMUM} \le w[n_i] \le w_{MAXIMUM} \qquad (1)$$

  - **statistical algorithms** – detection of statistical values of signal *w[n]*, where *N* is a number of samples. These algorithms are used for computation of these parameters of the measured signal:

Mean value $$w_{str} = \lim_{N\to\infty} \frac{1}{N} \sum_{n=-N/2}^{N/2} w[n] \qquad (2)$$

Effective value $$w_{ef} = \sqrt{\lim_{N\to\infty} \frac{1}{N} \sum_{n=-N/2}^{N/2} w^2[n]} \qquad (3)$$

Dispersion $$\sigma^2 = \lim_{N\to\infty} \frac{1}{N} \sum_{n=-N/2}^{N/2} \left(w[n] - w_{str}\right)^2 \qquad (4)$$

Mean power $$P = \lim_{N\to\infty} \frac{1}{N} \sum_{n=-N/2}^{N/2} w^2[n] \quad (5)$$

Function utilizing of the statistical algorithms in a time domain analysis is an Autocorrelation function R[κ]. The Autocorrelation function describes coupling signal values in a time. This function is used for a signal noise removing and a harmonic and periodic signal elements emphasis. Information about phase of the signal harmonic elements is lost.

$$R[\kappa] = \lim_{N\to\infty} \frac{1}{N} \sum_{n=-N/2}^{n=+N/2} w[n]w[n+\kappa] \quad (6)$$
$$\kappa = \ldots,-2,-1,0,1,2,\ldots$$

Time domain diagnostic methods usually used for monitoring of the mechanical devices are:

- Crest factor – the rate of effective signal value (PEAK) and maximum signal value (RMS) – PEAK/RMS. This analysis is sensitive to the mechanical failures already in the beginning.

- Curtosis factor – a statistical signal analysis of normal Gaussian distribution and the value of acuteness observation.

- **frequency domain signal analyses**

This analyses type is more precise. We can observe just a part of the signal bandwidth in a frequency domain. By this analysis, the fault can be located and it can be specified why it was happened, the phase and amplitude spectrum of the signal can be also traced, of course, if there is used a complex signal transform. In the case that some part of the signal is periodic, the Fast Fourier Transform (FFT) is used for converting the signal from the time to the frequency domain. Of course, these analysis methods are more sophisticated and it obtains more advantages but it is more the time consumption compares to the time analysis methods.

Discrete Fourier Transform (DFT) converts discrete-time signal *w[n]* from a time domain to a frequency domain. Result of transformation is *N* complex coefficients W_k of Fourier series, which represent frequency domain of the signal. Relations of direct and inverse Discrete Fourier Transform are:

$$W_k = FR\{w[n]\} = \sum_{n=0}^{n=N-1} w[n]\cdot e^{-j2\pi n\frac{k}{N}} \quad (7)$$
$$w[n] = FR^{-1}\{W_k\} = \frac{1}{N}\sum_{k=0}^{k=N-1} W_k \cdot e^{j2\pi n\frac{k}{N}}$$
$$n = \langle 0, N-1\rangle$$
$$k \in \langle 0, N-1\rangle$$

An amplitude spectrum is even function. It is composed of coefficients W_k by relation:

$$^{FR}|\mathrm{W}| = \{|W_k|\} = \left\{\sqrt{\mathrm{Re}\{W_k\}^2 + \mathrm{Im}\{W_k\}^2}\right\} \quad (8)$$

Relation between samples and frequency of the signal is equal:

$$f = \frac{k\cdot f_S}{N} \quad (9)$$

Where *fs* is sampling frequency of the time-discrete signal and *N* is number of the signal samples used for Discrete Fourier Transform computation.

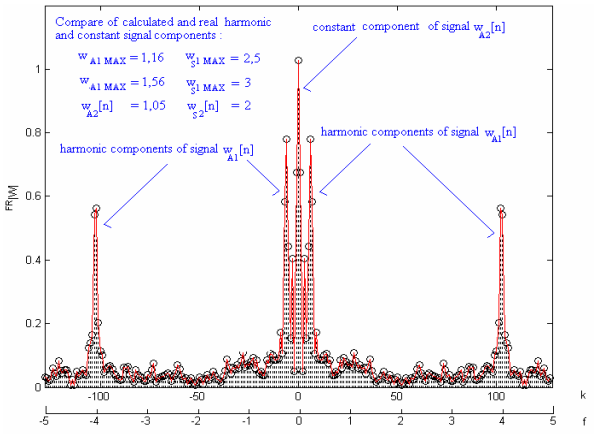

Fig. 5. Example of analysed signal in frequency domain

A phase spectrum is composed of coefficients W_k and it is odd function. The phase spectrum is defined by relation:

$$^{FR}|\theta| = \{\theta_k\} = \left\{arctg\frac{\mathrm{Im}\{W_k\}}{\mathrm{Re}\{W_k\}}\right\} \quad (10)$$

A power spectrum is composed of coefficients W_k by relation:

$$^{FR}P = \left\{|W_k|^2\right\} = \left\{\mathrm{Re}\{W_k\}^2 + \mathrm{Im}\{W_k\}^2\right\} \quad (11)$$

Fast Fourier Transform (FFT) algorithm is used for faster analysis computation compare to Discrete Fourier Transform (DFT). Number of the signal samples has to be choose by relation $N=2^m$, where *m* is integral positive number. Transformation from time to frequency domain and its inversion is given by numbers of multiplications and additions used for transfer:

DFT for *N* samples of discrete-time signal *w[n]* – N^2 additions and N^2 multiplications.

FFT for $N=2^m$ samples of discrete-time signal *w[n]* – *m.N* additions and $\frac{m\cdot N}{2}$ multiplications.

Windows Function (weight function) damps inaccuracy of the frequency signal spectrum computation. Good localization of a measured signal *w[n]* in time interval accordant with samples number *N* raises accuracy of the results. Modified signal $w_A[n]$ by Windows function $w_O[n]$ is equal:

$$w_A[n] = w_O[n] \cdot w[n] \tag{12}$$

Basic used widows functions are:

- Rectangular Windows function

$$w_O[n] = \begin{cases} 1 & 0 \le n \le N_O - 1 \\ 0 & n < 0 \cup n > N_O - 1 \end{cases} \tag{13}$$

- Hanning Windows function

$$w_O[n] = \begin{cases} 1 - \cos\left(\frac{2\pi n}{N-1}\right) & 0 \le n \le N-1 \\ 0 & n < 0 \cup n > N-1 \end{cases} \tag{14}$$

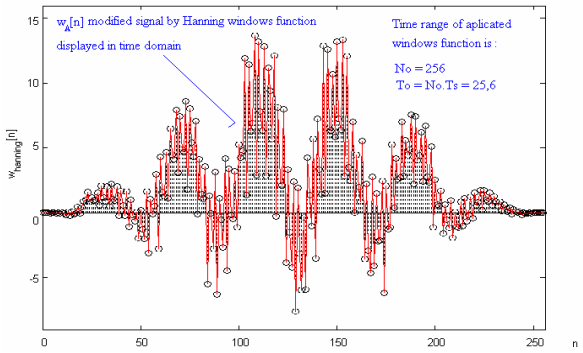

Fig. 6. Example of modified signal $w_A[n]$ in time domain

- Flat-Top Windows function

$$w_O[n] = \begin{cases} 1 - 1,98\cos\left(\frac{2\pi n}{N-1}\right) + 1,29\cos\left(\frac{4\pi n}{N-1}\right) \\ -0,388\cos\left(\frac{6\pi n}{N-1}\right) + 0,0322\cos\left(\frac{8\pi n}{N-1}\right) \quad 0 \le n \le N-1 \\ 0 \qquad n < 0 \cup n > N-1 \end{cases} \tag{15}$$

Improvements of the frequency signal spectrum results can be obtain by the frequency signal spectrum modification. One of the improvement possibilities is **Frequency Spectrum Averaging**, which is equal with relation:

$$W_{k,K} = \frac{1}{K}\sum_{i=1}^{K} W_{k,i} \qquad k = \langle 0, N \rangle \tag{16}$$

The second of the improvement possibilities is **Frequency Spectrum Overlaying**, which is completion of the Frequency Spectrum Averaging. Overlaying of the frequency spectrum improves results and failures eliminates by signal damping at the edge of measured data records. The Frequency Spectrum Overlaying is defined by percents of spectrum overlaying 50%,66.7%,75%.

$$\frac{N_P}{N} \cdot 100\% \tag{17}$$

Frequency domain diagnostic methods usually used for monitoring of the mechanical devices are:

- HF High Frequency Emission method – the energy of vibrations in high frequencies is increasing as early as beginning failure of the monitored device.

- LIN – a signal analysis is based on a wide frequency bandwidth 0,8Hz-16kHz. This analysis is very simple and computed quickly.

- LF Low Frequency Emission method – a vibration speed signal analysis in a frequency bandwidth between 10 – 1000 Hz.

- Envelope analysis – the complex method enables a very detailed detection and analysis. By this diagnostic method there is possible to dedicate part, type of failure, state failure. Theoretically every segment of a rotation device part and every other segment could be analyzed separately, because relative rotation speed of every part is different. The failures can be proved by different frequencies in measured vibration signal. Energy of an analyzed signal is increasing with failure execution especially in high frequencies. In this method, there are measured vibration impulses on a monitored device. The input measured signal is modified by a band-pass digital filter algorithm. Then it is possible to use the Fast Fourier Transform (FFT) for the failure type recognition. The vibration impulses in a signal aren't of a harmonic character. Usually they are modulating the other harmonic components with failure components in a signal on a carrier frequency.

IV. EVALUATION ALGORITHMS

The evaluation algorithms enable determine actual state of monitored mechanical device and likewise it allows estimate impending monitored device states and failures. Parameters of the evaluation algorithms are set by user in the automated user system. The results of the signal analysis methods and the signal algorithms are an input data for evaluation algorithms. The developed evaluation algorithms are composed of Neural Network algorithms. The parameters of the Neural Network algorithms are adjustable by user and some parameters are set by studying signal analyses results from monitored device in diagnostic system learning state. Weight of the inputs and limits of neurons in the Neural Network are set by a training user. The presumption of the correct parameters setting of the Neural Network is to user's knowledge about monitored mechanical device behaviors and the possible device states. Likewise user has to know an estimate time to start device failure or some state from the first problems signifies.

V. CONCLUSION

The specific automated diagnostic and maintenance system application has been developed for real-time and short time data measurement, communication, analysis, and reaction with the use of an embedded system. One of the major research targets is a system upgrading more accurate and faster diagnostics and maintenance computations. The solution of this problem could be predictive or improved control methods implementation. This is a very interesting and formidable task. It is necessary to use a complex mathematical theory and joint it with digital signal processing. For this, we will use a mathematical programming environment – Matlab Simulink and helpful Matlab toolboxes. This program runs on a personal computer PC. The signal processing toolbox is very helpful for Fast Fourier Transformation, various filters, correlation, statistical and other signal computations. By simulation in Matlab Simulink, we can verify measured and calculated real diagnostic system data with simulating data. By these computations, we could recognize the best methodology for the control and the diagnostic of a monitored device. Additionally, we can transfer these pieces of knowledge to the developing embedded system, to the developing program for the diagnostic and maintenance system. The evaluation algorithms allow automatically decide about actual monitored device state and allow automatically predict potential device states.

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Microwave planar band-pass filters using defected ground microstrip structures

Nicolae Militaru[1], Marian Gabriel Banciu[2], Teodor Petrescu[1], George Lojewski[1]

Abstract – In this paper a study of some microwave microstrip band-pass filters using defected ground structures (DGS) is presented. It is shown that the presence of a slot in the ground plane can substantially enhance the electric coupling, or the electric part of a mixed coupling between two microwave resonators. This technique allows designs of tight couplings without the necessity of using very narrow coupling gaps. Based on the results of this study, a 4-pole cross-coupled planar microwave band-pass filter (BPF) with a slot in the ground plane was designed. Compared to a similar microstrip filter without defected ground, its simulated performances indicate some advantages.
Keywords: filter, cross-coupling, defected ground

I. INTRODUCTION

Ground slots have many applications in microwave techniques. Slot antennas [1] and slot coupled antennas [2] have been continuously developed and are widely used in communications. The slot coupling is a convenient way to couple microstrip lines in multilayer circuits [3]. Moreover, stacked filters with slot coupled resonators can provide small-size filter solutions [4].
In this paper investigations on the effects of a ground slot on couplings between hairpin resonators are presented. A slot in the ground plane can enhance the electric coupling, or the electric part of a mixed coupling between two resonators. The above results were used in the design of a 4-pole cross-coupled planar microwave band-pass filter (BPF) with a pair of attenuation poles at finite frequencies, and with a slot in its ground plane.

II. COUPLING CONFIGURATIONS

The configuration of the investigated microstrip defected-ground (DG) structures, presented in Fig.1., contains three dielectric layers. The microstrip circuit was designed on a FR4 dielectric substrate with a thickness of 1.6mm, a dielectric constant of 4.6 and a cooper metallization thickness of 0.035mm. On the top and bottom of the microstrip two air layers of 20mm thickness each were considered, for simulation purposes only.

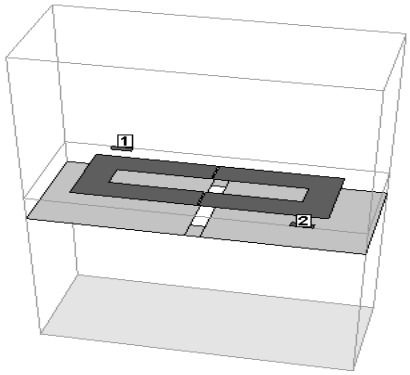

Fig. 1. Geometry of the investigated microstrip DGS

For investigations, 16.6mm long and 12mm wide microstrip hairpin resonators were used, in order to develop applications for the 2.4GHz ISM frequency band. The ground slots are all rectangular, with lengths l_{slot} and widths w.

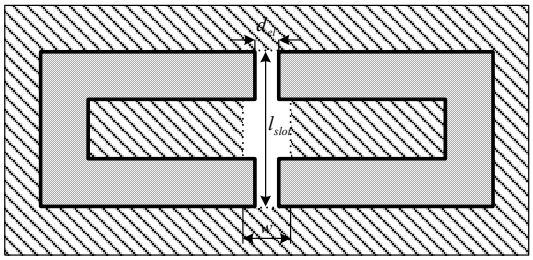

Fig. 2. Electric coupling configuration

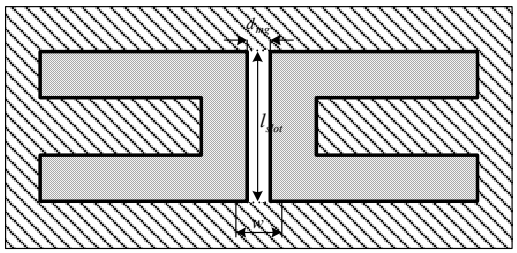

Fig. 3. Magnetic coupling configuration

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The slot length l_{slot} was of 12mm for the electric and magnetic coupling configurations, and 16.6mm for the mixed couplings. The width w was considered as a parameter, in order to study the effect of the ground slot on coupling between resonators.

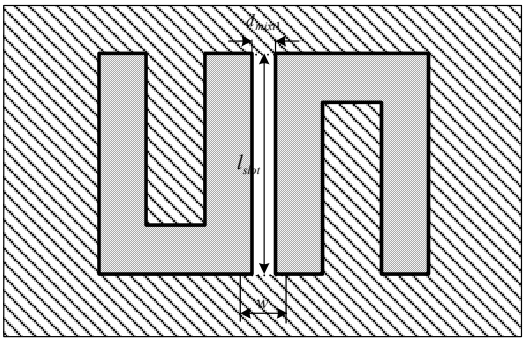

Fig. 4. Type-I mixed coupling configuration

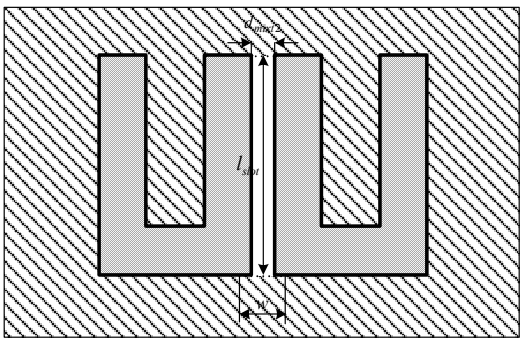

Fig. 5. Type-II mixed coupling configuration

The geometries of the electric and magnetic coupling configurations are shown in Fig.2. and in Fig.3. The geometries of the type-I and the type-II mixed couplings are shown in Fig.4. and Fig.5. Here d_{el}, d_{mg}, d_{mixed1} and d_{mixed2} are the variable coupling gaps for the electric, magnetic, type-I and type-II mixed couplings, respectively.

III. COUPLING COEFFICIENTS

The frequency responses of the coupling structures were obtained by using a method of moments (MoM) simulation software [5]. The coupling coefficient was calculated from the relation

$$k = \frac{f_{p2}^2 - f_{p1}^2}{f_{p2}^2 + f_{p1}^2}, \qquad (1)$$

where f_{p1} and f_{p2} are the two split-resonance frequencies [6].

Fig.6. shows the dependence of the electric coupling coefficient k_{el} on the gap d_{el} between resonators, for several widths w of the ground slot. As expected, the electric coupling coefficient k_{el} is increased by the presence of the defected ground slot.

As shown in Fig.7., the magnetic coupling coefficient k_{mg} is slightly larger, compared to the classical microstrip structure.

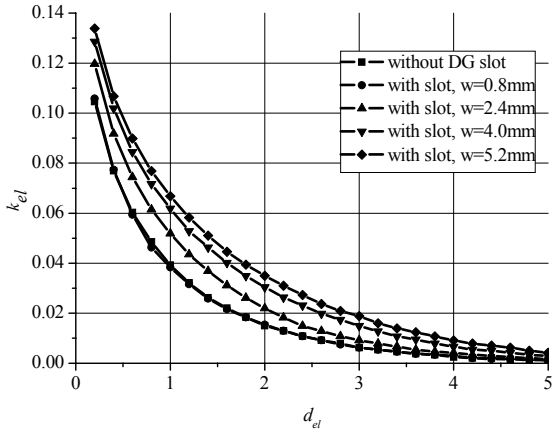

Fig. 6. Electric coupling coefficient, vs. coupling gap (in mm)

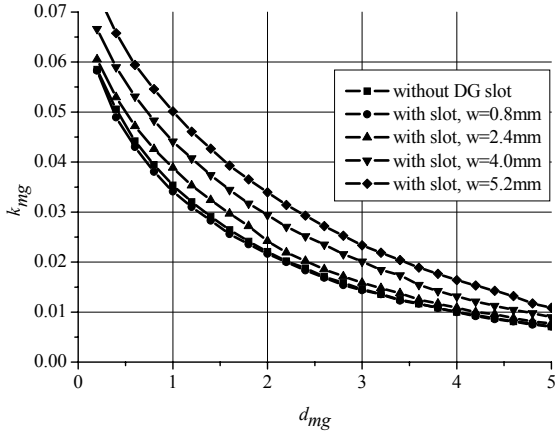

Fig. 7. Magnetic coupling coefficient, vs. coupling gap (in mm)

From Fig.8., it can be noticed that the presence of the slot leads to a significantly increased type-I mixed coupling coefficient k_{mixed1}.

For the electric and type-I mixed coupling coefficients versus the coupling gaps, a monotonic variation was obtained. However, for the type-II mixed coupling, a zero and a local maximum of the coupling coefficient k_{mixed2} versus gap occur. This behavior can be explained by the fact that the electric part of type-II mixed coupling has an opposite sign as its magnetic part. At small gaps d_{mixed2}, the electric part of the coupling is predominant. At larger distances, this part of the coupling decreases faster than the magnetic part; therefore, there is a gap where the two couplings cancel each other. At large distances, the magnetic coupling predominates.

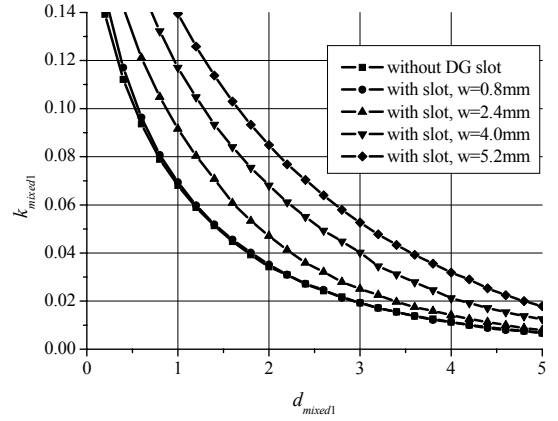

Fig. 8. Type-I mixed coupling coefficient, vs. coupling gap (in mm)

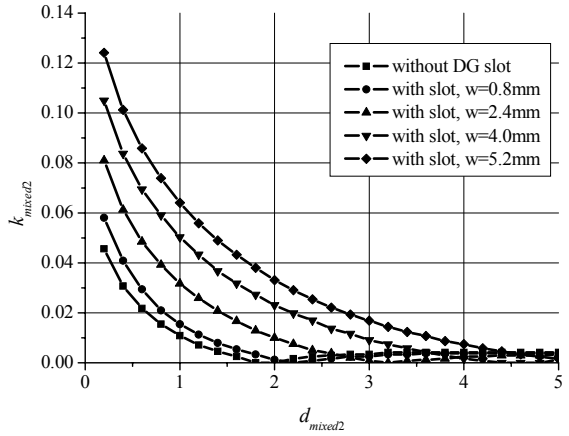

Fig. 9. Type-II of mixed coupling coefficient, vs. coupling gap (in mm)

This behavior is in agreement with other previous results [7] obtained for microstrip resonators without slots in the ground plane.

The results shown in Fig.9. can be used in designing planar band-pass filters with topologies containing type-II mixed couplings.

IV. BAND-PASS FILTER DESIGN AND SIMULATION

Based on the above results, a 4-pole cross-coupled planar microwave band-pass filter with a slot in the ground plane was designed. This band-pass filter meets the following specifications: a center frequency of 2400MHz, a frequency bandwidth of 168MHz, (a 3dB fractionary bandwidth of 7%), and a 4-th order Chebyshev response with a return loss of 20dB in the pass-band. The filter should exhibit two attenuation poles at the frequencies of 2232MHz and 2568MHz.

Using the procedure developed in [8] and an in-house developed program, the extended coupling matrix **M** was computed for a normalized band-pass filter having two attenuation poles at the normalized frequencies:

$$f_{z1} = \frac{1}{FBW}\left(\frac{f_1}{f_0} - \frac{f_0}{f_1}\right) \cong \frac{f_1 - f_0}{\Delta f} = -2 \qquad (2)$$

$$f_{z1} = \frac{1}{FBW}\left(\frac{f_2}{f_0} - \frac{f_0}{f_2}\right) \cong \frac{f_2 - f_0}{\Delta f} = 2 \qquad (3)$$

The obtained matrix,

$$\mathbf{M} = \begin{bmatrix} 0 & 0.371111 & 0.62138 & -0.62138 & -0.37111 & 0 \\ 0.371111 & -1.2872 & 0 & 0 & 0 & 0.37111 \\ 0.62138 & 0 & 0.6904 & 0 & 0 & 0.62138 \\ -0.62138 & 0 & 0 & -0.6904 & 0 & 0.62138 \\ -0.37111 & 0 & 0 & 0 & 1.2872 & 0.37111 \\ 0 & 0.37111 & 0.62138 & 0.62138 & 0.37111 & 0 \end{bmatrix} \qquad (4)$$

corresponds to a transversal 4-th order canonical filter satisfying the specified requirements. Such a filter is almost impossible to be fabricated. However, starting from this **M** matrix, other **M'** matrices corresponding to some topologies suitable for filter realization can be derived, using similitude transformations [9]. Applying some properly chosen similitude transformations on the matrix (4), one gets:

$$\mathbf{M'} = \begin{bmatrix} 0 & -1.02356 & 0 & 0 & 0 & 0 \\ -1.02356 & 0 & 0 & -0.87057 & -0.17046 & 0 \\ 0 & 0 & 0 & -0.76726 & 0.87057 & 0 \\ 0 & -0.87057 & -0.76726 & 0 & 0 & 0 \\ 0 & -0.17046 & 0.87057 & 0 & 0 & 1.02356 \\ 0 & 0 & 0 & 0 & 1.02356 & 0 \end{bmatrix} \qquad (5)$$

The matrix (5) corresponds to a filter having a topology easy to be realized in the form of a planar band-pass filter, composed of four identical microstrip resonators. The layout of such a filter with four hairpin resonators is shown in Fig.10. The input and output lines, directly coupled with resonators no. 1 and 4, have widths of 2.9mm assuring standard 50Ω terminations for the filter.

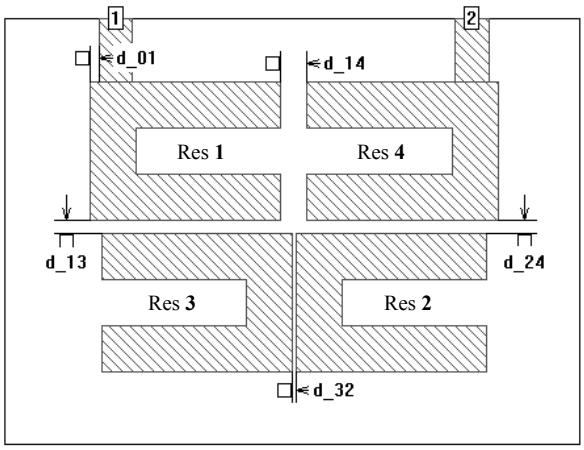

Fig. 10. Layout of the BPF in a classical microstrip technology

The design of the filter from Fig.10. stays in finding the gaps *d*, in order to obtain the necessary external and mutual couplings for the resonators, as derived from the extended coupling matrix **M'**, by a de-normalizing procedure [9]. The de-normalized coupling values are shown in Table 1. The corresponding gaps, as resulted from a full-wave EM-field simulation technique, are presented in Table 2.

Table 1

$Q_{ext0\text{-}1}$	$k_{1\text{-}3}$ (type I mixed)	$k_{1\text{-}4}$ (electric)	$k_{2\text{-}3}$ (magnetic)	$k_{2\text{-}4}$ (type-I mixed)
13.6	0.0609	0.0119	0.0537	0.0609

Table 2

$d_{0\text{-}1}$ [mm]	$d_{1\text{-}3}$ [mm]	$d_{1\text{-}4}$ [mm]	$d_{2\text{-}3}$ [mm]	$d_{2\text{-}4}$ [mm]
0.8	1.18	2.3	0.3	1.18

The necessary magnetic coupling coefficient $k_{2\text{-}3}$ needs a very narrow gap $d_{2\text{-}3}$, of only 0.3mm, technologically hardly to obtain. For a defected ground structure, the same value of the magnetic coupling coefficient can be obtained with the configuration from Fig.3., for a ground slot of 2.8mm

width and 12mm length, and for a gap $d_{2\text{-}3}$ between the resonators 2 and 3 of 0.4mm.
The 3D view of the complete structure of the BPF with a slot in the ground plane is shown in Fig.11.

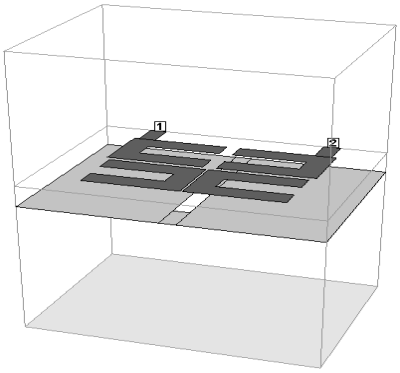

Fig. 11. 3D view of the DG band-pass filter

The EM-simulated performances of the designed band-pass filters are plotted in Fig.12. and Fig.13.

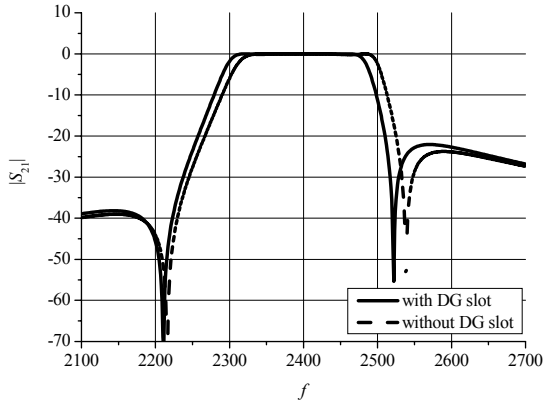

Fig. 12. $|S_{21}|$ (in dB) of the filters from Fig. 10. and Fig. 11., vs. frequency f (in MHz)

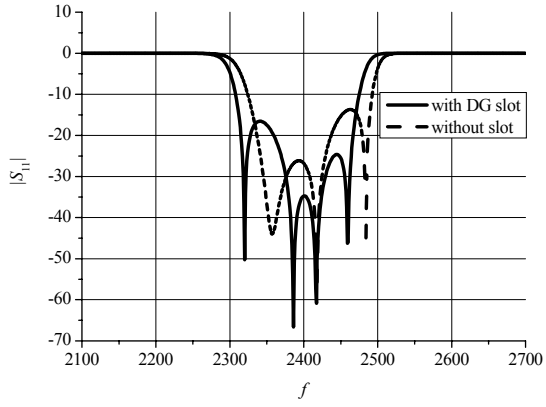

Fig. 13. $|S_{11}|$ (in dB) of the filters from Fig. 10. and Fig. 11., vs. frequency f (in MHz)

It can be noticed that these simulated characteristics are, in general, close enough to the filter requirements.
The filter from Fig.10. exhibits its first attenuation pole at a frequency of 2220MHz, very close to the specification, while the second attenuation pole is located at a frequency of 2540MHz, slightly different to the requirement. The resulted bandwidth is of 150MHz, slightly inferior to the specifications.
The frequency characteristics of the filter with a ground slot are also in good agreement with the specifications.
The presence of the slot leads to a frequency shift of almost 10MHz for $|S_{21}|$, while the in-band return loss seems to be improved, in comparison to the filter without ground slot.
The main advantage of the BPF with a slot stays in the possibility of using a larger gap between resonators 2 and 3 and thus to relax fabrication tolerances.

V. CONCLUSIONS

The increase of couplings in the presence of a ground slot has a simple physical explanation. For a conventional microstrip structure, in the electric coupling configuration, many of the electric lines starting from a resonator end on the ground plane. In the presence of the slot, a part of these lines are forced to end on the other resonator, enhancing this way the electric coupling, or the electric part of a mixed coupling.
These results were used in the design of a BPF with a ground slot. The needed couplings were obtained using an in-house developed program.
The filter's layout was designed after a study of the coupling coefficients versus gaps, based on EM-field simulation.
EM-simulation of the designed defected ground filter structure showed the possibility of using larger gaps between resonators, when tight couplings are needed. This design technique can be applied to many other types of band-pass filters, allowing a relaxation of the fabrication tolerances.

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Modeling, Analysis and Simulation Results Regarding a Power Factor Correction Rectifier

Mircea Băbăiţă[1], Viorel Popescu[2], Adrian Popovici[3], Petru Papazian[4]

Abstract – This paper proposes a new control technique for single-phase boost power-factor-correction (PFC) rectifiers that improves the dynamic response of the converter to load steps without the need of a high crossover frequency of the voltage loop. So a low distortion of the input current is easily achieved. A 100W power-factor correction rectifier with the proposed control scheme has been designed, simulated and implemented, validating the concept.
Keywords: Power factor correction, average current control, rectifiers, power conversion

I. INTRODUCTION

The power-factor-correction rectifiers based on a boost converter are one of the most popular topologies in accordance with harmonic distortion standards, like IEC 6100-3-2, IEC 6100-3-4 and CISPR 11 [3], [4], [5]. Low harmonic distortion is achieved by using average current-mode control (ACC) [1], [2] with bandwidth of the voltage loop limited to about 20 Hz in order to properly attenuate the second line harmonic (100Hz) that appears at the output voltage of the converter [6]. As a result, the dynamic response of the output voltage to load changes is slow.

In the last years, several techniques have been proposed to overcome this problem. The basis of those methods is to eliminate the ripple at the frequency of the second line harmonic from the control signals in order to increase the voltage loop crossover frequency. The main drawback of those solutions is that they all significantly increase the complexity of the control circuit, by adding multipliers/dividers, A/D circuits, digital controllers, field-programmable gate arrays etc.

This paper proposes a new robust model-following ACC scheme (RMACC) with a high disturbance rejection and an analog implementation applied to boost PFC rectifiers. In case of a PFC rectifier, the amplification of the output voltage ripple would be especially disturbing, because the second line harmonic present at the control signals would be amplified. The advantages of the proposed control loop applied to PFC rectifiers are:

- RMACC uses a reference model that has a low-pass nature, so that the output voltage ripple is not amplified. Therefore the contents of the second line harmonic present at the control signals is similar to that of conventional ACC, so that a low input current distortion can be achieved.
- RMACC decreases significantly the closed-loop output impedance of the PFC rectifier at low frequencies. Hence, the dynamic response of the output voltage to load steps is faster.
- RMACC does not add significant complexity to the control circuits.

The proposed control method for PFC converters is useful in those applications that request fast response of the output voltage to load steps: uninterruptible power system (UPS), power supplies systems for telecom, computers applications, etc [9].

A 100-W PFC rectifier based on a boost converter with RMACC has been designed, simulated and implemented, validating the concept.

II. DESCRIPTION OF THE RMACC

II.1. Small-Signal Model of an ACC Rectifier

The ACC scheme of a typical boost PFC rectifier with feedforward of the rectifier input voltage is shows in Fig.1. A linear small-signal model of the ACC-controlled boost PFC rectifier is shown in Fig.2, where:

Rs	current sensing gains;
β	voltage sensing gains;

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$\hat{v}_g(s)$ rectified input voltage;

$\hat{v}_o(s)$ output voltage;

$\hat{i}_L(s)$ inductor current;

V_{ref} reference voltage;

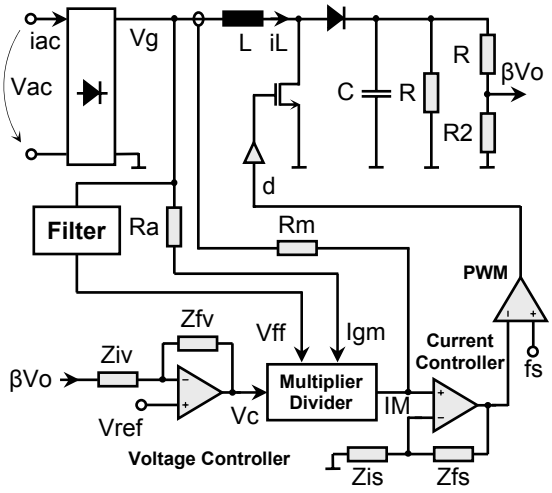

Fig.1 Typical Boost rectifier with ACC.

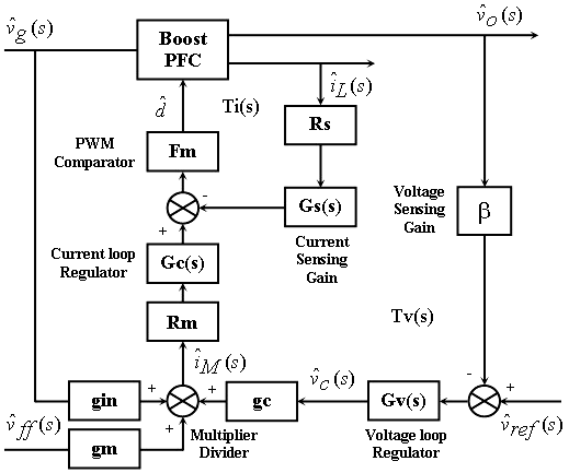

Fig.2 Small-signal model of the PFC rectifier.

F_m PWM modulator gain;

$G_s(s)$ transfer function of the current regulator;

$$G_s(s)=\frac{Z_{fs}(s)}{Z_{is}(s)},\quad G_c(s)=1+G_s(s), \tag{1}$$

$G_v(s)$ transfer function of the voltage regulator;

$$G_v(s)=\frac{Z_{fv}(s)}{Z_{iv}(s)}, \tag{2}$$

$T_i(s)$ loop gain of the current loop;

$T_v(s)$ loop gain of the voltage loop;

$\hat{i}_{gm}(s)$, $\hat{v}_{ff}(s)$, $\hat{v}_c(s)$, $\hat{i}_M$, small signal of the input/output multiplier-divider block;

I_{gm}, V_{ff}, V_c, I_M, steady state input/output of the multiplier-divider block;

g_{in}, g_c, g_m equivalent gains of the multiplier-divider small signal model.

$$g_{in}=\frac{K_{ac}\cdot V_c}{V_{ff}^2} \tag{3}$$

$$g_c=\frac{K_{ac}\cdot V_{g-RMS}}{V_{ff}^2}\approx\frac{K_{ac}}{K_{ff}^2\cdot V_{g-RMS}} \tag{4}$$

$$g_m=-2\cdot\frac{I_M}{V_{ff}^2} \tag{5}$$

$$K_{ac}=\frac{i_{gm}(t)}{v_g(t)}=\frac{1}{R_{ac}} \tag{6}$$

$$K_{ff}=\frac{V_{ff}}{V_{g-DC}}\approx\frac{V_{ff}}{V_{g-RMS}} \tag{7}$$

Closing the current loop *Ti(s)*, the voltage regulator *Gv(s)* must compensate an ACC power stage transfer function $VOC(s)=\hat{v}_o(s)/\hat{v}_c(s)$. This can be approximated by a first order system [1], [2], as shown in [10]. $Z_O(s)=\hat{v}_o(s)/\hat{i}_o(s)\big|_{\hat{v}c=0}$ and $\hat{i}_o$ are the ACC open-loop output impedance and the load disturbance. An approximation of *VOC(s)* can be derived by neglecting the high-frequency dynamics:

$$VOC(s)=\frac{\hat{v}_o(s)}{\hat{v}_c(s)}\Big|_{\hat{i}_O=0}\approx\frac{K_{ac}\cdot R_m}{K_{ff}^2}\cdot\frac{1}{2V_o}\cdot\frac{\frac{R}{R_s}}{1+\frac{RC}{2}s} \tag{8}$$

Do to the action of the feedforward, *VOC(s)* doesn't depend on the input voltage *Vg*, K_{ac} and K_{ff} are constant.

The stability of the control system is given by the voltage loop gain, *Tv(s)*:

$$T_v(s)=G_v(s)\cdot VOC(s)\cdot\beta \tag{9}$$

The closed-loop output impedance $Z_{ocl}(s)$ is expressed by:

$$Z_{ocl-ACC}(s)=\frac{Z_o(s)}{1+T_v(s)}=Z_o(s)\cdot S(s) \tag{10}$$

where $S(s)=1/(1+T_v(s))$ is the sensitivity function, being $|S(j\omega)|<1$ up to the crossover frequency of the voltage loop, f_{cv}, and $|S(j\omega)|\approx 1$ at frequencies higher than f_{cv}. *S(s)* expresses the disturbance rejection, being a powerful index to analyze the robust performance of a control system.

The general expression of $G_v(s)$ in conventional ACC is:

$$G_v(s)=\frac{\omega_{iv}\cdot(1+\frac{s}{\omega_{zv}})}{s\cdot(1+\frac{s}{\omega_{pv}})}=\frac{\frac{\omega_{c-v}}{K\cdot\beta}\cdot(1+s\frac{R_{nom}C}{2})}{s\cdot(1+\frac{s}{2\pi f})} \tag{11}$$

The zero ω_{zv} is chosen to compensate the dominant pole of the power stage, *VOC(s)*. In order to atenuate

the second line harmonic at the control signals, the pole ω_{iv} is placed around half the frequency of the output voltage ripple, i.e., around the line frequency f (50Hz). The gain ω_{iv} :

$$\omega_{iv} = \frac{\omega_{c-v}}{\frac{K_{ff}^2 2V_o R_s}{K_{ac} R_m R_{nom}}\beta} = \frac{\omega_{c-v}}{K \cdot \beta} \qquad (12)$$

is chosen taking into account the desired crossover frequency, ω_{c-v}, of $T_v(s)$. R_{nom} is the load resistance at full load.

II.2. The Proposed RMACC Rectifier

The proposed RMACC scheme is shown in Fig.3.

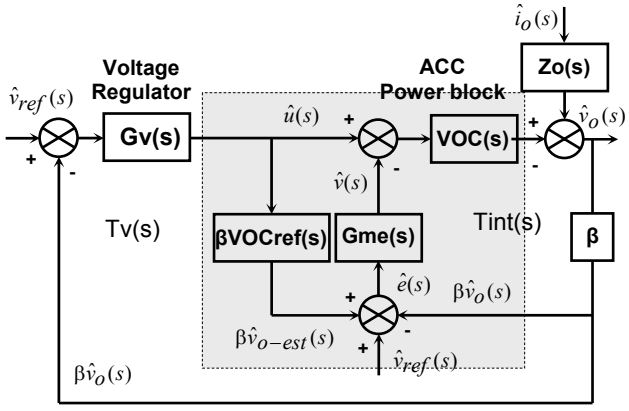

Fig.3 The proposed RMACC scheme.

After some block algebra, results the equivalent scheme presented in Fig.4, where $T_{ref}(s) = \beta G_{me}(s) VOC_{ref}(s)$. The current loop $T_i(s)$ is the same as in conventional ACC and it contains the same current regulator, $G_s(s)$, so that $T_i(s)$ is not represented in Fig.3.

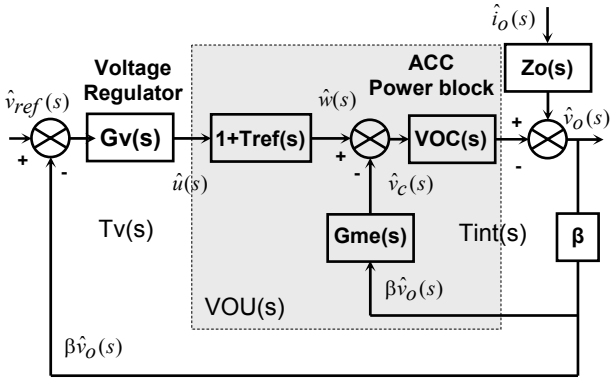

Fig.4. Equivalent scheme of the proposed RMACC.

An additional internal loop with model-following effects $T_{\text{int}}(s)$ is added before closing the outer voltage loop $T_v(s)$ with the voltage regulator $G_v(s)$. The internal loop contains two blocks: a „modeling error" PI regulator $G_{me}(s)$ and a fixed reference model transfer function $\beta \cdot VOC_{ref}(s)$, which is low pass and first order like a conventional ACC power stage. The expression of the reference model is:

$$VOC_{ref}(s) = \frac{K_{ac} \cdot R_m}{K_{ff}^2} \cdot \frac{1}{2V_o} \cdot \frac{\frac{R_{nom}}{R_s}}{1 + \frac{R_{nom} C}{2} s} \qquad (13)$$

The output of the reference model $\beta \cdot v_{o-est}$ is an estimation of the sensed output voltage $\beta \cdot v_o$ if $VOC(s) = VOC_{ref}(s)$ and without disturbances. Thus, the signal *e(s)* is an estimated error that represents the difference between the actual power stage and the chosen reference model. The modeling error regulator $G_{me}(s)$ is designed for the adequate loop shaping of $T_{\text{int}}(s)$. The gain of $T_{\text{int}}(s)$ at the frequency of the second line harmonic must be low enough to assure that no significant distortion appears in the line current. Therefore, the crossover frequency of $T_{\text{int}}(s)$, $f_{C-\text{int}} = \omega_{C-\text{int}} / 2\pi$, should be limited to around 10-20 Hz. The loop gain of the internal loop is:

$$T_{\text{int}}(s) = \beta \cdot G_{me}(s) \cdot VOC(s) \qquad (14)$$

The intermediate transfer functions are:

$$VOW(s) = \frac{\hat{v}_o(s)}{\hat{w}_o(s)}\Big|_{\hat{i}o=0} = \frac{VOC(s)}{1 + T_{\text{int}}(s)} \qquad (15)$$

$$T_{ref}(s) = \beta G_{me}(s) VOC_{ref}(s) \qquad (16)$$

This are used for the definition of the modified power stage transfer function *VOU(s)*:

$$VOU(s) = \frac{\hat{v}_o(s)}{\hat{u}(s)}\Big|_{\hat{i}o=0} = VOW(s) \cdot (1 + T_{ref}(s))$$
$$= VOC(s) \cdot \frac{(1 + T_{ref}(s))}{(1 + T_{\text{int}}(s))} \approx VOC_{ref}(s) \qquad (17)$$

VOU(s) is the transfer function „seen" by the outer voltage regulator of RMACC $G_v(s)$. $T_{ref}(s)$ is a fixed transfer function and it can be defined as a „reference loop gain", because it agrees with $T_{\text{int}}(s)$ if $VOC(s) = VOC_{ref}(s)$. The range of frequencies where $|T_{\text{int}}(j\omega)| >> 1$ and $|T_{ref}(j\omega)| >> 1$, the transfer function seen by the voltage regulator is a fixed one and it agrees with $VOC_{ref}(s)$, i.e., $VOC(s) \approx VOC_{ref}(s)$. Therefore, the controller of the main voltage loop $G_v(s)$ can be designed to compensate the reference model, which is a fixed transfer function. That is the basis of the model following action of the inner loop and it justifies the approximation made in the last term of (17), which is valid in the frequency range where $|T_{\text{int}}(j\omega)| >> 1$ and $|T_{ref}(j\omega)| >> 1$.

However, the main benefit of RMACC in this application is not the model-following effect, but the improvement of the closed-loop output impedance by means of an easy and systematic technique. The loop shaping of $T_v(s)$:

$$T_v(s) = \beta \cdot G_v(s) \cdot VOU(s) \approx \beta \cdot G_v(s) \cdot VOU_{ref}(s) \quad (18)$$

by means of the voltage controller must take into account that the crossover frequency is limited by the distortion of the line current. Therefore, a crossover frequency $f_{C-\text{int}} = \omega_{C-\text{int}} / 2\pi$ up to about 10-20 Hz should be chosen of $T_v(s)$.

In Fig.3 a double injection of the reference voltage in the loop can be noticed: as a reference voltage for $G_v(s)$ and as a reference of $G_{me}(s)$. The reason for this is that in steady state the integrating character of both regulators yields $V_{ref}(s) = \beta V_o$, and $\beta V_{o-est} + V_{ref} - \beta V_o = 0$, so that $\beta V_{o-est} = 0$. With this double injection of V_{ref} the output of the reference model is zero in steady state, only acting around zero in the presence of disturbances. It's an easy way to avoid the saturation of the reference model output.

II.3. Improvement of the Closed-Loop Output Impedance

With ACC and a conventional PI voltage regulator, the reduction of $Z_{ocl}(s)$ at low frequencies implies to increase the crossover frequency, f_{C-v} of $T_v(s)$, which is strongly limited by the distortion of the line current. With RMACC, $Z_{ocl}(s)$ depends not only on $G_v(s)$, but also on $T_{\text{int}}(s)$ and on $T_{ref}(s)$. Therefore, the low-frequency closed-loop output impedance can be reduced without the need of having a high f_{C-v}.

In PFC boost rectifiers with feedforward loop, the actual power stage *VOC(s)* suffers from little variations with respect to $VOC_{ref}(s)$ around the crossover frequency of the voltage loop, i.e., $VOC(s) \approx VOC_{ref}(s)$. Therefore, if $G_v(s) = G_{me}(s)$, the loop gains will be similar i.e., $T_{\text{int}}(s) \approx T_{ref}(s) \approx T_v(s)$. In this way, a single loop shaping has to be performed for the three loop gains, simplifying the design of RMACC (Fig.4).
Moreover, the closed loop output impedance can be expressed by:

$$Z_{ocl-RMACC}(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} \approx \frac{Z_o(s)}{(1+T_v(s))^2} = Z_o(s) \cdot S^2(s) = Z_{ocl-ACC}(s) \cdot S(s) \quad (19)$$

Both $T_{\text{int}}(s)$ and $T_v(s)$ have a low crossover frequency like the voltage loop gain in the conventional ACC of a PFC rectifier. In spite of having low crossover frequencies, the low frequency output impedance of the PFC rectifier is lower with RMACC than with ACC, so that the dynamic response to load steps is expected to be faster.

III. DESIGN OF THE RMACC RECTIFIER

Conventional ACC and the proposed RMACC schemes have been applied to a boost PFC rectifier with: $V_{ac} = 220V$, $f = 50Hz$, $V_o = 400V$, $P_o = 100W$, $L = 1mH$, $C = 470\mu F$, $f_s = 100kHz$, $R_s = 0{,}2\Omega$, $\beta = 0{,}0125$, $K_{ac} = 1{,}47 \cdot 10^{-6}\, A/V$, , $F_m = 0{,}19V^{-1}$, $R_m = 4{,}3 \cdot 10^3\,\Omega$, $R_{nom} = 640\Omega$, $K_{ff} = 17{,}63 \cdot 10^{-3}$.

The values of *L* and *C* have been chosen so that the inductor current ripple $\Delta i_L \approx 1A$, with a holdup time $\Delta t \approx 64ms$. Δt is defined as the time at which the output voltage decreases to $V_o = 300V$ after disconnecting the line voltage.

A current regulator $G_s(s)$ designed by means of conventional loop-shaping techniques [1], [2] has been chosen. The current loop crossover frequency is about 16kHz with a phase margin of 60°. The same current regulator is used with ACC and with RMACC. The voltage loop with conventional ACC is closed with a voltage regulator. The theoretical crossover frequency with that controller is about 8 Hz. The gain of $Tv(j\omega)$ at the frequency of the second line harmonic (100 Hz) is lower than -35dB.

Due to the feedforward path, *VOC(s)* does not depend on the input voltage around the voltage loop crossover frequency. The load variations only affect *VOC(s)* at very low frequencies, so that the approximation $VOC(s) \approx VOC_{ref}(s)$ can be made.
$G_v(s) = G_{me}(s)$ and $T_{\text{int}}(s) \approx T_{ref}(s) \approx T_v(s)$. If the gain of $T_{\text{int}}(s)$ at 100Hz has been designed to be small, also the gain of $T_v(s)$ results as small. Following that approach, the transfer functions of the chosen regulators are:

$$G_s(s) = \frac{100000}{s} \cdot \frac{1+s/15000}{1+s/300000} \quad (20)$$

for ACC and RMACC;

$$G_v(s) = \frac{60}{s} \cdot \frac{1+s/8}{1+s/120} \quad (21)$$

for ACC and RMACC;

$$G_{me}(s) = \frac{60}{s} \cdot \frac{1+s/8}{1+s/120} \quad (22)$$

$$\beta VOC_{ref}(s) = \frac{0{,}85}{1+s/8} \quad (23)$$

IV. SIMULATION RESULTS

A boost PFC rectifier with the same values (Fig.5) and regulation circuits has been simulated (in CASPOC), built and tested. The control stage schematic has been built with a UC3854 PFC integrated circuit [8]. Schematic of the experimental prototype of the additional internal loop is shows in Fig.6.

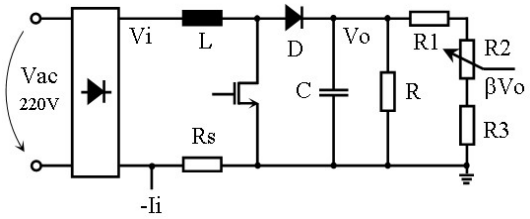

Fig.5 The used boost PFC rectifier.

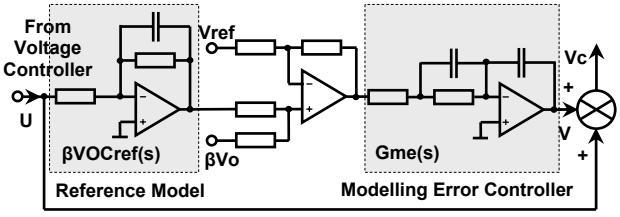

Fig.6. Schematic of the experimental prototype of the additional internal loop.

Fig.7 shows the measured gain Bode plots of the open-loop output impedance $Zo(j\omega)$ and of the closed-loop output impedance with both ACC and RMACC $Z_{ocl-ACC(j\omega)}$ and $Z_{ocl-RMACC(j\omega)}$, respectively, with $P_o = 100W$ (full load) and $V_g = 220V$.

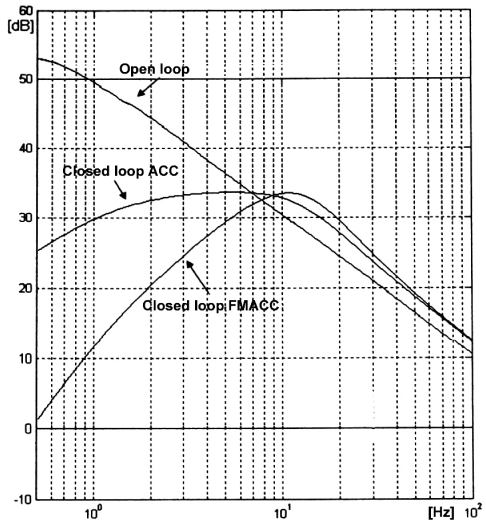

Fig.7 Module of the measured output impedance with ACC and RMACC.

An improvement of more than 20 dB at low frequencies in favor of RMACC is noticed. Note that the output impedance of RMACC is much smaller at low frequencies than that of ACC. Therefore, the dynamic response of the output voltage to load steps is expected to be faster.

Fig.8 and Fig.9 shows the line voltage, the input current and the normalized harmonic spectrum of the line current for 220V, $P_o = 100W$ with ACC.

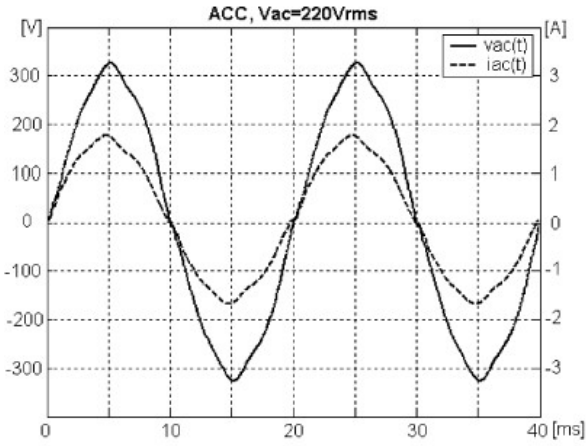

Fig.8. The line voltage and the input current with ACC.

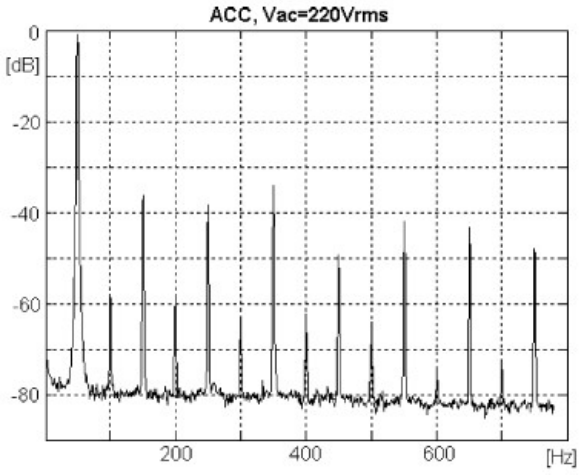

Fig.9. The input current harmonics with ACC.

Fig.10, Fig.11 and Fig.12 shows the same measurements, in the same conditions with RMACC.

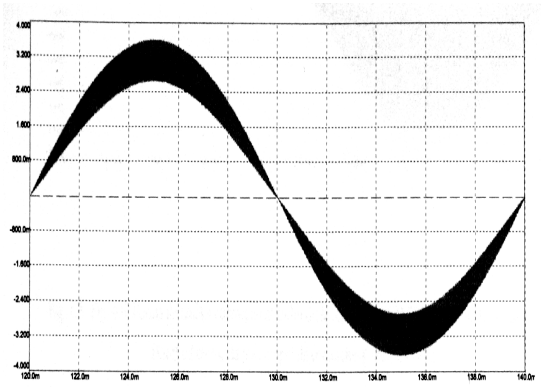

Fig.10. The input current with RMACC.

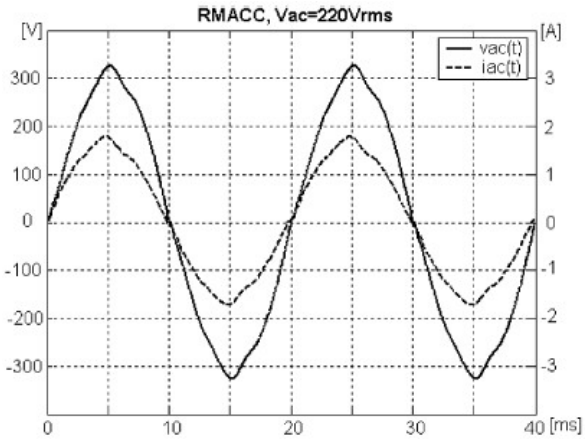

Fig.11. The line voltage and the input current with RMACC.

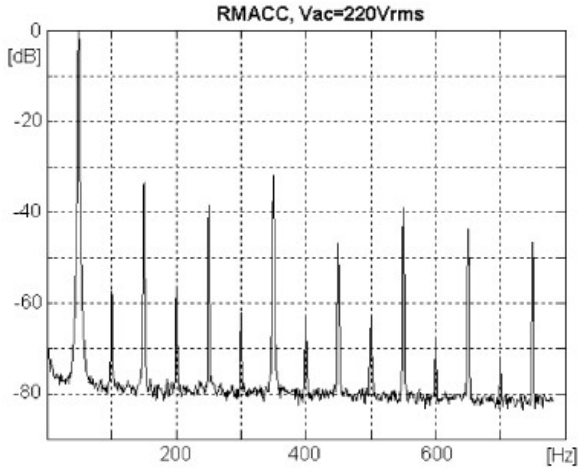

Fig.12. The input current harmonics with RMACC.

Table 1 shows the comparative experimental results of the input voltage distortions THDv %, of the line current distortion THDi % and of the power factor PF, with conventional ACC and with the proposed RMACC control scheme.

Table 1

Control Mode	Parameter	Line Voltage-Input Current 220V – 1,2A
ACC	THDv	3,6%
	THDi	6,2%
	PF	0,99
RMACC	THDv	3,6%
	THDi	5,8%
	PF	0,99

Note that no significant differences between ACC and RMACC are remarkable, so that their performances from the line point of view are similar. In other words, the improvement of the closed-loop output impedance is achieved with no additional; distortion of the line current.

V. CONCLUSIONS

This paper analyzed a robust model-following ACC loop applied to a 100W boost PFC rectifier. It has been shown that the low-frequency output impedance of the converter is greatly reduced, so that the dynamic response of the output voltage to load steps is faster. The improvement of the transient response is achieved with similar values of the input current distortion and of the power factor as with conventional ACC. RMACC improves the output impedance without the need of high crossover frequencies in any of its loops, so that the control signals ripple at the frequency of the second line harmonic is easily attenuated.

The practical implementation of RMACC consists of adding an inner loop based on a low-pass first-order reference model and a conventional PI regulator, besides the outer voltage loop.

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New Control for Charge Pump Buck Converter

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Abstract – The paper proposes a new voltage control methodology for the "Charge Pump Buck Converter". During each commutation, the converter pumps a defined charge to the load circuit. The original circuit was improved and is able to control the output current both through the switching frequency and through the amount of electrical charge which is delivered to the load during each commutation. The control through the charge is very efficient for low rates between output voltage and input voltage. The main equations that can be used for the converter's design are also presented in the paper.
Keywords: dc/dc power converter

I. INTRODUCTION

The circuit presented in this paper tries to respond to present dc/dc converters' demands: high reliability, fast transient response and small values for the passive L-C components involved both in the converter topology and in the dc output filter's circuit. The circuit presented in Fig.1 assures high reliability and a less power switcher's stress due to zero current switch (ZCS) for all turn off commutations. The output frequency of the output current pulses is two times greater than the devices' switching freque variation.

II. OPERATION PRINCIPLES AND OPERATION

The circuit scheme of the proposed converter is shown in Fig.1. The circuit is composed by switches $S_1 \div S_4$ and capacitor C, which is equivalent to a controlled switch, the equal inductances $L_1=L_2=L$ and the switches S_5 and S_6 used as controlled turn on diodes. One time the switches S1 and S3 are turned on and the switches S_2 and S_4 are turned off and the input current i_i (Fig.1) flows through inductance L_1 . When the voltage across S_5 riches a defined value ($u_{S5}=U_X \geq 0$), the S_5 is turn on and the current i_{L1} is transferred through device S_5 . The other time the switches S_2 and S_4 are turned on and the switches S_1 and S_3 are turned off and the input current i_i flows through inductance L_2 . Device S_6 will assure the current flows through inductance L_2 in the same conditions as device S_5 . During the commutation process, the voltage across capacitor C varies between the limits $\pm(U_i + U_X)$ where U_X represents the positive voltage across S_5 or S_6 that determines the turn on command of these devices and U_i is the input dc voltage.

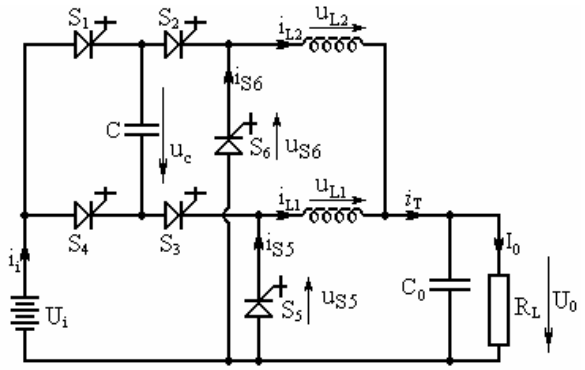

Figure 1. Proposed circuit topology

With respect to the shape of the inductance current i_{L1} and i_{L1}, two conduction modes can be performed:

- Discontinuous operation mode, when the current through the inductor L_1 or L_2 has zero value intervals.
- Continuous operation mode, when the current through the inductor L_1 or L_2 has no zero value intervals.

III. DISCONTINUOUS MODE OPERATION

Discontinuous operation mode is described in Fig.2. There are six stages. The voltage across the capacitor C, the currents $i_{S1}=i_{S3}$, the voltage u_{S5} and the current i_{S5} are plotted with continue line the current i_{L2} and the voltage u_{S6} are plotted with dot line.

D.1. The First stage

The First stage [$t \in (t_{0d1} ; t_{1d1})$] starts at t_{0d1} when S_1 and S_3 are soft (ZCS – zero current switch) turned on. The voltage across capacitor C at point t_{0d1} is $-(U_i + U_X)$. In this stage, the resonant L_1-C circuit

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assures a resonant charge of the capacitor C, from $-(U_i+U_X)$ to $+(U_i+U_X)$. For this stage the input current $i_i(t)$ is equal to inductance current $i_{L1}(t)$ (Fig.2). The equivalent circuit for this stage is plotted in Fig.3. The equations which describe the behaviour of the circuit are:

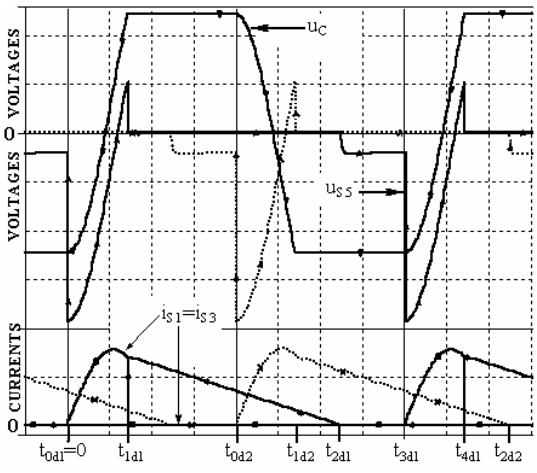

Fig. 2. Discontinuous mode circuit operation

$$U_i = u_C(t) + u_{L1}(t) + U_0 \qquad (1)$$

We suppose that the input voltage U_i and the output voltage U_0 have constant DC values.
The relations (2) are also available.

$$u_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} \qquad u_C(t) = \frac{1}{C}\int i_{L1}(t) \qquad (2)$$

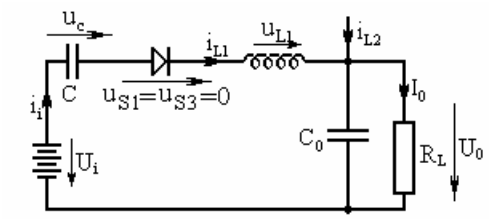

Fig. 3. Equivalent circuit for stage 1

Relations (2) are inserted in equation (1) and equation (3) might found out:

$$\frac{d^2 i_{L1}(t)}{dt} + \omega_0^2 i_{L1}(t) = 0 \quad \text{where} \quad \omega_0^2 = \frac{1}{L_1 C} \qquad (3)$$

At the point $t_{0d1}=0$ the values of the current through the inductance and voltage across capacitor C are:

$$i_L(t_{0d1}=0) = 0 \quad \text{and} \quad u_C(t_{0d1}=0) = -(U_i+U_X) \qquad (4)$$

From equation (1) the voltage across inductance, at point t_{0d1} is :

$$u_L(t_{0d1}=0) = U_i - u_C(t_{0d1}) - U_0 = 2U_i + U_X - U_0 \qquad (5)$$

Solving equation (3) according to the initial conditions (4) and (5), the main circuit's electric parameters may be found out:

$$\begin{aligned} i_L(t) &= C\omega_0(2U_i + U_X - U_0)\sin\omega_0 t \\ u_C(t) &= U_i - U_0 - (2U_i + U_X - U_0)\cos\omega_0 t \\ u_L(t) &= (2U_i + U_X - U_0)\cos\omega_0 t \end{aligned} \qquad (6)$$

The voltage across switch S_5 (Fig. 1.), is:

$$u_{S5}(t) = -U_0 - (2U_i + U_X - U_0)\cos\omega_0 t \qquad (7)$$

At the point $t_{0d1}=0$, the voltage across switch S_5 is $-(2U_i+U_X)$ and represents the maximum reverse voltage of this device. At the point t_{1d1}, the voltage across switch S_5 is $U_X \geq 0$, and S_5 is turn on. The point t_{1d1} can be found out from equation (7):

$$t_{1d1} = \frac{1}{\omega_0}\arccos\left(-\frac{U_0 + U_X}{2U_i + U_X - U_0}\right) \qquad (8)$$

At the point t_{1d1} the voltage across capacitor C has a maximum value of:

$$u_C(t_{1d1}) = U_i + U_X \qquad (9)$$

The capacitor C must be a bipolar one with a breakdown voltage larger than (U_i+U_X).
The maximum current I_{LMd} through the inductance is performed when $\omega_0 t = 0.5\pi$ (from equation 6).
At point t_{1d1} the current I_{1d1} through the inductance L_1 may be found out from equations (6) and (8).

$$I_{LMd} = i_{L1}\left(\frac{\pi}{2\omega_0}\right) = C\omega_0(2U_i + U_X - U_0) \qquad (10)$$

$$I_{1d1} = i_{L1}(t_{1d1}) = 2C\omega_0\sqrt{U_i^2 + U_i U_X - U_i U_0 - U_0 U_X} \qquad (11)$$

In case $U_X = 0$, S_5 is soft turn on, and it behaves as a diode.

D.2. The Second stage

The Second stage [$t\in(t_{1d1}\ ;\ t_{2d1})$] starts at point t_{1d1} when the voltage across capacitor C is (U_i+U_X), switch S_5 turns on and the currents through S_1 and S_3 becomes zero. During this stage the devices S_1 and S_3 may be soft (ZCS) turned off before point t_{2d1}. The currents $i_{L1}(t)$ and $i_{S5}(t)$ are equal and linearly decrease to zero in the time interval $t_{1d1} \div t_{2d1}$. The equivalent circuit for this stage is presented in Fig.4.

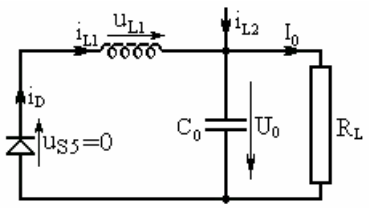

Figure 4. Equivalent circuit for stage 2

The equations that describe the behaviour of the circuit are:

$$\begin{aligned} u_{L1}(t) &= L_1 \frac{di_{L1}(t)}{dt} \\ u_{L1}(t) + U_0 &= 0 \end{aligned} \qquad t\in[t_{1d1}\ ,t_{2d1}] \qquad (12)$$

Solving the equation (12) according to the restriction presented in relation (11), the current variation through inductance L, may be found out:

$$i_L(t) = -\frac{U_0}{L_1}(t - t_{1d1}) + 2C\omega_0\sqrt{U_i^2 + U_iU_X - U_iU_0 - U_0U_X}$$
$$t \in [t_{1d1}, t_{2d1}] \quad (13)$$

From the equation (13), the point t_{2d1} when the current $i_{L1}(t)$ becomes zero, may be found out:

$$t_{2d1} = t_{1d1} + \frac{2}{\omega_0 U_0}\sqrt{U_i^2 + U_iU_X - U_iU_0 - U_0U_X} \quad (14)$$

D.3. The Third stage

The third stage [$t \in (t_{2d1}$; t_{3d1})] is characterized by zero current values for all semiconductor devices. In this stage the load is fed by the energy stored in the output capacitor C_0 , and by the current which flows through L_2. The next three stages are associated to the contribution of the current i_{L2} to the output current i_T , (Fig.1).

D.4. The Fourth stage

The fourth stage [$t \in (t_{0d2}$; t_{1d2})] starts at t_{0d2} when S_2 and S_4 (Fig.1) are soft (ZCS – zero current switch) turned on. In this stage, the resonant L_2-C circuit assures a resonant charge of the capacitor C, from $+(U_i + U_X)$ to $-(U_i + U_X)$. For this stage the input current $i_i(t)$ is equal to inductance current $i_{L2}(t)$. Due to this fact, the equivalent circuit from Fig.3 is valid, but the capacitor C is connected in a reversed position. All the equations presented till now are valid with the correction (15).

$$\begin{aligned} &u_C(t) \to -u_C(t) \\ &L_1 \to L_2 \\ &i_{L1}(t) \to i_{L2}(t) \\ &t_{0d1} \to t_{0d2} = 0.5\cdot(t_{0d1} + t_{3d1}) \\ &t_{nd1} \to t_{nd2} \quad were \quad n = 1;2;3; \end{aligned} \quad (15)$$

The currents behaviour is similar to those described in the first stage. At the point t_{1d2} the voltage across capacitor C is $-(U_i + U_X)$ (see Fig. 1 and Fig,2). The devices S_2 and S_4 naturally turn off because the current flow is transferred to device S_6 .

D.5. The Fifth stage

In this stage [$t \in (t_{1d2}$; t_{2d2})] the current through the inductance L_2 (Fig.1, 2 and 3) linearly decreases to zero. The equations (12), (13), (14) and the equivalent circuit plotted in Fig. 4 are also valid. The turn off command for the devices S_2 and S_4 (Fig.1) may be performed in this stage too.

D.6. The Sixth stage

This stage is similar to the third stage (Fig.2). The currents through the inductance L_2 and through the switch S_6 are zero, and the load is fed by the energy stored in the output capacitor C_0 and by the current $i_{L1}(t)$.

IV. ENRGETIC EVALUATION

During the first and the fourth stage, the input source U_i , delivers to the circuit a charge quantity equal to:

$$\Delta Q = \int_{t_{0d1}}^{t_{1d1}} i_{L1}(t)dt = C[u_C(t_{1d1}) - u_C(t_{0d1})] = 2C(U_i + U_X) \quad (16)$$

That means that for each turn on operation, the input source U_i , delivers to the circuit a quantity of energy ΔW, equal to:

$$\Delta W = \int_{t_{0d1}}^{t_{1d1}} U_i \cdot i_{L1}(t)dt = U_i \cdot \Delta Q = 2CU_i(U_i + U_X) \quad (17)$$

The power absorbed from the input source is:

$$P_i = \Delta W f = 2fCU_i(U_i + U_X) \quad (18)$$

where f is the frequency of 'switch on' signals, equal to the frequency of current pulses of the output current $i_T(t)$. This frequency is two times greater than devices $S_1 \div S_6$ switching frequency.

$$f = \frac{1}{T} = \frac{1}{t_{0d2} - t_{0d1}} = \frac{2}{t_{3d1} - t_{0d1}} \quad (19)$$

If we consider no loses in the circuit, the output power P_0 is equal to the input power P_i .

$$P_0 = P_i \Leftrightarrow U_0 I_0 = 2fCU_i(U_i + U_X) \quad (20)$$

If it is imposed a fix dc output voltage, the control of the average output current I_0 , may be done either through the switch frequency '*f*' (if devices S_5 and S_6 are turned on when the voltage across them riches a imposed value $U_X \geq 0$ eq.21), or through the voltage level, U_X , across devices S_5 and S_6, that performs the turn on command of these devices (considering a constant switch operation-eq.22).

$$I_0 = \frac{2CU_i(U_i + U_X)}{U_0} \cdot f \quad (21)$$

$$I_0 = \frac{2CfU_i}{U_0} \cdot U_X + \frac{2CfU_i^2}{U_0} \quad where \quad U_X \geq 0 \quad (22)$$

The conclusion which results from equations 21 and 22 is that the control of the converter presented in Fig.1 can be linearly done. Also it is possible to control the converter both through frequency and the voltage's value U_X . In this case a very good dynamical behaviour for the pulsed output current i_T , can be obtained.

V. CONTINOUS MODE OPERATION

For continuous mode operation, the switch frequency must be larger than f_{DM} , defined in the equation (23). In this case, the current through the inductances L_1 and L_2 will never have a zero value. The stages three and six from Fig.2, are not present any more.

$$f_{MD} = \frac{2}{t_{2d1} - t_{0d1}} = \frac{2}{t_{2d2} - t_{0d2}} \quad (23)$$

The behaviour of the circuit can be described in four stages, only two of them being different (Fig.5). The pulsed output current, (Fig. 1), is the sum between the currents i_{L1} and i_{L2}.

The first stage [$t \in (t_{0c1}$; t_{1c1})] may be defined almost identically like in the discontinuous mode operation. The equivalent circuit is also the same (Fig. 3) and the

equations which described the circuit behaviour are similar to equations (1), (2) and (3).
The initial conditions are different. These are:

$$i_{L1}(t_{0c1}) = I_{L0} \quad \text{and} \quad u_C(t_{0c1}) = -(U_i + U_X) \qquad (24)$$

According to these initial values, the relations of the main circuit's electric parameters may be found out:

$$\begin{aligned} i_{L1}(t) &= C\omega_0(2U_i + U_X - U_0)\sin\omega_0 t + I_{L0}\cos\omega_0 t \\ u_{L1}(t) &= (2U_i - U_0)\cos\omega_0 t - \omega_0 L I_{L0}\sin\omega_0 t \\ u_C(t) &= U_i - U_0 - u_{L1}(t) \end{aligned} \qquad (25)$$

where I_{L0} represents the initial (or minimal) value of the current through the inductance L_1 or L_2 (equation 24).

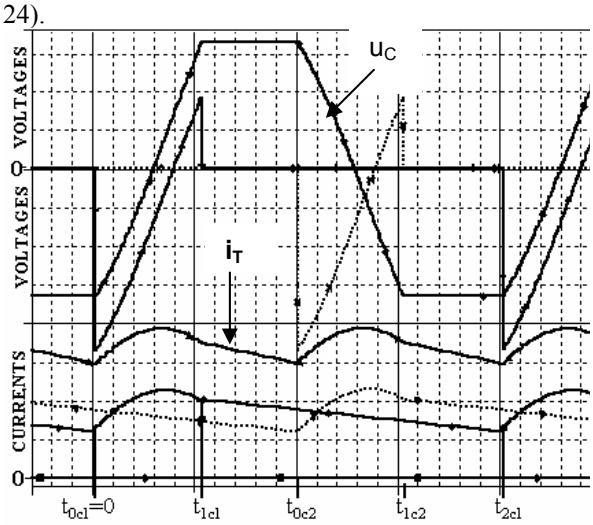

Fig. 5. Continuous mode circuit operation

At the point t_{1c1} the voltage across S_5 and the voltage across the capacitor C becomes equal to U_X and $+(U_i + U_X)$, respectively. According to equations (25), the equation (26) might be written:

$$\omega_0 L I_{L0}\sin\omega_0 t_{1c} - (2U_i + U_X - U_0)\cos\omega_0 t_{1c} = U_0 + U_X \qquad (26)$$

Also, at the point t_{1c1} , the current through the inductance L_1, will be :

$$I_{1c} = C\omega_0(2U_i + U_X - U_0)\sin\omega_0 t_{1c} + I_{L0}\cos\omega_0 t_{1c} \qquad (27)$$

The second stage [$t \in (t_{1c1} ; t_{2c1})$] starts at the point t_{1c1} , when the current through the devices S_1 and S_3 is transferred through the switch S_5. At the point t_{2c1} a new turn on commutation of the devices S_1 and S_3 is performed. The point t_{2c1} is given by the equation:

$$t_{2c1} = t_{0c1} + 2T = 0 + 2T = 2T \qquad (28)$$

where $(T)^{-1}$ is the circuit output current (i_T) pulses frequency. The current through the inductance L, has a similar equation as in the discontinuous mode operation:

$$i_{L1}(t) = -\frac{U_0}{L_1}(t - t_{1c}) + I_{1c1} \qquad t \in [t_{1c1}, t_{2c1}] \qquad (29)$$

At the point t_{2c1} the current through inductance L_1 will have again the value I_{L0} . Combining (28) with (29), results:

$$I_{L0} = I_{1c} - \frac{U_0}{L_1}(2T - t_{1c}) \qquad (30)$$

From equations (26), (27) and (30), the values of t_{1c1} and I_{L0} may be found out.

The stages tree and four are similar to the stages one and two. In this case the current flows through S_2 , S_4 , L_2 and S_6 . The position of the point t_{0c2} is:

$$t_{0c2} = 0.5 \cdot (t_{0c1} + t_{2c1}) \qquad (31)$$

In the continuous operation mode, the relations (20÷22) are preserved, so both control methodologies methodology may be used to assure the needed average output current I_0.
Continuous mode of operation is recommendable due to the less output current pulse ripple.

VI. CONCLUSIONS

The circuit presented in this paper has the following advantages comparing to the conventional buck circuit:

- The output current depends on the circuit switch frequency, on the value of capacitor C and on a dc control voltage (which control in fact the voltage variation across the capacitor C). Because the dc output voltage is controlled only by the converter's output current, a very small ratio between output voltage U_0 and input voltage U_i may be achieved. These small rates are difficult to be assured by the standard Buck converter at a high frequency.
- Using both control modes (frequency and voltage) a very good dynamic of the output current may be obtained.
- The circuit assures turn off soft commutations for all the devices, and the output current frequency is two times greater than the switching frequency for each device. The devices involved in the circuit may be selected only according to their turn on capabilities. For high power operation, fast thyristors may be used.
- The possibility to design and select the inductances L_1 and L_2 in relation to capacitor C, gives the designer the opportunity to select a lesser value for the inductances than in the case of standard Buck converter for the same performances.

The circuit can be used for both high power and small power as well.

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Direct Field-Oriented Control Based on Backstepping Strategy with Fuzzy Rotor Resistance Estimator for Induction Motor Speed Control

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Abstract – In this paper, the speed control of an induction motor using backstepping design with fuzzy rotor resistance estimation is proposed. First, the direct field oriented control IM is derived. Then, a backstepping for direct field oriented control is proposed to compensate the uncertainties which occur in the control. The effectiveness of the proposed control scheme is verified by numerical simulation. The numerical validation results of the proposed scheme have presented good performances compared to the conventional direct-field oriented control.

I. INTRODUCTION

Nowadays, like a consequence of the important progress in the power electronics and of micro-computing, the control of the AC electric machines known a considerable development and a possibility of the real time implantation applications. The Induction machine (IM) known by its robustness, cost, reliability and effectiveness is the subject of several researches [1]. However, it is traditionally for a long time, used in industrial applications that do not require high performances, this because of its high non-linearity and its high coupled structure. On the other hand, the direct current (D.C) machine was largely used in the field of the variable speed applications, where torque and flux are naturally decoupled and can be controlled independently by the torque producing current and the flux producing current. Since Blashke and Hasse have developed the new technique known as vector control [1, 2, 3], the use of the induction machine becomes more and more frequent. This control strategy can provide the same performance as achieved from a separately excited DC machine, and is proven to be well adapted to all type of electrical drives associated with induction machines[4]. The vector control technique combines the slip calculation with a rotor-position or speed measurement [5]. The calculation of the slip speed in the direct vector control involves the rotor time constant, which may vary considerably over the operational range of the motor mainly due to changes in rotor resistance with temperature. An error in the slip speed calculation gives an error in the rotor flux position, resulting in coupling between the flux and torque-producing currents due to axis misalignment. This results in a torque response with possible overshoot or undershoot and a steady-state error. Therefore variations in motor parameters, particularly rotor resistance, should be tracked as they occur. For this reasons, many research have been done on automated tuning of induction motor parameters by various authors [5, 6, 7, 8].

The most widely used controller in the industrial applications is the PID-type controllers because of their simple structures and good performances in a wide range of operating conditions [9]. The PID controller's parameters are selected in an optimal way by known methods such as the Zeigler and Nichols, poles assignment... etc. However, the PID controllers are simple but cannot always effectively control systems with changing parameters or have a strong nonlinearity; and may need frequent on-line retuning [10].

Due to new developments in nonlinear control theory, several nonlinear control techniques have been introduced in the last two decades. One of the nonlinear control methods that has been applied to induction motor control is the backstepping design [11, 12]. The backstepping is a systematic and recursive design methodology for nonlinear feedback control. This approach is based upon a systematic procedure for the design of feedback control strategies suitable for the design of a large class of feedback linearisable nonlinear systems exhibiting constant uncertainty, and guarantees global regulation and tracking for the class of nonlinear systems transformable into the parametric-strict feedback form. The backstepping design alleviates some of these limitations [11,13]. It offers a choice of design tools to accommodate uncertainties and nonlinearities and can avoid wasteful cancellations. The idea of

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backstepping design is to select recursively some appropriate functions of state variables as pseudo-control inputs for lower dimension subsystems of the overall system. Each backstepping stage results in a new pseudo-control design, expressed in terms of the pseudo-control designs from the preceding design stages. When the procedure terminates, a feedback design for the true control input results which achieves the original design objective by virtue of a final Lyapunov function, which is formed by summing up the Lyapunov functions associated with each individual design stage [14].

In this paper we apply the backstepping technique to design a speed controller for the induction motor with fuzzy rotor resistance adaptation. The output of the backstepping controller is the current (i_{qs}) required to maintain the motor speed close to the reference speed. The current (i_{qs}) is forced to follow the control current by using current regulators. The direct field-oriented of induction machine is presented in section 2, the backstepping technique for IM control is summarized in section 3. The proposed fuzzy estimation of the rotor resistance is derived in section 4. Section 5 concludes the paper.

II. DIRECT FIELD-ORIENTED CONTROL OF THE IM

The dynamic model of three-phase, Y-connected induction motor can be expressed in the *d-q* synchronously rotating frame as [1, 2, 3]:

$$\begin{cases} \dfrac{di_{ds}}{dt} = \dfrac{1}{\sigma . L_s}\left(-\left(R_s + \left(\dfrac{L_m}{L_r}\right)^2 . R_r\right) i_{ds} + \sigma . L_s . \omega_e . i_{qs} + \dfrac{L_m . R_r}{L_r^2} . \phi_{dr} + \dfrac{L_m}{L_r} . \phi_{qr} . \omega_r + V_{ds}\right) \\ \dfrac{di_{qs}}{dt} = \dfrac{1}{\sigma . L_s}\left(-\sigma . L_s . \omega_e . i_{ds} - \left(R_s + \left(\dfrac{L_m}{L_r}\right)^2 . R_r\right) i_{qs} - \dfrac{L_m}{L_r} . \phi_{dr} . \omega_r + \dfrac{L_m . R_r}{L_r^2} . \phi_{qr} + V_{qs}\right) \\ \dfrac{d\phi_{dr}}{dt} = \dfrac{L_m . R_r}{L_r} i_{ds} - \dfrac{R_r}{L_r} . \phi_{dr} + \left(\omega_e - \omega_r\right)\phi_{dr} \\ \dfrac{d\phi_{qr}}{dt} = \dfrac{L_m . R_r}{L_r} i_{qs} - \left(\omega_e - \omega_r\right)\phi_{dr} - \dfrac{R_r}{L_r} . \phi_{qr} \\ \dfrac{d\omega_r}{dt} = \dfrac{3}{2}\dfrac{P^2 . L_m}{L_r . J}\left(i_{qs} . \phi_{dr} - i_{ds} . \phi_{qr}\right) - \dfrac{f_c}{J} . \omega_r - \dfrac{P}{J} . T_l \end{cases} \quad (1)$$

Where σ is the coefficient of dispersion and is given by (2):

$$\sigma = 1 - \frac{L_m^2}{L_s L_r} \quad (2)$$

L_s, L_r, L_m stator, rotor and mutual inductances;

R_s, R_r stator and rotor resistances;

ω_e, ω_r electrical and rotor angular frequency;

ω_{sl} slip frequency $(\omega_e - \omega_r)$;

τ_r rotor time constant (L_r / R_r);

P pole pairs

The main objective of the vector control of induction motors is, as in DC machines, to independently control the torque and the flux; this is done by using a *d-q* rotating reference frame synchronously with the rotor flux space vector [2, 3]. In ideally field-oriented control, the rotor flux linkage axis is forced to align with the *d*-axes, and it follows that [3, 4, 12]:

$$\phi_{rq} = \frac{d\phi_{rq}}{dt} = 0 \quad (3)$$

$$\phi_{rd} = \phi_r = cons\tan t \quad (4)$$

Applying the result of (3) and (4), namely field-oriented control, the torque equation become analogous to the DC machine and can be described as follows:

$$T_e = \frac{3}{2}\frac{p \cdot L_m}{L_r} \cdot \phi_r \cdot i_{qs} \quad (5)$$

And the slip frequency can be given as follow:

$$\omega_{sl} = \frac{1}{\tau_r}\frac{i_{qs}^*}{i_{ds}^*} \quad (6)$$

Consequently, the dynamic equations (1) yield:

$$\frac{di_{ds}}{dt} = -\left(\frac{R_s}{\sigma L_s} + \frac{1-\sigma}{\sigma \tau_r}\right) i_{ds} + \omega_e i_{qs} + \frac{L_m}{\sigma L_s L_r \tau_r}\phi_{rd} + \frac{1}{\sigma L_s} V_{ds} \quad (7)$$

$$\frac{di_{qs}}{dt} = -\left(\frac{R_s}{\sigma L_s} + \frac{1-\sigma}{\sigma \tau_r}\right) i_{qs} - \omega_e i_{ds} + \frac{L_m}{\sigma L_s L_r \tau_r}\phi_{rd} + \frac{1}{\sigma L_s} V_{ds} \quad (8)$$

$$\frac{d\phi_r}{dt} = \frac{L_m}{\tau_r} i_{ds} - \frac{1}{\tau_r}\phi_{rd} \quad (9)$$

$$\frac{d\omega_r}{dt} = \frac{3}{2}\frac{P^2 L_m}{J L_r} i_{qs}\phi_{rd} - \frac{f_c}{J}\omega_r - \frac{P}{J} T_l \quad (10)$$

Using (3) and (4) the desired flux in terms of i_{ds} can be found from:

$$\phi_{dr} = \frac{L_m / T_r}{s + 1/T_r} \quad (11)$$

The decoupling control method with compensation is to choose inverter output voltages such that [10]:

$$V_{ds}^* = \left(K_p + K_i \frac{1}{s}\right)\left(i_{ds}^* - i_{ds}\right) - \omega_e \sigma L_s i_{qs}^* \quad (12)$$

$$V_{qs}^* = \left(K_p + K_i \frac{1}{s}\right)\left(i_{qs}^* - i_{qs}\right) + \omega_e \sigma L_s i_{ds}^* + \omega_r \frac{L_m}{L_r}\phi_{rd} \quad (13)$$

According to the above analysis, the indirect field-oriented control (IFOC) [1, 4, 10] of induction motor with current-regulated PWM drive system can reasonably presented by the block diagram shown in the Fig. 1.

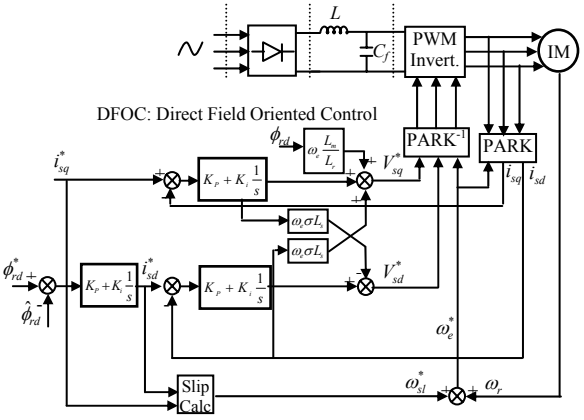


Fig. 1: Block diagram of DFOC for an induction motor.

III. THE SPEED CONTROL OF THE IM USING BACKSTEPPING TECHNIQUE

A. *Backstepping technique*

Consider the system:

$$\dot{x} = f(x) + g(x)u\ ,\ f(0) = 0 \tag{14}$$

Where $x \in R^n$ is the state and $u \in R$ is the control input. Let $u_{des} = \alpha(x),\ a(0) = 0$ be a desired feedback control law, which, if applied to the system in (14), guarantees global boundedness and regulation of $x(t)$ to the equilibrium point $x = 0$ as $t \to \infty$, for all $x(0)$ and $V(x)$ is a control Lyapunov function, where :

$$\frac{\partial V(x)}{\partial x}[f(x) + g(x)\alpha(x)] < 0\ ,\ V(x) > 0 \tag{15}$$

Consider the following cascade system:

$$\dot{x} = f(x) + g(x)y\ ,\ f(0) = 0 \tag{16}$$

$$\dot{\zeta} = m(x,\zeta) + \beta(x,\zeta)u\ ,\ h(0) = 0 \tag{17}$$

$$y = h(x) \tag{18}$$

Where for the system in (16), a desired feedback $a(x)$ and a control Lyapunov function *V(x)* are known. Then, using the nonlinear block backstepping theory in [17], the error between the actual and the desired input for the system in (16) can be defined as $z = y - \alpha$, and an overall control Lyapunov function $V(x,\zeta)$ for the systems in (16) and (17) can be defined by augmenting a quadratic term in the error variable z with $V(x)$:

$$V(x,\zeta) = V(x) + \frac{1}{2}z^2 \tag{19}$$

Taking the derivative of both sides gives:

$$\dot{V}(x,\zeta) = \dot{V}(x) + \frac{1}{2}z\dot{z} \tag{20}$$

From which solving for $u(x,\zeta)$, which renders $\dot{V}(x,\zeta)$ negative definite, yields a feedback control law for the full system in (16-18). One particular choice is [17]:

$$u = \left(\frac{\partial h(\zeta)}{\partial \zeta}\beta(x,\zeta)\right)^{-1}\left\{-c(y-\alpha) - \frac{\partial h(\zeta)}{\partial \zeta}m(x,\zeta) + \frac{\partial \alpha(x)}{\partial x}\dot{x} - \frac{\partial V(x)}{\partial x}g(x)\right\},\qquad c > 0 \tag{21}$$

B. *Application to induction motor*

In this section we use the backstepping algorithm to develop a control law to regulate the speed of the induction motor. The speed will converge to its desired value from a wide set of initial conditions.

Step 1:

We first consider the tracking objective of the direct current (ϕ_{dr}). A tracking error $z_1 = \phi_{dr}^* - \phi_{dr}$ is defined and the derivative becomes:

$$\dot{z}_1 = \frac{d\phi_{dr}^*}{dt} - \frac{R_r}{L_r}\cdot(L_m \cdot i_{ds} - \phi_{dr}) \tag{22}$$

To initiate backstepping, we choose i_{ds} as our first virtual control. If the stabilising function is chosen as:

$$i_{ds}^* = \frac{\phi_{dr}}{L_m} + c_1 \cdot \frac{\tau_r}{L_m}\cdot z_1 + \tau_r \cdot \frac{d\phi_{dr}}{dt} \tag{23}$$

We obtain:

$$\dot{z}_1 = c_1 \cdot z_1 + \frac{1}{\tau_r}\cdot(i_{ds} - i_{ds}^*) \tag{24}$$

Due to the fact that i_{ds} is not a control input an error variable $z_2 = i_{ds} - i_{ds}^*$ is defined and we have the derivative as follows:

$$\dot{z}_2 = c_1 \cdot z_1 + \frac{1}{\tau_r}\cdot z_2 \tag{25}$$

Step 2:

The derivative of the error variable $z_2 = i_{ds} - i_{ds}^*$ is:

$$\begin{aligned}\dot{z}_2 = &-\frac{L_m}{\tau_r}\cdot(L_m \cdot i_{ds} - \phi_{dr}) + c_1 \cdot \left(i_{ds} - \frac{\phi_{dr}}{L_m} - \tau_r \cdot \frac{d\phi_{dr}^*}{dt}\right) - \frac{\tau_r}{L_m}\cdot\frac{d^2\phi_{dr}}{dt^2} \\ &+ \frac{1}{\sigma \cdot L_s}\cdot V_{ds} - \frac{1}{\sigma \cdot L_s}\left(R_r \cdot i_{ds} - w_e \cdot \sigma \cdot L_s \cdot i_{qs} + \left(\frac{L_m}{L_r}\right)^2 \cdot R_r \cdot \left(i_{ds} - \frac{\hat{\phi}_{dr}}{L_m}\right)\right) \\ &+ \frac{\left(\frac{L_m}{L_r}\right)^2 \cdot R_r}{\sigma \cdot L_s}\cdot\frac{\phi_{dr}}{L_m} + w_r \cdot \frac{L_m}{\sigma \cdot L_s \cdot L_r}\cdot\phi_{qr}\end{aligned} \tag{26}$$

Viewing ϕ_{dr} and ϕ_{qr} as unknown disturbances we apply nonlinear damping [13, 17] to design the control function:

$$\begin{aligned}\frac{1}{\sigma \cdot L_s}\cdot V_{sd} = &\frac{1}{\sigma \cdot L_s}\left(R_s \cdot i_{ds} - w_e \cdot \sigma \cdot L_s \cdot i_{qs} + \left(\frac{L_m}{L_r}\right)^2 \cdot R_r \cdot \left(i_{ds} - \frac{\hat{\phi}_{dr}}{L_m}\right)\right) \\ &\cdot\left(\frac{1}{\tau_r} - c_1\right)\cdot\left(i_{ds} - \frac{\hat{\phi}_{dr}}{L_m}\right) + c_1\frac{\tau_r}{L_m}\cdot\frac{d\phi_{dr}^*}{dt} + \frac{\tau_r}{L_m}\cdot\frac{d^2\phi_{dr}^*}{dt^2} \\ &- c_2 \cdot z_2 - \frac{1}{\tau_r}\cdot z_1 - d_2 \cdot \left\{\left(\frac{(L_m/L_e)^2 R_r}{\sigma L_s}\right)^2 + \left(w_r \cdot \frac{(1-\sigma)}{\sigma}\right)^2\right\}\cdot z_2\end{aligned} \tag{27}$$

We define:

$$\phi_1 = \frac{\left(\frac{L_m}{L_r}\right)^2 \cdot R_r}{\sigma \cdot L_s}\ ,\ \phi_2 = w_r \cdot \frac{\frac{L_m^2}{L_r}}{\sigma \cdot L_s} \text{ and } \phi^2 = \phi_1^2 + \phi_2^2\ .$$

The insertion of the control function in the dynamics for the error variable z_2 gives :

$$\dot{z}_2 = -c_2 \cdot z_2 - \frac{1}{\tau_r}z_1 - d_2 \cdot \phi^2 \cdot z_2 + \phi_1 \cdot \frac{\phi_{dr}}{L_m} + \phi_2 \cdot \frac{\phi_{qr}}{L_m} \tag{28}$$

Step 3:

We now search to find the error torque tracking. A tracking error is for $\phi_{dr} \neq 0$ defined as:

$$z_3 = i_{qs} - \frac{T_e^*}{\left(P \cdot \frac{L_m}{L_r}\cdot\phi_{dr}\right)} \tag{29}$$

Then, its derivative is:

$$\dot{z}_3 = \frac{1}{\sigma \cdot L_s} \cdot V_{qs} - \frac{1}{\sigma \cdot L_s} \cdot \left(R_s \cdot i_{sq} + w_e \cdot \sigma \cdot L_s \cdot i_{ds} + \left(\frac{L_m}{L_r}\right)^2 \cdot R_r \cdot i_{qs} + w_r \cdot (1-\sigma) \cdot L_s \cdot \frac{\hat{\phi}_{dr}}{L_m} \right) - \frac{\left(\frac{L_m}{L_r}\right)^2 \cdot R_r}{\sigma \cdot L_s} \cdot \frac{\phi_{qr}}{L_m} + w_r \cdot \frac{\frac{L_m^2}{L_r}}{\sigma \cdot L_s} \cdot \frac{\phi_{dr}}{L_m} + \frac{L_r \cdot T_e^*}{P \cdot \phi_{dr}^2} \cdot \frac{1}{\tau_r} \cdot \left(i_{ds} - \frac{\hat{\phi}_{dr}}{L_m} \right) - \frac{L_r}{P \cdot L_m \cdot \hat{\phi}_{dr}} \cdot \frac{dT_e^*}{dt} \tag{30}$$

Viewing ϕ_{dr} and ϕ_{qr} as unknown disturbances we apply nonlinear damping [13, 17] to design the control function:

$$\frac{1}{\sigma \cdot L_s} \cdot V_{qs} = \frac{1}{\sigma \cdot L_s} \cdot \left(R_s \cdot i_{qs} - w_e \cdot \sigma \cdot L_s \cdot i_{qs} + \left(\frac{L_m}{L_r}\right)^2 \cdot R_r \cdot i_{qs} + w_r \cdot (1-\sigma) \cdot L_s \cdot \frac{\hat{\phi}_{dr}}{L_m} \right) - \frac{2 \cdot L_r \cdot T_e^*}{3 \cdot P \cdot \phi_{dr}} \cdot \frac{1}{T_r} \cdot \left(i_{ds} - \frac{\hat{\phi}_{dr}}{L_m} \right) + \frac{2 \cdot L_r}{3 \cdot P \cdot L_m \cdot \hat{\phi}_{dr}} \cdot \frac{dT_e^*}{dt} - c_3 \cdot z_3 - d_3 \cdot \left\{ \left(\frac{\left(\frac{L_m}{L_r}\right)^2 \cdot R_r}{\sigma \cdot L_s} \right)^2 + \left(w_r \cdot \frac{(1-\sigma)}{\sigma} \right)^2 \right\} \cdot z_3 \tag{31}$$

The insertion of the control function in the dynamics for the error variable z_3 then gives:

$$\dot{z}_3 = -c_3 \cdot z_3 - d_3 \cdot \phi^2 \cdot z_3 + \phi_1 \cdot \frac{\phi_{qr}}{L_m} + \phi_2 \cdot \frac{\phi_{dr}}{L_m} \tag{32}$$

The combined controller is shown in figure 2 where we have:

$$\begin{cases} V_{ds,ff} = R_s \cdot i_{ds} - \omega_s \cdot \sigma \cdot L_s \cdot i_{qs} + \left(\frac{L_m}{L_r}\right)^2 \cdot R_r \cdot \left(i_{ds} - \frac{\hat{\phi}_{dr}}{L_m} \right) \\ V_{qs,ff} = R_s \cdot i_{sq} - \omega_s \cdot \sigma \cdot L_s \cdot i_{qs} + \left(\frac{L_m}{L_r}\right)^2 \cdot R_r \cdot i_{sq} + \omega_r \cdot (1-\sigma) \cdot L_s \cdot \frac{\hat{\phi}_{dr}}{L_m} \\ V_{ds,nl} = \sigma \cdot L_s \cdot \left\{ \left(\frac{1}{\tau_r} - c_1 \right) \cdot \left(i_{ds} - \frac{\hat{\phi}_{dr}}{L_m} \right) - \frac{1}{L_m \cdot \tau_r} \left(\hat{\phi}_{dr} - \phi_{dr}^* \right) \right\} \\ V_{qs,nl} = -\frac{2 \cdot L_m^2 \cdot T_{em}^*}{3 \cdot P \cdot (1-\sigma) \cdot L_s \cdot \phi_{dr}^2} \cdot \frac{\sigma \cdot L_s}{\tau_r} \cdot \left(i_{ds} - \frac{\hat{\phi}_{dr}}{L_m} \right) \end{cases} \tag{33}$$

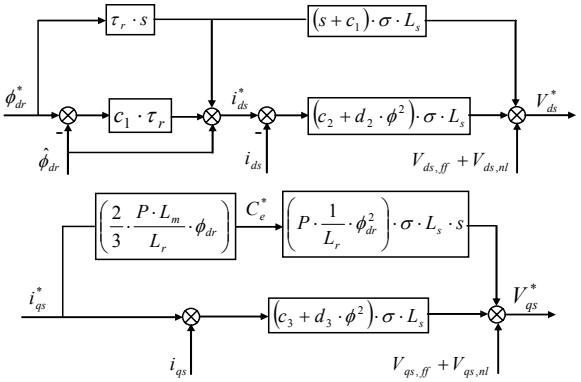


Fig. 2: Nonlinear field-oriented control of IM using Backstepping technique

C. *Speed control of IM using backsteping*

To control the speed of the induction motor, we look to search the error speed tracking. We consider that i_{qs}^* is the control law, so tracking error is defined as:

$$z_0 = \omega_r^* - \omega_r \tag{34}$$

So, its derivate is given as :

$$\dot{z}_0 = \dot{\omega}_r^* - \dot{\omega}_r \tag{35}$$

$$\dot{z}_0 = \dot{\omega}_r^* - \left[\frac{3}{2} \frac{P^2 \cdot L_m}{L_r \cdot J} \cdot i_{qs} \cdot \phi_{dr} - \frac{f_c}{J} \cdot \omega_r - \frac{P}{J} \cdot T_l \right] \tag{36}$$

The control law obtained is :

$$i_{qs}^* = \frac{2}{3} \frac{L_r \cdot f_c}{P^2 \cdot L_m \cdot \phi_{dr}} \cdot \omega_r + c_0 \frac{2 \cdot L_r \cdot J}{3 \cdot P^2 \cdot L_m \cdot \phi_{dr}} z_0 + \frac{2}{3} \frac{L_r}{P \cdot L_m} \cdot T_l \tag{37}$$

IV. FUZZY ROTOR RESISTANCE ESTIMATION

In this section, the fuzzy rotor resistance estimation is proposed. The first challenge in the design of this fuzzy logic estimator is to determine its inputs variables. Since the time constant for the variation of the rotor resistance is much larger than the time constant of the IM, the rotor resistance estimation process can be running under steady-state conditions (no changes of load torque and reference speed command).

In order to study the influence of the rotor resistance, a characteristic function F is utilized [5, 6]:

$$F = \frac{1}{\omega_r \omega_e} \left[\left(V_{ds} - \sigma L_s \frac{di_{sd}}{dt} \right) i_{sq} - \left(V_{qs} - \sigma L_s \frac{di_{sq}}{dt} \right) i_{sd} \right] + \sigma L_s \left(i_{sd}^2 + i_{sq}^2 \right) \tag{38}$$

This function can also be defined from a modified expression of field orientation conditions as follows:

$$F = \frac{L_m}{L_r} \left(\frac{d\phi_{rd}}{dt} i_{sq} - i_{sd} \cdot \phi_{rd} \right) \tag{39}$$

In steady state $\left(\frac{d\phi_{rd}}{dt} = 0 \right)$, this equation becomes:

$$F_0 = -\frac{L_m}{L_r} i_{sd} \cdot \phi_{rd} \tag{40}$$

Note that the function given in Equ. (40) differs from F by the effect of change of R_r [7]. In fact, the rotor resistance used in flux estimator is not actual value of R_r unless a rotor resistance adaptation is present. The error (F-F_0) reflects the rotor resistance variation, and can be used as a correction function for the adaptation of the rotor resistance in the fuzzy logic estimator.

The proposed estimator based on fuzzy logic principle is shown in Fig. 7. Functions F_0 and F are first calculated. The error between F and F_0 (ΔF) and its first time derivative are employed as inputs of FLE. The operation principle of FLE is similar as of a fuzzy logic controller (FLC). The membership functions for the fuzzy sets corresponding to the error ΔF , its time variation and incremental rotor resistance ΔR_r are defined in fig. 3 and fig. 4.

Because the data manipulated in the fuzzy inference mechanism is based on the fuzzy set theory, the associated fuzzy sets involved in the fuzzy control rules are defined as follows:

NB : Negative big
NM : Negative medium
NS : Negative small
ZE : Zero
PS : Positive small
PM : Positive medium
PB : Positive big

And their universe of discourses are assigned to be between [-1, 1] for the inputs (ΔF and its time variation), and [-1,1] for the outputs variable (ΔR_r). The incremental rotor resistance ΔR_r is continuously added to the previously estimated rotor resistance R_{r0} .

Since only seven fuzzy subsets, NB, NM, NS, ZE, PS, PM and PB, are defined for ΔF , its time variation and ΔR_r , the fuzzy inference mechanism contains 49 rules. The resulting fuzzy inference rules for the incremental rotor resistance are as follows:

Table 1: Rule bases of the fuzzy estimator

	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NB	NM	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PS	PB	PB	PB	PB

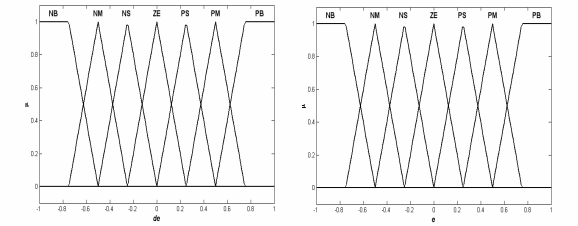


Fig. 3: Membership functions for antecedent part

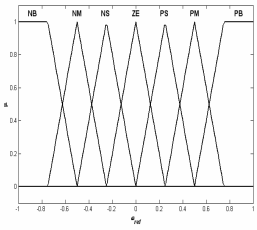


Fig. 4: Membership functions consequent part

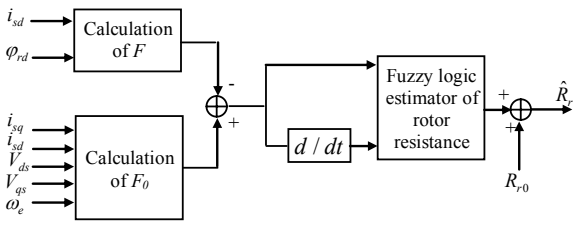


Fig. 5: Block diagram of rotor resistance estimation using fuzzy logic

V. RESULTS OF SIMULATION

To prove the rightness and effectiveness of proposed control scheme, we apply the designed controller to the control of the induction motor. The induction motor is a wound three phase, *Y* connected, four pole, 1.5 kW, 1420min^{-1} 220/380V, 50Hz. The machine parameters are given in appendix. The configuration of the overall control system is shown in Fig. 6. It mainly consists of an induction motor, a ramp comparison current-controlled pulse width modulated (PWM) inverter, a slip angular speed estimator, an inverse park, nonlinear filed oriented control based on backstepping technique, and an outer speed feedback control loop contains on a backstepping controller.

Fig. 7 shows the disturbance rejection of backstepping controller when the machine is operated at 200 [rad/sec] under no load and a nominal load disturbance torque (10 N.m) is suddenly applied and eliminated at 1.5sec, 2.5ec respectively, followed by a reversed reference (-200rad/sec) at 4sec. The backstepping controller rejects the load disturbance rapidly with a negligible steady state error.

This controller rejects the load disturbance very rapidly with no overshoot and with a negligible steady state error more than the PI controller which is shown clearly in figs. 11-12.

Fig. 8 and 9 show a comparison between the classical field oriented control using PI controller and which based on backstepping design technique. It shows clearly that the decoupling control is more maintained for the backstepping design than which obtained by a classical PI controllers (current and flux regulators).

In the next simulation, the rotor resistance is supposed to be changed from 100% of its rated value to 200% linearly (step or ramp change). The responses of direct and quadratic rotor flux for the two cases (without and with rotor resistance adapting) and for step change are shown in Fig. 13. It's observed in these figures that when the estimated rotor resistance deviates from its real value, the field orientation scheme is detuned. Fig. 13 shows also the maintained performance of the IM drive using the rotor resistance adaptation to track its real value. In this case, the field orientation condition can be maintained by applying a step change of rotor resistance. It's observed that the detuned problem is removed completely ($\phi_{rd} = \phi_r$ and $\phi_{rq} = 0$).

Fig. 15 shows the responses of the direct and quadratic rotor flux with and without adaptation, for ramp change of rotor resistance. The same remarks can be observed for the responses shown in fig. 13. Finally, Fig. 14 and 16 show the rotor resistance tracking for step and ramp change. In both cases, the rotor resistance tracking is excellent and the field orientation condition is still maintained. We can analyze finally the principle of the obtained results for rotor resistance adaptation. If the system is under no-load condition, the torque current becomes zero. The calculated function F and F_0 are not affected by the rotor resistance change. This is shown in Fig.13 and Fig.15 from 0sec until 1.5sec. However, if the load is added to the motor, the rotor resistance errors will affect the calculated functions.

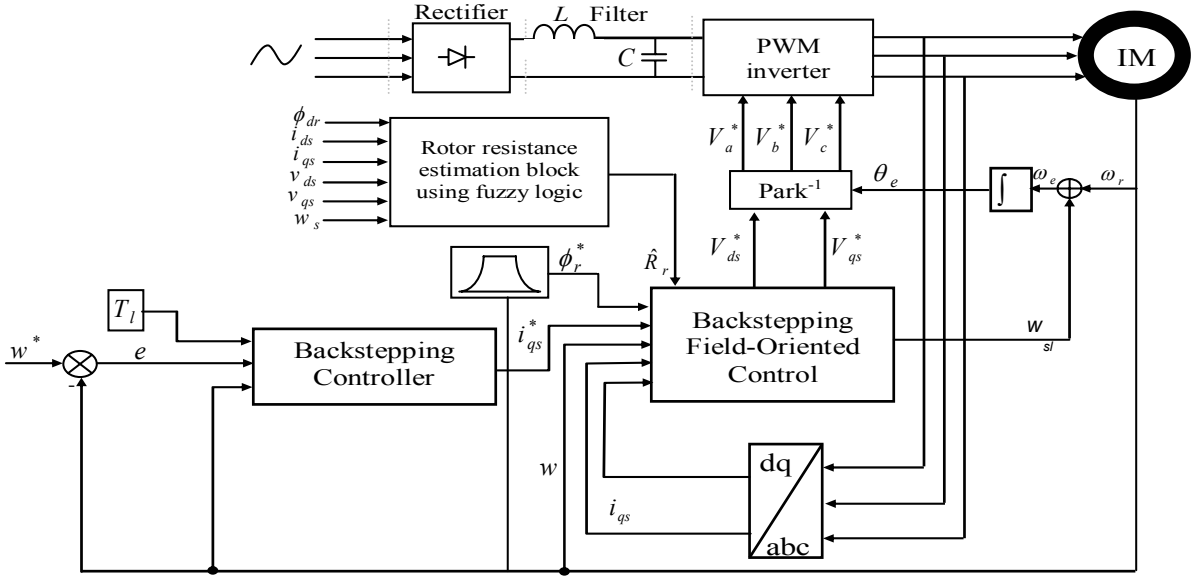
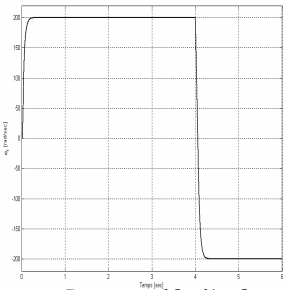
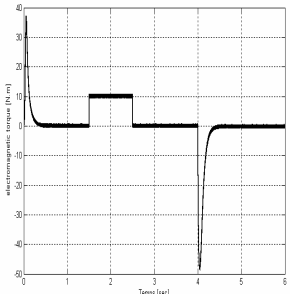


Fig. 6: Block of the speed control and field oriented control of IM using backstepping technique with fuzzy rotor resistance estimator

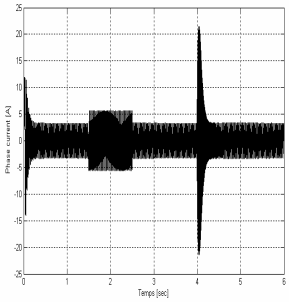
The figures show that the proposed scheme achieves good performances as it achieves compensation of the rotor resistance changes.



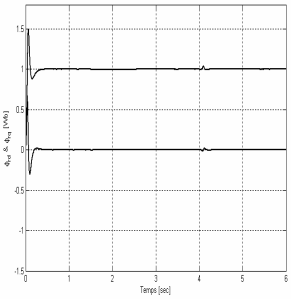
Rotor speed [rad/sec]



Torque [N.m]



Phase current Ia [A]



ϕ_{rd} and ϕ_{rq} [Wb]

Fig. 7: Simulated results of backstepping controller for IM

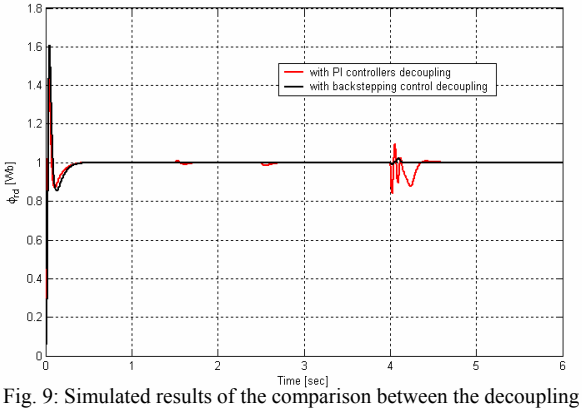


Fig. 9: Simulated results of the comparison between the decoupling obtained by PI and backstepping design for IM.

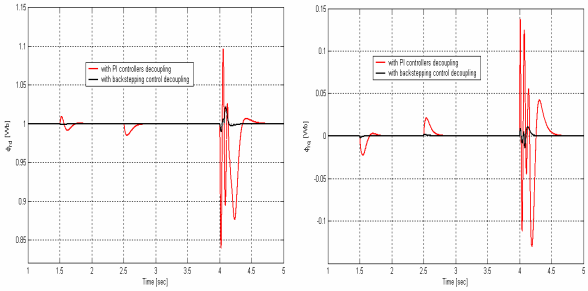


Fig. 10: Zoomed responses of decoupling obtained by PI, backstepping control for IM.

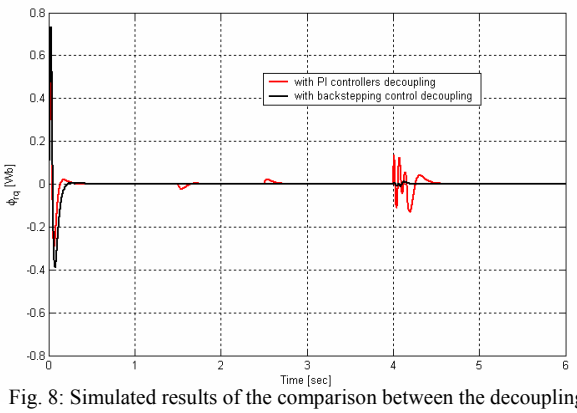


Fig. 8: Simulated results of the comparison between the decoupling obtained by PI and backstepping design for IM.

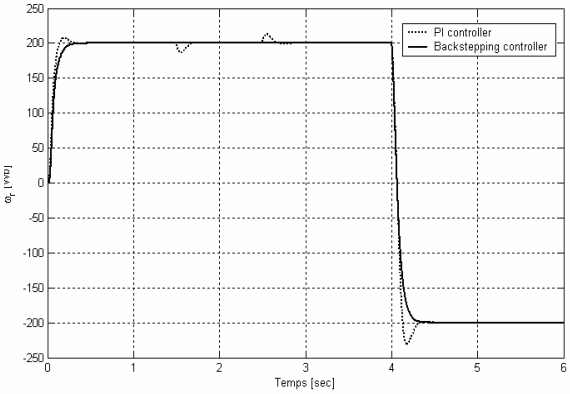


Fig. 11: Simulated results of the comparison between the PI and backstepping design for IM speed control.

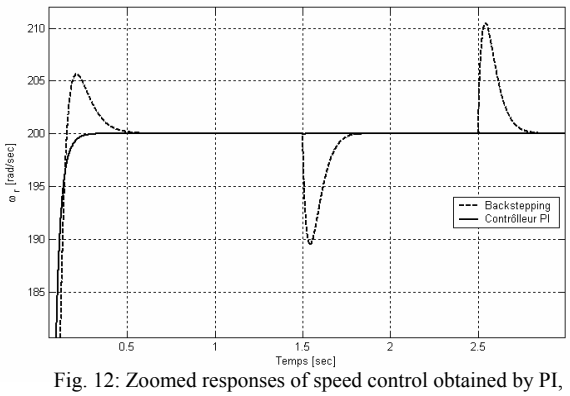


Fig. 12: Zoomed responses of speed control obtained by PI, backstepping control for IM.

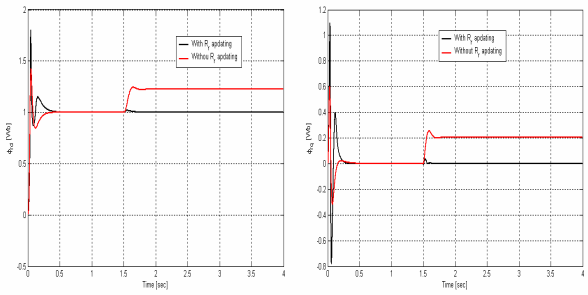


Fig. 13: Simulated results of the direct and quadratic flux without and with rotor resistance adaptation (step change).

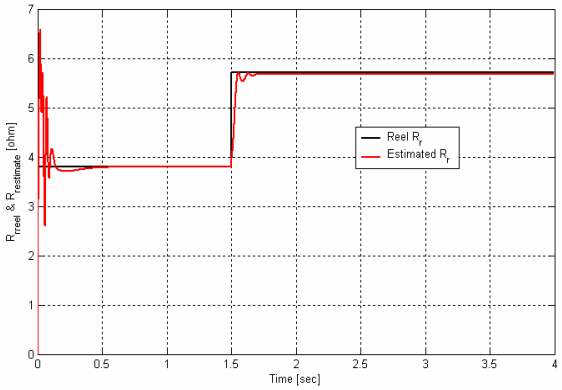


Fig. 14: Rotor resistance tracking for step change

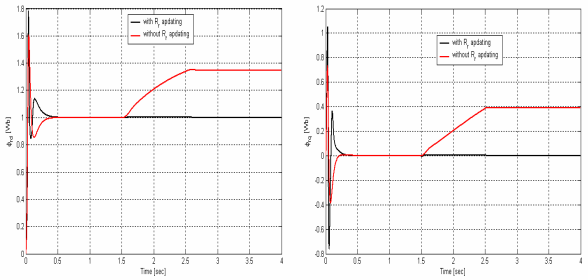


Fig. 15: Simulated results of the direct and quadratic flux without and with rotor resistance adaptation (ramp change).

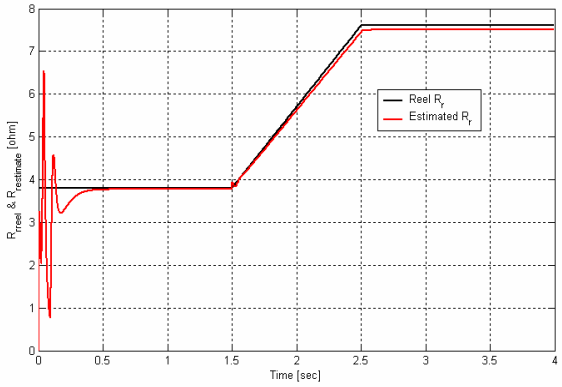


Fig. 16: Rotor resistance tracking for ramp change

VI. CONCLUSION

In this work, we have presented a backstepping technique associated with fuzzy rotor resistance estimation in order to offer a choice of design tools to accommodate uncertainties and nonlinearities. This study has successfully demonstrated the design of the backstepping technique for the speed control of an induction motor and the nonlinear field orientation control design. The Proposed scheme has presented satisfactory performances (no overshoot, minimal rise time, best disturbance rejection) for parameter variations, time-varying external force disturbances. The proposed fuzzy rotor resistance estimator produces a correction signal which is added to the rated value of the rotor resistance. The simulation results obtained have confirmed the excellent flux responses and the efficiency of the proposed scheme. Finally, the effectiveness of the PI controller and the nonlinear field orientation based on the backstepping strategy has been verified through simulation.

APPENDIX

Induction motor parameters:

P_n [kW]	1.5	R_s [Ω]	4.85	f_n [Hz]	50
V_n [V]	220	R_r [Ω]	3.805	J_n [kg/m^2]	0.031
η	0.78	L_r [H]	0.274	f_c [N.m.s/rd]	0.0014
Cosφ_n	0.8	L_s [H]	0.274	p	2
ω_n[min^{-1}]	1428	L_m [H]	0.258		

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OTA-C BIQUAD CELLS EMULATION OF LC LADDER FILTERS

Andrei Câmpeanu and János Gal [1]

Abstract – The paper presents a method to design continuos-time filter based on the node-voltage simulation of LC ladder structures. The node voltages are used as variables to generate transfer functions. The OTA-C biquad cells are realized in distributed-feedback configuration and use node current injection to permit multiple input action. Both all-pole and finite-transmission-zeros LC low-pass and high-pass filters are implemented. Applying standard low pass to bandpass frequency transformation to OTA-C circuits capacitors, bandpass and bandstop filters are easily obtained from their low-pass or high-pass active filters prototypes.
Keywords: filter synthesis, OTA-C biquads

I. INTRODUCTION

Passive double loaded ladder networks are commonly used as prototypes for active filters because their low sensitivity is preserved by active simulations. Nevertheless, the well known „leap-frog" active filter synthesis technique, based on the simulation of current-voltage relationships existing in a LC-ladder prototype [1], [2] do not solves satisfactorily the simulation of finite-zeros filters [3], the resulting circuits in these cases having usually floating capacitors which are responsible for parasitic bottom-plate capacitances and undesirable non-observable poles.

An alternative to classical simulation method proposed in [4], uses the mesh currents description of the passive circuit. This approach uses coupled-biquad filter cells to implement mesh equations of the passive network. In order to implement finite-zeros passive filters simulation by the mesh currents method in circuits consisting only from operational amplifiers with grounded inputs, capacitors and resistors, we used succesfully in [5], a universal multiple-inputs biquad cell based on the well-known Tow-Thomas structure. In this case, each biquad cell implements the currents equations that take place in one of circuit meshes.

The aim of the present paper is to extend the area of coupled-biquad method to OTA-C circuits. We investigate also the use of the node-voltage description of the passive ladder network as an equivalent alternative to the mesh current simulation method. With that end in view, an important effort was done to establish an optimal OTA-C biquad cell that suits best to coupled-biquad applications. Therefore, the OTA-C biquads must permit multiple inputs, contain only grounded capacitors and realize all types of filtering functions. These requirements can be fulfilled only by connecting three or four additional OTAs to the three OTA basic biquad circuit [3], [6]. This does not represent a major overhead, since in integrated circuits, OTAs can be fabricated very efficiently and economically.

II. SYNTHESIS PROCEDURE

Consider a general RLC ladder network with n nodes, as shown in Fig. 1. The work of the passive network can be described using the voltages in the nodes of the network: $V_1, V_2, \ldots, V_n$. The most general form of the equation that can be written for any node of the network is

$$V_k = \frac{I_k}{Y_k^n} + \frac{Y_{2k-2}}{Y_k^n} V_{k-1} + \frac{Y_{2k}}{Y_k^n} V_{k+1}, \quad k = 1, 2, \ldots, n \qquad (1)$$

where Y_k^n is the total admitance connected to node k of the network ($Y_k^n = Y_{2k-2} + Y_{2k-1} + Y_{2k}$). I_k represents the value of current sources connected to the node. Only for $k = 1$, $I_1 \neq 0$ and $V_0 = 0$. In the last node of the network: $V_{k+1} = 0, k = n$.

According to eq. (1), the ladder filter network can be implemented using RC active circuits cells with multiple inputs. Moreover, as the denominators of all the terms on the right side of (1) are identical, Y_k^n, a unique active circuit structure with multiple inputs can be used to implement the desired functions. Depending on the position of the node in the RLC

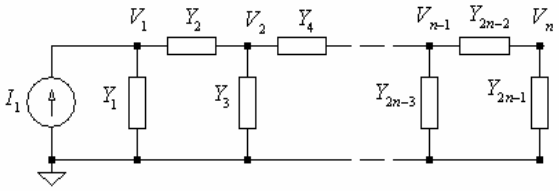

Fig. 1 Using node voltages to describe the work of a RLC ladder network

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network, these functions are first or second order RC active circuits transfer functions. Refering to node k, we will denote the corresponding transfer functions in eq. (1) as

$$T_{ik}(s)=\frac{1}{Y_k^n};\ T_{k-1,k}(s)=\frac{Y_{2k-2}}{Y_k^n};\ T_{k+1,k}(s)=\frac{Y_{2k}}{Y_k^n} \quad (2)$$

Consequently, an active filter cell will realize the equation

$$V_k=T_{ik}I_k+T_{k-1,k}(s)V_{k-1}+T_{k+1,k}V_{k+1},\quad k=1,2,\ldots,n \quad (3)$$

There are two forms of RLC ladder filter structures: T-shaped and π-shaped circuits. Both of them can be implemented by this method, but it is normal to choose for simulation the most efficient one, vewing that the emulation of first-order transfer functions uses almost the same number of OTAs as second-order function cells. From this point of view, π-shaped circuits are the choice, because, with the exception of the last node in an even-order filter, all transfer functions in (3) are second-order rational functions.

III. BIQUAD OTA-C FILTER BUILDING BLOCKS

First and second-order filter cells are needed to implement eq. (3). Since the solutions for first-order sections are obvious, we will focus on second-order solutions used in our approach. A convenient OTA-C biquad filter cell is a two-inputs device able to perform second-order functions with identical poles but different zeros regarding the inputs. Multiple inputs is obtained by the technique of node current injection [3], which apply the input voltages through extra single-ended input OTAs to some circuit nodes. The OTA-C biquad itself has not the simplest structure, viewing the necessity of an indepedent tuning of parameters ω_o and Q. We choosed a distributed-feedback (DF) two-integrator loop structure with four OTAs and two grounded capacitors [3].

A. *Finite-Q OTA-C Biquad Cell*

These cells are used to emulate network voltage equations for nodes which total admittance Y_k^n includes a real part. It's the case in a double terminated RLC ladder filter for the first and the last node of the network. The complete circuit is shown in Fig. 2. Choosing for convenience $C_1=C_2=C$ and $g_1=g_2=g$, the transfer function of the circuit is given by

$$V_o=\sum_i^2 \frac{\pm\frac{g_{ai3}C^2}{g^2g_4}s^2\pm\frac{g_{ai2}g_3C}{g^2g_4}s\pm\frac{g_{ai1}g_3}{gg_4}\pm\frac{g_{ai3}}{g_4}}{\frac{C^2}{g^2}s^2+\frac{g_3C}{g_4g}s+1}V_i \quad (4)$$

Depending on the node voltage equation that is emulated, the circuit can realize any kind of second order relationship established at the terminal nodes of a low-pass or high-pass double-terminated passive ladder filter. The sign ± simply means both non-inverting and inverting inputs of OTAs in the *Input Sections* can be used, depending on application. Not all OTAs in the *Input Sections* are used simultaneously. The shape of the numerator of the transfer function in (4) dictates which OTA remains, $g_{aij}\neq 0$, and which OTA is removed, $g_{aij}=0$. It is seen that the circuit can realize a low-pass filter if $g_{ai2}=g_{ai3}=0$ and a bandpass filter for $g_{ai1}=g_{ai3}=0$. The single shortcoming of this structure is the coefficient difference matching needed to realize a high-pass filter: $g_{ai1}=-(g_4/g_3)g_{ai3}, g_{ai2}=0$. In defiance of this, any filter characteristics can be realized, making the architecture the best suited for our application.

B. *Infinite-Q OTA-C Biquad Cell*

For network nodes to which are connected only reactances, the corresponding OTA-C biquad cells exhibit infinite-Q second order transfer functions. It is a situation met in all internal nodes of an RLC ladder filter. Though, it were possible to use the circuit in Fig. 2 by removing the feedback between g_4 and g_2, we preferred to eliminate the drawback of this structure which we talk about before, by using the circuit shown in Fig. 3.

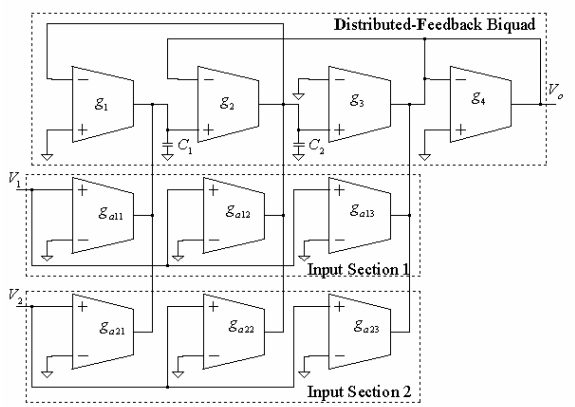

Fig. 2 Double-input finite-Q OTA-C biquad cell used in coupled-biquad filter implementation

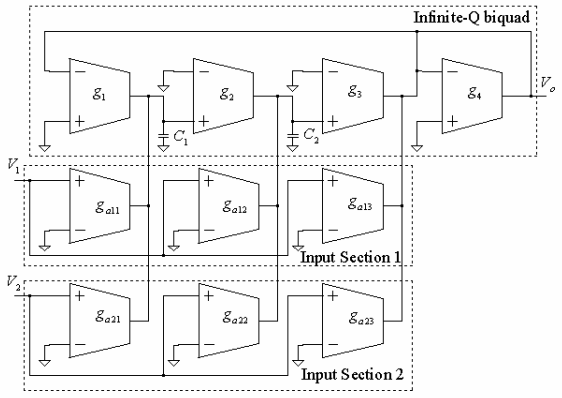

Fig. 3 Double-input infinite-Q OTA-C biquad cell used in coupled-biquad filter implementation

To write the transfer function, the same simplifications like in (4) will be made: $C_1 = C_2 = C$, $C_1 = C_2 = C$. Now, the transfer function of the infinite-Q OTA-C biquad cell is given by

$$V_o = \sum_i^2 \frac{\pm\frac{g_{ai3}C^2}{g^2 g_3}s^2 \pm \frac{g_{ai2}C}{g^2}s \pm \frac{g_{ai1}}{g}}{\frac{g_3 C^2}{g^2 g_4}s^2 + 1} V_i \qquad (5)$$

There are no more coefficient difference matching involved, thus the architecture is insensitive to variations in transconductances values. As in previous case, not all OTAs in the *Input Sections* are used simultaneously, and the change of sign in the terms from the numerator simply means to pass from a non-inverting input to an inverting input of OTAs in the *Input Sections*. More simplifications are obtained if simple low-pass and bandpass characteristics must to be implemented. It's the case of low-pass all-pole filters, where the four OTAs biquad structure, g_1, g_2, g_3, g_4 is reduced to g_1, g_2.

IV. LOW-PASS AND HIGH-PASS FILTERS DESIGN EXAMPLES

The emulation of RLC ladder filter networks by the node-voltage simulation method consists in an adequate coupling of biquad OTA-C cells introduced in the previous Section. Viewing the large number of OTAs involved by the use of cells in Fig. 2 and Fig. 3, it is obvious that OTA-C coupled-biquad implementation represents an alternative only in those areas where the „traditional" leap-frog method do not perform well: finite-zeros passive ladder filters emulation. The complexity of a filter synthesis depends on the choice of the prototype network and, as we pointed before, π-shaped filter networks are best suited to our purposes.

The design procedure of an OTA-C filter based on the node-voltage emulation method starts by the selection of an appropiate RLC ladder prototype. Next, a description of passive network work is made by its set of node-voltage equations. Then, each equation is replaced by one of OTA-C biquad cells from the previous Section, or by a first-order OTA-C filter. Drawing a parallel between the passive network equations and the transfer functions of OTA-C filter

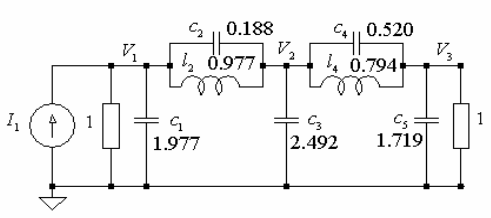

Fig. 4 Fifth-order elliptic low-pas passive ladder filter used as prototype in node-voltage emulation method.

cells, the values of OTAs transconductan-ces and capacitances are computed. Finally, the neighbouring filter cells are connected in accordance with passive filter equations.

To illustrate the node-voltage approach, a fifth-order low-pass elliptic passive filter prototype will be used to obtain equivalent OTA-C coupled-biquad filters. The LC ladder prototype shown in Fig. 4 has 1dB ripple in the passband and minimum 55db attenuation in the stopband. Node-voltage analysis leads to the following system of equations:

$$\begin{aligned}
V_1 &= T_{01}I_1 + T_{21}V_2 = \frac{sl_2 I_1 + \left(s^2 c_2 l_2 + 1\right)V_2}{s^2\left(c_1 + c_2\right)l_2 + sl_2 + 1} \\
V_2 &= T_{12}V_1 + T_{32}V_3 \\
&= \frac{\left(s^2 c_2 \frac{l_2 l_4}{l_2 + l_4} + \frac{l_4}{l_2 + l_4}\right)V_1 + \left(s^2 c_2 \frac{l_2 l_4}{l_2 + l_4} + \frac{l_2}{l_2 + l_4}\right)V_3}{s^2\left(c_2 + c_3 + c_4\right)\frac{l_2 l_4}{l_2 + l_4} + 1} \qquad (6) \\
V_3 &= T_{23}V_2 = \frac{\left(s^2 c_4 l_4 + 1\right)V_2}{s^2\left(c_4 + c_5\right)l_4 + sl_4 + 1}
\end{aligned}$$

Each pair of these transfer functions (f.i. T_{01} and T_{21}) have the same poles but different zeros. This enables the realization of each equation in (6) by one OTA-C

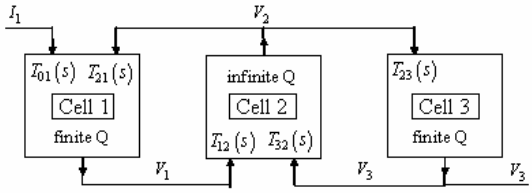

Fig. 5 Block diagram of the node-voltage coupled-biquad active filter emulation of ladder filter in Fig. 4. The various transfer functions are given in the text.

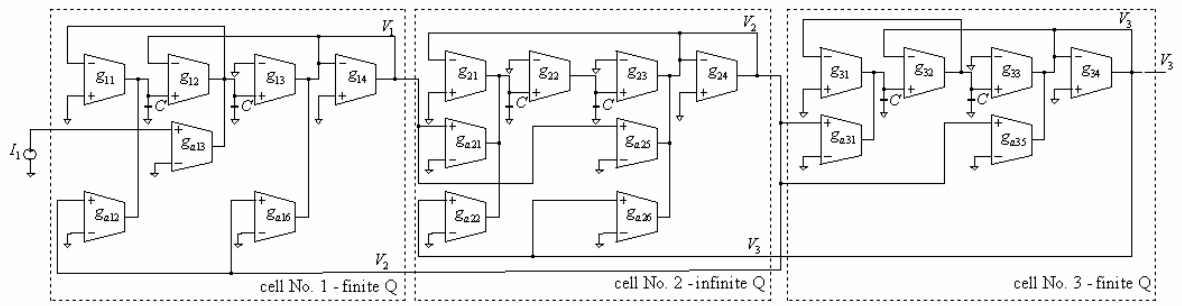

Fig. 6 The OTA-C realization of fifth-order elliptic low-pass ladder prototype filter in Fig. 4.

biquad circuit cell.. The result is that for the fifth-order filter under discussion, three OTA-C coupled biquad cells are used for a total of 21 OTAs. The block diagram of the circuit is given in Fig. 5 and a complete schematic of OTA-C coupled biquad filter is shown in Fig. 6. Denoting the cut-off frequency of the active low-pass filter by ω_o and choosing C as the value of the capacitors, Table 1 gives the design relationships for the first two cells of the filter.

As a matter of fact, the design of a high-pass filter equivalent to the prototype in Fig. 4 is very simple, and leads after the standard frequency transformation and the use of the design procedure developped in this Section to a circuit quite identical with the low-pass structure shown in Fig.6. Table 1 presents the design equations of first two cells of a fifth-order elliptic OTA-C coupled-biquad high-pass filter. The negative sign used in the table for the transconductance of g_{a2} OTA means that signals V_2 and V_3 are applied on the inverting inputs of g_{a12} respectively g_{a31} OTAs instead of their non-inverting inputs. It is the single difference between the low-pass implementation in Fig. 6 and the high-pass realization.

To verify the method described above, SPICE simulations were performed. The fifth-order low-pass elliptic passive filter prototype was used to design the circuit in Fig. 6 for low-pass and high-pass filters. Here, in Fig. 7 we only give the simulated result of a high-pass OTA-C circuit having the cut-off frequency of 10kHz.

V. CONCLUSIONS

The node-voltage emulation method reveals as a powerful method of simulation of pasive ladder filters by active filters, being equivalent from the point of view of performances with the mesh current approach.

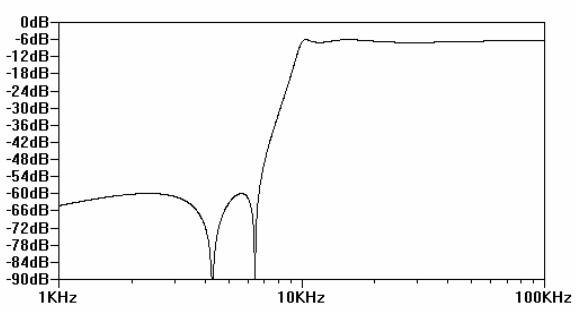

Fig. 7 Simulated magnitude response of high-pass OTA-C coupled-biquad implementation of low-pass prototype of Fig. 4

The method implements the passive network by the interconnection of multiple inputs biquad cells. The paper proposes two general OTA-C biquad cells that suits well in all cases of low-pass and high-pass network filter implementations. Fifth order low-pass and high-pass coupled biquad filters were designed and simulated.

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Table 1 Design relationships used for cells 1 and 2 in low-pass (LP) respectively high-pass (HP) OTA-C filter realizations of the coupled-biquad schematic of Fig. 6.

OTA's g_m	Cell No. 1 – finite Q		Cell No. 2 – infinite Q	
	LP Filter	**HP Filter**	**LP Filter**	**HP Filter**
g_1	$g_{11L}=\omega_o C\Big/\sqrt{(c_1+c_2)l_2}$	$g_{11H}=\omega_o C\sqrt{(c_1+c_2)l_2}$	$g_{21L}=\omega_o C\Big/\sqrt{(c_2+c_3+c_4)\frac{l_2l_4}{l_2+l_4}}$	$g_{21H}=\omega_o C\sqrt{(c_2+c_3+c_4)\frac{l_2l_4}{l_2+l_4}}$
g_2	g_{11L}	g_{11H}	g_{21L}	g_{21H}
g_3	$\sqrt{l_2/(c_1+c_2)}g_{11L}$	$\sqrt{l_2/(c_1+c_2)}g_{11H}$	g_{21L}	g_{21H}
g_4	g_{11L}	g_{11H}	g_{21L}	g_{21H}
g_{a1}	-	-	$l_4/(l_2+l_4)\,g_{21L}$	$c_2/(c_2+c_3+c_4)\,g_{21H}$
g_{a2}	$c_1\Big/\sqrt{(c_1+c_2)l_2}\;g_{11L}$	$-c_1\Big/\sqrt{(c_1+c_2)l_2}\;g_{11H}$	$l_2/(l_2+l_4)\,g_{21L}$	$c_4/(c_2+c_3+c_4)\,g_{21H}$
g_{a3}	g_{11L}	g_{11H}	-	-
g_{a4}	-	-	-	-
g_{a5}	-	-	$c_2/(c_2+c_3+c_4)\,g_{21L}$	$l_4/(l_2+l_4)\,g_{21H}$
g_{a6}	$c_2/(c_1+c_2)\,g_{11L}$	g_{11H}	$c_4/(c_2+c_3+c_4)\,g_{21L}$	$l_2/(l_2+l_4)\,g_{21H}$

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Precisely Measuring Using Behavioural Blocks in PSpice

Mihaela Cîrlugea[1], Fazakas Albert[2], Sorin Hintea[3]

Abstract – We created specialized behavioral blocks that compute fast and accurately the power, the rms and average values of a signal. The signals can be seen through an adjustable "examination window". The method was tested on some filters and illustrated on some DC-DC converters, where the switch period is of μseconds and it is hard to obtain accurate data. The signals can be seen through an adjustable window.

Keywords: behavioural blocks, VIP, VIMED

I. INTRODUCTION

Generally, the problem of the system analysis is to find a system's response at given excitations. Therefore establishing necessary and sufficient parameters is necessary for obtaining the response's signals. In this measuring method we are interested in obtaining the response's signals through numerical simulation, using Pspice.

A no harmonic but periodic excitation can be developed in Fourier series as a sum of harmonic components and one can apply the superposition principle. The analysis can be reduced to find the response of each harmonic excitation component that actually means determining the magnitudes and initial phases for the harmonic components. The principle of superposition cannot be applied on nonlinear systems. The response of a nonlinear system to a harmonic excitation is not harmonic, but periodic so that, even if the excitation has only one harmonic component, the response will have more components with different frequencies [3]. One defines a harmonic signal equivalent to the given signal (no harmonic but periodic) setting the condition that both signals must have the same rms value. The rms value for a periodic signal x(t) with period T is [3]:

$$X_{rms} = \sqrt{\frac{1}{T}\int_T x^2(t)dt} \qquad (1)$$

The instantaneous power of the energy transfer between two uniports is:

$$p(t) = v(t) \cdot i(t) \qquad (2)$$

Even if the circuits are nonlinear, phenomena are periodical and one can define the average power:

$$P_{avg} = \frac{1}{T}\int_T v(t) \cdot i(t)dt \qquad (3)$$

During a Pspice simulation one can measure instantaneous values, time domains or one can use Pspice offered functions. Such an example is RMS() [2]. The root mean square value is computed using specific Pspice techniques (products, filters) and not by applying an integral relation and thus, the function response is oscillatory damped. Experimental studies we made showed that the RMS() function response's damping in Pspice was slower than the computing time used by the techniques described here. For obtaining a convenient precision, the time for a regular Pspice simulation is very long.

Because of these reasons, we created some specialised behavioral blocks for measurement, VIP and VIMED, more faster and precise. For rigorously applying relation (1), the integral must be computed on an interval multiple of the signal's period and, for a higher precision, the computation is done after the transitory regime is finished. The signals can be seen through an adjustable „examination window"[6].

The blocks used for measuring the rms and average values perform mathematic relations between the corresponding input and output signals. This is why the blocks are created as macromodels containing controlled "mathematic expression" or "table" sources and predefined mathematic functions of the Pspice simulator.

The whole work is done during the periodic regime of the measured signals. By *transitory regime* we mean the simulation transitory time for each simulation running until the model reaches its

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permanent regime. Nonperiodical signals have not been studied.

II. MACROMODELS

A. *The Hanning window*

One defines an examination window by a function f(t) that gives the weights according to the signal inside the examination interval and is zero outside this interval. If the signal x(t) is examined during an interval θ, between the moments $t_1$and t_2, with t_2-t_1=θ, the active signal is:

$$x_1(t) = f(t)\cdot x(t) = \begin{cases} f(t)\cdot x(t), t_1 < t < t_2 \\ 0 \quad , \quad \text{otherwise} \end{cases} \tag{4}$$

The window is used to control an *integration process* and must not affect the integral value, so the following normalization relation has to be assessed:

$$\int_{t_1}^{t_2} f(t)dt = 1 \tag{5}$$

The rectangular window gives the same weight along all points of the examination interval of the signal.
The macromodel of the Hanning window is obtained by developing the rectangular window by adding a cos(2πt/θ) block, thus the mathematic expression of the Hanning window is:

$$\text{hann}(t) = \begin{cases} \frac{1}{\theta}\cdot\left[1+\cos\left(2\pi\cdot\frac{t-\tau}{\theta}\right)\right] & , \ |t-\tau| < \frac{\theta}{2} \\ 0 & , \ |t-\tau| > \frac{\theta}{2} \end{cases} \tag{6}$$

where θ is the examination time, $\theta = t_2 - t_1$, and τ is the middle of the examination interval, $\tau = \frac{t_2+t_1}{2}$.

B. *The VIP Block*

The VIP block has been created for measuring the rms values of the voltage (V) and current (I) and the power (P). This block is used in a section of a conveyor chain and also for measuring the active power sent to a load impedance. There are inputs used for voltages and also "current-controlled voltage sources" inputs, that means of "const*i" type. The block becomes active after a number of N_0 signal periods, after the transitory regime is over, and is measuring the signals over N signal periods.
The "fer" input, connected at the "fer" entrance of every integrator, does control the integration interval. These integrators have been developed from the INTEG integrator of the abm.olb library. The integrator INTEG3 has been modified to have three inputs, accomplishing the function:

$$v_{out}(t) = GAIN\cdot\int v_{fer}(t)\cdot v_{x1}(t)\cdot v_{x2}(t)dt \tag{7}$$

This integrator will accomplish the function (3), choosing GAIN=1/T=frequency, $v_{x1}(t)$=v(t), controlled by the window $v_{fer}(t)$=fer(t). At the output of this block a voltage is obtained, computationally equal to the transferred power. The VALEF integrators have been developed from INTEG of the Pspice library, which have added a new input and do extract the square root. Thus, they calculate the function:

$$v_{out}(t) = \sqrt{GAIN\cdot\int v_{fer}(t)\cdot v_x^2(t)dt} \tag{8}$$

Choosing GAIN=1/T=frequency, $v_x(t)$=v(t), controlled by the window $v_{fer}(t)$=fer(t), the first integrator will compute the rms value of the voltage and the second integrator has the input X connected to a voltage with the same value to that of the current and will generate, after the active window time interval, the rms value of the current $v_2[V] = k[\Omega]\cdot i[A]$ where k=+1 is the gain of H1, measured in Ohms. H1 is a current controlled voltage source. The VIP block has only one transparent parameter, called "frecv", set at the default value of 50Hz [1].

C. *The VIMED Block*

The VIMED block has been created for measuring the average values (MED comes from medium) of the current (I) and voltage (V) in a section of a conveyor chain. The block becomes active after a number of N_0 signal periods, after passing the transitory regime, and is measuring the signals over N signal periods. The signal transmitted from the input to the output of the circuit is not influenced by the VIMED block. The "fer" input of the window block, connected at the "fer" entrance of every integrator, does control the integration interval, that means it opens the window at t_1=N_0T and closes it at t_2=(N_0+N)T.
The VALMED integrators have been obtained from INTEG of the Pspice library, which extracts the square root. These blocks must accomplish the function:

$$v_{med}(t) = \sqrt{GAIN\cdot\int v_{fer}(t)v_x(t)dt} \tag{9}$$

Setting GAIN=1/T=frequency, $v_{x1}(t)$=v(t), $v_{fer}(t)$=fer(t) the integrator will compute the average value of the voltage, for the first integrator and the average value of the current for the second integrator. The VIMED block has only one transparent

parameter, called “frecv”, set at the default value of 50Hz[1].

stable and the transitory regime is finished so the values can be measured.

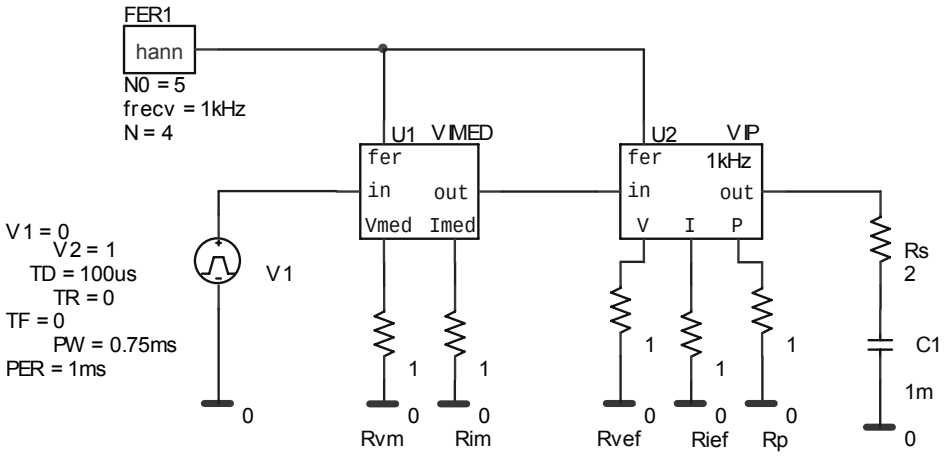

Fig. 1 Low pass filter circuit for testing the method for rms, average values and power

III. RESULTS OBTAINED IN PSPICE SIMULATIONS

A. *Filters*

An example is shown in the circuit in fig.1, where the blocks VIP and VIMED are set between the voltage source V_1 and the load resistance R_s. There were made a lot of tests using a high pass (RL) filter and respectively a low pass (RC) filter. After we obtained good results while testing, we used the method for CC-CC converters [4]. When testing we used a pulse voltage source because in CC-CC converters we need this kind of voltage source.

VIMED and VIP blocks are serial with the inductance L1 in first case and serial with the capacitor C1 in the second case. At the resistance terminals R_{vm} is measuring the average value (Vmed) of the filter voltage, R_{im} the average value of the current, R_{vef} the rms value of the voltage (V), R_{ief} the rms value of the current (I) and R_p the load power (P). These resistances have an unitary value for simplifying the reading results: the signal values at the measurement terminals are equal to the current values through the unitary resistances. There were made measurements for different values of the delay time, in every decade from 0μs to 100μs, one has used different values of the duty factor of 0.25ms, 0.5ms and 0.75ms and different values for the integration step, like 0.1, 0.5, 1, 1.5μs. For all these cases, the errors between the simulated and computed values were measured, the validity and utility of the blocks have been checked.

The Hanning window has its parameters set: the frequency to 1kHz, N_0=5, N=4 because one considered that after the fifth period, the LPF signal is

In case of the low pass filter circuit, the duty factor is given, by:

$$f_u = \frac{\theta}{T} \tag{10}$$

The average value of the voltage is calculated using the expression

$$V_{med} = V\frac{\theta}{T} = 1V \cdot \frac{\theta}{T} \tag{11}$$

and the rms voltage

$$V_{ef} = \sqrt{\frac{1}{T}\int_0^{\theta} v^2 dt} = 1V \cdot \sqrt{\frac{\theta}{T}} = 1V \cdot \sqrt{f_u} \tag{12}$$

all that because one consideres the voltage unitary at the circuit input [4].

One write the current described by the equations [4]

$$i(t) = \begin{cases} \dfrac{V}{R}\dfrac{1-e^{-(T-\theta)/\tau}}{1-e^{-T/\tau}} \cdot e^{-t/\tau} = i_1(t), & 0 < t < \theta \\ \dfrac{V}{R}\dfrac{e^{-\theta/\tau}-1}{1-e^{-T/\tau}} \cdot e^{-(t-\theta)/\tau} = i_2(t), & \theta < t < T \end{cases} \tag{13}$$

with the expressions for the average current

$$I_{med} = \frac{1}{T}\int_T I(t)dt = \frac{1}{T}\int_0^{\theta} i_1(t)dt + \frac{1}{T}\int_{\theta}^{T} i_2(t)dt \tag{14}$$

and the rms value:

$$I_{ef} = \sqrt{\frac{1}{T}\int_0^{\theta} i_1^2(t)dt + \frac{1}{T}\int_{\theta}^{T} i_1^2(t)dt} \qquad (15)$$

Under these circumstances, measurements were done obtaining smaller errors than with Pspice techinques.

TABLE 1. Results for HPF

Quantity	F_{duty}=0.25		F_{duty}=0.5		F_{duty}=0.75	
	Val.	*Err %*	*Val.*	*Err %*	*Val.*	*Err %*
Vavg [mV]	250	0.2	500	0.2	750	0.2
Vrms [mV]	500	0.2	707.1	0.2	866	0.19
Iavg [mA]	125	0.06	250	0.06	375	0.06
Irms [mA]	135.3	0.07	259.2	0.19	378	0.18
P [mW]	366.2	0.15	134.4	0.3	286	0.3

There have been made a lot of comparison tables for the computed values (using formulas) and for the measured ones [4] in all situations described above. In tables 1 and 2 there is a short form of all error tables, it's something like the average value. The percentage-errors that have been obtained are very small, for voltages and currents percentage errors were less than 0.2% and for power less than 0.4 %[5].

TABLE 2. Results for LPF

Quantity	F_{duty}=0.25		F_{duty}=0.5		F_{duty}=0.75	
	Val.	*Err %*	*Val.*	*Err %*	*Val.*	*Err %*
Vavg [mV]	250	0.3	500	0.3	750	0.2
Vrms [mV]	500	0.12	707	0.16	866	0.14
Iavg [mA]	216	0.02	249	0.01	216	0.02
Irms [mA]	216	0.04	249	0.01	216	0.02
P [mW]	93.3	0.23	124	0.16	93.3	0.4

B. *CC-CC Converters (Boost)*

Another circuit over which tests were done, is the **Boost CC-CC** converter[3]. In figure 2 is shown the circuit of the step-up converter and, at input and output, set the measurement behavioural blocks controlled by the Hanning block. The frequency of the Hanning window was set to the switch frequency. The final scheme consists on three parts, at the input there is the behavioural block for the Hanning measuring window, the VIMED block that measures the average values of the signals (current and voltage) at the input of the converter, the VIP block used for measuring rms values of the voltage (V) and current (I) and the power (P) at the input of the converter. The second part of the circuit is given by the converter itself; the last part is represented by the VIP and VIMED blocks at the output of the converter, used to measure the average (VIMED) respectively the rms and power (VIP) values of the output signals (current and voltage).

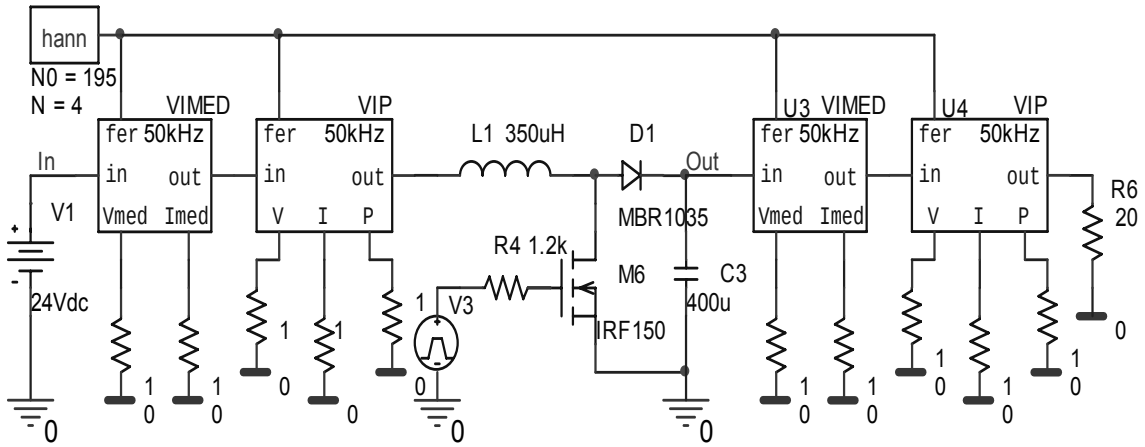

Fig.2. Testing the behavioural blocks for a Boost CC-CC converter

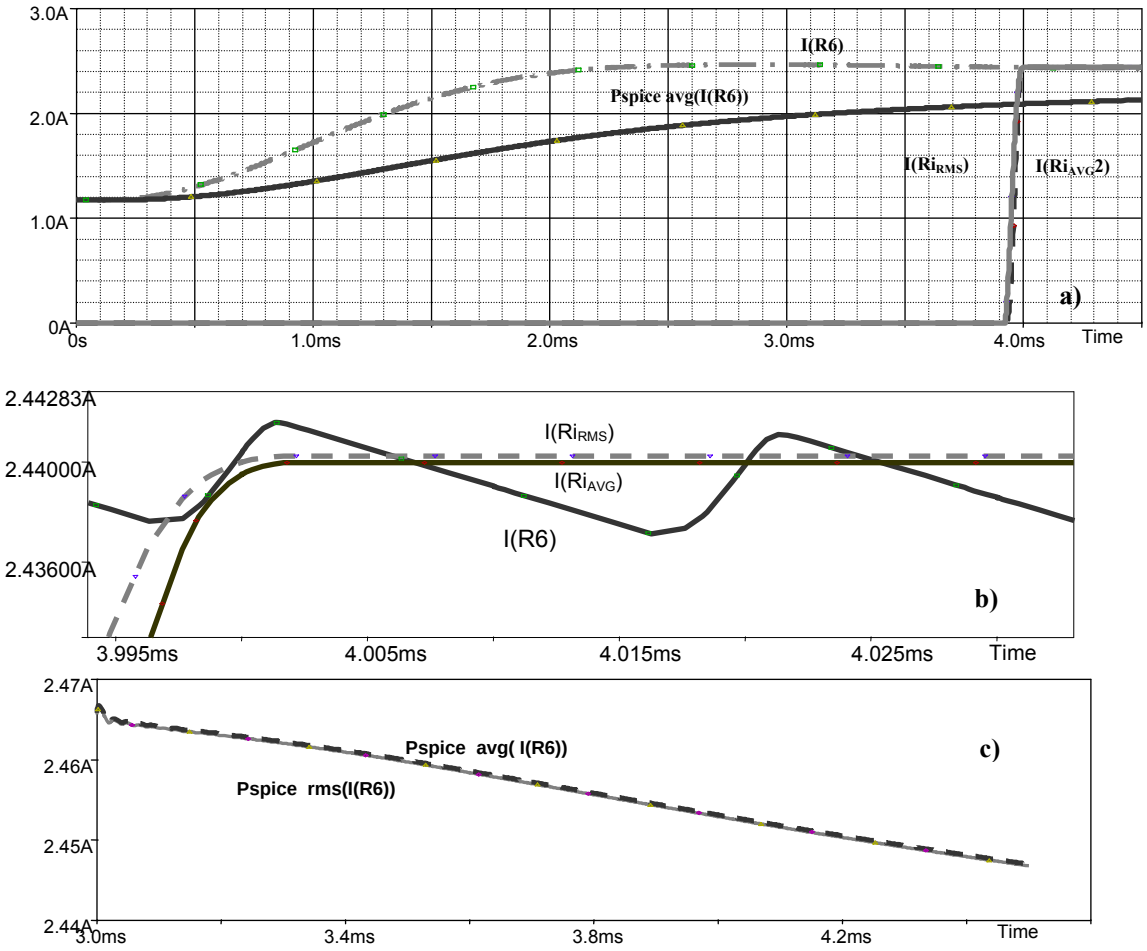

Fig. 3. Output current through the load resistance (ideal value=6A)
a) Comparison of the current, the AVG Pspice function and the AVG and RMS obtained with behavioural blocks b) detail c) zoom

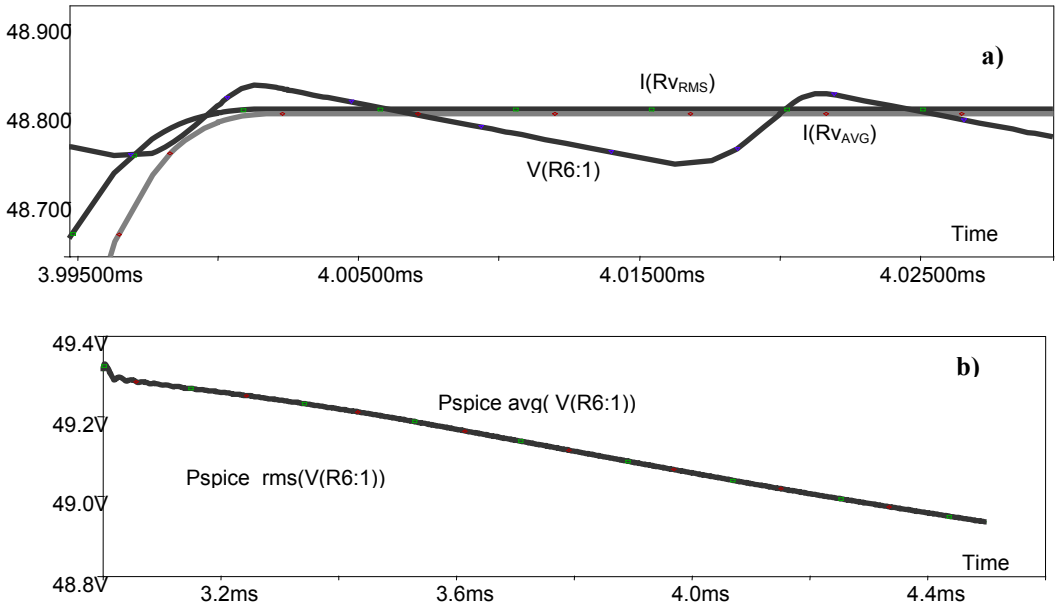

Fig.4. Output voltage (ideal value=48V)
a) Comparison of the current, the AVG Pspice function and the AVG and RMS obtained with behavioural blocks b) zoom

The simulation results of the circuit in fig.2 are shown in fig.3. In fig.3.a there is a comparison between the values obtain with the two methods, the classical Pspice and the one presented here. The advantage of the new method is it's accuracy and the fact that, after applying the observation window, the values are constant and easily to read. This detail is shown in fig.3b and also the behaviour of the RMS and AVG Pspice functions in fig.3c for the output current, behaviour which is everything else that constant. In fig.6 is also presented the output voltage, in fig.4a are shown the values obtained with VIP and VIMED blocks and in fig.4b the behaviour of the RMS and AVG Pspice functions of the same signal.

An important observation is that Pspice computes the values over the entire simulation interval, using all data collection. This means, if we want to obtain an accurate result we have to save the simulation data after the transitory regime is finished. A first conclusion can be drawn that the user must manually do a whole procedure that is avoided by using the measuring blocks. The use of the observation window eases the procedure. Pspice works on a history, meaning that the obtained values are calculated on a history so it is possible that, using exactly the same circuit, one can obtain different values for the same currents or voltages, depending on the history and of the moment in time when the simulation is done. The same phaenomenon happens with the transmitted power. This never happens using the behavioural blocks which work in the permanent regime, so another reason why this method is more accurate.

IV. CONCLUSIONS

This paper presented techniques of measuring power, rms and average values of the signals over a circuit, using some behavioural blocks developed with elements of the ABM library.

For a simple use of this method, all windows have an unitary area. To measure rms values and power the VIP block is used and to measure average values the VIMED block is used.

The "window" technique is very useful for setting the integration interval because the error does not depend on this window, neither on the window's position on the characteristic. The measurements can be done in permanent regime. It is not possible to use the FFT (Fast Fourier Transformation) instead, because FFT would obtain the component's magnitudes in a nonharmonic regime[6]. For the rms, average and power values, otherwise than using this method, some extra computations would be necessary. For the FFT precision, the simulation step should be very small and this would lead to a very long simulation time and huge simulations. This measuring method is original and one obtains very good results, percentual errors less than 1%, usually they are even smaller than 0.5%. It was showed an example using a simple circuit and comparing the results obtained by computation and simulation [6]. Then the method was used over a more complicated circuit, illustrated here by a Boost-converter, where the switching times are also very small (μ-seconds) and thus the precision is very important[2].

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Preconditioning Circuit for Electrical Power System Disturbances Measurement

Ciprian Dughir[1], Gabriel Găşpăresc[2]

Abstract – This paper is focused on how to reduce the amplitude of electrical disturbances which appears in the electrical power systems to a low voltage supported by the acquisition boards, without loosing any important disturbances. Is well known the fact that the maximum input voltage of the most popular acquisition boards is about ±10V. The disturbances may heave 10kV amplitude, and if we simply divide the input voltage by 1000 to reduce the 10kV to 10V, the main power system voltage (220V) will be reduced to 0.22V which is too low to obtain a sufficient accuracy in the measurement process, counting that the most of the disturbances have amplitudes in the area of 0-100V.

Keywords: power system, disturbance, voltage divisor, nonlinear

I. INTRODUCTION

The power quality study involves an important step, i.e., monitoring the actual voltage and current waveforms, classifies these waveforms and displays them when certain thresholds are exceeded. These waveforms exhibit certain distinguishing characteristics and can be identified to belong to a certain waveform class. The classification scheme has to be robust and accurate to handle the noisy data collected from the transmission or distribution networks.

The main problem in the electrical power systems is monitoring and detecting of disturbances. Because of the multitudes of types the disturbances are, each disturbances with her specificity, it is difficult to detect and capture such types of disturbances. The common types of disturbances are that can produce little variations of the power system voltage around 220V. Another type of disturbances is the disturbances with amplitudes between 500V and 2kV, and last one with amplitudes over 2kV, disturbances which occurs very rare.

II. THE METHOD PROPOSED

The method proposed in this paper is focused on how to divide the input voltage to a value that complies with the acquisition board, without losing any type of disturbances. This method consists in the use of a functional transformer [4][5] with the transfer function presented in figure 2. Because most of the disturbances present smaller variations around 220V, the first cut point is set to 500V to preserve sufficient the amplitude of the output signal. Very small disturbances around the 220V can be now analyzed. The second segment is from 0.5kV to 2kV where is to found the disturbances which occur more rarely then the first class, and the last segment represent the disturbances which appears very rare in the signal.

After the acquisition process, the signal is processed for detecting the disturbances, and if the algorithm found any disturbances, the signal is reverted to the original shape and then recorded to a file to be analyzed or viewed later [5][6].

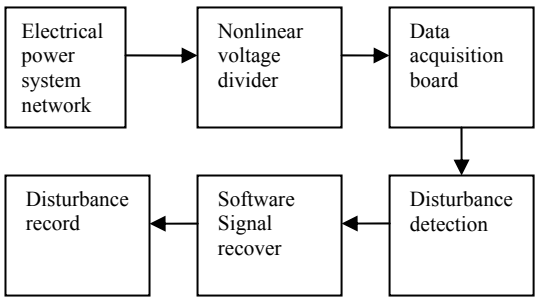

Fig. 1. Bloc diagram

The functional transformer uses a operational amplifier with very low bias current because the value of the input resistor R_{in}. If the value of R_{in} increases, the voltage on that resistor increases. This voltage must be insignificant in rapport with the input signal. If the input resistance decreases, the value of R_2 and R_4 becomes comparable with the conduction resistance of the diode D_2 and D_4. For this purpose was chosen the AD8616 operational amplifier produced by Analog Devices. This OA has an input bias current of 200 fA..

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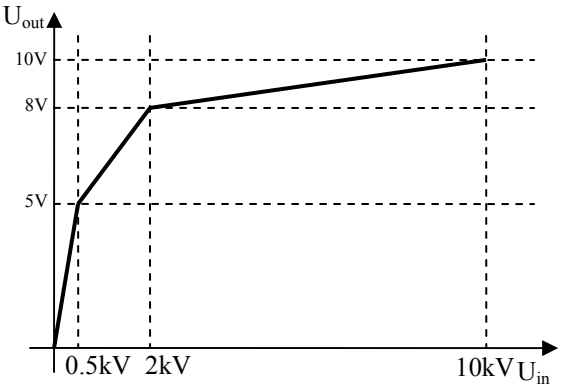

Fig. 2. The transfer function of the circuit

The schematic diagram of the functional transformer is presented in fig. 3. This is a classical functional transformer with diodes.

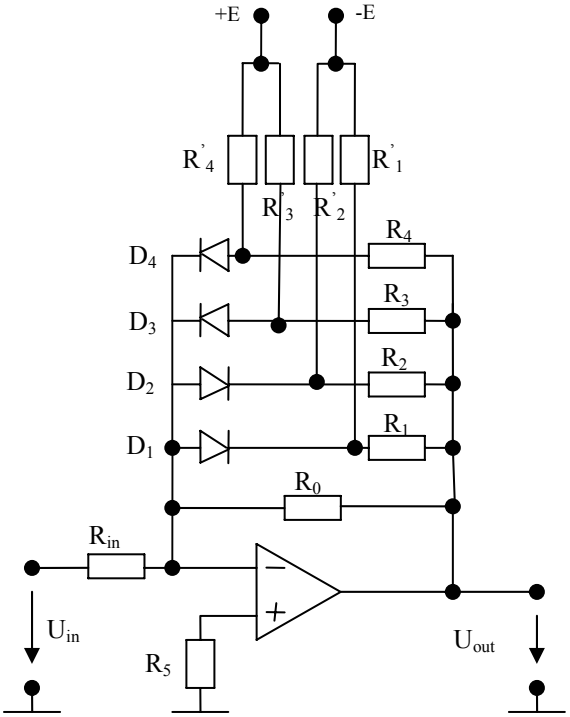

Fig. 3. Circuit schematic

The value of the input resistance R_{in} was chosen after multiples calculus and simulations to be 1MΩ. Starting from this values has been computed the values for the other resistors in the circuit. The first voltage divider consisting in R_{in} and R_0 must realize the first segment of the transfer function. If the input voltage exceeds the value of 500V, the diode D_1 begins to conduct and the resistor R_1 is introduced in the circuit. The result is that the resistor R_1 is now in parallel with resistor R_0 and the division ratio of the voltage divider is considerably higher then in the first case. If the input voltage is higher than 2kV, the diode D_1 is still conducting and the diode D_2 begins to conduct. In this case, the resistor R_0 is in parallel with R_1 and R_2. The division ratio is in this case bigger then the second case, end very big comparing to the first case. The resistances R_0, R_1 and R_2 is controlling the input voltage breakpoints, and the resistors R_0 , R'_1 and R'_2 is controlling the output voltage breakpoints. For the case presented here, it is possible to calculate the points of the transfer function, by determining the slope of each segment.

$$a_k = \frac{U_{out_{k+1}} - U_{out_k}}{U_{in_{k+1}} - U_{in_k}} \qquad (1)$$

After each slope is calculated, next is to calculate the division ratio of each divider, and the values of resistances composing the divider with relation (2).

$$\begin{aligned} &R_0 = a_0 \cdot R_{in} \\ &R_{ech1} = a_1 \cdot R_{in}\,, \quad R_{ech1} = R_0 \parallel R_1 \\ &R_{ech2} = a_2 \cdot R_{in}\,, \quad R_{ech2} = R_0 \parallel R_1 \parallel R_2 \end{aligned} \qquad (2)$$

The last step in the projecting of the circuit is to establish the breakpoints of the output voltage.

$$\begin{aligned} R'_1 &= R_1 \frac{V_{D1} - E}{V_{Out1} - V_{D1}} \\ R'_2 &= R_2 \frac{V_{D1} - E}{V_{Out2} - V_{D1}} \end{aligned} \qquad (3)$$

III. EXPERIMENTAL RESULTS

The circuit was simulated in PSpice using the model provided especially for AD8616 by Analog Devices. The results are very close to the projecting data. The figure 4 shows the transfer characteristic of the circuit.

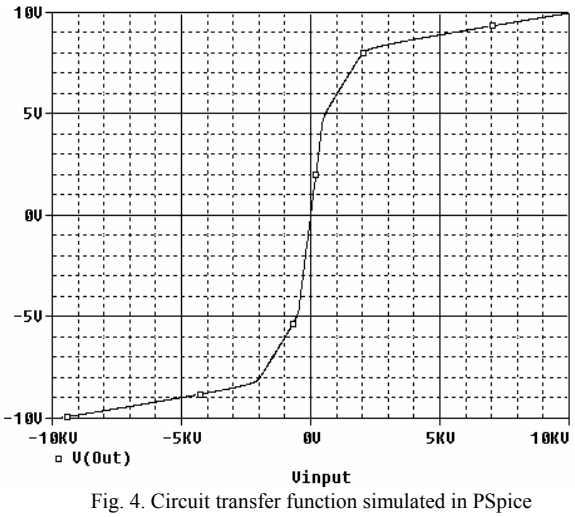

Fig. 4. Circuit transfer function simulated in PSpice

One thing that is interesting is the error on the breakpoints. Serious contributions to these types of error have the internal resistance of the diodes used, and the forward voltage drop of the diodes. This is a disadvantage of this kind of voltage divider.

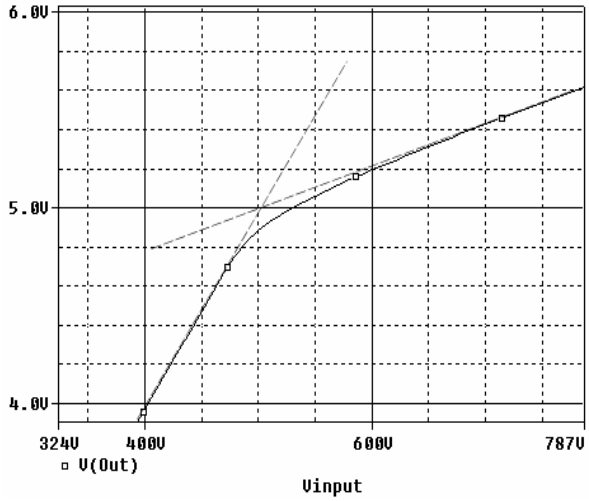

Fig. 5. Errors at 500V

As it can be seen in the figure 5, the ideal breakpoint (marked with dashed lines) is exactly at 500V and 5V. The real characteristic has a rounding error due to the fact that the diodes don't enter in the conductive state instantaneously. This error has a quantum of 1% from the output voltage.

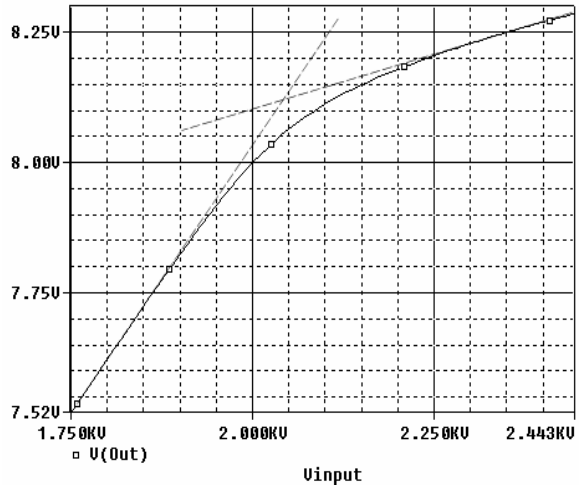

Fig. 6. Errors at 2kV

On the second breakpoint the error is significantly higher because of propagation from the first breakpoint. In plus, here is another error due to the fact that in the calculus of R_1 has been made some approximations about the forward drop voltage of the diode D2. The maximum error at this breakpoint is 1.5%.

In the last case, the error at 10kV is 0.2%. This error is made by the approximation of the value of diode D_2 conducting resistance, since its value is comparable with resistor R_2. To minimize this error the value of R_2 must be 5-10 times bigger than conducting resistance of diode D_2. But this is not possible, because increasing the value of R_2 will increase the value of the resistor R_{in} which is not a good idea as mentioned earlier in this paper.

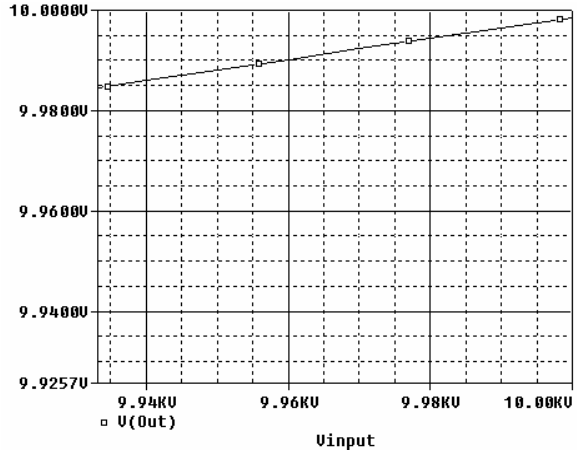

Fig. 7. Errors at 10kV

A parameter who might keep in count is the temperature. The temperature can modify the internal resistance and the forward drop voltage of the diodes. The influence of the temperature is shown in the figures below for each breakpoint.

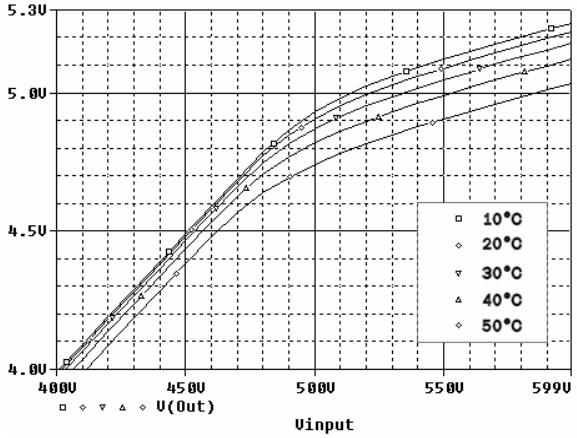

Fig. 8. The influence of the temperature at 500V

The temperature can modify the internal resistance and the opening voltage of the diodes, raising the error of the circuit.

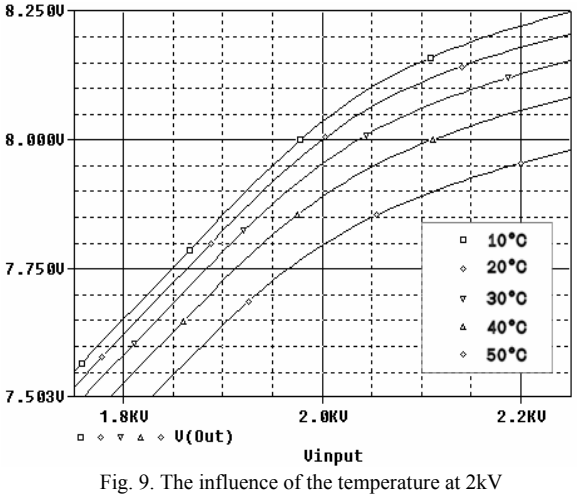

Fig. 9. The influence of the temperature at 2kV

It can be seen that the higher the temperature, the higher is the error.

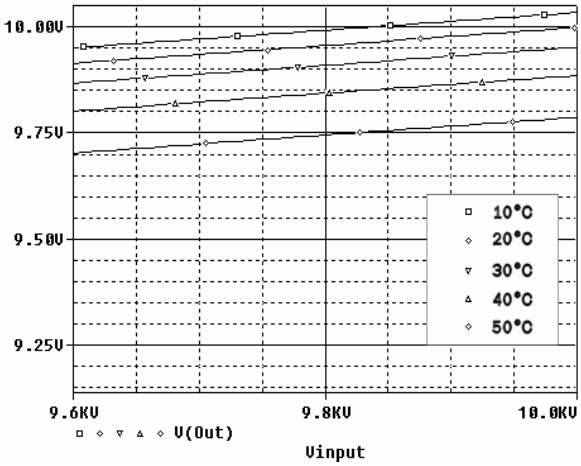

Fig. 10. The influence of the temperature at10kV

These variations of the output voltage with temperature must be eliminated.

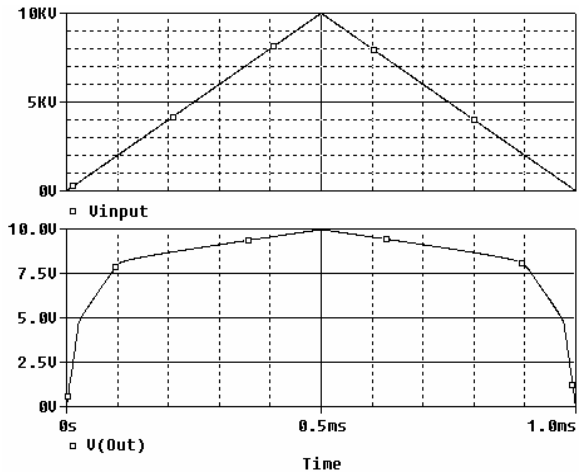

Fig. 11. Input and output signals

To see how the circuit works, at the input was applied a triangular signal because with this shape is more easy to observe how the circuit work. The triangular shape heaves a linear variation, suitable to observe any nonlinearity on the output signal.

The triangular signal has 1 kHz frequency and amplitude of 10kV. At the output of the circuit, the signal presents the 2 breakpoints at 5V and at 8V.

The output signal from the circuit is software recovered to the initial amplitude. In the figure 12 is shown both the input and recovered signal. The recovered signal has not the same shape with the input signal because of the errors on the first and second breakpoints. These errors can be software minimized. The triangular shape can be used in the process of minimizing these errors. The idea is to apply at the input of the circuit a triangular signal and to determine each error and her sign for discrete values of the input voltage. Then, with this values, can be made an interpolation to establish the shape of the variation of the errors.

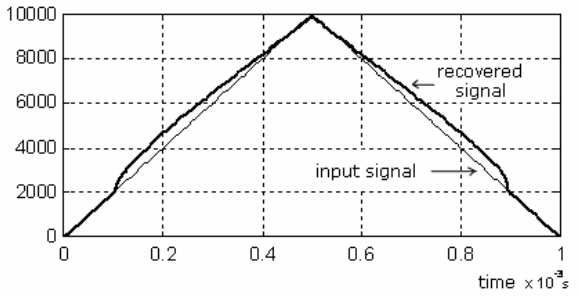

Fig. 12. Software recovered signal

The spectral analysis of the input and recovered signal show a significant modification in the recovered signal spectrum, especially the apparition of the second order harmonics.

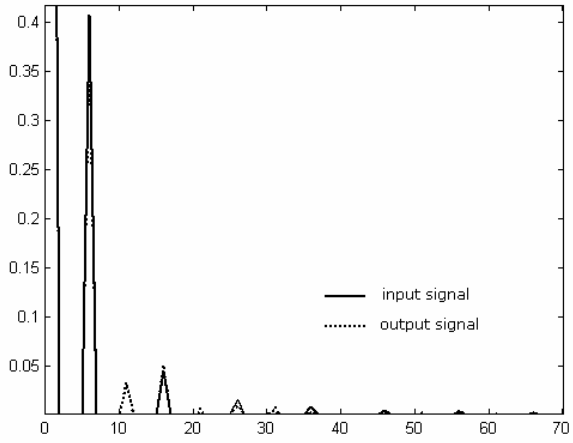

Fig. 13. FFT of the input and recovered signal

Because the triangular signal is rarely present in practical conditions, we are chose two types of signals more present in practical conditions: the spike and the damped oscillatory wave.

Most high amplitude disturbances in the electrical power system heave a spike shape.

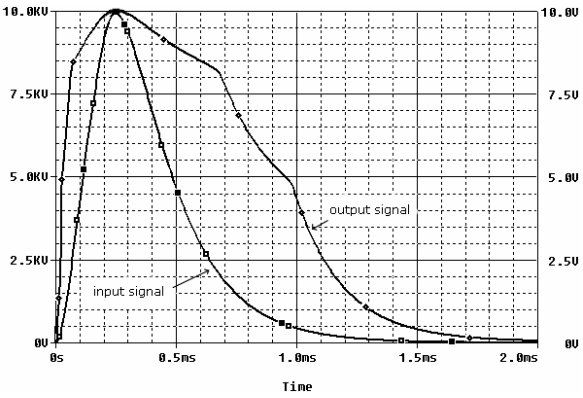

Fig. 14. Spike signal

The spike disturbances are an extremely high and nearly instantaneous increase in voltage with a very short duration measured in microseconds. Spikes are often caused by lightning or by events such as power coming back on after an outage. In the figure 14 is represented a spike input signal and the signal at the output of the circuit.
The signal from the output of the circuit is applied to the recovery block resulting in a signal with the shape verry similar to the shape of the input signal. The error is due to the breakpoints of the transfer characteristic of the circuit. It can be observed in the figure 15 that at 2kV the error heaves an important value (25%), because of propagation of the error from the first breakpoint. At 500V the error is smaller (about 15%), but unfortunately this error amplifies the error at the second breakpoint.

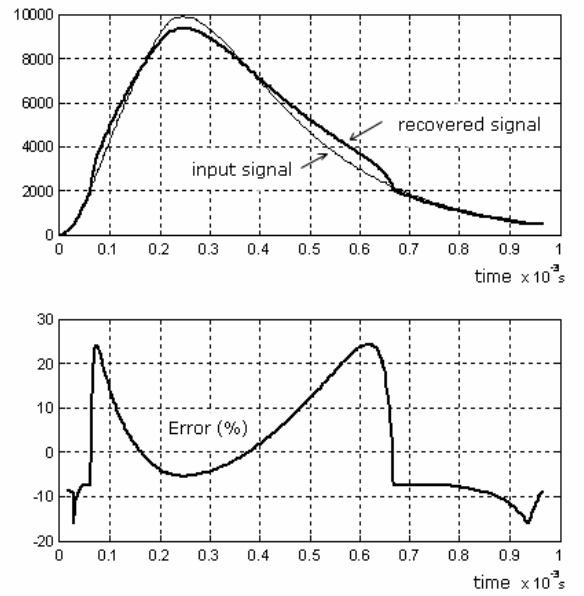

Fig. 15. Biexponential signal applied at the input and the recovered signal

At the 10kV, the recovered signal is smaller than the input signal, at this point the error is about 5%.

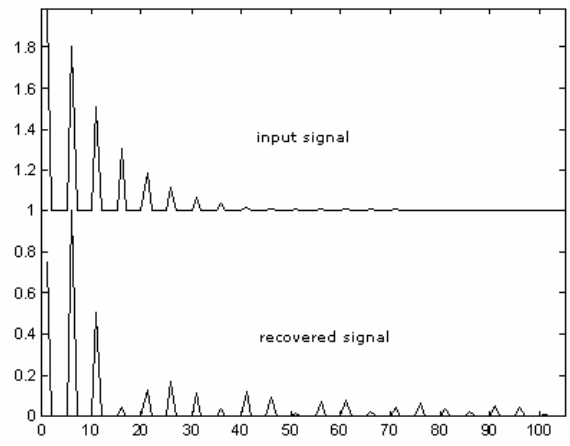

Fig. 16. Spectrum of the spike input and recovered signal

To minimize this errors, it can be observed that if to the output signal is applied a constant voltage, the error can be reduced at about 10%.
In the spectrum of the recovered signal can be observed an increased number of high frequency harmonics. This harmonics is generated by the circuit transfer function around the 2kV breakpoint. The transition around the 2kV is not smooth, which generate the high frequency harmonics.
Another type of disturbances is the sag disturbances. Sag is defined as a short duration drop in voltage. The amplitude of the electrical power system decreases to 0.9 of their nominal value, but this is not always done instantaneously. Such type of disturbances is presented in the figure 17.

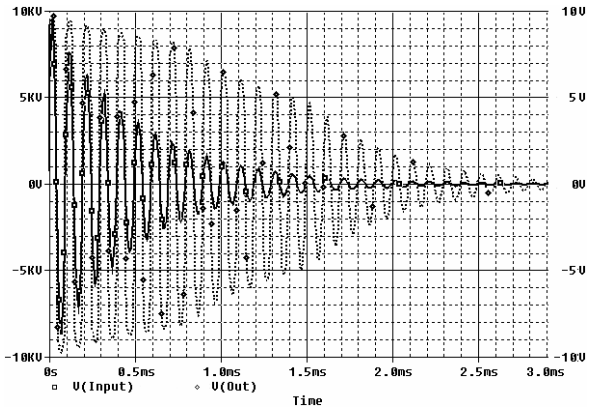

Fig. 17. Damped oscillatory wave

Basically, this disturbance consists in a sine wave with the amplitude varying over an exponential shape. With continuous line is plotted the input signal, and with dotted line is plotted the signal at the output of the circuit.

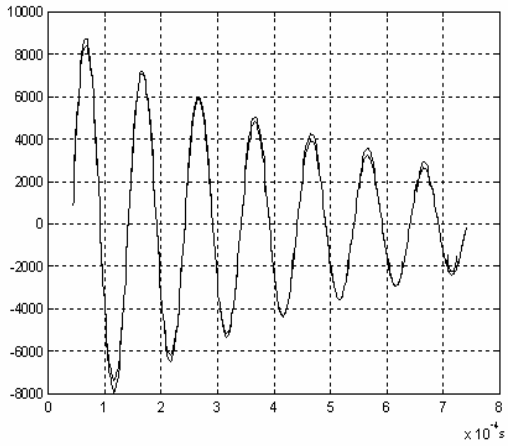

Fig. 18. Damped oscillatory wave at the input of the circuit and after the software recovery

The signal of the output of the circuit is applied to the recovery block to reconstruct its original shape. The differences between the input and the recovered signal are relatively small, the maximum errors being 10%. In this case, the error at 2kV is smaller than the case of the spike. In the figure 19 is represented the

relative errors at the peaks of the damped oscillatory wave.

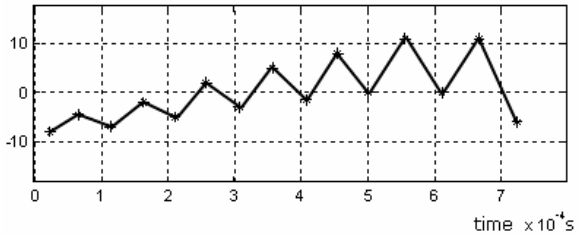

Fig. 19. The relative errors of the maximum amplitude of damped oscillatory wave after the software recovery

Around the value of 10kV the errors are negatives and their values are under 10%, being smaller around 6kV and increasing again when the amplitude of the signal becomes around 2kV. The bigger value of the errors for smaller amplitudes of the signal is not an inconvenient. It can be observed that the errors for the positive and negative side of the signal are not the same value and sign. This is caused by the diodes on the positive and negative side of the functional transformer, diodes which don't heave the same conductive resistance and the forward drop voltage. To prevent this, the diodes must be carefully selected.
Like in the other cases, the spectrum of the recovered signal presents high frequency harmonics.
This harmonics is produced, like in the cases above, by the breakpoints of the circuit and it is necessarily to reduce their amplitude.

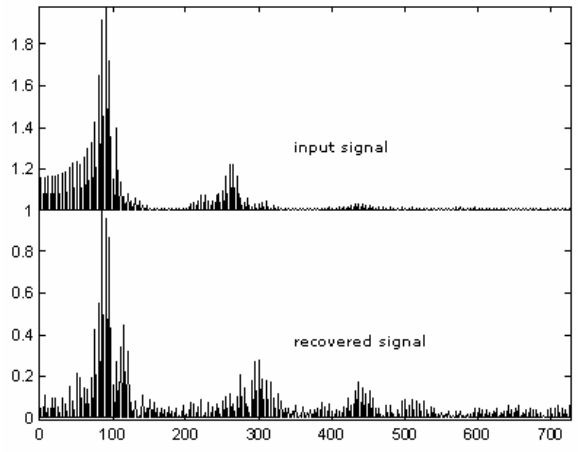

Fig. 20. Spectrum of the damped oscillatory wave

IV. CONCLUSIONS

Analyzing an important parameter of the signal, the power of the input and recovered signal, it has been observed that the relative error of the power of the triangular output signal is 6%, so the power of the output signal is 0.06 times bigger than the input signal power. For the spike signal, the relative error of the power of the signal is 1.86%, and for the dumped oscillatory wave, this error is -6.1%.
For the spike signal we observed that the rise time of the recovered signal is decreased with about 10% from the input signal, and the time at half amplitude is increased with 11% from the input signal.
To maintain the accuracy of the output voltage the circuit must be compensated with the temperature. A maximum error value of 5% is satisfactory for the goal proposed. To maintain the error at this point it's necessarily to thermally isolate the circuit. A ±2 ºC in temperature variations is maximum allowed. To reduce the errors caused by the diodes, it must be known the conductive resistance and the forward drop voltage. The diodes are the elements that generate the biggest error in the circuit. The diodes must be selected carefully to heave the same parameters. The errors at the first and second breakpoint can be software corrected, once their shape is known. For that, the software recovery circuit must heave a self calibration circuit to minimize this type of errors.
Another source of errors is the resistive elements of the circuit like resistors and PCB. All resistances must heave a maximum error of 0.5%.

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Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 51(65), Fascicola 1, 2006

Rejection of potentially defective CMOS IC

Popo Rodion[1]

Abstract – In this paper, some measures of increase of operational reliability of microcircuits at stages of manufacture and operation are examined.
Keywords: microcircuits

I. INFLUENCE OF GAMMA IRRADIATION AND ANNEALING ON SENSITIVE PARAMETERS IC 564LE5

Research was spent on IC current manufacture on the algorithm submitted on fig. 1. Results on change sensitive parameters have shown, that the most changing parameter at an irradiation is the current of consumption, and, it grows almost by one order more at potentially defective IC. However, at room temperature there is a fast decrease of values with gradual returning to reference values after an exhibitor. From the analysis of experimental results it is possible to draw the following conclusions:

1) Measurement of values of a current of consumption IC 564LE5 during 1 hour after an irradiation a doze 105 R allows to classify them on suitable and a spoilage (to suitable IC at what the current of consumption does not exceed shop norm – 60 nA concern);

2) Relative changes on other parameters are less than on a current of consumption (though values are higher);

3) At room temperature in day of return to reference values of parameters it is not observed;

4) the annealing at temperature 150-180^{0}C within several hours does not return all parameters to reference values while annealing at 350^{0}C during 0,5-1 hour returns all parameters to reference values (including at defective).

The accelerated tests investigated IC at temperature 125^{0}C and a pulse feed within 1 month have shown, that their parameters have remained within the limits of norms THAT.

II. REJECTION OF POTENTIALLY DEFECTIVE IC ON PLATES

Rejection of potentially defective IC on plates after an irradiation is more expedient. However, today it represents some industrial difficulties connected to necessity of the control of parameters of structures within several hours - day. At plenty of plates it is possible to use the express train of sample, but it reduces reliability of rejection.

The researches which have been carried out on algorithm, submitted on fig. 2, have shown, that after ETT and the subsequent gamma irradiation relative changes of a current of consumption are much higher (2118 % - 1st part, 1192 % - 2nd part, 129O than % - 3rd part), than without carrying out ETT (parts 2 and 3) while relative changes of a target current of a high level differ on 3,3 % (45,9 % - for 1st part, 49,2 % - for 3rd part). Annealing IC within 0,5-1 hours at temperature 350^{0}C returns parameters to reference values, but after carrying out again ETT the consumption current grows more at potentially defective IC. The annealing within 3 days at temperature 150^{0}C reduces values of a current of consumption (after ETT were checked once again) up to reference values of effective articles. It means that in one hour the annealing at temperature 350^{0}C for investigated IC was insufficiently for full restoration of parameters (system oxide - silicon remains unstable). It is possible to assume, that the CJ assembly (planting on the eutectic in the investigated case, hermetic sealing) results in mechanical pressure of a crystal which are added to internal pressure in oxide and on border oxide silicon. These pressures (voltages) are shown at temperature processing and gamma irradiation on changes of parameters. Gamma irradiation promotes display of deeper levels, and the annealing temperature to display at finest. As a result of gamma irradiation and the annealing there is an improvement of structure for one part of crystals and deterioration - for another which is potentially defective.

So:

1) Rejection of potentially defective IC can be carried out with the help of gamma irradiation and annealing and it's better to make it on plates;

2) The temperature mode of manufacturing oxide substrate and the subsequent operations of manufacturing IC should be supervised well that it was as small as possible formed internal and mechanical pressure.

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III. REJECTION OF POTENTIALLY DEFECTIVE IC: A METHOD OF TEMPERATURE RISE AND SUBMISSION OF AN EXCEEDING PULSE PRESSURE ON THE TRUNK OF A FEED

In this section accelerated tests IC of memory 565RU1 and 556RT5 are examined. The problem of accelerated tests (UI) IC for EA developers is essential as refusals IC can't do without any financial losses (for example, in space objects).

Let's consider results of research IC of memory with the help of the forced tests thermal training with applying the increased electric loadings and the subsequent check of functioning in conformity about THAT.

At a choice of temperature of tests it is necessary to take into account the physical phenomena occurring in concrete tested IC, opportunities of the test equipment. The size of an exceeding pressure got out so that there was no breakdown (transitions) in oxide substrates and oxides of remembering elements. The conclusion has been made of the analysis of work IC 565RU1, that a mode at which all elements 565RU1 work practically, the mode of record is. The time of submission of an exceeding pressure is determined by the diagram of conditions (for 565RU1 on an input it should be equal 60-150 nanosecond, beginning from the moment of submission on input "CE" 12 B). Thus a pressure (up to 20 B), temperature (700^0C), and duration of an exceeding pulse (up to 700 nanoseconds) have been picked up. During tests it was supervised OUR IC 565RU1.

Displacement of bottom border OUR is typical of the majority investigated IC on UDD aside increases on 0,8 – 2 In, and on UBB changes are insignificant. At action of temperature 700^0C within 8 hours and amplitude 4 In from 70 investigated IC five did not begin to store an exceeding pulse "1", one - "0", one "0" and "1", one - was restored. At action of the same temperature and an exceeding amplitude pulse of 8 In within 24 hours 10 %, as well as in the first case have broken down 7 IC from 70, that is. The conclusion arises, that over 8 hours to maintain IC at 70^0C is inexpedient, that influence on size of an exceeding pulse in 4 In and 8 In do not differ. From investigated IC the set in 70 pieces which was exposed to temperature and electric influence within 140 hours per the same modes has been made. Any of them has not broken down, while from untried 70 IC for same time 6 pieces have broken down. The analysis failed IC has shown, that at the majority of them the dielectric is punched.

In conformity about OST IC of 556 series are tested at temperature 70^0C in a nominal mode 5 In within 168 hours. ETT it is carried out after "the burn-through" smooth crosspieces and it is directed on revealing restored the ENCORE. Features of construction of internal structures and programming ENCORE PPZU allow applying them the following technique which essence is considered on an example 556RT5.

The principal cause of the smooth crosspieces overgrowing in PPZU after programming is diffusion, accelerated at ETT in temperature and an electric field. If in a "reading" mode to submit exceeding pulses on the trunk of a feed 5B (duration of pulses is compared to duration of pulses of programming and frequency of their submission is determined by the diagram of conditions) the percent of crosspieces overgrowing considerably decreases. These ways of the accelerated tests are introduced in NIZEVT, NPO "Cascade", and MNIIPA. For ways of the accelerated tests MOS IC and bipolar PPZU it is received two copyright certificates.

It is possible to draw the following conclusions:

1) The accelerated tests 565РУ1 allow to assert, that under certain conditions ETT it is possible to speed up rejection of potentially unreliable IC;

2) Selection of temperature of the accelerated tests and exceeding pressure should be carried out in view of manufacturing techniques, design features and functioning IC;

3) Failure IC at the accelerated tests is connected, basically, with breakdown of poor made oxide.

IV. CONCLUSIONS

1. Gamma irradiation can be used for rejection of potentially defective CMOS IC with the help such sensitive parameters as a current of consumption, a target current of a high level, etc.

2. As for restoration of parameters after gamma irradiation it is necessary to use the annealing at temperature 350^0C for reduction of the formed volumetric and superficial defects and as this temperature promotes formation of inter-metallic compounds it is better to carry out rejection on plates. Besides, rejection CJ on plates allows saving a significant amount of cases.

3. The use of gamma irradiations for rejection of potentially defective crystals on plates is economically justified and does not worsen reliability CJ the ambassador annealing plates.

4. Forced tests CJ (with the help of rise in temperature and submission of an exceeding pulse pressure) can be used as a method of the accelerated rejection of potentially defective CJ, and, time of tests in comparison with ETT is reduced till 2-8 o'clock.

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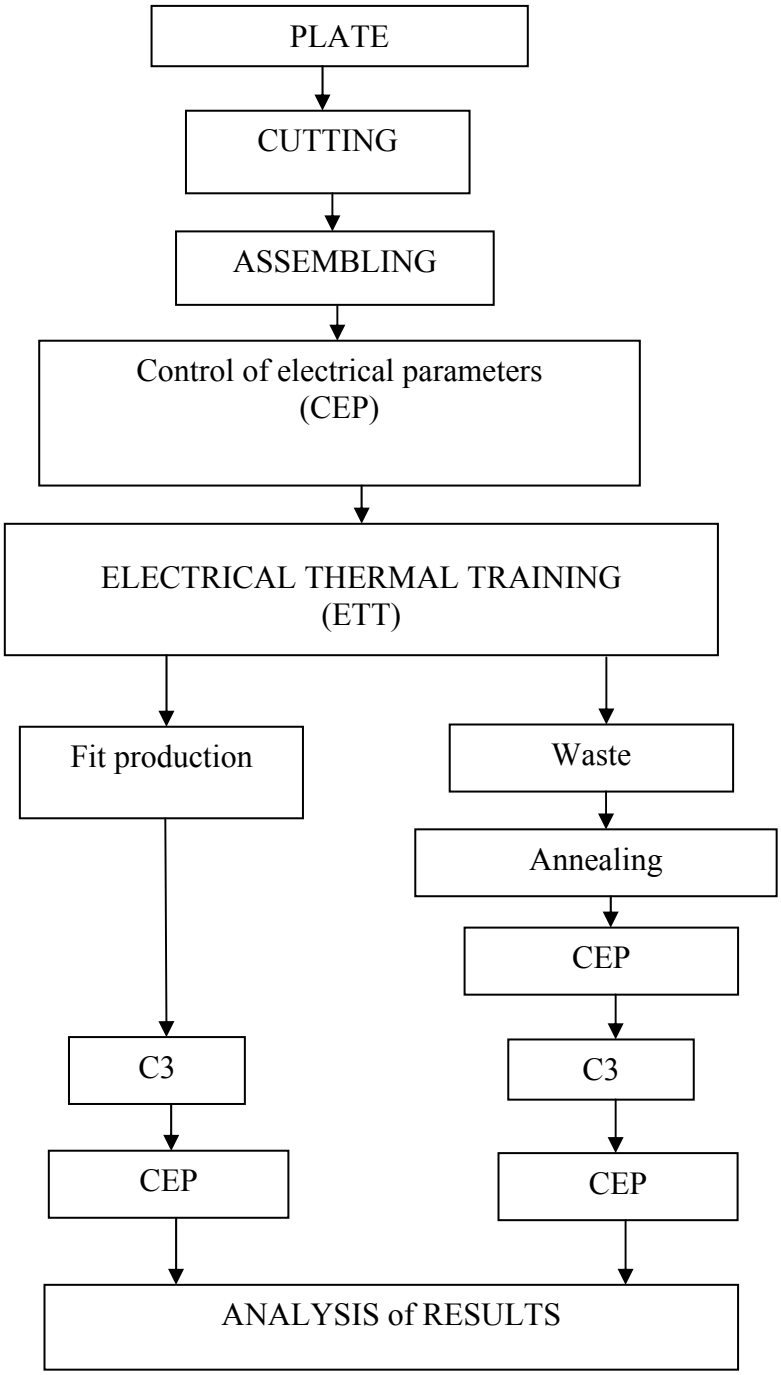

Fig 1. Algorithm of carrying out of research on influence of an irradiation on electro parameters IC.

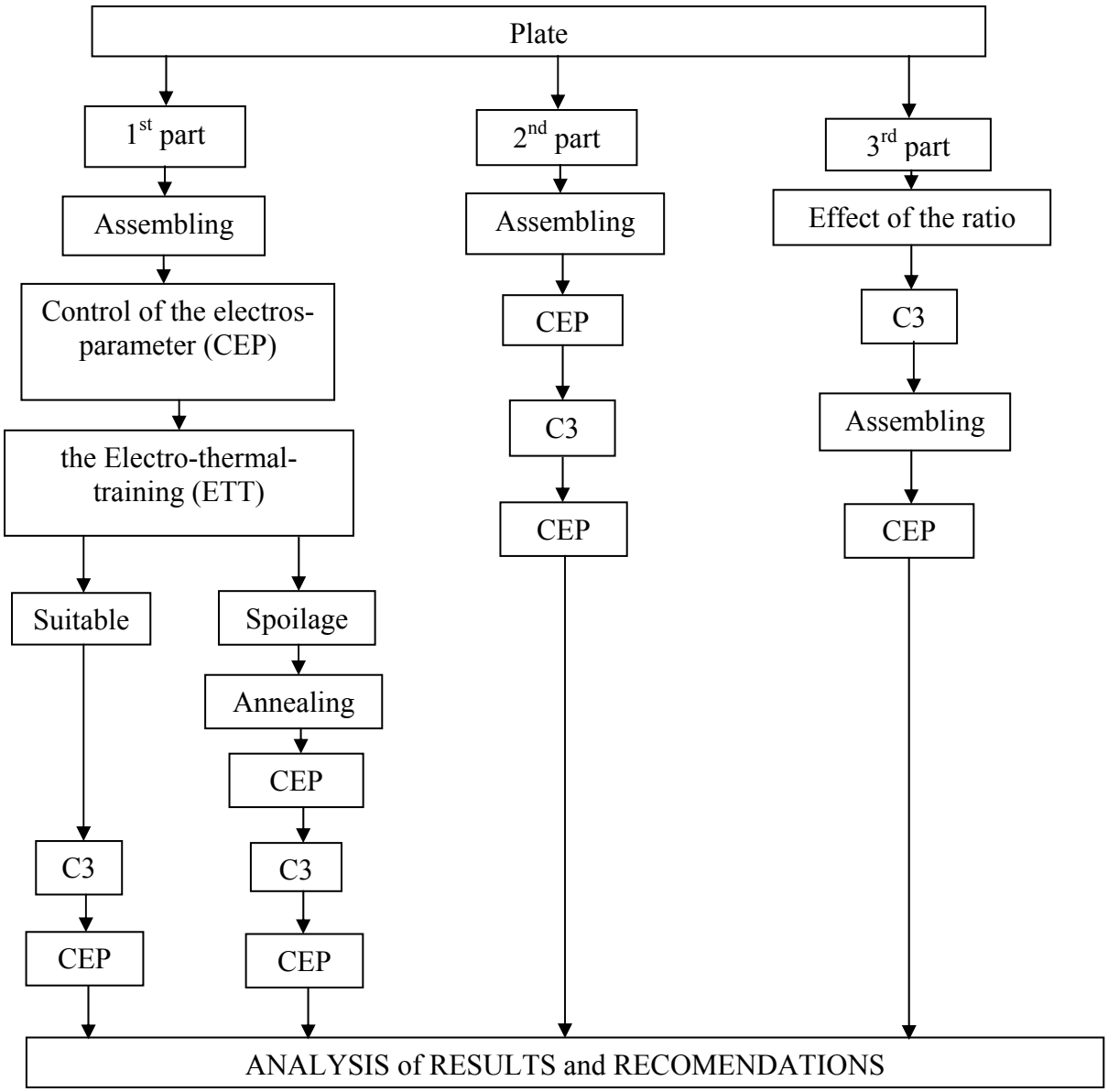

Fig. 2. Algorithm of carrying out of the comparative researches IC made of one plate

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Superior-Order Curvature-Corrected Voltage Reference with Improved Performance

Cosmin Popa, Anca Manolescu, Anton Manolescu[1]

Abstract - A new curvature-correction technique for improving the temperature behavior of a CMOS voltage reference will be presented. The reducing of the temperature coefficient for the reference voltage will be realized compensating the nonlinear temperature dependence of the gate-source voltage for a MOS transistor working in weak inversion with the difference between two gate-source voltages. These MOS transistors are polarized at drain currents with different temperature dependencies ($PTAT$ and $PTAT^{\alpha}$, respectively), α parameter being selected to the optimal value for the implementing technology. The $PTAT$ voltage generator will be designed using an original Offset Voltage Follower block, with the advantage that matched resistors are replaced by matched transistors and, in consequence, with a relatively smaller degradation of the circuit temperature behavior caused by devices' mismatches. SPICE simulation reports $TC = 1.95\,ppm/K$ for an extended temperature range, $273K < T < 363K$, without considering the parameters spread.

Keywords: Offset Voltage Follower block, subthreshold operation, superior-order curvature-correction technique, temperature coefficient

I. INTRODUCTION

The voltage reference represents a very important stage in applications such as A/D and D/A converters, data acquisition systems, memories or smart sensors.

There are two important classes of voltage references. The first class includes low-voltage low-power voltage references, with medium performances, but with the main goal of a very small minimal supply voltage and supply current. The second class is focusing to the high performances voltage references, which are mainly characterized by a very small value of the temperature coefficient for a relatively large temperature range, with the price of increasing the minimal required supply voltage, current consumption and complexity.

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Because of the superior performance of bipolar references with respect to the circuits using MOS transistors, the first approaches of high-performance voltage reference were implemented in bipolar technology.

However, due to the nonlinear temperature dependence of the base-emitter voltage [1], there exists a theoretical limit for improving the temperature stability of a simple BGR. Basic bandgap references, with a temperature coefficient of about hundred ppm/K, useful only for applications that do not require a very good accuracy of the reference voltage, have been extensively presented in literature. In order to improve the temperature behavior of the bandgap reference, a lot of curvature-correction techniques have been developed.

The first group of these techniques is based on the correction of the nonlinear temperature dependence of the base-emitter voltage by a suitable polarization of the bipolar transistor. A polarization at a $PTAT^3$ + $PTAT^4$ collector current was proposed in [1], allowing a simulated temperature coefficient in the range of $4-8\,ppm/K$. The curvature-correction technique from [2], based on the polarization of the bipolar transistor at a $PTAT^n$ current, reports a TC about $20\,ppm/K$ without trimming and thermal stabilization of the chip.

The second possibility to improve the temperature dependence of a BGR is to compensate the nonlinear temperature characteristic of the base-emitter voltage by a correction voltage, which is added to the basic reference voltage [3], or by a correction current added to the PTAT current [4], [5]. The reference voltage presented in [3] has a relatively large temperature coefficient, about $30\,ppm/K$ for a limited temperature range, due to the MOS parameters mismatches. The compensation technique based on the correction current decreases the temperature dependence under $10\,ppm/K$, but it has the disadvantages of a large silicon occupied area and of the incompatibility with CMOS processes.

In CMOS bandgap references that are still using bipolar transistors, the required bipolar devices are realized as parasitic vertical or lateral transistors,

available in CMOS technology. The result will be a small degradation of the temperature behavior of the circuit due to the poorer match of MOS devices' parameters with respect to those of bipolar transistors.

Another approaches of CMOS references, using exclusively MOS devices and (or without) resistors implements the *CTAT* (ComplemenTary with Absolute Temperature) voltage reference using a threshold voltage extractor circuit, which generates at its output the MOS device threshold voltage, with a negative linear temperature dependence. The disadvantage of this class of CMOS references is that the exact temperature dependence of V_T is not so simple to estimate, so a curvature correction technique for improving its thermal behavior is relatively difficult to design.

The proposed realization of a CMOS voltage reference uses a gate-source voltage of a MOS transistor working in weak inversion as *CTAT* voltage generator. The negative linear dependent term from $V_{GS}(T)$ expression will be compensated by a complementary term implemented using an *OVF* (Offset Voltage Follower) block. The new curvature-correction technique is based on the compensation of the nonlinear temperature dependence of the gate-source voltage by using the difference between two gate-source voltages for MOS transistors with different temperature dependencies of theirs drain currents (*PTAT* and $PTAT^{\alpha}$, respectively), α being a constant parameter that will be further analyzed.

II. THEORETICAL ANALYSIS

A. The temperature dependence of the gate-source voltage

Similarly with the bipolar approach, the gate-source voltage represents the simplest implementation in CMOS technology of a *CTAT* voltage with the great advantage of a very good controllability through the temperature dependence of the operating drain current.

Considering a subthreshold operation of the MOS transistor, the temperature dependence of the gate-source voltage could be expressed as:

$$V_{GS}(T) = V_{FB} + E_G + \frac{V_{GS}(T_0) - V_{FB} - E_G}{T_0} T + \\ + \frac{nkT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_0} \qquad (1)$$

where T_0 is the reference temperature, γ is a technological constant and α models the temperature dependence of the drain current that biases the MOS device (it was supposed that $I_D(T) = ct.T^{\alpha}$). The first term is a constant term, the second one is a linear term, which will be compensated by a complementary linear voltage summed with the gate-source voltage and the last term models the nonlinearity of the gate-source voltage temperature dependence. This term will be compensated by a suitable logarithmic dependent on temperature term, also added to $V_{GS}(T)$.

B. The superior-order curvature-corrected voltage reference

The gate-source voltage (1) represents the zero-order compensated reference voltage. Its temperature dependence is primarily represented by the linear term, which will be cancel out (the first-order compensation) using an *OVF* (Offset Voltage Follower) block, having two important advantages: an improved accuracy achieved by replacing matched resistors by matched MOS transistors and a reduced silicon occupied area obtained by removing any resistor from the circuit. In order to remove the additional superior-order errors introduced by the last logarithmical term from (1), a curvature-correction technique will be implemented.

The superior-order curvature-corrected voltage reference is presented in Fig. 1.

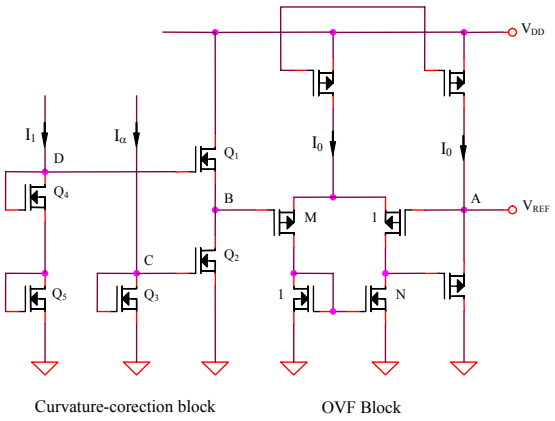

Fig. 1. The superior-order curvature-corrected voltage reference

The temperature dependence of the gate-source voltage for a MOS transistor in weak inversion is strongly increased by the linear temperature dependent term from relation (1). In order to cancel it, an original technique for implementing a complementary *PTAT* voltage will be presented, using an *OVF* (Offset Voltage Follower) block [6]. The output voltage of the *OVF* block is $V_{AB} = nV_t \ln(MN)$. For a proper choice of the aspect ratios M and N, the linear dependent term from expression (1) will be cancel out by the complementary *PTAT* voltage V_{AB}, resulting the first-order compensated reference voltage expression:

$$V_{GS}(T) = V_{FB} + E_G + \frac{nkT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_0} \qquad (2)$$

Because of the nonlinear temperature dependence (2) of the gate-source voltage for a MOS transistor working in weak inversion, the original idea is to obtain a correction term having a temperature dependence complementary to the logarithmic dependent on temperature term from (1). This correction term, summed with the zero-order compensated voltage reference (1), is represented in Fig. 1 by V_B potential and it will be obtained by subtracting a gate-source voltage (V_{GS_3}) from two summed gate-source voltages (V_{GS_4} and V_{GS_5}). The resulting expression of the reference voltage (after first- and superior-order compensations) will be:

$$V_{REF}^{(SUP)} = V_{AB} + V_B = E_G + V_{FB} + \frac{nKT}{q}(\gamma - \alpha)\ln\frac{T}{T_0} \quad (3)$$

In conclusion, the linear term from the expression of the gate-source voltage temperature dependence has been cancel out by using an OVF block, while the logarithmic dependent on temperature term from (1) could be minimized for $\alpha \cong \gamma$. The constant γ is a technological parameter, strongly dependent on the current technology. The original idea for reducing the circuit temperature dependence by minimizing the logarithmical term from (3) is to design a circuit that must be able to compute the proper value of α for the current used technology. The core of the circuit that generates a current having a $PTAT^{\alpha}$ temperature dependence (α value being optimally selected in a fixed range) is represented by a current-mode squaring circuit which must compute the function $I_B = I_C^2 / I_A$. Choosing $I_C = I_1$ (with a $PTAT$ variation) and $I_A = I_O$ (in a first-order approximation, independent on temperature), it results an output current I_B proportional to the square of the absolute temperature. For obtaining a $PTAT^3$ output current, another identical squaring circuit will be used, having $I_C = I_B^{(O)}$ and $I_A = I_1$. In the same manner, $I_B^{(n)}$ current will be $PTAT^{n+2}$, $I_B^{(I)} = I_1^3 / I_O^2$. In conclusion, all the possible integer values for the exponent α of the absolute temperature in the output current dependence have been obtained. In the following lines, the method for obtaining the non-integer values of the same exponent will be presented. For example, in order to obtain 0.5 value of the exponent, relation (6) will be used, choosing $I_A = I_1$ and $I_B = I_O$. For 0.25, $I_A = \sqrt{I_1 I_O}$ and $I_B = I_O$.

The total value of the exponent is obtained by multiplying the proper partials currents, resulting the desired value of parameter α.

III. SIMULATED RESULTS

The curvature-corrected voltage reference was implemented in $0.35\mu m$ CMOS technology. The SPICE simulation $V_{REF}(T)$ based on previous mentioned technology parameters is presented in Fig. 2.

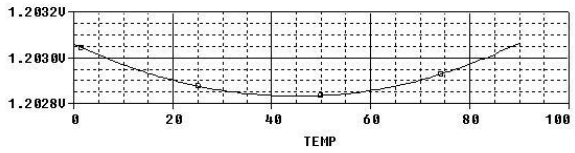

Fig. 2. SPICE simulation $V_{REF}(t)$ for the curvature-corrected voltage reference

The supply voltage is $V_{DD} = 2.5V$. The most important MOS parameters used in the previous simulation are: $V_{T_n} = 0.4V$, $V_{T_p} = -0.5V$. The simulated temperature coefficient of the reference voltage is $TC = 1.95\,ppm/^o C$ for an extended temperature range, $0 < t < 90^o C$. For sub micron processes, channel-length modulation effect will affect the bandgap reference performances, imposing the use of cascode current mirrors (having the disadvantage of increasing the minimal supply voltage of the circuit).

IV. CONCLUSIONS

A new curvature-correction technique for improving the temperature behavior of a CMOS voltage reference has been presented. The reducing of the temperature coefficient for the reference voltage has been realized compensating the nonlinear temperature dependence of the gate-source voltage for a MOS transistor working in weak inversion with the difference between two gate-source voltages. These MOS transistors were polarized at drain currents with different temperature dependencies ($PTAT$ and $PTAT^{\alpha}$, respectively), α parameter being selected to the optimal value for the implementing technology. The $PTAT$ voltage generator has been designed using an original Offset Voltage Follower block, with the advantage that matched resistors are replaced by matched transistors and, in consequence, with a relatively smaller degradation of the circuit temperature behavior caused by devices' mismatches. SPICE simulation reports $TC = 1.95\,ppm/K$ for an extended temperature range, $273K < T < 363K$, without considering the parameters spread.

ACKNOWLEDGEMENT

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SVM Classifier using LUT-based RAM on a Spartan 3 FPGA

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Abstract – Support Vector Machines are widely used in pattern recognition, being the newest achievements in neural network structures. This paper presents an implementation example of an SVM classification function using a Spartan3 FPGA device. A Block Ram based implementation is compared versus a distributed LUT-based RAM one. Aspects regarding memory geometry and instantiation are presented. The number of required clock periods and the maximum clock frequency is calculated and a speed comparison of the implemented system with software running on a PC targeting the same application is also made
Keywords: SVM, Block RAM, LUT-based RAM, FPGA

I. INTRODUCTION

Support Vector Machines (SVM) are considered to be the newest achievements on neural network structures [1]. In Chapter 2, the basic idea of the SVM is presented and their advantages are highlighted. Chapter 3 presents an application example for classification of the Ibermatica database images. The role of the classification function is to decide whether a particular image is face- or non-face image. The major advantage offered by an FPGA device, the possibility to implement parallel structures is used in the system implementation. An implementation example of the kernel function using Block RAM components follows. Chapter IV presents the implemented system that is based on distributed RAM cells also called LUT (LookUp Table) RAM cells, to tackle the drawbacks that come with the Block RAM based implementation. Approximations made in order to reduce the data bus widths are also presented. The total number of clock cycles required for the classification function to perform its operations is calculated and the maximum clock frequency is determined. Finally, a comparison between the speed of the system implemented on the FPGA and the speed of a classification software running on a PC is also presented.

II. SUPPORT VECTOR MACHINES

In the nineties, the neural networks knew a very significant importance in the scientific and engineering domains. Industrial products are offered today on the market with a real success even if we do not have the associated physical model for diagnosis. It is necessary to consider the neural networks as a manner of building an empirical model with what that supposes of inaccuracy and risk for the application. The theory of the statistical learning became more interesting with new results in generalization and with the proposal of the SVM model. The model is the most recent proposition on neural network structures [1]. This model is founded on the statistical learning Theory. The Support Vector Machine model consists of a transformation of the input vectors X in a space of higher dimension Z through a nonlinear transformation, selected a priori. It is in this new space Z that we can build an optimal hyperplane [2]. For the particular case of pattern recognition, the SVM make a distinction of two classes by finding a decision surface constructed from certain points of the entire learning database, called Support Vectors A second important idea of Support Vector Machines is the use of kernel functions. The kernel functions were proposed to be able to build nonlinear algorithms from linear algorithms by calculating the inner product not in the input space but in the feature space. By using kernels it can be taken into account the statistics of greater order without a combinatorial explosion of the complexity than it would have met even for moderate values of examples and the dimension of the kernel function. The most used kernel functions are the polynomial, sigmoid (neural network) and the Radial basis function.

II.1. The Support Vectors

Vapnik [2]. proposes a representation of a SVM in the form of one hidden layer neural network whose number of cells is equal to the number of "support vectors", and not to the dimension of the space of the internal representations, as we could have supposed it initially. In this manner the number of neurons is obtained in an automatic way with the resolution of a quadratic problem. The support vectors are the input vectors *xi* for which equality $y_i((w_0x_i+b_0)=1$ holds. Concretely, they are the closest points to the optimal

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hyper plane. For all the other examples, there is thus a factor α=0 that eliminates them from the solution. We thus know that the decision function is calculated from the examples that are on the margin, presented in figure 1. In the non-linear case, it is enough to replace the scalar products $(x \times x_i)$ by kernels $k(x, x_i)$.

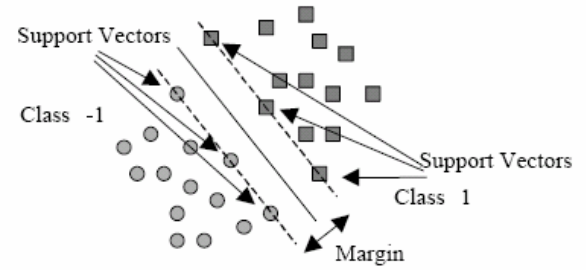


Fig. 1. The support vectors are the closest vectors to the optimal hyperplane [1].

II.1. The Polynomial Kernel

There are three options for the selection of the kernel function of the SVM method: Polynomial, RBF or sigmoid Neural networks [1]. The Sigmoid Neural network kernel function option was rejected because of the difficulty of a possible hardware implementation. Moreover in the literature the performances obtained with this kernel function were lower than those obtained with the two others.
The following is the general equation of the SVM decision function for classification:

$$f(x, \alpha) = \text{sign}\left(\sum_{\text{Support Vectors}} y_i \alpha_i K(x_i, x) + b \right) \quad (1)$$

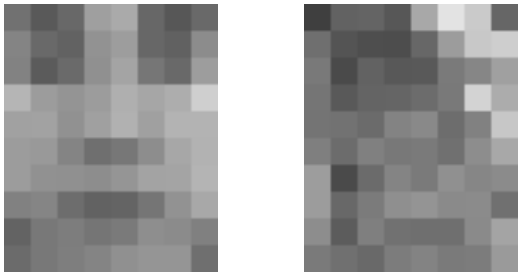
Where:
y_i $a_i = w_i$, are the networks weights,
X_i, are the support vectors of the solution,
b, is the threshold of the function, and
$K(X, X_i)$.is the kernel function.
As it can be seen, the solution is the sign of the addition, so this is the generalization function for two-class's classification. In our case, the kernel function is then the polynomial function of degree d:

$$K(X, X_i) = (X^T \cdot X_i + c)^d \quad (2)$$

III. IMPLEMENTATION EXAMPLE

III.1. The classification function parameters

Our objective is to implement a classification function for the image database provided by Ibermatica [3]. The database is composed of 8X10 pixel resolution 8-bit grayscale images. The classification problem for the SVM is to decide whether or not the image is representing a human face. Figure 2. a) shows a positive example and figure 2. b) a negative example from the Ibermatica database training set.



a.) b)

Fig. 2. Example images from the Ibermatica image database a) positive (face image) example b) negative (non-face image) example

Training was done for the SVM on 112 images from the image set. The SVM parameters were:

- Degree of the kernel function d=2;
- Constant c=1
- Threshold value b=1.5215772
- Number of support vectors: 17
- Feature index i.e. image size: 80

The implementation is done on a SPARTAN 3 XC3S200 device, due to its availability on the Digilent S3 development boards.

III.2. Spartan-3 Block RAM implementation considerations

According to the specifications above, the data size required to store the image to be classified and the support vectors is

$$17 \times 80 \times 8 + 80 \times 8 = 11520 \text{ bits} = 11.25 \text{ Kbits} \quad (3)$$

This amount of data can be easily fit into the considered device [4]. Moreover, the Spartan-3 device features twelve 18-Kbit dual-port RAM memories, also called Block RAM (BRAM) memories. Results that a single BRAM is sufficient to fit the amount of data considered. However, in this case the whole data is processed sequentially and the number of clock cycles required to implement one kernel function is 80. This is multiplied by the number of support vectors and some extra clocks are added for pipelining purposes.
The required number of clock cycles can be significantly reduced if the advantage of an FPGA implementation, the possibility of parallel processing is used wherever is possible.
Basically, the classification function operations consist in a set of multiplication and summing-accumulate, i.e. MAC operations. The embedded 18-bit multipliers will be used for implementing the kernel function. For the weighting operation, a multiplier larger than of 18 bits will be needed due to the increase of the data bus width as result of the multiplication-summing procedure in the kernel function. A number of 10 multipliers will be considered to work in parallel for implementing the kernel function. The number of ten was chosen because the image size considered is dividable with

10, in fact, most of the image sizes feature this property, making the application easily adaptable to different image sizes.

Therefore the values of the X image and the X_i support vectors are distributed in ten RAM blocks; each block basically stores eight pixels of the X image and the corresponding 17X8=136 pixels of the X_i support vectors. The RAM blocks can be configured into various geometries [5]. For the specified application, the geometry chosen for the BRAm-s is of 1KX16 bits. The X pixels are stored in the upper and the X_i pixels in the lower byte of the memory. Basically only 136 locations are used in each memory block from the available 1024. Assuming a number of 17 support vectors, the system configured in this way supports an image size of 600 pixels, with any aspect ratio.

Fig. 3 shows the block schematic of the kernel function implemented with Block RAM components and Table 1 shows an example for the placement of the X() image data and the X_i() support vector data in the BRAM-s, i.e. a memory map example. Obviously, the data can be placed in various ways into the memory until the placement is uniformly distributed and the stored X() image data corresponds with the X_i() support vector data stored at the same locations.

Each block memory contains eight pixels of the analyzed image, repeated the number of support vector times. Due to this redundancy the memory map is inefficiently organized, however this placement of the data insures one multiplication at each clock cycle, therefore the kernel function is able to perform its operations for one support vector in a total number of 8 clock cycles.

Table 1. BRAM memory map example

Addr.	BRAM0		BRAM1			BRAM9	
	[15:8]	[7:0]	[15:8]	[7:0]		[15:8]	[7:0]
000	X(0)	X_1(0)	X(8)	X_1(8)	.	X(72)	X_1(72)
001	X(1)	X_1(1)	X(9)	X_1(9)	.	X(73)	X_1(73)
.	.	.	.	.	.	.	.
007	X(7)	X_1(7)	X(15)	X_1(15)	.	X(79)	X_1(79)
008	X(0)	X_2(0)	X(8)	X_2(8)	.	X(72)	X_2(72)
009	X(1)	X_2(1)	X(9)	X_2(9)	.	X(73)	X_2(73)
.	.	.	.	.	.	.	.
00F	X(7)	X_2(7)	X(15)	X_2(15)	.	X(79)	X_2(79)
.	.	.	.	.	.	.	.
086	X(6)	X_{17}(6)	X(14)	X_{17}(14)	.	X(78)	X_{17}(78)
087	X(7)	X_{17}(7)	X(15)	X_{17}(15)	.	X(79)	X_{17}(79)
088	0	0	0	0	.	0	0
.	.	.	.	.	.	.	.

The summing and accumulating circuit performs the unsigned sum of ten 8-bit numbers. Two-input 8-bit adders were used on more levels to add all the ten numbers, therefore the required number of the adders is 5 on the first level, 2 on the second level and 1 on the third and fourth levels. The multiplier outputs and each summing level outputs are registered for pipeline considerations. Results that the total number of required clock cycles to perform the kernel function operations, for all of the support vectors increases with 6, becoming

$$17 \times 8 + 6 = 142 \text{ clock cycles} \qquad (4)$$

Because the image data has to be repeated in the BRAM blocks, results that loading a new image into the memory implies sweeping the whole used memory

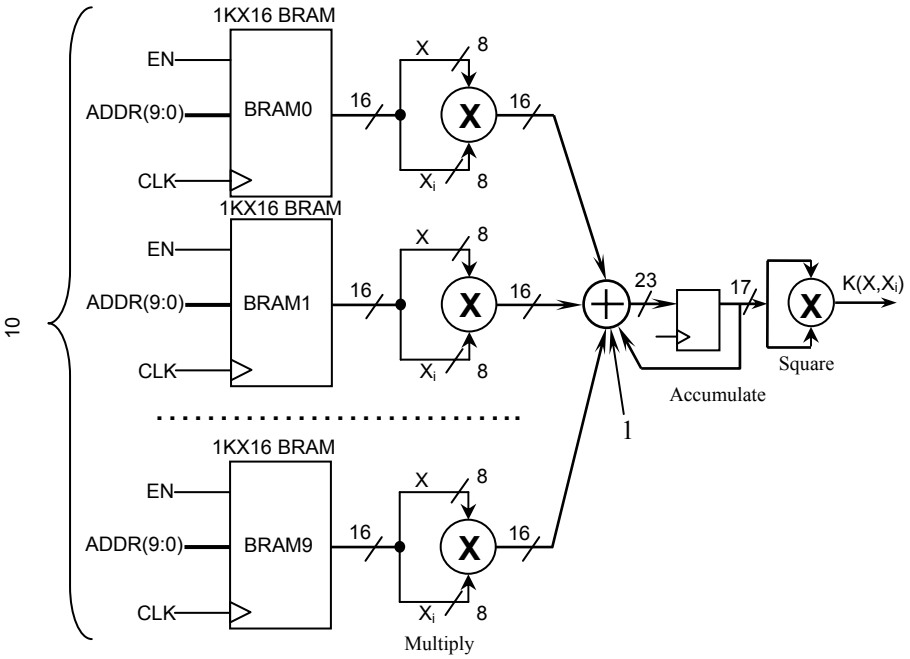


Fig. 3. Block schematic of the kernel function implemented with Block RAM

address space, i.e. loading a new image would take a minimum of 17X8=136 clock cycles, assuming that the ten RAM blocks are loaded simultaneously.
Loading the BRAM memories with new data is eased by the fact that the Xilinx Block RAM components are true dual-port memories, allowing simultaneous read and write from two different ports. The only restriction is applied to the fact that the same memory location cannot be accessed simultaneously from both ports. The dual-port RAM facility allows loading the new image on the second access port while the first one is used for the kernel function operations. In order to avoid address conflict, data loading starts with one clock cycle earlier i.e. memory write is performed on the current memory address-1. Taking into account that the support vector data i.e. the lower byte in each memory is not changing when a new image is loaded, the lower byte is buffered and reloaded in the memory with the new image data. The incoming image data is also buffered and formatted in the remaining two BRAM components. The image data loading system is not shown in fig. 3. due to the lack of space.
Taking into account that the kernel function multiplies and accumulates unsigned data, the maximum possible result from the MAC operations of the kernel function i.e. the maximum number at the output of the accumulator can be

$$255 \cdot 255 \cdot 10 \cdot 8 + 1 = 5{,}202{,}001 \qquad (5)$$

The number above can be represented on 23 bits. However, only the most significant 17 bits will be taken into account as the result of the kernel function, to be able to use the remaining embedded multiplier that accepts up to 18-bit signed or 17-bit unsigned operands. It means that the kernel function is scaled with

$$K(X, X_i) = \left(\frac{X^T \cdot X_i + 1}{2^5} \right)^2 = \frac{\left(X^T \cdot X_i + 1 \right)^2}{1024} \qquad (6)$$

Other scaling operations will result from the weighting and summing operations that follow the kernel function in the classifier implementation.

IV. LUT-BASED RAM IMPLEMENTATION

IV.1. Distributed memory considerations

Although the BRAM-based implementation offers operation at a high-speed by reducing the number of the clock cycles required to calculate the kernel function result, it suffers from significant drawbacks.
First, the incoming image data has to be buffered and formatted to be distributed across the BRAM components. The data formatting and RAM loading circuit takes significant resources from the FPGA. Second, the SVM classifier based on BRAM-s cannot be implemented in an embedded system together with the Xilinx proprietary MicroBlaze or PowerPc soft processor systems, because these systems use primary the BRAM-s for processor data and code memory purposes, making these components partially or completely unavailable for custom design.
In order to overcome to the incoming data formatting and distributing problem, a system with distributed memory cells was considered, that can be implemented by the Xilinx Distributed RAM (also called LUT RAM) feature

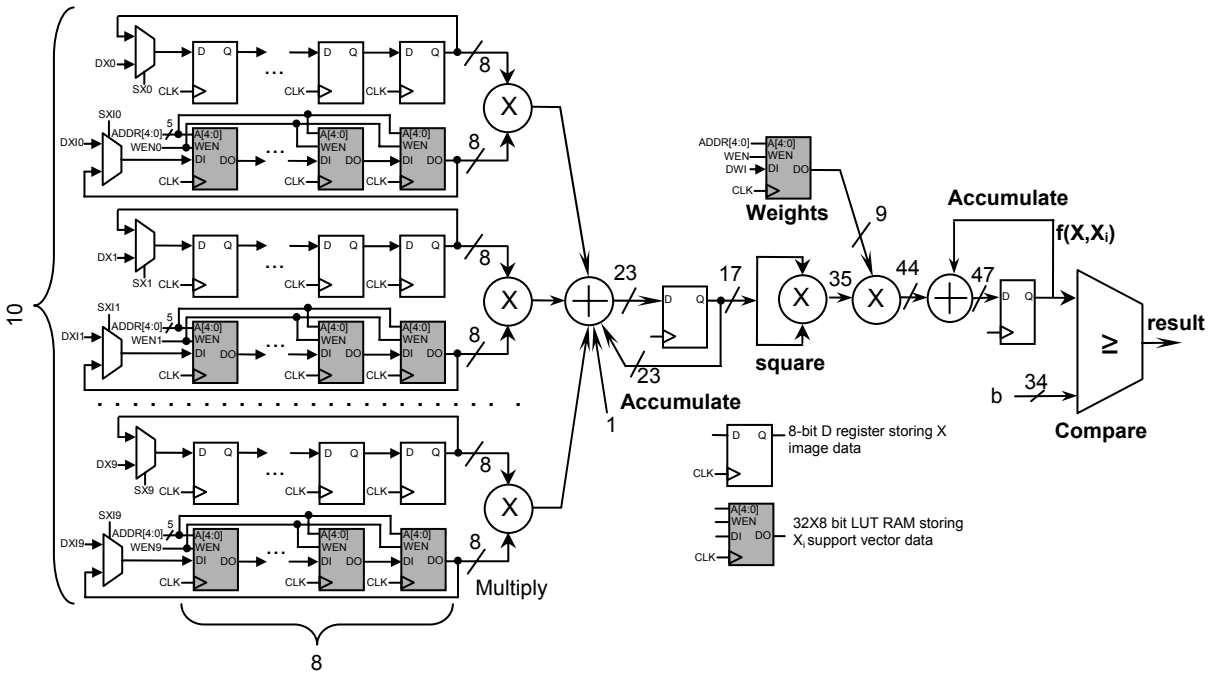


Fig. 4. Block schematic of the SVM classification function implemented with LUT RAM blocks

The LUT memory cells are built on the Configurable Logic Block (CLB) logic function generator circuits, also called Lookup Tables. In the Spartan 3 FPGA structure, one CLB consists of four slices from which two of the slices contain two 4-bit lookup tables that can be configured as dual-port or single-port RAM memories. Therefore one CLB can have up to 32 bits of dual-port memory or 64 bits of single-port memory. Results that one 32X1 bit size distributed RAM fits in a single CLB slice.

Figure 4 presents the block schematic of the implemented SVM classifier function. The system is an improved version of the SVM classifier presented in [7], where D registers were considered to store both the image and support vector data. Due to the fact that in that case the number of the D registers used is too large, taking most of the FPGA D flip-flops, the support vector data is stored in the LUT RAM blocks while the image data is stored in the adjacent D flip-flops.

The left part of Fig. 4 until the squaring circuit represents the implementation of the kernel function. The white cells are representing the D registers storing the X image data, while the gray cells the LUT RAM blocks storing the X_i support vectors. The implementation is similar to the one presented in Fig. 3 regarding the number of parallel multiplications and the way the first accumulator circuit is organized. Both the X input vector and the X_i support vector memories are organized in a circular FIFO memory matrix with a size of 10X8, resulting a number of 80X8 cells placed in the FPGA.

To store the X_i data, the distributed memory cells are organized in 32X8 bit size, allowing storage of up to 32 support vectors. A specific LUT RAM cell stores the data from the support vectors according to the expression

$$\mathrm{MEM_I}\left(\mathrm{ADDR}\right)=\mathrm{X_{ADDR[4:0]}}\left(\mathrm{I}\right) \tag{7}$$

where I is the index of the memory cell and ADDR represents the 5 bit address of the memory. Therefore the addresses of all the memory cells are connected together, creating a multiple page memory, each page containing one support vector.

Due to the circular structure of the X and X_i memories, at every 8 clock periods the memory content will be reloaded to its initial value and the address is incremented. Correspondingly, the output summing and accumulating circuit advances with one clock.

The SX0...SX9 and SXI0…SXI9 selector signals allow loading of new image and support vector data through the DX0...DX9 and the DXI0…DXI9 data lines, respectively. Formatting and loading a new image data is significantly simpler comparing to the BRAM implementation. For example, the DX0…DX9 data lines can be connected together and the SX0…9 selector lines decide which row will be loaded with the new image data. In the case of using a high-speed I/O peripheral, data can be loaded in parallel in the ten rows when the last support vector product is calculated. In the same way, a new support vector data can be loaded into the distributed RAM cells through the DXI0...9 data lines, controlled by WEN0...9 write enable lines or from the SXI0…9 selector lines.

The ADDR lines also select the corresponding weight of the support vector from the weight memory, built as well on LUT RAM cells, organized in a 32X9 bit format, with the following considerations: Initially the weights were in floating point format. Due to the fact that floating point operations would require too wide data buses and considerably more computing time, obviously were be transformed into fixed point format. The smallest weight of the support vectors for the application considered in this paper has the absolute value of

$$y_{16}\cdot\alpha_{16}=9.7740856\text{e-}014 \tag{8}$$

Note that only several decimal places were shown. The highest value of the weights, in absolute value, is

$$y_7\cdot\alpha_7=2.006978\text{e-}011=205.3\cdot y_{16}\cdot\alpha_{16} \tag{9}$$

If $y_{16}\cdot\alpha_{16}$ is normalized i.e. scaled to 1, then all of the weights can be represented on 9 bits with sign, meaning that all of the weights will be scaled with $\frac{1}{y_{16}\cdot\alpha_{16}}$. In order to avoid an unattended change of the classification function sign from equation (1), results that the threshold *b* has to be also scaled. Taking into account from relation (6) that the kernel function is also scaled, equation (1) will become

$$\mathrm{f(x,}\ \alpha)=\mathrm{sign}\left(\sum_{i=0}^{16}\mathrm{y_i}\alpha_\mathrm{i}\mathrm{K}\ (\mathrm{X_i},\mathrm{X})+b\right)\frac{1.023\text{e+}13}{1024} \tag{10}$$

Thus, the *b* threshold becomes 1.52026e+10. This value can be represented on 34 bits, from there results the bus width for the threshold *b*.

The weighting multiplier has the size of 35X9 bits, where the 9 bits are signed, being wider than the 18 bit embedded multipliers, resulting that it has to be implemented by the FPGA lookup table logic.

IV.1. Distributed memory implementation and speed considerations

Xilinx ISE provides behavioral VHDL templates that can be used to instruct the synthesis tool to extract block RAM or distributed RAM from the code. Although the block schematic in Fig. 4 can be easily described in behavioral VHDL, it was found that by describing the circular multiple-page memory from Fig. 4 in behavioral, the XST (Xilinx Synthesis Tool)

will extract D flip-flops for the memory cells together with decoding logic rather than distributed RAM cells. This behavior occurs due to the fact that the synthesizer will understand to extract shift registers on 8 bits that are basically implemented with flip-flops.

Results that for implementing the kernel memory part of the system in Fig. 4., a structural VHDL or schematic approach has to be used. The distributed RAM cells were built on RAM32X8S components in the Xilinx ISE software. The RAM32X8S represents a 32X8 bit single-port distributed RAM. The X memory cells were built on FD8CER components, representing an 8-bit D register with count-enable and asynchronous clear ports. The memory loading and controlling state-machine and the multiply-accumulate circuit were described in behavioral VHDL.

Due to the similarity of the structures between the BRAM and LUT-RAM implementations, the number of clock periods required for all of the kernel function operations is the same, i.e. 142. Four extra clock periods are needed for the squaring and weighting-accumulating operations. Results a total number of 146 clock periods for the classification function operations.

The embedded multipliers are placed close to the BRAM cells in the FPGA structure, resulting lower propagation times for the BRAM implementation than for the LUT-RAM one. However, the highest clock frequency is rather limited by the propagation times of the combinational arithmetic circuits, i.e. the embedded multipliers and the unsigned adders.

The synthesis tool reported a maximum propagation time of 4.828 ns, meaning a maximum clock frequency of 207.1 MHz. For safety purposes, half of this frequency was used. Note that the squaring and the weighting multipliers, and the final accumulator have to operate at only every eight kernel memory cock periods, allowing operations at lower frequency. A quarter of the kernel memory frequency was chosen, i.e. 25MHz. In this case, without taking into account the time needed for I/O operation, i.e. data download and memory load, the total time will be

$$T = 142 \cdot \frac{1}{100MHz} + 4 \cdot \frac{1}{25MHz} = 1.58\mu S \quad (11)$$

Due to the introduction of pipelining in the kernel function operations, the time was improved versus [7]. Comparing to the expression (11), the time spend for classification of 442 images on a Pentium IV, 1.2 GHZ PC, without taking into account the time for I/O operations, was 0.02 seconds, resulting 45.2μS per image. Obviously, for larger images the time spent for the classification function implemented on the FPGA board increases due to the window sweeping technique that has to be used.

Data downloading was made through the serial interface of the S3 board. An USB connection with the PC is under development.

V. CONCLUSIONS

In this paper an example of implementation for an SVM classification function on a Spartan 3 XS3S200 FPGA device was presented. The example is made for the Ibermatica 8X10 pixel face image database. The proposed system takes the advantage of parallel circuits offered by an FPGA implementation.

Two approaches were considered to implement the kernel function, the first one based on Block RAM memory components included in the Xilinx Spartan devices, and the second one based on distributed i.e. LUT RAM memory cells. Although the Block RAM implementation is more compact and simpler, the memory content loading can represent a difficult operation. On the other hand, the BRAM based implementation cannot be made if the SVM classifier is intended to be included in an embedded system with MicroBlaze or PowerPc soft processors that use the Block RAM as primary processor memory. The solution to these problems is offered by the distributed RAM implementation, where data loading can be easily done.

Using the parallel data processing feature offered by the FPGA devices, the required number of clock periods reduces drastically. To keep the maximum clock frequency at a high level, pipelining was used for the arithmetic operation implementations. The implemented system was performing the operations more than ten times faster than a similar software application running on a PC, with the same SVM and the same images.

In the case of larger images, a window sweeping technique has to be used that increases the computation time. Using a higher density FPGA device, the number of parallel circuits can be further increased to compensate the increase of the execution time.

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TCP Identification of contactless measurement systems

Philipp Roebrock[1]

Abstract - This paper describes an algorithm to determine the robot tool transformation and tool center point (TCP) for contactless measurement systems. Valid types of sensors are those who provide metric information about one or multiple points within the sensors coordinate system. The reference objects are geometrical primitives (planes, spheres). The algorithm starts with estimated values for the tool transformation and the reference object definition and optimizes them in an iterative process. The optimisation result is tested for convergence with a simulation.

Keywords: sensor, robot tool transformation, TCP, tool center point, optimisation, Jacobian matrix

I. INTRODUCTION

In most applications with industrial robots it is common to have sensor systems with one or more sensors. The information gathered with a sensor system is mostly used for robot guidance or for quality assurance. If a sensor is part of the robot tool it is recommendable to identify its tool transformation and the origin of the sensor coordinate system, the tool center point (TCP). The tool transformation describes the transformation from the robot flange coordinate system to the tool coordinate system thus in this case the sensor coordinate system. There are some reasons for the determination of the tool transformation:

1. With a known tool transformation the robot can be moved in respect of the tool coordinate system and the tool center point. This makes teaching of robot programs much easier.
2. If the sensor has to be replaced due to a sensor malfunction it cannot be guaranteed that the replacement sensor can be mounted at exactly the same position the defect sensor was. If the robot programs were teached in respect of the tool coordinate system, the new tool transformation has to be determined and the problem is solved. Otherwise all robot programs have to be modified to fit to the new sensor position. Under normal circumstances this is a very time consuming and therefore expensive task.
3. With a known tool transformation the information provided by the sensor can referred to the base coordinate for each robot pose. This means the local sensor information becomes global information. In a multisensor system it may be a requirement to have a common reference for all sensor information.

The robot manufacturers provide software tools implemented in the robot control system to determine the tool transformation for common robot tools like grippers or welding tools. In the classical 4-point method (see e.g. [1], page 33ff) the TCP of the tool is moved to a fixed reference point from four different directions. The translative component of the tool transformation can be calculated together with an error estimation basing on four different positions and orientations of the robot flange. For most applications the knowledge of the translative component of the tool transformation is sufficient. But the rotational component of the tool transformation can be identified with similar methods. Either the robot has to be moved along the coordinate axes of the tool coordinate system or the tool coordinate system has to be aligned to the axes of the base coordinate system of the robot in a special way.

But these methods are not satisfactory to determine a sensors tool transformation. Sensors do not have a certain physical point as their TCP. The TCP lies somewhere in the measurement range of the sensor. It is difficult to use one of the methods described above to move the sensors TCP to the reference point even with the usage of software tools to display the current sensor information. The usage of special devices mounted at the sensor to mark the sensors TCP with a physical point may make the determination of the tool transformation easier but there is still a problem of the low accuracy of these methods. Mainly the determination of the rotational component of the tool transformation is quite inaccurate. The accuracy requirements for the TCP transformation may vary from application to application. But in most use cases the sensors TCP transformation has to be known in all six degrees of freedom with an accuracy that is not much lower than most inaccurate system component (sensor or robot).

This paper describes a method to optimize a given estimated TCP transformation determined by CAD data or by the methods provided by the robot manufactures. The algorithm is iterative and is based on sensitivity matrices and Jacobian matrices. A similar approach is described in [2]. This solution uses simple reference objects and free selectable robot poses too, uses similar error functions, but the optimisation is based on statistical methods (Bayesian

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search algorithms).

II. SYSTEM STRUCTURE

The total systems structure is shown in Figure 1. The sensor is attached to the end-effector of the robot. The sensor is a device that provides information about the position of a number of points within its field of view based on its sensor coordinate system. A simple example for a sensor would be a laser distance sensor which determines the position of a single point in its coordinate system (e.g. by triangulation or by time-of-flight). Other examples for sensor systems are laser stripe sensors (position of multiple points along a laser line), 3D cameras (position of multiple points of a matrix) or other intelligent camera systems. Important condition is that the sensor is calibrated and provides metric information. The sensor has a reference object within its field of view. The reference object is the representation of a geometrical primitive like a plane or a sphere. The position of the reference object is defined in the robots base coordinate system. Estimated values for the tool transformation and the reference object definition are known.

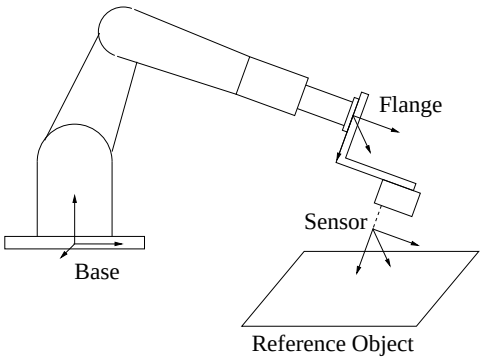

Figure 1: Basic System Structure

III. ERROR FUNCTION

First objective before optimizing the estimated values is the definition of an error function that allows the evaluation of a given tool transformation for the current robot pose. As defined above the sensor provides information about the position of a number of m points within its sensor coordinate system:

$$^{\text{Sensor}}\underline{p}_j \quad \text{with } j \in \{1, \ldots, m\} \tag{1}$$

These points have to be transformed into the base coordinate system in which the reference object is defined. This is the necessary transformation:

$$^{\text{Base}}\underline{\underline{T}}_{\text{Sensor}} = {}^{\text{Base}}\underline{\underline{T}}_{\text{Flange}} \cdot {}^{\text{Flange}}\underline{\underline{T}}_{\text{Sensor}} \tag{2}$$

And this transforms all points into the base coordinate system:

$$^{\text{Base}}\underline{p}_j = (^{\text{Base}}\underline{\underline{T}}_{\text{Sensor}})^{-1} \cdot {}^{\text{Sensor}}\underline{p}_j \tag{3}$$

Using an optimal reference object definition and an optimal tool transformation, all points $^{\text{Base}}\underline{p}_j$ measured by the sensor should be points of the reference object. But because of the inaccuracy of the estimated values there is a certain deviation. The sum of the deviation for every single point is a good error function. The error function is called "E".

If for example the reference object is a plane and the sensor a laser stripe sensor, the error function can be expressed as followed. The plane can be defined in the Hessian normal form:

$$\underline{n} \cdot \underline{x} - d = 0 \quad \text{with } |\underline{n}| = 1 \tag{4}$$

Because of

$$|\underline{n}| = \left| \begin{pmatrix} n_x \\ n_y \\ n_z \end{pmatrix} \right| = \sqrt{n_x^2 + n_y^2 + n_z^2} = 1 \tag{5}$$

it is possible to reduce one more degree of freedom in the plane description:

$$n_z = \sqrt{1 - n_x^2 - n_y^2} \tag{6}$$

The plane definition is now dependent from three factors: from n_x, n_y and d. The error function can be defined as the average distance of the distances of all points to the plane:

$$E = \frac{1}{m} \sum_{j=1}^{m} \left| \underline{n} \cdot {}^{\text{Base}}\underline{p}_j - d \right| (\tag{7}$$

Figure 2 shows the laser stripe sensor points transformed into the base coordinate system and their distances to the plane as reference object.

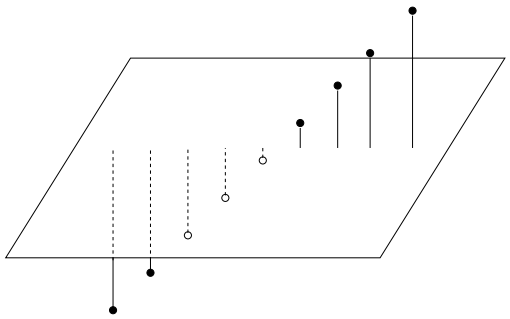

Figure 2: Laser Stripe Sensor Points

IV. OPTIMIZATION

The optimisation process is an iterative process that optimizes the tool transformation and (as a byproduct) the definition of the reference object. The number of factors to be optimized are up to six for the tool transformation (x, y, z, α, β, γ) and for the reference object definition usually three (plane or sphere with known radius), in total o factors. May

$$\underline{F} = (F_1, \ldots, F_o) \tag{8}$$

be a vector that contains all factors that should be optimized within the optimisation process and

$$\underline{f} = (f_1, \ldots, f_o) \tag{9}$$

current values for the optimisation factors (initially the estimated ones). Because of the high number of factors to optimize one single robot pose is not a sufficient base for the optimisation process. The base is a set of l different robot poses which have to vary in all degrees of freedom to provide enough information about the system structure:

$$^{\text{Base}}\underline{\underline{T}}_{i\ \text{Flange}} \quad \text{with } i \in \{1 \dots l\} \tag{10}$$

and a fixed set of m sensor points for each of the l poses:

$$^{\text{Sensor}}\underline{p}_{i,j} \quad \text{with } i \in \{1 \dots l\} \text{ and } j \in \{1 \dots m\} \tag{11}$$

Because the error function depends on the robot pose and a vector of optimisation values the error function becomes:

$$E = E(i, \underline{F}) \quad \text{with } i \in \{1 \dots l\} \tag{12}$$

For a given vector of optimisation factors $\underline{f}$ the error vector $\underline{e}$ is defined as

$$\underline{e} = (e_1, \dots, e_l) \quad \text{with } e_i = E(i, \underline{f}) \tag{13}$$

The sensitivity matrix $\underline{\underline{S}}$ describes how the result of the error function for a certain robot pose depends on a change of the optimisation factors in the near of the current optimisation factors f:

$$s_{i,k} = \left(\frac{\partial E(i, \underline{F})}{\partial F_k} \right)_{\underline{f}} \tag{14}$$

One single matrix element of $\underline{\underline{S}}$ can be calculated by a simple difference quotient:

$$\begin{aligned} s_{i,k} \quad = \quad & \frac{1}{2\delta_k} \cdot [E(i, (f_1, \dots, f_k + \delta_k, \dots, f_o)) - \\ & E(i, (f_1, \dots, f_k - \delta_k, \dots, f_o))] \end{aligned} \tag{15}$$

The Jacobian matrix J is the inverse of the sensitivity matrix and describes how the optimisation factors depend on a change of the result of the error function for a certain robot pose near the current optimisation factors f:

$$j_{k,i} = \left(\frac{\partial F_k}{\partial E(i, \underline{F})} \right)_{\underline{f}} \tag{16}$$

Because $\underline{\underline{S}}$ is rarely a square matrix, $\underline{\underline{J}}$ is calculated using the Moore-Penrose matrix inverse of $\underline{\underline{S}}$ (see [3]):

$$\underline{\underline{J}} = \underline{\underline{S}}^{+} = \left(\underline{\underline{S}}^{\mathrm{T}} \cdot \underline{\underline{S}} \right)^{-1} \cdot \underline{\underline{S}}^{\mathrm{T}} \tag{17}$$

If a vector of optimisation factors $\underline{f}$ is available and the corresponding error vector $\underline{e}$ and the Jacobian matrix $\underline{\underline{J}}$ have been determined, the improved vector of factors $\underline{f'}$ is calculated by:

$$\underline{f'} = \underline{f} - \left(\underline{\underline{J}} \cdot \underline{e} \right) \tag{18}$$

The complete optimisation algorithm is now:

1. Start with an initial vector of estimated optimisation factors $\underline{f}$ and with an fixed set of robot poses and sensor values.
2. Calculate error vector $\underline{e}$ for $\underline{f}$
3. Calculate Jacobian matrix $\underline{\underline{J}}$ for $\underline{f}$
4. Calculate new optimisation factors $\underline{f'}$
5. Stop if distance between $\underline{f}$ and $\underline{f'}$ is small enough
6. Set $\underline{f} = \underline{f'}$ and continue at step 2.

An alternative stop criterion would be a check if the current error vector $\underline{e}$ is small enough.

V. SIMULATION

To check the usability of the algorithm and the convergence behavior of the optimisation a simulation in MATLAB (see [4]) has been implemented. Part of the simulation is a module for the kinematics of an industrial robot. Mounted at the robots hand is a simulated laser stripe sensor with a plane as reference object in his field of view. The error function has been implemented as shown above (see (7)). With this simulation it is possible to test different robot poses with a correctly defined tool transformation and reference object ($E = 0$) and with slightly wrong tool transformations and reference objects ($E \neq 0$).

The simulated sensor provides position information about 10 points in its coordinate system, base of the optimisation are 20 robot poses. The factors to optimize are 9 in total:

$$\underline{F} = (x, y, z, \alpha, \beta, \gamma, n_x, n_y, d) \tag{19}$$

The sensitivity matrix is:

$$\begin{pmatrix} \frac{\partial E(1,\underline{F})}{\partial x} & \frac{\partial E(1,\underline{F})}{\partial y} & \cdots & \frac{\partial E(1,\underline{F})}{\partial d} \\ \frac{\partial E(2,\underline{F})}{\partial x} & \frac{\partial E(2,\underline{F})}{\partial y} & \cdots & \frac{\partial E(2,\underline{F})}{\partial d} \\ \vdots & \vdots & & \vdots \\ \frac{\partial E(20,\underline{F})}{\partial x} & \frac{\partial E(20,\underline{F})}{\partial y} & \cdots & \frac{\partial E(20,\underline{F})}{\partial d} \end{pmatrix} \tag{20}$$

And this is the Jacobian matrix:

$$\begin{pmatrix} \frac{\partial x}{\partial E(1,\underline{F})} & \frac{\partial x}{\partial E(2,\underline{F})} & \cdots & \frac{\partial x}{\partial E(20,\underline{F})} \\ \frac{\partial y}{\partial E(1,\underline{F})} & \frac{\partial y}{\partial E(2,\underline{F})} & \cdots & \frac{\partial y}{\partial E(20,\underline{F})} \\ \vdots & \vdots & & \vdots \\ \frac{\partial d}{\partial E(1,\underline{F})} & \frac{\partial d}{\partial E(2,\underline{F})} & \cdots & \frac{\partial d}{\partial E(20,\underline{F})} \end{pmatrix} \tag{21}$$

Table 1 shows an optimisation process of eight steps. The first row shows the deviation of the tool transformation from the correct tool transformation in all degrees of freedom. The other rows show the progress of the optimisation process. After eight steps the size of the deviation is smaller than the repeat accuracy of an common industrial robot. The values for n_x, n_y and d are skipped. Figure 3 and Figure 4 display the deviations over the optimisation steps.

Simulations with different random start deviations from optimal tool transformation have shown that a distance up to $10\,mm$ for x, y and z, a distance of $5°$ for α, β and γ and a distance of $0.1\,mm$ for n_x, n_y and d lead to certain convergence to the optimal transformation: the global minimum. If the deviation raises up to $15\,mm$, $7.5°$ and $0.2\,mm$ it is

x	y	z	α	β	γ
-6.983	-3.958	-2.433	3.537	0.936	3.600
-2.780	-2.798	-0.435	1.256	0.966	3.538
-0.042	-0.275	-0.025	0.026	0.123	3.541
0.068	-0.202	-0.096	-0.036	0.046	1.750
0.047	-0.093	-0.057	-0.026	0.018	0.870
0.039	-0.051	-0.030	-0.020	0.008	0.432
0.045	-0.029	-0.025	-0.019	0.004	0.212
0.030	-0.020	-0.016	-0.012	0.002	0.105
0.021	-0.009	-0.025	-0.007	0.001	0.053

Table 1: Simulation Result

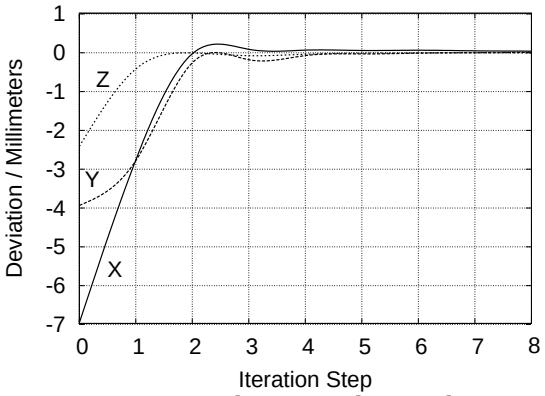

Figure 3: Simulation Result: Translation

not guaranteed that the optimisation process finds the optimal values. Result is a local minimum or a divergence. The convergence behavior shows that there is some slight overshooting. For speeding up the optimisation this can be compensated by introducing an attenuation factor $\lambda \leq 1$ applied when calculating the correction:

$$\underline{f'} = \underline{f} - \lambda \cdot \left(\underline{\underline{J}} \cdot \underline{e}\right) \tag{22}$$

The attenuation factor can be fixed or dynamically adapted.

The robot poses have to be chosen carefully. The set of robot poses has to contain variations for all degrees of freedom of the robot position to ensure a well-conditioned sensitivity matrix. In case of an ill-conditioned sensitivity matrix the Jacobian matrix can not be determined and the optimisation fails.

An additional note about the accuracy of the tool transformation that is result of the optimisation: the resulting tool transformation is an artificial entity that has no physical counterpart. The result depends on the selected robot poses and the chosen workspace where the robot poses are located. It depends on the all errors of the robot and the sensor system. It is the transformation that solves the given problem in an optimal way. If choosing different work spaces the resulting tool transformation varies.

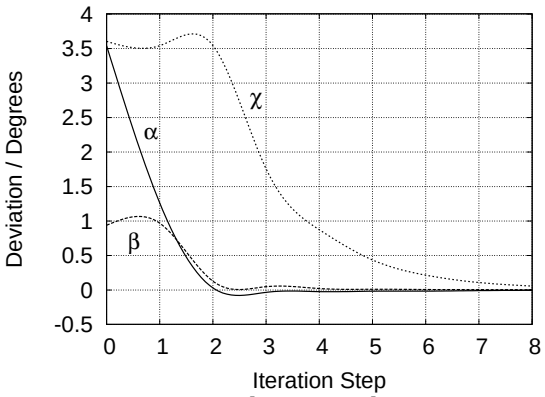

Figure 4: Simulation Result: Rotation

VI. MODIFICATION

If the sensor is not attached to the robot tool but fixed in the robot cell and its important to know the sensors position in respect of the robot its possible to use the algorithm from above with a slight modification. Figure 5 shows the changed system structure. Attached to the robots tool is the reference object which is defined in the robots flange coordinate system. This transforms all sensor points to the robots flange coordinate system:

$$^{\text{Flange}}\underline{p}_j = \left(^{\text{Base}}\underline{\underline{T}}_{\text{Flange}}\right)^{-1} \cdot {}^{\text{Base}}\underline{\underline{T}}_{\text{Sensor}} \cdot {}^{\text{Sensor}}\underline{p}_j \tag{23}$$

From here the solution is the same as for the base problem. The definition of the reference object in the flange coordinate system and the transformation from base to sensor are the factors to be optimized.

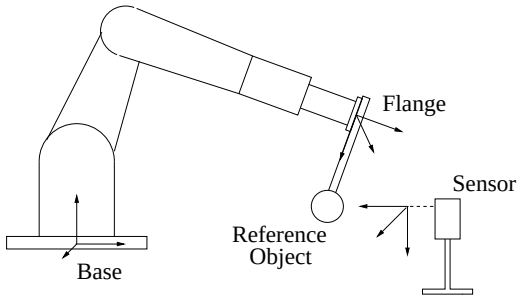

Figure 5: Modified System Structure

VII. CONCLUSION

This paper has demonstrated a method to determine a sensors tool transformation, a problem that occurs in practical industrial applications with robots. The method is based on an optimisation using Jacobian matrices. The convergence quality of the algorithm has been confirmed with a software simulation.

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The Mealy in Moore conversion of an automaton

Alioşa V. Hriţcu[1]

Abstract – In this article , it presents a new demonstration of the Mealy in Moore conversion theorem and an new matrix algoritm witch, just manually, can be easy realised for automatons with a great number of internal states. The Mealy in Moore conversion is a stage in the logical synthesis of a Mealy automaton using, for example, programmable logic arrays or delays.
Keywords: editing, Symposium, author

I. INTRODUCTION

An automaton is noted *A=(X, Z, Y, f, g)* and has the next significances for notations: *X*=lot of input combinations , *Z*=lot of internal states, *Y*=lot of output combinations, *f*=transition logical function defined by

$$f: X\times Z\to Z \ , \quad f(x_n, z_n) = z_{n+1} \ ,$$

g=output logical function witch for an Mealy automaton is defined by

$$g: X\times Z\to Y \ , \quad g(x_n, z_n) = y_{n+1}$$

and for an Moore automaton by

$$g: X\times Z\to Y \ , \quad g(z_n) = y_{n+1} \ .$$

An automaton is represented by truth table or connections matrix. In the connections matrix, for every internal state it allocats one row and one column, the column containing the input transitions to the internal state and the row containing the output transitions from the internal state. In a automaton synthesis, it must identifier, in the *Z* lot, the equivalence classes for to generate the reduced form of the automaton by keeping only one single state from every equivalence class. Because the truth table and the connections matrix are easier handled for an Moore automaton, in a Mealy automaton synthesis is necessary a Mealy in Moore conversion ; [1], [2].

II. THEORETICAL SUPPORT

The possibility of a Mealy in Moore conversion of an automaton is justifyed by the next

Theorem
Any Mealy automaton has an equivalent Moore one.
Demonstration
Let it be $A = (X, Z, Y, f(x_n, z_n), g(x_n, z_n))$ an Mealy automaton, whose output function can be writed

$$g(x_n, z_n) = g(\overset{-1}{f}(z_{n+1})) \overset{not}{=} G(z_{n+1}) \qquad (1)$$

only if the transitions to a internal state of the Mealy automaton have the same output for automaton, so that the function

$$\overset{-1}{f}: Z \to X\times Z \qquad \overset{-1}{f}(z_{n+1}) = (x_n, z_n) \qquad (2)$$

don't introduce output undeterminations. The last relation shows that it's an Moore automaton, noted $A' = (X, Z, Y, f(x_n, z_n), G(z_n))$, having the same outputs like the Mealy automaton, but the outputs being delayed by one single transition. So, for to pass from the Mealy automaton at the Moore automaton it uses the functions group *h=(α, β, δ)* , in witch :

$$\begin{cases} \alpha : X\to X \ , & \alpha(x_n) = x_n \\ \beta : Z\to Z \ , & \beta(z_n) = z_n \\ \delta : Y\to Y \ , & \delta(g(x_n, z_n)) = g(x_{n-1}, z_{n-1}) \end{cases} \qquad (3)$$

Because :

$$g(x_{n-1}, z_{n-1}) = g(f(z_n)) = G(z_n) = G(\beta(z_n)) \qquad (4)$$

and, by building manner of the Moore automaton, *h=(α, β, δ)* is both injective and surjective, the Moore and Mealy automatons are in a equivalence relation. Any Mealy automaton can be transformed, so that the transitions to a internal state have the same output for automaton, dividing any internal state in so many new internal states how many different outputs are in the transitions to the internal state. Thus, a new internal state keeps, from the origin internal state, the same output transition, but only the input transitions with the same output for automaton. An transformation example of a internal state z_k in two new internal

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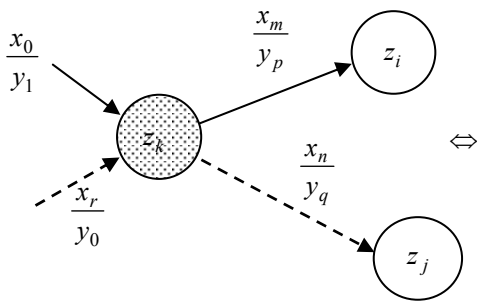
states z_{k0} and z_{k1} is presented in Fig.1, by fluency graph.



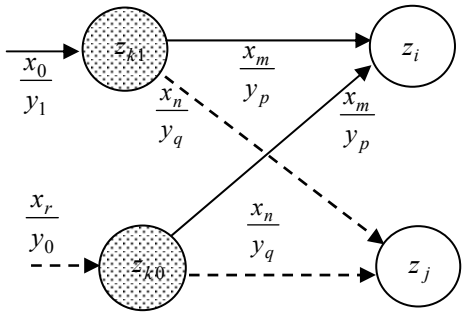


Fig.1

III. THE CONVERSION ALGORITHM

The Mealy in Moore conversion algorithm of an automaton uses the previous theorem, and has the next two phases:

a) In the initial Mealy automaton, it forms an intermediary Mealy automaton having in the input transitions to a internal state the same output for automaton. So, it obtains the connections matrix of the intermediary Mealy automaton by dividing every internal state in so many new internal state, how many different outputs are in the input transitions from the column of the divided internal state. Every new internal state keeps from origin internal state, in its row all output transitions and in its column only input transitions with the same output for automaton, so that the new internal states with same origin have identical rows, but different columns.

b) It forms the equivalent Moore automaton delaying the outputs of the intermediary Mealy automaton by one single transition. For that, in the connections matrix of the intermediary Mealy automaton, it moves the outputs from input transitions of a internal state column, to the output transitions of the same internal state row ; [3].

In the example presented below, the matrix noted M and the incomplete matrix noted M_i show witch internal states are divided and how it does this. In the intermediary matrix noted M_{INT} it's shown the forming mode of the rows for the new internal states z_{11} and z_{21}.

Example

$$A \overset{def}{=} \begin{array}{c|ccc} & z_1 & z_2 & z_3 \\ z_1 & - & \frac{x_0}{y_0} & \frac{x_2}{y_0} \\ z_2 & \frac{x_2}{y_0} & \frac{x_1}{y_0} & \frac{x_3}{y_0} \\ z_3 & \frac{x_0}{y_1} & \frac{x_1}{y_1} & \frac{x_3}{y_0} \end{array} \quad Mealy =$$

$$z_1 \to \begin{cases} z_{10} \\ z_{11} \end{cases} \quad z_2 \to \begin{cases} z_{20} \\ z_{21} \end{cases} \quad z_3$$

$$\begin{array}{c|ccc} & z_{10} & z_{20} & z_3 \\ z_1 & - & \frac{x_0}{y_0} & \frac{x_2}{y_0} \\ = z_2 & \frac{x_2}{y_0} & \frac{x_1}{y_0} & \frac{x_3}{y_0} \\ z_3 & \frac{x_0}{y_1} & \frac{x_1}{y_1} & \frac{x_3}{y_0} \end{array} = M =$$

$$\begin{array}{c|ccccc} & z_{10} & z_{20} & z_3 & z_{11} & z_{21} \\ z_{10} & & & & - & \frac{x_0}{y_0} \\ z_{20} & & & & \frac{x_2}{y_0} & \frac{x_1}{y_0} \\ = z_3 & & & & - & - \\ z_{11} & & & & & \\ z_{21} & & & & & \end{array} = M_i =$$

$$\begin{array}{c|ccccc} & z_{10} & z_{20} & z_3 & z_{11} & z_{21} \\ z_{10} & - & - & \frac{x_2}{y_0} & - & \frac{x_0}{y_0} \\ z_{20} & - & - & \frac{x_3}{y_0} & \frac{x_2}{y_0} & \frac{x_1}{y_0} \\ = z_3 & \frac{x_0}{y_1} & \frac{x_1}{y_1} & \frac{x_3}{y_0} & - & - \\ z_{11} & - & - & \frac{x_2}{y_0} & - & \frac{x_0}{y_0} \\ z_{21} & - & - & \frac{x_3}{y_0} & \frac{x_2}{y_0} & \frac{x_1}{y_0} \end{array} = M_{INT} =$$

$$
\begin{array}{cc|ccccc|}
 & & z_{10} & z_{20} & z_3 & z_{11} & z_{21} \\
 & & \uparrow & \uparrow & \uparrow & \uparrow & \uparrow \\
z_{10} & \rightarrow & - & - & \frac{x_2}{y_1} & - & \frac{x_0}{y_1} \\
z_{20} & \rightarrow & - & - & \frac{x_3}{y_1} & \frac{x_2}{y_1} & \frac{x_1}{y_1} \\
= z_3 & \rightarrow & \frac{x_0}{y_0} & \frac{x_1}{y_0} & \frac{x_3}{y_0} & - & - \\
z_{11} & \rightarrow & - & - & \frac{x_2}{y_0} & - & \frac{x_0}{y_0} \\
z_{21} & \rightarrow & - & - & \frac{x_3}{y_0} & \frac{x_2}{y_0} & \frac{x_1}{y_0}
\end{array} \quad \textit{Moore} \qquad = A'
$$

IV. CONCLUSIONS

The Mealy in Moore conversion algorithm, proposed in this article, is, just manually, easier handled for automatons with a great number of internal states and is based on a siple mathematical demonstration. This algorithm simplifies logical synthesis of an sequantial automaton witch can be realised with programmable logic arrays or relays.

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The Micropower Translinear Network Implementation of Rational Approximated Functions

Elena Doicaru[1]

Abstract – In this paper are presented several translinear topologies suitable for static and dynamic analog signal processing at very low supply voltage. The one variable objective functions, firstly are rational approximated, then are decomposed in continued fractions and finally implemented with CMOS translinear networks. Such implementation is preferred in application that required small errors of signal procesing.

Keywords: analog signal processing circuits, translinear circuits, CMOS integrated circuits, low power and low voltage circuits.

I. INTRODUCTION

Nonlinear objective-functions are widely applied in practical VLSI electronic systems and there are many cases in which the translinear networks are the best solutions of implementation of these. The synthesis of nonlinear networks is a heavy task. However a systematic procedure for the synthesis of translinear circuits was developed by Evert Seevinck [5]. The proposed synthesis method consists in three parts: objective-function approximation, approximate-function decomposition and realization of translinear network for the function obtained after decomposition. Using at starting point the Seevinck synthesis method in period 1999-2003 I have developed the algorithms and I have realized a few programs in C++ code which permit the automatic synthesis of translinear circuits but only whit bipolar transistors, named TLSS, [1], [2], [3].

In practical CMOS VLSI mixal signal electronic systems the power supply voltage continues to scale down. Future analog circuits will have to operate successfully at supply voltages slightly higher than the MOS threshold voltage. The suitable topologies for signal processing at such low values of supply voltages are the translinear circuits because are operating in current domain and in this way the very small voltage swings are avoided. The MOS transistors have exponential current-voltage characteristics in weak inversion (or sub-threshold) region. Therefore in these circuits the MOS transistors will operate in this region. The main problems of this operating region are the relatively low speed capability and inferior matching. But these problems are relatively solved in sub-micron technology.

In this paper are presented several CMOS translinear topologies that implement one variable objective functions, rational approximated and decomposed in continued fractions. Such functions processing leads to implementations with small errors and relatively small number of devices.

II. THE MOS TRANSISTORS IN WEAK INVERSION

In above section was argued that the MOS transistor in low-voltage translinear circuits will operate in weak inversion. It is well known the general expression of drain current of MOS transistor:

$$I_D = \beta \cdot \int_{V_S}^{V_D} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}V \qquad (1)$$

with

$$\beta = \mu \cdot C_{ox} \cdot (W / L) \qquad (2)$$

where

W, L width, length of the channel;
C_{ox} gate capacitance per unit area;
μ charge carrier mobility;
Q_i induced mobile charge in channel;
V_D, V_S drain, source voltages referred to the local substrate;
V channel potential.

This expression may be decomposed into:

$$I_D = \beta \cdot \int_{V_S}^{\infty} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}V - \beta \cdot \int_{V_D}^{\infty} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}V = I_F - I_R \qquad (3)$$

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where I_F is called forward current (controlled by source voltage V_S) and I_R is called reverse current (controlled by drain voltage V_D).
In weak inversion we have [4]:

$$Q_i / C_{ox} \sim \exp\left(\frac{V_P - V}{V_T}\right) \tag{4}$$

where

V_P pinchoff voltage which is a nonlinear function of gate voltage V_G and represents the body effect;
V_T thermal voltage ($k \cdot T / q$).

Thus we have the following proportionality

$$\begin{aligned} I_F &\sim \beta \cdot \exp\left(\frac{V_P - V_S}{V_T}\right) \\ I_R &\sim \beta \cdot \exp\left(\frac{V_P - V_D}{V_T}\right) \end{aligned} \tag{5}$$

and the drain current has the expression

$$I_D = I_S \cdot \exp\left(\frac{V_P}{V_T}\right) \cdot \left[\exp\left(-\frac{V_S}{V_T}\right) - \exp\left(-\frac{V_D}{V_T}\right)\right] \tag{6}$$

or in terms of V_{GS} and V_{GD} as follows

$$I_D = I_S \exp\left(\frac{V_P - V_G}{V_T}\right) \cdot \left[\exp\left(\frac{V_{GS}}{V_T}\right) - \exp\left(\frac{V_{GD}}{V_T}\right)\right] \tag{7}$$

where I_S is specific current (limit of weak inversion). The specific current is proportional to W/L, follows explicitly shown:

$$I_S \cdot \exp\left(\frac{V_P - V_G}{V_T}\right) = \frac{W}{L} \cdot I_\Diamond(V_G) \tag{8}$$

with $I_\Diamond(V_G)$ the zero-bias ($V_{GS} = 0$) current for a square transistor, which represents the body effect. So, the forward and reverse currents become:

$$\begin{aligned} I_F &= \frac{W}{L} \cdot I_\Diamond(V_G) \cdot \exp\left(\frac{V_{GS}}{V_T}\right) \\ I_R &= \frac{W}{L} \cdot I_\Diamond(V_G) \cdot \exp\left(\frac{V_{DS}}{V_T}\right) \end{aligned} \tag{9}$$

If $I_R << I_F$, then the MOS transistor is saturated, otherwise the MOS transistor is non-saturated. In figure 1.a are shown the two operation regions for weak inversion, which are defined by the ratios I_D / I_F and V_{DS} / V_T [8].

Therefore, each of the drain current components (expressed by (9)) of a non-saturated transistor may be relate to an equivalent saturated transistor with gate-source voltage V_{GS} and V_{GD} respectively and the non-saturated transistor may be decomposed into two identical saturated transistors connected anti-parallel [9]. This is symbolically shown in figure 1.b. The transistor that corresponds to reverse current component is shown in dashed line, and represents the effect of the non-saturated operation of the real transistor.

III. THE CMOS TRANSLINEAR IMPLEMENTATION OF RATIONAL APPROXIMATED OBJECTIVE FUNCTIONS

The objective-functions are first normalized, so that theirs variables to take values only in interval [-1, 1]. Then the one variable normalizes functions are approximated by using *Padé approximation* or *Chebyshev rational approximation* so that the maximum relative error of approximation to be $0.01\% \div 0.1\%$. Finally, it is changed the x variable of the rational function in auxiliary variable $y = y(x)$ so that $y > 0$, $\forall x \in [-1;1]$.

The result of these processes must be manipulated into products of linear terms in the input and output variables. These linear terms have real coefficients and they must always remain positive for all combinations of input variable values. In conformity with decomposition algorithm developed by me and presented in [3], the general final form of continued fraction that incorporate all cases that can be encountered in the decomposition process is:

$$f_{ar}(y) = h_0 + \cfrac{g_1}{h_1 + \cfrac{g_2}{h_2 + \cfrac{g_3}{h_3 + \ldots \cfrac{}{h_{q-1} + \cfrac{g_q}{h_q}}}}} \tag{10}$$

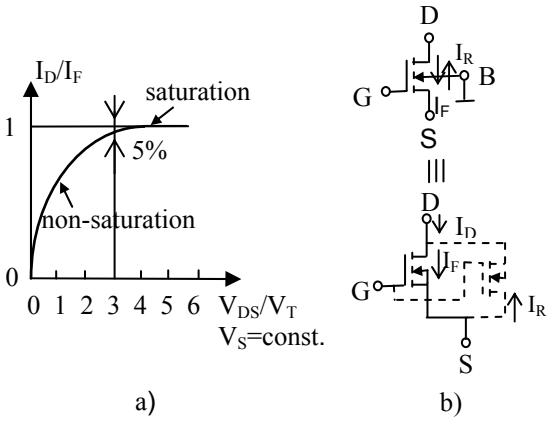

Figure 1. a) The operation regions in weak inversion of the MOS transistor; b) Non-saturated MOS transistor equivalent to two saturated transistors connected anti-parallel.

The significance of used function g_i and h_i in (10) in function of encountered cases is presented by fallow expressions:

$$h_0 = \begin{cases} 0 & \text{when the dominator of } f_{ar} \text{ is positive} \\ & \text{or real roots of dominator are not placed} \\ & \text{in the range of y variation} \\ \dfrac{b_0}{c_{00}} - p_0 \cdot y; & p_1 \div p_{q-1} = 0 \end{cases}$$

$$g_i = \begin{cases} c'_{10} \cdot y^{i_1} & \text{when } h_0 = 0,\ i = 1 \\ c_{i0} \cdot y^{1+i_i} & \text{when } p_0 \neq 0 \\ c'_{i0} \cdot y^{i_i+1} & \text{when } h_0 = 0 \end{cases} \Bigg\} \begin{array}{l} c'_{i0} = a_{i-1} \cdot c_{i0} \\ i = 1 \div q \end{array}$$

$$\underset{i=1\div(q-1)}{h_i} = \begin{cases} a_{i-1} \cdot c_{i-1,0} & \text{when } p_i = 0 \\ a_{i-1} c_{i-1,0} - p_i y^2 & \text{when} \begin{cases} p_i \neq 0 \\ p_{i+1} \div p_{q-1} = 0 \end{cases} \end{cases}$$

$$h_q = \begin{cases} c^*_{q-1,0} + c^*_{q-1,1} \cdot y & \text{when } \exists p_i \neq 0 \\ c'_{q-1,0} & \text{when } \forall p_i = 0 \end{cases}$$

$$c^*_{q-1,j} = \begin{cases} c^*_{q-2,0} \cdot c^*_{q-3,j+1} - c^*_{q-3,0} \cdot c^*_{q-2,j+1} & \text{for q even} \\ c^*_{q-1,0} \cdot c^*_{q-2,j+1} - c^*_{q-2,0} \cdot c^*_{q-1,j+1} & \text{for q odd} \end{cases}$$

$$a_i = \begin{cases} 1 & \text{when the denominator} \\ & c'_{i0} + c'_{i1} \cdot y + c'_{i2} \cdot y^2 + \ldots + c'_{ir_i} \cdot y^{r_i} \\ & \text{is positiv in the variation range of } y \\ < 0, & a_i \in \mathbf{Z} \end{cases} \quad (11)$$

For the one variable function decomposed in the general form (10) the following set of equations must be implemented:

$$\begin{cases} g_q = g'_q \cdot g''_q \\ z_q \cdot h_q = g'_q \cdot g''_q \\ \ldots \\ (z_i + h_{i-1}) \cdot z_{i-1} = g'_{i-1} \cdot g''_{i-1}; \quad i = 2,\ldots,q \\ g_{i-1} = g'_{i-1} \cdot g''_{i-1} \\ \ldots \\ z = f_{ar}(y) = h_0 + z_1 \end{cases} \quad (12)$$

These equations can be easily implemented using the expandable generic network presented in figure 1.a. It is very easy to see that in this network, all transistors, except T_{i8} and T_{i10} transistors of the current sources, are saturated, $I_R << I_F$ and therefore to good approximation we have:

$$I_{Dij} = I_{Fij} = \frac{W_{ij}}{L_{ij}} \cdot I_\Diamond(V_{Gij}) \cdot \exp\left(\frac{V_{GSij}}{V_T}\right) \quad (13)$$
$$i = \overline{1,q},\ j = \overline{1,9}\ j \neq 8$$

For a minimum supply voltage, the current-source transistors T_{i8} and T_{i10} will be non-saturated. Therefore, in accordance with decomposition technique described in section two (see figure 1.b.), the fictitious transistors T'_{i8} and T'_{i10} are added in order to account the non-saturation of these transistors (see figure 2.b). From those presented in previous section, it follows that all shown network transistors can now be regarded as saturated. The section i of proposed network are three translinear loops: $T_{i1} - T_{i6}$, next T_{i3}, T_{i5}, T_{i7} and T'_{i8} and finally T_{i4}, T_{i6}, T_{i9} and T'_{i10}, which are immune from the body effect. Assuming equal-sized transistors for the translinear loops and applying the Kirchoff low to those it is obtained the following expressions:

$$\begin{aligned} &V_{GS_{i1}} + V_{GS_{i3}} + V_{GS_{i6}} = V_{GS_{i2}} + V_{GS_{i4}} + V_{GS_{i5}} \\ &V_{GS_{i3}} + V'_{GS_{i8}} = V_{GS_{i5}} + V_{GS_{i7}} \\ &V_{GS_{i4}} + V'_{GS_{i10}} = V_{GS_{i6}} + V_{GS_{i9}} \end{aligned} \quad (14)$$

It can see that the oppositely connected transistor pairs T_{i1} - T_{i2}, T_{i3} - T_{i5}, T_{i4} - T_{i6}, T_{i7} - T'_{i8} and T_{i9} - T'_{i10} have the same gate voltage:

$$\begin{aligned} &V_{G_{i1}} = V_{G_{i2}};\ V_{G_{i3}} = V_{G_{i5}};\ V_{G_{i4}} = V_{G_{i6}} \\ &V_{G_{i7}} = V'_{G_{i8}};\ V_{G_{i9}} = V'_{G_{i10}} \end{aligned} \quad (15)$$

It is follows that

$$\begin{aligned} &I_\Diamond(V_{Gi1}) = I_\Diamond(V_{Gi2});\ I_\Diamond(V_{Gi3}) = I_\Diamond(V_{Gi5}) \\ &I_\Diamond(V_{Gi4}) = I_\Diamond(V_{Gi6}) \\ &I_\Diamond(V_{Gi7}) = I_\Diamond(V'_{Gi8});\ I_\Diamond(V_{Gi9}) = I_\Diamond(V'_{Gi10}) \end{aligned} \quad (16)$$

and the equation (14) becomes a classical translinear relationship independent of the body effect:

- for the first loop

$$(g'_i + I_{0i}) \cdot I_{Di1} \cdot I_{0i} = I_{0i} \cdot I_{Di2} \cdot (z_i + I_{0i}) \quad (17)$$

- for the second loop

$$(g''_i + I_{0i}) \cdot I_{0i} = (g'_i + I_{0i}) \cdot I'_{Di8} \quad (18)$$

with

$$I'_{Di8} = g''_i + I_{0i} - I_{0i} - I_{Di1} = g''_i - I_{Di1}. \quad (19)$$

- for third loop

$$I_{0i} \cdot (h_i + z_{i+1} + I_{0i}) = I'_{Di10} \cdot (z_i + I_{0i}) \quad (20)$$

with

$$I'_{Di10} = h_i + I_{0i} - I_{Di2} - I_{0i} = h_i - I_{Di2}. \quad (21)$$

Eliminating I_{Di1} and I_{Di2} yields:

$$(z_{i+1} + h_i) \cdot z_i = g'_i \cdot g''_i \quad (22)$$

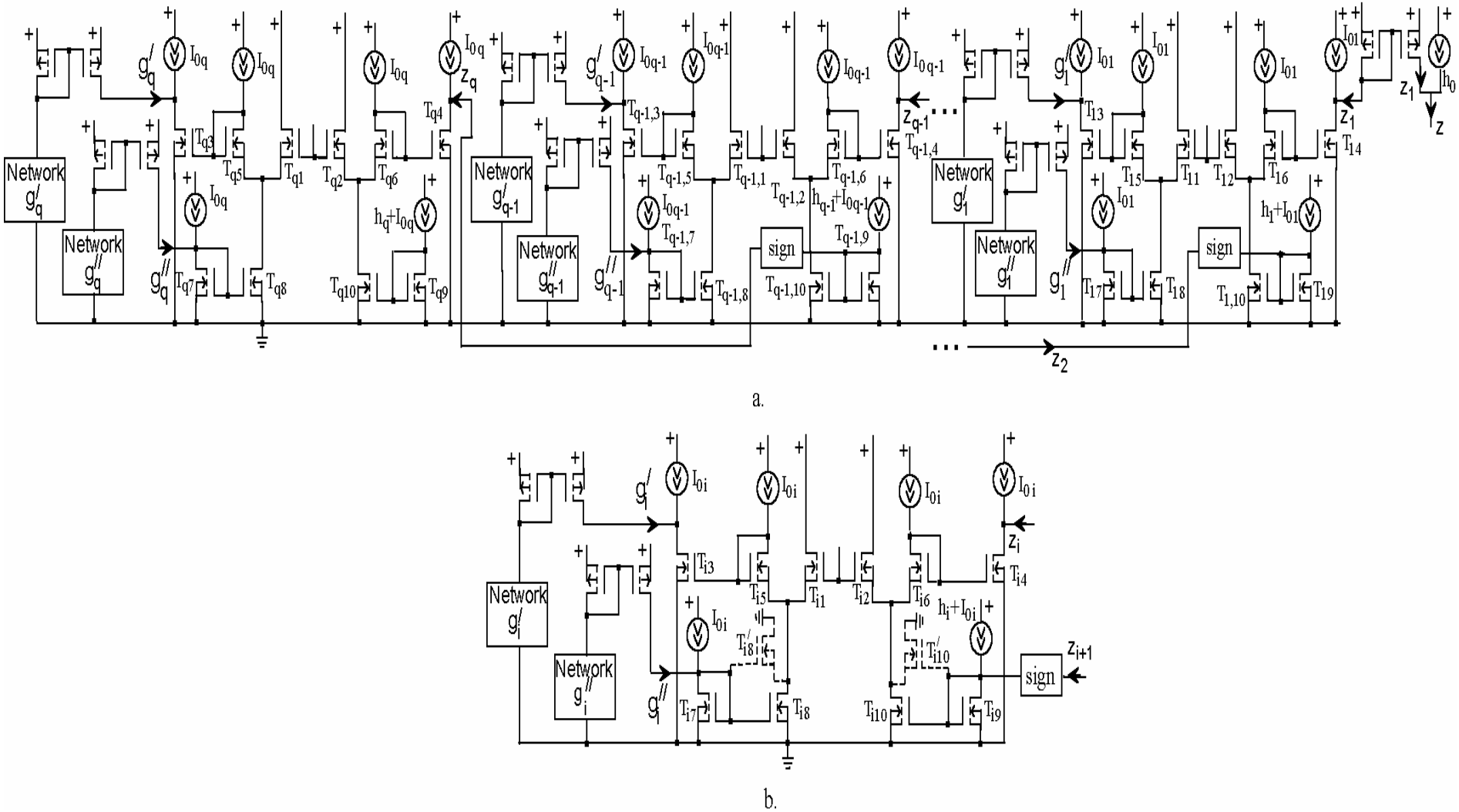

Figure 2.a. The CMOS translinear expandable generic network that implements
the one variable rational approximated objective functions; b. The i section of generic network.

The expressions for the drain currents of transistors T_{i1} and T_{i2} are:

$$I_{Di1} = \frac{g_i^{/} \cdot g_i^{//} - I_{0i}^2}{g_i^{/} + I_{0i}}$$
$$I_{Di2} = \frac{g_i^{/} \cdot g_i^{//} - I_{0i}^2}{z_i + I_{0i}} \qquad (23)$$

and relive that

$$\min\left|g_i^{/} \cdot g_i^{//}\right| > I_{0i}^2 \qquad (24)$$

for a well operating of network.

The supplementary networks used for implementation of h_i functions and $g_i^{//}$ functions are presented in figures 2 and 3. The analisys for this networks is similary with those maked for the section i of general network. In conformity with these analisys it is obtained:

- for the h_i network

$$\left|p_i\right|^{-1} \cdot \left(a_{i-1} \cdot c_{i-1,0} - h_i\right) = y \cdot y$$
$$h_i = a_{i-1} \cdot c_{i-1,0} - \left|p_i\right| \cdot y^2 \qquad (25)$$

- for the g_i network

$$\left|c_{i0}\right|^{-1} \cdot g_i = y \cdot y^{i_i}$$
$$g_i = \left|c_{i0}\right| \cdot y^{1+i_i} \qquad (26)$$

Must mentioned that in the case of the g_i network, in function of values of i, h_0 and p_0, we have different forms for the network. So, when h_0=0 and i=1 the network presented in figure 3 will be easy changed: $c_{i0}^{/}$ instead of c_{i0}, y^{i_1-1} instead of y^{i_1}. When h_0=0 and $i \neq 1$ then c_{i0} will be changed with $c_{i0}^{/} = a_{i-1} \cdot c_{i0}$. The functions y^{i_i} are obtained using similar topology with those presented in figure 3, but instead of $\left|c_{i0}\right|^{-1}$ will be 1 and instead of y^{i_i} will be y^{i_i-1}. Similarly will be obtained the y^{i_i-1} as is suggested in figure 3 by quadripoles N_{i_i}.

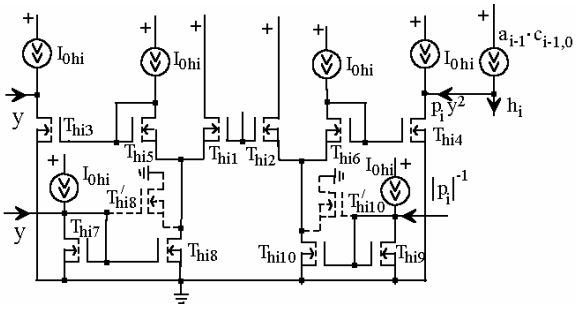

Figure 2. The network that implements the h_i functions

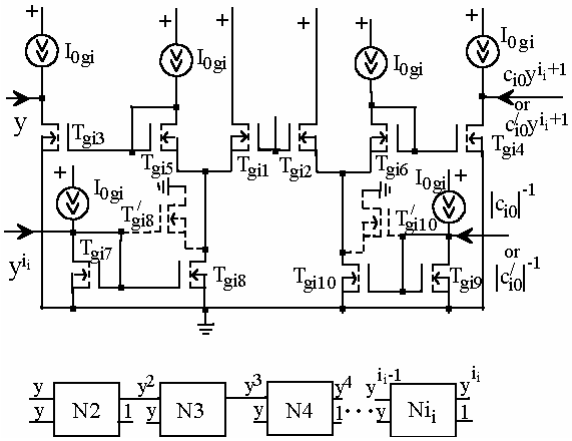

Figure 3. The networks that implement the g_i functions.

The network for changing the sign in conformity with a_I is, in MOS technology, a simple current mirror and for that she wasn't presented.

We must pointed that the current-mode signals are natural for translinear circuits, but in the real-word systems voltage-signals are generally used and therefore voltage-current interfacing will be needed in practice.

IV. CONCLUSION

The suitable topologies for signal processing at very low values of supply voltages are the translinear circuits because are operating in current domain and in this way the very small voltage swings are avoided. In this paper are presented several translinear topologies suitable for static and dynamic analog signal processing in mixed-signal chips fabricated in digital CMOS technology and operated at very low supply voltage. First, it is presented the expandable generic translinear network that is implementing the rational approximated one variable functions that are continue in entire definition domain. The minimum value of supply voltage required for this circuit is given by the sum of the MOS transistor threshold voltage and the drain-source saturation voltages of current sources. Next it is presented the g_i and h_i networks used for obtaining the necessary signals for expandable network. Like expandable network, these can operate at minimum value of supply voltage. Since the value of the supply voltage is low and the require of translinear principle to have a exponential I-V characteristic, the all transistors of these networks will operated in weak inversion. Therefore, bandwidth will be limited and the circuits will be sensitive to the threshold voltage matching.

For the previous presented networks will be developed algorithms so those to be integrated to the TLSS synthesis program. The TLSS is a program in C++ code, realized by me in period 1999-2000, which

permits the automatic synthesis of translinear circuits. Also, will be studied the bandwidth, noise and errors due to transistors mismatching and will try to correct them.

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A New Approach to Higher Education

Popo Rodion[1]

Abstract – The traditional form of the maximum Russian higher education consists in a certain sequence of lecturing, carrying out practical and laboratory researches during a semester which comes to an end with offsets and examinations. This paper describes a few issues in the Russian higher education. It also proposes a solution to its crisis.
Keywords: higher education.

I. CYCLIC STUDIES

The traditional form of the highest Russian higher education consists in a specific sequence of reading lectures, carrying out practical and laboratory training during the semester, which concludes with tests and examinations. This form of instruction has a number of deficiencies.

First, a mixture is formed in the students mind from the information gathered at different courses during the days of a week. If the obtained information ("written down in memory") does not fortify itself by its realization for lack of time, then it is forgotten ("is erased"). Secondly, during test and examination sessions it is not possible for that brief time interval to realize studies even when desired.

Therefore for the more effective mastering expedient it would be to divide them into the cycles, during when 1-2 weeks is studied each day not more than 2-3 objects (for example, physics + philosophy + physical training). The student daily "bathes" in these objects, which makes it possible to master them better (in medical Institutes of Higher Education this form of instruction it has been used for a long time).

This form of training requires more professional and physical preparation of teachers; in the interruption between the cycles the instructors can be occupied by preparation for the following cycle, systematic and scientific work. This form of instruction makes it necessary for teachers and students to work more intensively.

This is more convenient for those students who have temporary financial difficulties and have to make extra earnings (at present many students are compelled to work because of the smallness of allowance).

II. COMPUTER TECHNOLOGY

Together with the "cyclic" form of training, it is necessary to leave the former, and to apply much more the computer technology, which makes it possible to considerably decrease routine works and to accelerate the study of curricula.

The teacher should be assisted by training programs, and electronic versions of the studied courses. Programs for courses should be adapted not only to the current standards, but also to today's needs.

III. THE INTERNET

The more claimed at present in the presence Internet is the external-studies department (but it does not save from the army), which makes it possible to individualize educational process, to be adapted to changing living conditions. With the presence of external-studies department (to correspondence form of education) the "evening form" of instruction will be gradually reduced naturally.

IV. INTERNATIONAL STANDARDS IN EDUCATION

Upon transition to the international standards of education, on the form (bachelor, master, doctoral studies) is possible, but the education programs must change considerably slower. Yes, even excessively late completion of high school (with the inoculated sexual freedom) is the negative factor of western instruction. Probably, it is necessary to give freedom of choice in the instruction to each licensed university, which should confer a rank of experts on specialties of training, to confer scientific degrees and ranks. It is possible to welcome only a reduction of a significant amount of officials from education and sciences which use service positions in the mercenary purposes under good intentions.

The scientific degree should be one (as in the West-doctor of sciences), but the requirements for its awarding must be higher than during awarding of Candidate of Sciences, and should be determined by the concrete university. For eliminating the conflict situations at the Minister of Science and Education

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there should be the commission, which can solve the problem of protection, after directed it into another university. Red tape should be shown to a minimum. The concrete university should assign the wage and the grant funds, without having to worry about tomorrow. The wage of the minister and professors must not differ by an order or more, and to be in the reasonable limits.

V. CONCLUSIONS

At present science and education are not supported properly by the state (the intelligence has not even received an opportunity to privatize a building in which he/she worked unlike trade workers, etc). Low wages of teachers (on the average below the wage of the cleaning woman sometimes), low grant funds lead to destruction of a science and education system. Many students formally spend 5 to 6 years in the universities and formally present degree projects, thus being "rescued" from the obligation to be a soldier in the army. The majority of parents do not have the financial possibility to feed and dress properly their children who are compelled to work in parallel with study during school hours (are especially demanded those students who have skills of work on computers, programmers). And in such situation, created by the state, is it possible to conduct conversations on moral foundations?!

It is necessary to make responsible, first of all, the state which has created conditions for trade in diplomas, by certificates in transitions of the underground open (which too act from hands of officials from the ministry of science and education).

Thus, the basic moments are:

1) the traditional form of instruction, the instruction in "cycles", the external-studies department;
2) the independence of universities;
3) the transition to the education of bachelors, masters, doctoral candidates;
4) the transition to a uniform scientific degree of Doctor of Sciences of concrete university;
5) the reduction of officials from the science and the education minister.

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Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 51(65), Fascicola 1, 2006

Preconditioning Circuit for Electrical Power System Disturbances Measurement

Ciprian Dughir[1], Gabriel Găşpăresc[2]

Abstract – This paper is focused on how to reduce the amplitude of electrical disturbances which appears in the electrical power systems to a low voltage supported by the acquisition boards, without loosing any important disturbances. Is well known the fact that the maximum input voltage of the most popular acquisition boards is about ±10V. The disturbances may heave 10kV amplitude, and if we simply divide the input voltage by 1000 to reduce the 10kV to 10V, the main power system voltage (220V) will be reduced to 0.22V which is too low to obtain a sufficient accuracy in the measurement process, counting that the most of the disturbances have amplitudes in the area of 0-100V.

Keywords: power system, disturbance, voltage divisor, nonlinear

I. INTRODUCTION

The power quality study involves an important step, i.e., monitoring the actual voltage and current waveforms, classifies these waveforms and displays them when certain thresholds are exceeded. These waveforms exhibit certain distinguishing characteristics and can be identified to belong to a certain waveform class. The classification scheme has to be robust and accurate to handle the noisy data collected from the transmission or distribution networks.

The main problem in the electrical power systems is monitoring and detecting of disturbances. Because of the multitudes of types the disturbances are, each disturbances with her specificity, it is difficult to detect and capture such types of disturbances. The common types of disturbances are that can produce little variations of the power system voltage around 220V. Another type of disturbances is the disturbances with amplitudes between 500V and 2kV, and last one with amplitudes over 2kV, disturbances which occurs very rare.

II. THE METHOD PROPOSED

The method proposed in this paper is focused on how to divide the input voltage to a value that complies with the acquisition board, without losing any type of disturbances. This method consists in the use of a functional transformer [4][5] with the transfer function presented in figure 2. Because most of the disturbances present smaller variations around 220V, the first cut point is set to 500V to preserve sufficient the amplitude of the output signal. Very small disturbances around the 220V can be now analyzed. The second segment is from 0.5kV to 2kV where is to found the disturbances which occur more rarely then the first class, and the last segment represent the disturbances which appears very rare in the signal.

After the acquisition process, the signal is processed for detecting the disturbances, and if the algorithm found any disturbances, the signal is reverted to the original shape and then recorded to a file to be analyzed or viewed later [5][6].

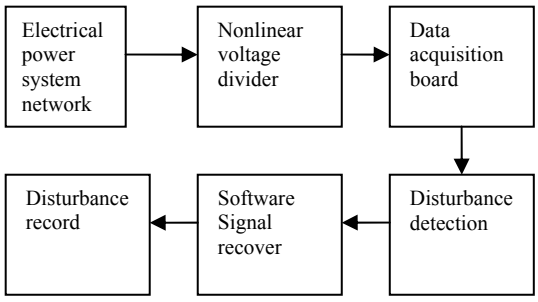

Fig. 1. Bloc diagram

The functional transformer uses a operational amplifier with very low bias current because the value of the input resistor R_{in}. If the value of R_{in} increases, the voltage on that resistor increases. This voltage must be insignificant in rapport with the input signal. If the input resistance decreases, the value of R_2 and R_4 becomes comparable with the conduction resistance of the diode D_2 and D_4. For this purpose was chosen the AD8616 operational amplifier produced by Analog Devices. This OA has an input bias current of 200 fA..

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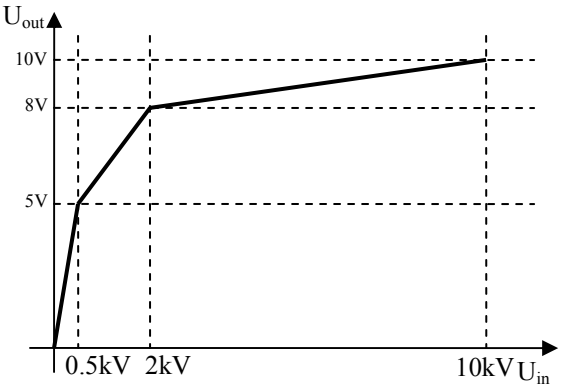

Fig. 2. The transfer function of the circuit

The schematic diagram of the functional transformer is presented in fig. 3. This is a classical functional transformer with diodes.

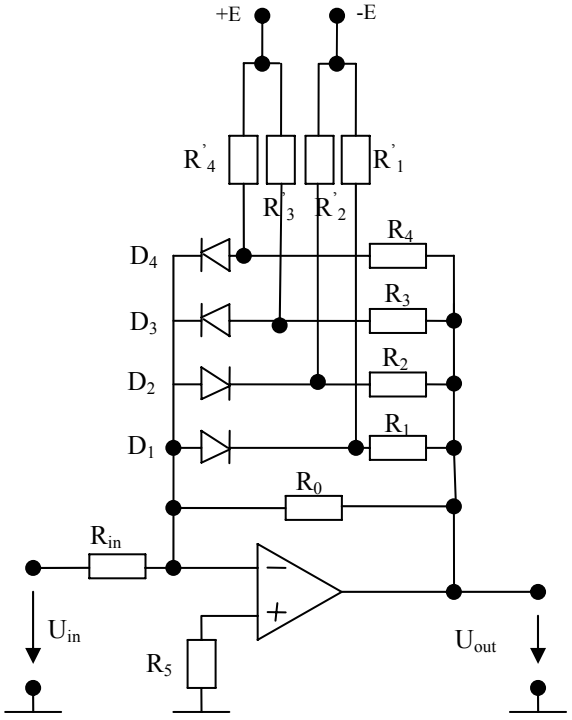

Fig. 3. Circuit schematic

The value of the input resistance R_{in} was chosen after multiples calculus and simulations to be 1MΩ. Starting from this values has been computed the values for the other resistors in the circuit. The first voltage divider consisting in R_{in} and R_0 must realize the first segment of the transfer function. If the input voltage exceeds the value of 500V, the diode D_1 begins to conduct and the resistor R_1 is introduced in the circuit. The result is that the resistor R_1 is now in parallel with resistor R_0 and the division ratio of the voltage divider is considerably higher then in the first case. If the input voltage is higher than 2kV, the diode D_1 is still conducting and the diode D_2 begins to conduct. In this case, the resistor R_0 is in parallel with R_1 and R_2. The division ratio is in this case bigger then the second case, end very big comparing to the first case. The resistances R_0, R_1 and R_2 is controlling the input voltage breakpoints, and the resistors R_0 , R'_1 and R'_2 is controlling the output voltage breakpoints. For the case presented here, it is possible to calculate the points of the transfer function, by determining the slope of each segment.

$$a_k = \frac{U_{out_{k+1}} - U_{out_k}}{U_{in_{k+1}} - U_{in_k}} \qquad (1)$$

After each slope is calculated, next is to calculate the division ratio of each divider, and the values of resistances composing the divider with relation (2).

$$\begin{aligned} &R_0 = a_0 \cdot R_{in} \\ &R_{ech1} = a_1 \cdot R_{in}\,, \quad R_{ech1} = R_0 \parallel R_1 \\ &R_{ech2} = a_2 \cdot R_{in}\,, \quad R_{ech2} = R_0 \parallel R_1 \parallel R_2 \end{aligned} \qquad (2)$$

The last step in the projecting of the circuit is to establish the breakpoints of the output voltage.

$$\begin{aligned} R'_1 &= R_1 \frac{V_{D1} - E}{V_{Out1} - V_{D1}} \\ R'_2 &= R_2 \frac{V_{D1} - E}{V_{Out2} - V_{D1}} \end{aligned} \qquad (3)$$

III. EXPERIMENTAL RESULTS

The circuit was simulated in PSpice using the model provided especially for AD8616 by Analog Devices. The results are very close to the projecting data. The figure 4 shows the transfer characteristic of the circuit.

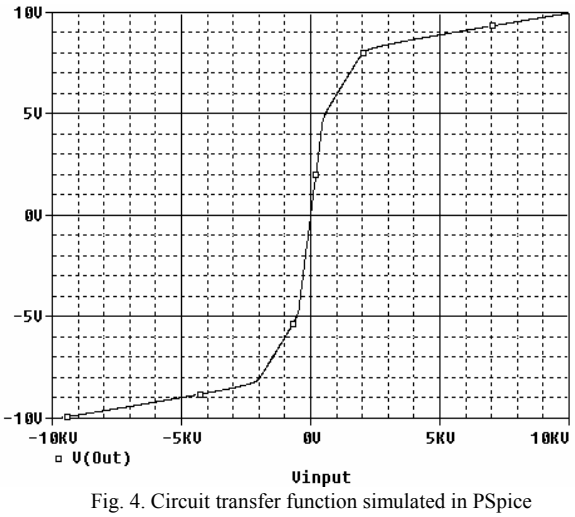

Fig. 4. Circuit transfer function simulated in PSpice

One thing that is interesting is the error on the breakpoints. Serious contributions to these types of error have the internal resistance of the diodes used, and the forward voltage drop of the diodes. This is a disadvantage of this kind of voltage divider.

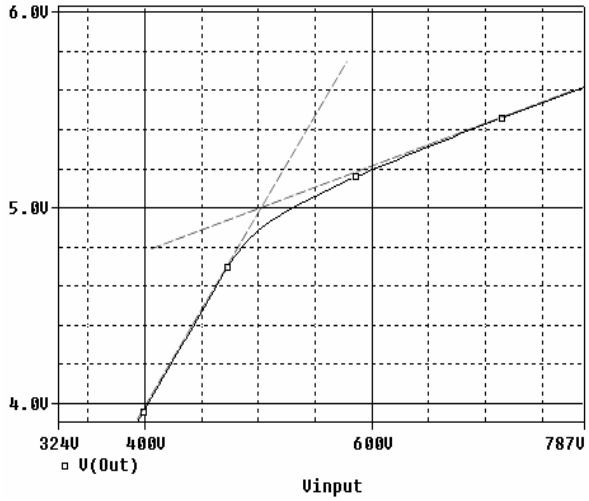

Fig. 5. Errors at 500V

As it can be seen in the figure 5, the ideal breakpoint (marked with dashed lines) is exactly at 500V and 5V. The real characteristic has a rounding error due to the fact that the diodes don't enter in the conductive state instantaneously. This error has a quantum of 1% from the output voltage.

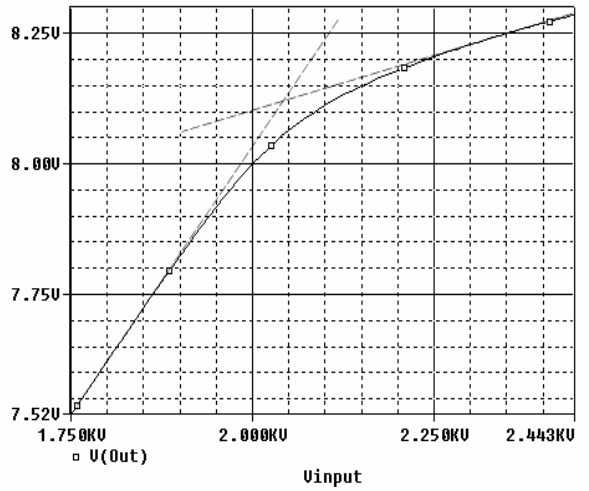

Fig. 6. Errors at 2kV

On the second breakpoint the error is significantly higher because of propagation from the first breakpoint. In plus, here is another error due to the fact that in the calculus of R_1 has been made some approximations about the forward drop voltage of the diode D2. The maximum error at this breakpoint is 1.5%.

In the last case, the error at 10kV is 0.2%. This error is made by the approximation of the value of diode D_2 conducting resistance, since its value is comparable with resistor R_2. To minimize this error the value of R_2 must be 5-10 times bigger than conducting resistance of diode D_2. But this is not possible, because increasing the value of R_2 will increase the value of the resistor R_{in} which is not a good idea as mentioned earlier in this paper.

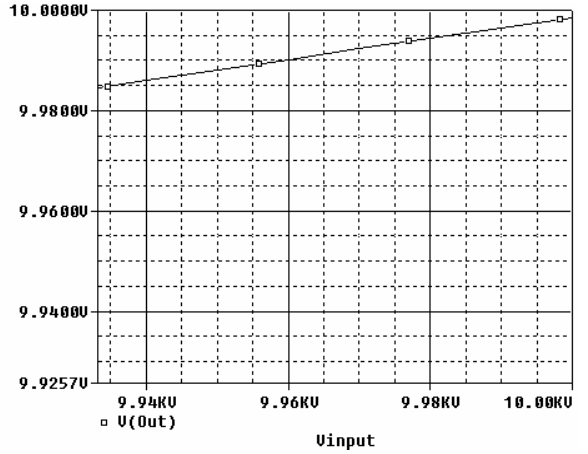

Fig. 7. Errors at 10kV

A parameter who might keep in count is the temperature. The temperature can modify the internal resistance and the forward drop voltage of the diodes. The influence of the temperature is shown in the figures below for each breakpoint.

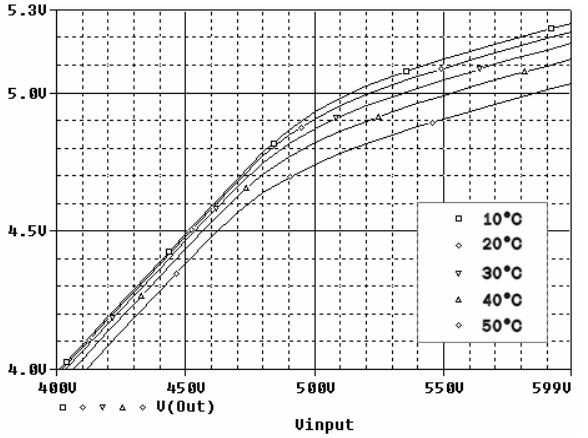

Fig. 8. The influence of the temperature at 500V

The temperature can modify the internal resistance and the opening voltage of the diodes, raising the error of the circuit.

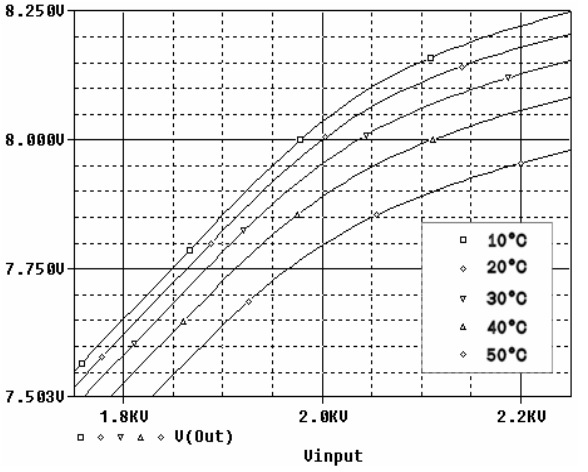

Fig. 9. The influence of the temperature at 2kV

It can be seen that the higher the temperature, the higher is the error.

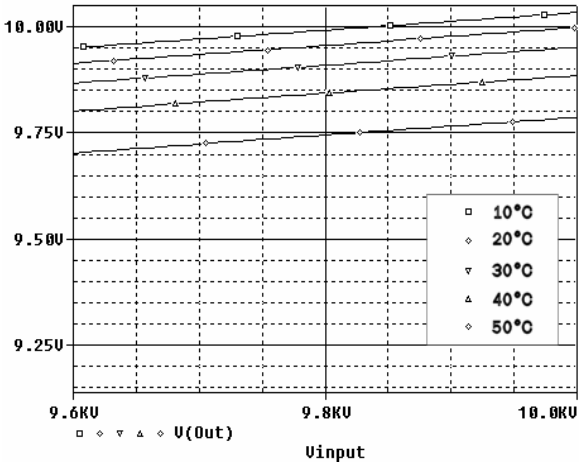

Fig. 10. The influence of the temperature at10kV

These variations of the output voltage with temperature must be eliminated.

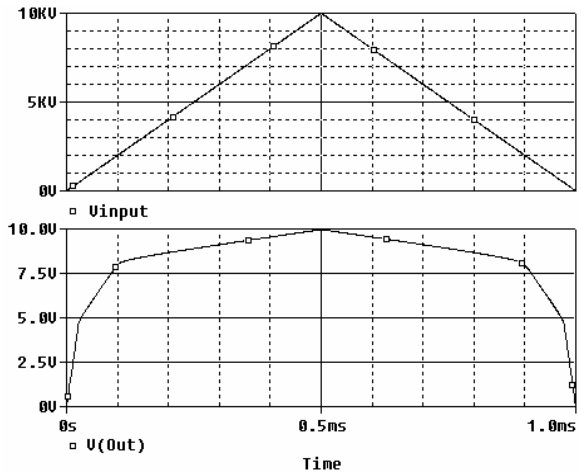

Fig. 11. Input and output signals

To see how the circuit works, at the input was applied a triangular signal because with this shape is more easy to observe how the circuit work. The triangular shape heaves a linear variation, suitable to observe any nonlinearity on the output signal.

The triangular signal has 1 kHz frequency and amplitude of 10kV. At the output of the circuit, the signal presents the 2 breakpoints at 5V and at 8V.

The output signal from the circuit is software recovered to the initial amplitude. In the figure 12 is shown both the input and recovered signal. The recovered signal has not the same shape with the input signal because of the errors on the first and second breakpoints. These errors can be software minimized. The triangular shape can be used in the process of minimizing these errors. The idea is to apply at the input of the circuit a triangular signal and to determine each error and her sign for discrete values of the input voltage. Then, with this values, can be made an interpolation to establish the shape of the variation of the errors.

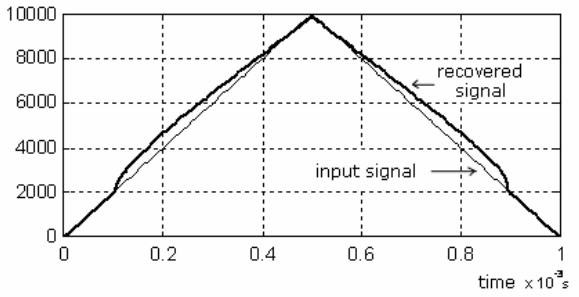

Fig. 12. Software recovered signal

The spectral analysis of the input and recovered signal show a significant modification in the recovered signal spectrum, especially the apparition of the second order harmonics.

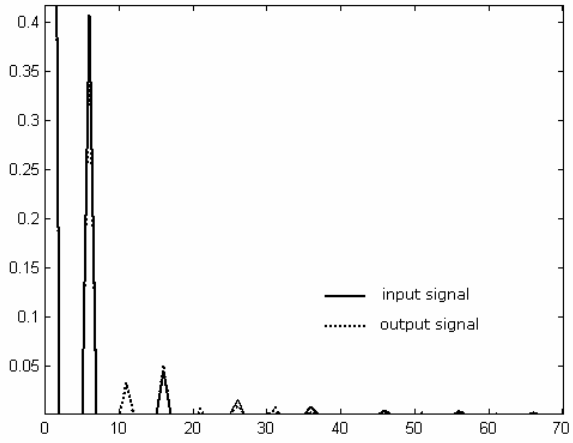

Fig. 13. FFT of the input and recovered signal

Because the triangular signal is rarely present in practical conditions, we are chose two types of signals more present in practical conditions: the spike and the damped oscillatory wave.

Most high amplitude disturbances in the electrical power system heave a spike shape.

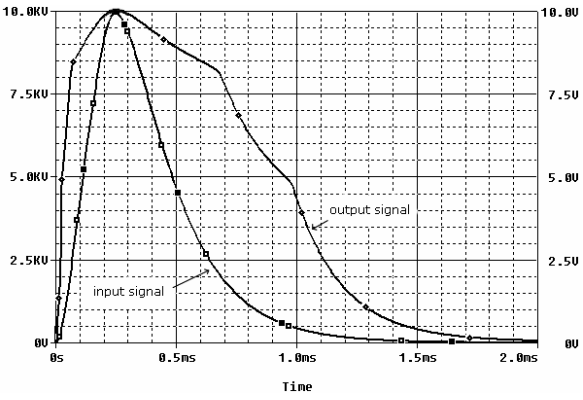

Fig. 14. Spike signal

The spike disturbances are an extremely high and nearly instantaneous increase in voltage with a very short duration measured in microseconds. Spikes are often caused by lightning or by events such as power coming back on after an outage. In the figure 14 is represented a spike input signal and the signal at the output of the circuit.
The signal from the output of the circuit is applied to the recovery block resulting in a signal with the shape verry similar to the shape of the input signal. The error is due to the breakpoints of the transfer characteristic of the circuit. It can be observed in the figure 15 that at 2kV the error heaves an important value (25%), because of propagation of the error from the first breakpoint. At 500V the error is smaller (about 15%), but unfortunately this error amplifies the error at the second breakpoint.

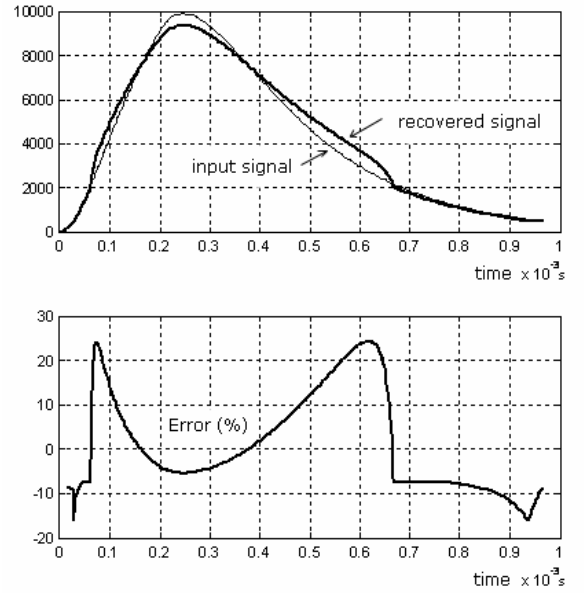

Fig. 15. Biexponential signal applied at the input and the recovered signal

At the 10kV, the recovered signal is smaller than the input signal, at this point the error is about 5%.

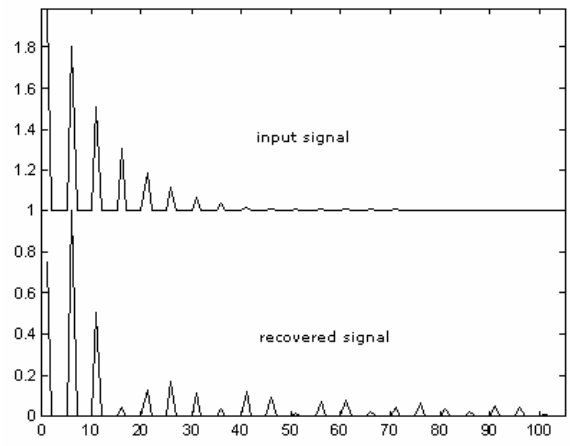

Fig. 16. Spectrum of the spike input and recovered signal

To minimize this errors, it can be observed that if to the output signal is applied a constant voltage, the error can be reduced at about 10%.
In the spectrum of the recovered signal can be observed an increased number of high frequency harmonics. This harmonics is generated by the circuit transfer function around the 2kV breakpoint. The transition around the 2kV is not smooth, which generate the high frequency harmonics.
Another type of disturbances is the sag disturbances. Sag is defined as a short duration drop in voltage. The amplitude of the electrical power system decreases to 0.9 of their nominal value, but this is not always done instantaneously. Such type of disturbances is presented in the figure 17.

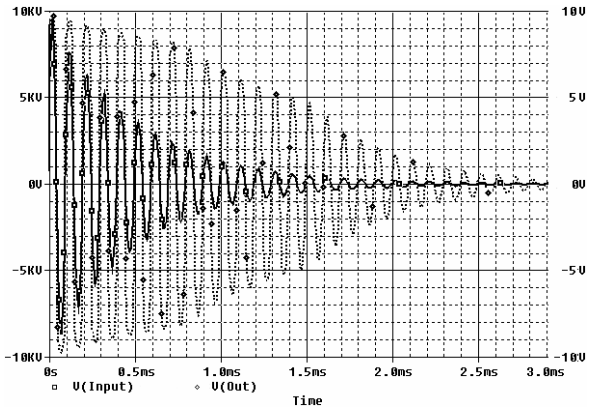

Fig. 17. Damped oscillatory wave

Basically, this disturbance consists in a sine wave with the amplitude varying over an exponential shape. With continuous line is plotted the input signal, and with dotted line is plotted the signal at the output of the circuit.

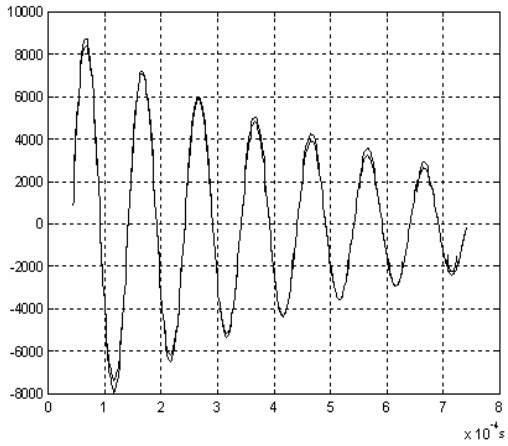

Fig. 18. Damped oscillatory wave at the input of the circuit and after the software recovery

The signal of the output of the circuit is applied to the recovery block to reconstruct its original shape. The differences between the input and the recovered signal are relatively small, the maximum errors being 10%. In this case, the error at 2kV is smaller than the case of the spike. In the figure 19 is represented the

relative errors at the peaks of the damped oscillatory wave.

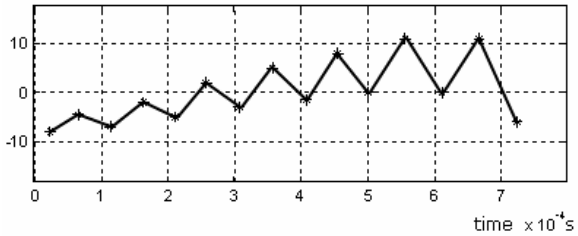

Fig. 19. The relative errors of the maximum amplitude of damped oscillatory wave after the software recovery

Around the value of 10kV the errors are negatives and their values are under 10%, being smaller around 6kV and increasing again when the amplitude of the signal becomes around 2kV. The bigger value of the errors for smaller amplitudes of the signal is not an inconvenient. It can be observed that the errors for the positive and negative side of the signal are not the same value and sign. This is caused by the diodes on the positive and negative side of the functional transformer, diodes which don't heave the same conductive resistance and the forward drop voltage. To prevent this, the diodes must be carefully selected.
Like in the other cases, the spectrum of the recovered signal presents high frequency harmonics.
This harmonics is produced, like in the cases above, by the breakpoints of the circuit and it is necessarily to reduce their amplitude.

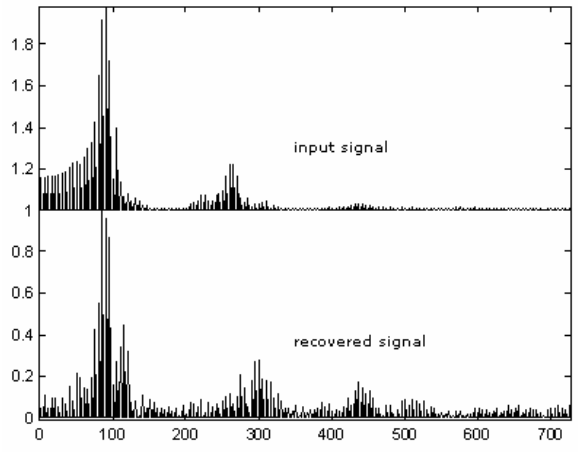

Fig. 20. Spectrum of the damped oscillatory wave

IV. CONCLUSIONS

Analyzing an important parameter of the signal, the power of the input and recovered signal, it has been observed that the relative error of the power of the triangular output signal is 6%, so the power of the output signal is 0.06 times bigger than the input signal power. For the spike signal, the relative error of the power of the signal is 1.86%, and for the dumped oscillatory wave, this error is -6.1%.
For the spike signal we observed that the rise time of the recovered signal is decreased with about 10% from the input signal, and the time at half amplitude is increased with 11% from the input signal.
To maintain the accuracy of the output voltage the circuit must be compensated with the temperature. A maximum error value of 5% is satisfactory for the goal proposed. To maintain the error at this point it's necessarily to thermally isolate the circuit. A ±2 ºC in temperature variations is maximum allowed. To reduce the errors caused by the diodes, it must be known the conductive resistance and the forward drop voltage. The diodes are the elements that generate the biggest error in the circuit. The diodes must be selected carefully to heave the same parameters. The errors at the first and second breakpoint can be software corrected, once their shape is known. For that, the software recovery circuit must heave a self calibration circuit to minimize this type of errors.
Another source of errors is the resistive elements of the circuit like resistors and PCB. All resistances must heave a maximum error of 0.5%.

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Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 51(65), Fascicola 1, 2006

High input, wide output voltage range linear regulators

Valentin-Ioan Maranescu[1], Cătălin D. Căleanu[1], Corneliu I. Toma[2]

Abstract – This paper proposes a method to obtain a high input voltage stabilizer by connecting adjustable voltage regulators in series. Wide output voltage range, maintaining maximum current was obtained without secondary breakdown risks. A method to equal distribute the power dissipation on series regulators was proposed leading to an extended equivalent safe operating area.

Keywords: voltage regulator, wide voltage range, safe operating area (SOA), thermal transfer.

I. INTRODUCTION

Integrated voltage regulators (VR) are common electronic devices present in almost all applications. VR offer constant voltages in conditions of input voltage variations and/or load current variations. Since they were first designed, three pins VR are the most used, due to their good performances and minimum number of external components requirement [1],[2]. Although a large variety of three pins VR exists, with fixed or adjustable output voltages, voltage regulators with inputs over 40V are hard to integrate due secondary breakdown risk of theirs pass element [3],[4],[5]. Adjustable high input stabilizers, with wide output voltage range are demanded for laboratory power supplies applications.

A method to extend the input voltage range for a voltage stabilizer is to add an element in series with the voltage regulator input. This element can be a simple wattage resistor, a bipolar transistor or even a voltage regulator. Using a resistor instead of a regulator will have the disadvantage that the voltage drop across it depends on the load current. A minimum load current is required in this case to avoid stress over datasheet maximum input voltage V_{IMAX} of the regulator. Fig.1. present a solution recommended by producers in theirs datasheets [6]. Connected in series with a preregulation transistor or a voltage regulator is possible to set a fixed voltage drop across output regulator. The line regulation is improved due to the constant input voltage of the output VR set by the preregulator. This solution will increase the input voltage range only with the fixed voltage drop set across the output regulator. The efficiency of this solution is optimum just if the output voltage is fixed or adjustable in a narrow range, in this case, the voltage drop across both regulators can be set almost equal, and the integrated protections [5] will start to work simultaneously. Except the fixed or narrow output voltage range, the equivalent safe operating area (SOA) of the stabilizer will gain just a small improvement, depending on preregulation element SOA. In the case of using a preregulation transistor, no protections to short circuit, overheating, or secondary breakdown will be available for it, requiring supplementary circuitry.

In this paper, we propose a solution to series interconnect two VR in order to increase the maximum input voltage V_{IMAX} of the stabilizer, and extended in the same time the output voltage range, without to reduce maximum load current, providing an efficient use of theirs SOA in all input and load conditions.

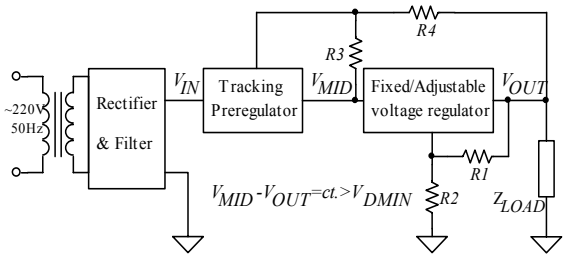

Fig.1. High input voltage range
stabilizer using a tracking preregulator

II. EXTENDED RANGE ADJUSTABLE VOLTAGE REGULATOR

Our proposal to extend to maximum both input and output voltage range of the stabilizer is presented in fig.2. It has the main advantage that keeps both the output VR and input VR with equal voltage drop across in the case of input voltage variations, or load variations. Voltages drop across each regulator are kept equal even when output voltage is adjusted, leading always to equal power dissipations on both VR. Because both input VR and output VR, adjust

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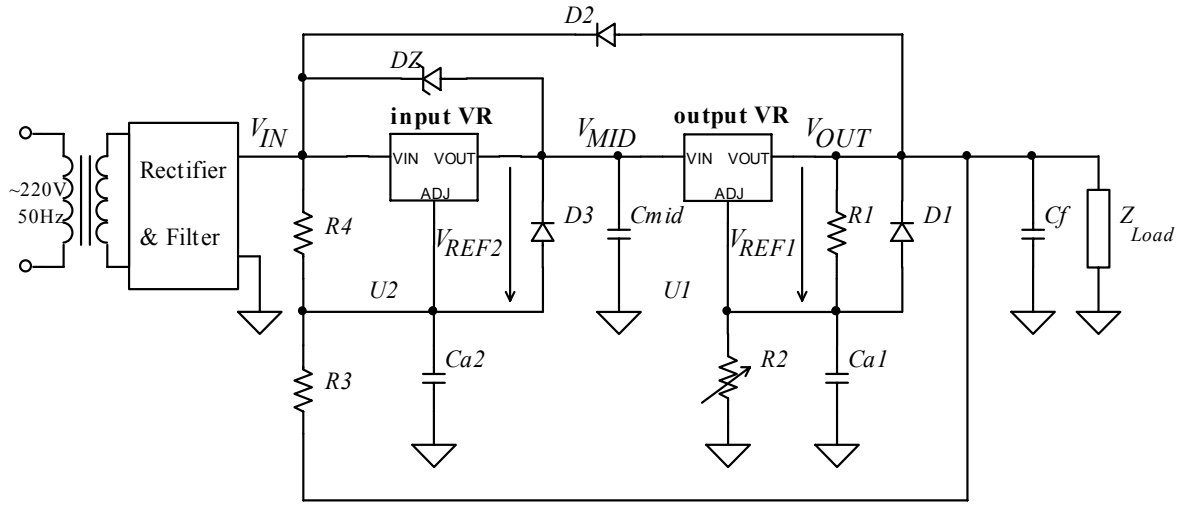

Fig.2. High input, high output voltage range - series regulators.

their input to output voltage drop when stabilizer output voltage is adjusted, twice the maximum output range compared with a single VR supply is obtained. This is an advantage compared with solutions using fixed voltage drop across output VR, where the maximum output voltage range is increased just with fixed voltage drop set across output VR, which usually is set with a few volts over minimum voltage drop V_{DMIN} to keep "cold" the output VR.

To achieve an equalization of the voltage drop across series regulators, the adjusting pin of the preregulator is biased from a resistive divider powered by input to output voltage difference $V_{IN,OUT}$ of the stabilizer. Neglecting adjusting pin current, the common net voltage V_{MID} is:

$$V_{MID} = k \cdot V_{IN} + (1-k) \cdot V_{OUT} + V_{REF2} \qquad (1)$$

Where V_{REF2}=1.25V represents the most usual value of the reference voltage within an adjustable regulator, and k the division ratio of input to output voltage at the adjusting pin of the input VR:

$$k = \frac{R3}{R3 + R4} \qquad (2)$$

Then, the voltage drops across pass element within regulators are:

$$V_{IN,MID} = (1-k) \cdot (V_{IN} - V_{OUT}) - V_{REF2} \qquad (3)$$

$$V_{MID,OUT} = k \cdot (V_{IN} - V_{OUT}) + V_{REF2} \qquad (4)$$

For an efficient use of the SOA for both regulators, these voltage drops must be set equally especially for maximum input voltage and lowest output voltage values, this situation representing the case of maximum power dissipation on regulators at maximum current load. The theoretical optimum value for k is obtained equalizing voltage drop across regulators in (3) and (4) for worst-case input and output conditions, resulting in:

$$k_{opt} = \frac{1}{2} - \frac{V_{REF2}}{V_{IN,MAX} - V_{OUT,MIN}} \qquad (5)$$

When choosing *R3* and *R4* to set k value, using equations (2) and (4), we must consider the V_{REF2} value factory dispersion, and the tolerances of resistors within divider. The minimum worst-case value of k must be greater than k_{opt}. To avoid the need of a minimum load current, and to improve regulator efficiency [7], *R3* and *R4* must not sink a current lager than adjusting resistors of the output regulator, this involving the following condition:

$$R3 + R4 > R1 \cdot \frac{V_{IN,MAX} - V_{OUT,MIN}}{V_{REF1}} \qquad (6)$$

To keep always voltages drop across regulators equal, the output VR must be the one that control the input VR. For the safety of the supply, the situation must be under control even when regulators reach theirs SOA margin. Voltage regulators present a decrease of the maximum limiting current as a function of voltage drop, to keep pass element in its SOA [4]. To be sure that output regulator will be first that limit the current, the voltage drop across it must be set slightly larger (with a few volts) than the voltage drop across the input regulator, by setting minimum worst-case k slightly over k_{opt}.

In the case of maximum current I_{MAX} values dispersion, it is possible for an overload that the input regulator to be the first that limit the current, resulting in an increase of its voltage drop. To prevent unbalancing the regulators voltage drops with the risks of theirs pass element breakdown, a breakdown diode *DZ* will limit the voltage drop across input VR.

The breakdown voltage of this diode must half of the maximum input to output voltage drop of the stabilizer, value that must be under V_{IMAX}. Protection diodes *D1* and *D2* will prevent reverse biasing of the regulators when having a large capacitive load at the output and input is short-circuited or fast discharged. Diode *D3* will prevent reverse biasing of the input VR.

Capacitors *Ca1*, *Ca2*, *Cmid* will help to improve response to input transients, and *Cf* will improve response to load transient [6].

By equally distribute power dissipation on regulators, the stabilizer equivalent SOA increases almost twice, keeping same I_{MAX}, but for an extended voltage range. In fig 3. the results obtained with SPICE [8] simulation for the new equivalent SOA are plotted. The area between V_{DMIN} and $2*V_{DMIN}$ will be lost, because the new equivalent voltage drop is twice as in the case of a single voltage regulator. Defining:

$$r(V_{IN,OUT}) = \frac{I_{OUT,MAX}(seriesVR)}{I_{OUT,MAX}(singleVR)} \qquad (7)$$

where $I_{OUT,MAX}(seriesVR)$ and $I_{OUT,MAX}(singleVR)$, represent maximum output currents at voltage $V_{IN,OUT}$ for series respective single VR. It can be observed from SOA simulations that this ratio becames greater than unity for $V_{IN,OUT}$ range where single VR output current is limited to keep power dissipation to a maximum value. As we state in a previous paper sing series pass elements configurations [9], series VR lead to an improvement of SOA at high voltage input range compared with a single regulator. Around V_{IMAX}, a maximum improvement for the value of *Iout*max was achieved. The new line regulation *LINREG* is worst compared with fixed drop voltage across output regulator solution, being reduced to *LINREG* of a single VR.

III. THERMAL TRANSFER

The voltage regulators will use a common heat sink with one of the regulators isolated from the heat sink because of series connection. The input regulator has a larger temperature margin due to its slightly smaller power dissipation. This will be a reason to choose to isolate the input VR from the heat sink, helping also to equalize the junction temperatures. The equivalent schematic with electrical lumped elements is presented in fig.4.a). In order to obtain equal junction temperature, the electrical isolation of the input VR can be compensated by unbalancing the power dissipation on voltage regulators. The condition to obtain equal junction temperatures is:

$$Pd1\cdot(Rjc1+Rcs1)=Pd2\cdot(Rjc2+Rcs2) \quad (8)$$

where P_{D1}, P_{D2} are power dissipations on output respective input VR, and R_{JC1}, R_{JC2} - junction to case thermal resistances, R_{CS1}, R_{CS2} - case to sink thermal resistances of output respective input VR using a common heat sink with R_S thermal resistance, in ambient temperature *Ta*. In the case of input VR heat sink isolation, R_{CS2} will include thermal resistance of the isolation. If VR have identical cases, then $R_{JC1}=R_{JC2}=R_{JC}$, $R_{CS1}=R_{CS}$, $R_{CS2}=R_{CS}+R_{IS}$. By replacing $P_{D1}=V_{MID,OUT}\cdot I_{OUT}$, $P_{D2}= V_{IN,MID}\cdot I_{OUT}$ in eq.(8), we obtain the relationship between thermal resistances and voltage drop across regulators that lead to equal junction temperatures:

$$\frac{V_{MID,OUT}}{V_{IN,MID}} = \frac{R_{JC}+R_{CS}+R_{IS}}{R_{JC}+R_{CS}} \qquad (9)$$

In the case of equal junction temperatures, the equivalent thermal schematic will have thermal resistances connected in parallel, as presented in fig.4.b). This is thermally equivalent with increasing

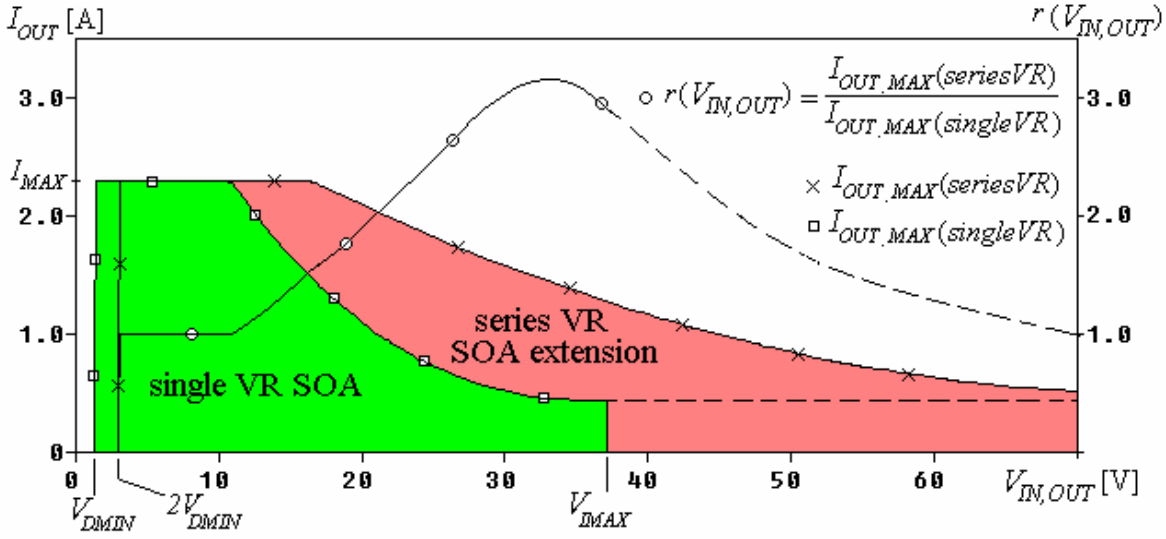

Fig.3. Simulated equivalent SOA extension for series voltages regulators

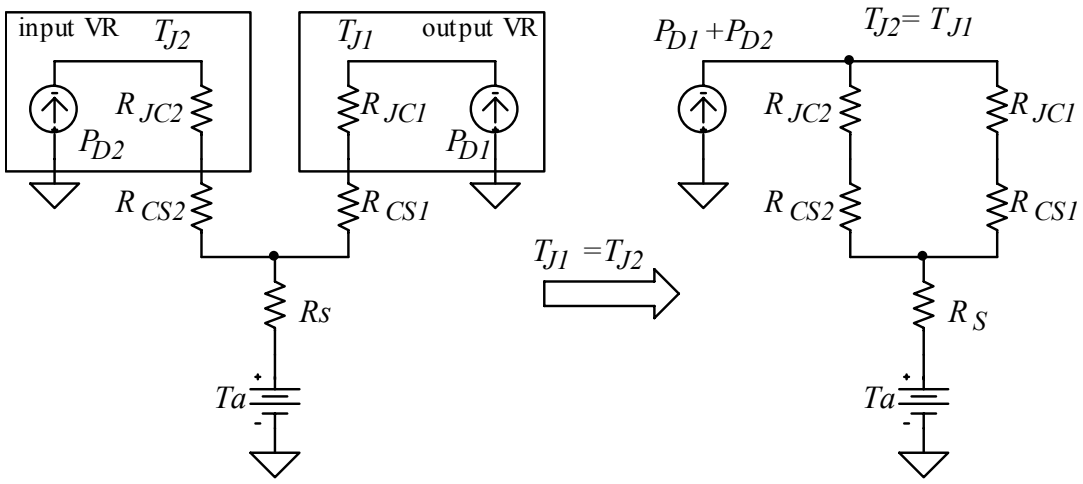

Fig.4. Equivalent thermal schematic with lumped elements for series regulators sharing same heat sink.
a) $T_{J1} \neq T_{J2}$ b) $T_{J1}=T_{J2}$

twice the area used to transfer the heat from junctions to sink. If we compare heat transfer at equal total power dissipation, series VR are more efficient than a single VR, by reducing junction's temperatures in similar line and load conditions.

From eq. (9), we conclude that equal voltage drop and equal junction's temperatures are possible just if thermal paths of both regulators are identical, leading also to an optimum thermal transfer. If VR have low R_{JC} cases, then by isolating one VR, strong unbalanced voltages drop are needed to equalize junction temperature. For voltage unbalanced voltages drop, the maximum input voltage range must be lower to protect against breakdown the input VR [3]. Low R_{JC} involve a tradeoff between equalizing junction temperatures or voltage drop across VR.

IV. CONCLUSIONS

High input voltage, wide output voltage range stabilizer was achieved by series connecting two voltage regulators, and equally distribute voltage drop across them. Solution can obtain optimum thermal transfer for identical thermal paths for both regulators. Having identical thermal paths, proposed solution lead to maximum input voltage range being twice the range of a single VR, in this case the equivalent SOA of proposed stabilizer representing twice the SOA of each regulator. As disadvantages of our proposal, we mention the increasing of V_{DMIN} to $2*V_{DMIN}$, and a low extension of the SOA for low thermal resistance cases, when tradeoffs between input voltage range maximum current at high voltage drops are demanded.

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Current-Steering Digital-to-Analog Converter/ Programmable Sub-Bandgap Voltage Reference with Split Input Code

Mircea Tomoroga, Lucian Jurca, Mircea Ciugudean[1]

Abstract - In this paper we will offer a concrete solution of a DAC which will be used in high speed and medium resolution applications. This DAC presents an important innovation as the voltage reference does not represent a distinct block, but it overlaps the functional diagram of the converter. This was considered to be of current-steering type with MOS transistors in standard CMOS technology like in most of the recent works. The new solution also implies the splitting in two equal parts of the digital input code applied to the converter. This will drastically diminish the number of large dimension transistors used in the current sources of the converter.
Keywords: current-steering digital-to-analog converter, sub-bandgap voltage reference, split input code

I. INTRODUCTION

The recent tendency in the field of analog and mixed integrated circuit manufacturing is to use technological processes which are accessible in terms of price as the standard CMOS process. Furthermore the supply voltages become lower and lower to meet the growing request of portable equipments on the market. Most of the works which deal with the subject of Nyquist frequency DAC-s design suggest the use of a reference voltage source which must be able to work at these low supply voltages. Thus, sub-bandgap reference voltage sources have been developed [8], [9], [10] and obviously they provide an output voltage lower than 1.2V.
There are two premises as starting point of this paper:
1. The sub-bandgap voltage source is attached to DAC either as a distinct integrated circuit or it is integrated in the same chip next to the converter as it is presented in [1], [2], [3], [4].
2. The most widespread types of Nyquist frequency DAC-s are current-steering DAC-s, a statement sustained by recent works, such as [1], [2], [4], [5]. For these types of converters, exact theoretical models have been elaborated. These models allow an easy evaluation of the static and dynamic performances of the converter [5], [6].
Taking into consideration these two aspects, we will show along this paper how the sub-bandgap source and the DAC will be joined in a single, inseparable circuit which will benefit of the qualities of both circuit types.

II. SUB-BANDGAP VOLTAGE REFERENCE

It is known that the bandgap voltage has two components: the first is represented by the voltage across a directly biased junction and the second is proportional to absolute temperature (PTAT). The negative temperature coefficient of the first component (-2mV/K) is compensated by the positive coefficient of the second. If, in order to get the PTAT voltage, the thermal voltage $V_T=kT/q$ is used, this has to be multiplied with approximately n=23. In these terms the bandgap voltage is given by equation (1):

$$V_{BG}=V_{BE}+n\frac{kT}{q} \qquad (1)$$

and it is ≈1.2V. In equation (1) k is Boltzmann's constant, T is absolute temperature and q is electronic charge.
By using a low supply voltage (e.g. 1V) it is obvious that the 1.2V value can not be produced anymore. However a fraction of this voltage with the same thermal properties can be generated if we can produce currents proportional with both V_{BE} and V_T. These currents will be weighted, summed up and injected in a resistor to obtain the desired output voltage. Finally, the value of the reference voltage will be obtained as a fraction of bandgap voltage, established by a resistor ratio. This type of circuit was suggested by Banba and Malcovati in [8] and [9] and it is shown in fig.1.
Through the pnp-lateral transistors Q1 and Q2 connected as diodes and with the ratio of emitter junction areas equal to N_E, the same current will pass, imposed by current mirror M1, M2 (pMOS transistors). As the operational amplifier (OPAMP) forces the potentials Va and Vb to be equal, the voltage across the resistor R0 will be $U_{R0}=\Delta V_{BE}=V_T\ln(N_E)$ and so the currents through R1

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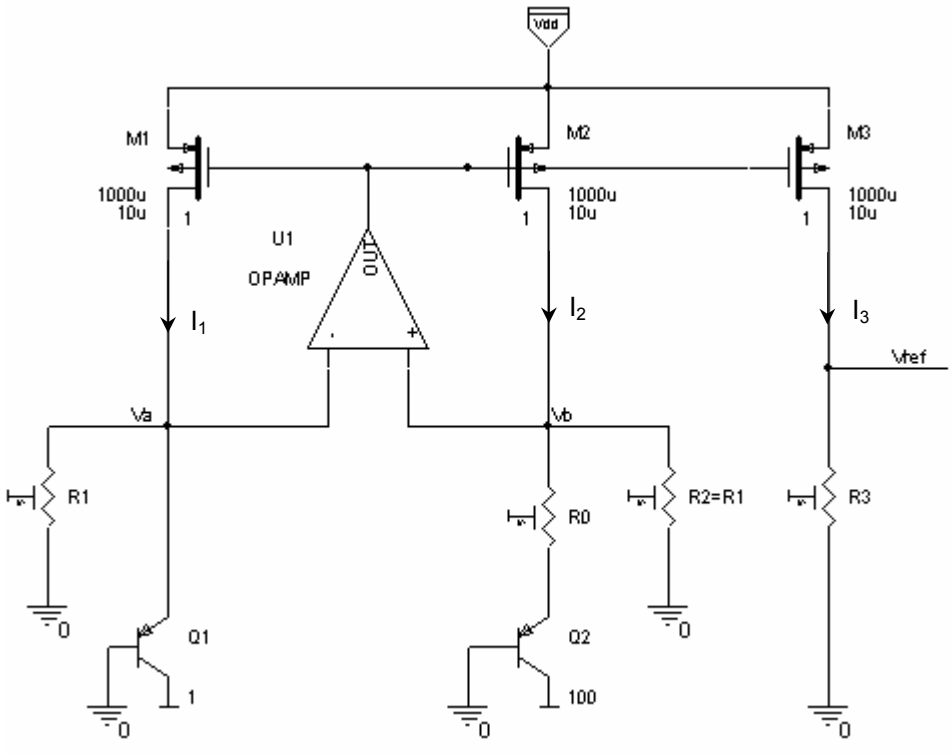

Fig.1 Sub-bandgap voltage reference

and R2, which are equal, will be proportional to V_{BEQ1} (i.e. they will have a negative temperature coefficient). Thus, the currents through M1, M2, M3 which are identical will have the following value:

$$I_1 = \frac{V_T \ln(N_E)}{R_0} + \frac{V_{BE}}{R_1} \tag{2}$$

The output voltage will be:

$$V_{out} = I_1 R_3 = V_T \frac{R_3 \ln(N_E)}{R_0} + V_{BE} \frac{R_3}{R_1} = \\ = \frac{R_3}{R_1}\left[\frac{R_1 \ln(N_E)}{R_0} V_T + V_{BE}\right] \tag{3}$$

The thermal compensation of the output voltage will take place only if :

$$\frac{R_1 \ln(N_E)}{R_0} = 23 \tag{4}$$

As we can see, the bandgap voltage of 1.2V can be weighted by the ratio R3/R1 and if R3 is small enough, very low value reference voltages can be obtained.

For example, imposing the value of the output voltage 0.5V, for N_E=100 the following values of the resistors resulted: R1=R2=80kΩ, R0=18.14kΩ and R3=34kΩ. Only R3 will change if we establish another value of the output voltage.

III. BLOCK DIAGRAM OF PROPOSED DAC

As it was shown in section II, the sub-bandgap reference taken into consideration allows us to obtain a current independent of temperature which is mirrored in the third branch of the circuit and injected in the resistor R3. This resistor must be made of the same kind of material as the other resistors from the circuit. We can say that the voltage reference becomes programmable if we can programme the value of R3.

Another way to obtain a programmable output voltage is to mirror the output current of the reference in more branches through which the currents are switched or not towards the resistor R3 of constant value. If, by using the unit element principle, like in [5], we add 2^N-1 unit current sources controlled by N switches which are supposed to lead or not a current through R3 we could obtain an N-bit DAC. Surely, the LSB will control a single unit current source, the next will control two unit current sources, while the MSB will control 2^{N-1} unit current sources.

As both the current sources block and the resistor R3 belong equally to the voltage reference and to the converter or, more precisely, because, in fact, the whole converter is included in the sub-bandgap mechanism, we obtained a single, inseparable circuit resulted from the overlapping of the two types of circuits.

In order to avoid a sudden current step on the switched current sources we must ensure dual, complementary current outputs. Thus, the currents corresponding to the digital input code as well as those which will not contribute to the output voltage manufacturing will be summed up in two distinct

nodes and will be led through equal value resistors towards the ground.

The major disadvantage of this type of converter is that it used a very large number of pMOS transistors. The number of the transistors which make up the unit current sources (which have to be of large dimensions in order to ensure a perfect equality of unit currents) is 2^N-1. For example, if N=10, we must use 1023 transistors.

Our new solution implies the splitting into equal parts (for an even number of bits) of the digital input code applied to the converter. In these conditions, we will have two identical blocks. Each block will be controlled by N/2 bits and will contain $2^{N/2}$-1 unit current sources. In order to ensure the weighting of $2^{N/2}$:1 in the output voltage contribution, the nodes in which the currents of the two blocks will be summed up are connected as shown in fig.2. The ratio of resistor values R8 and R9 (which replace R3), respectively R10 and R11 (for the complementary output) must be $2^{N/2}$-1. This will drastically diminish the number of large dimension transistors used in unit current sources. For example, if N=10, we must use only $2\times(2^5-1)=62$ transistors.

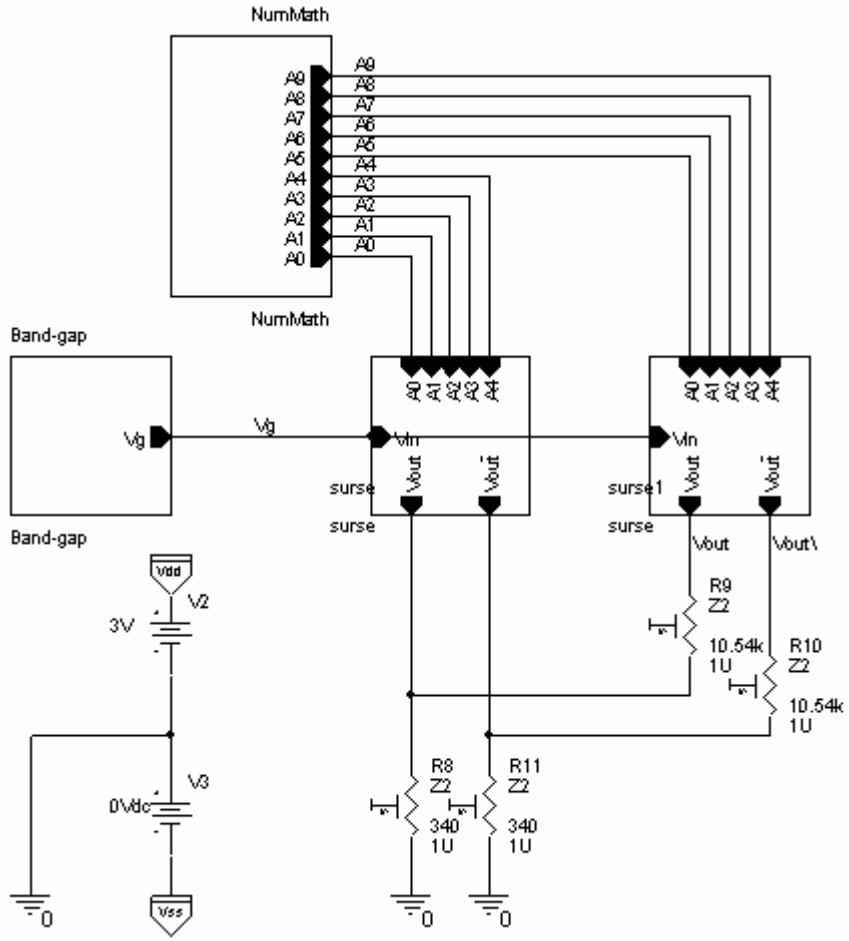

Fig.2 Block diagram of proposed DAC

The maximum number of bits of a converter that doesn't need trimming for the resistors mentioned above is given by the precision with which we can manufacture the ratio of the resistors and which is 0.1%, i.e. 1:1000 or roughly $1:2^{10}$. This limits the resolution of the converter to 10 bits.

In fig.2, the delimitation between the blocks "Band-gap" and "Surse" is purely formal and it was adopted for optimising and organising the block diagram of the converter on hierarchical blocks.

IV. DAC DESIGN AND SIMULATION

As mentioned in the previous section the ratio between R8 and R9 (which replaced R3 from fig.1) must be 1:31. As follows, we note the equal currents through the two first branches of the sub-bandgap block I_{BG} and the currents generated by the unit current sources I_u. The transfer function of the converter will be:

$$V_{out} = 1{,}2\frac{I_u}{I_{BG}}\left(\frac{R_8}{R_1}\sum_{i=0}^{4}A_i 2^i + \frac{R_8+R_9}{R_1}\sum_{i=0}^{4}A_{i+5}2^i\right) =$$

$$= 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}\left(\sum_{i=0}^{4}A_i 2^i + 32\sum_{i=0}^{4}A_{i+5}2^i\right) =$$

$$= 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}\left(\sum_{i=0}^{4}A_i 2^i + \sum_{i=0}^{4}A_{i+5}2^{i+5}\right) =$$

$$= 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}\sum_{i=0}^{9}A_i 2^i = 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}2^{10}\sum_{i=0}^{9}A_i 2^{i-10}$$

[V] (5)

Imposing the resolution of the converter to be 0.5mV and $I_u/I_{BG}=1/10$ ($(W/L)_u/(W/L)_{BG}=1/10$) the resulting values of the resistors R8, R9, R10 and R11 are shown in fig.2. The maximum output voltage of the converter is 0.5mV×1023=511.5mV.

The structure of the "Surse" blocks which include 31 unit current sources each is presented in fig.3.

The structure of the "S_unitara" block from fig.3 and which includes a unit current source (M4) and the corresponding switch is shown in fig.4. .

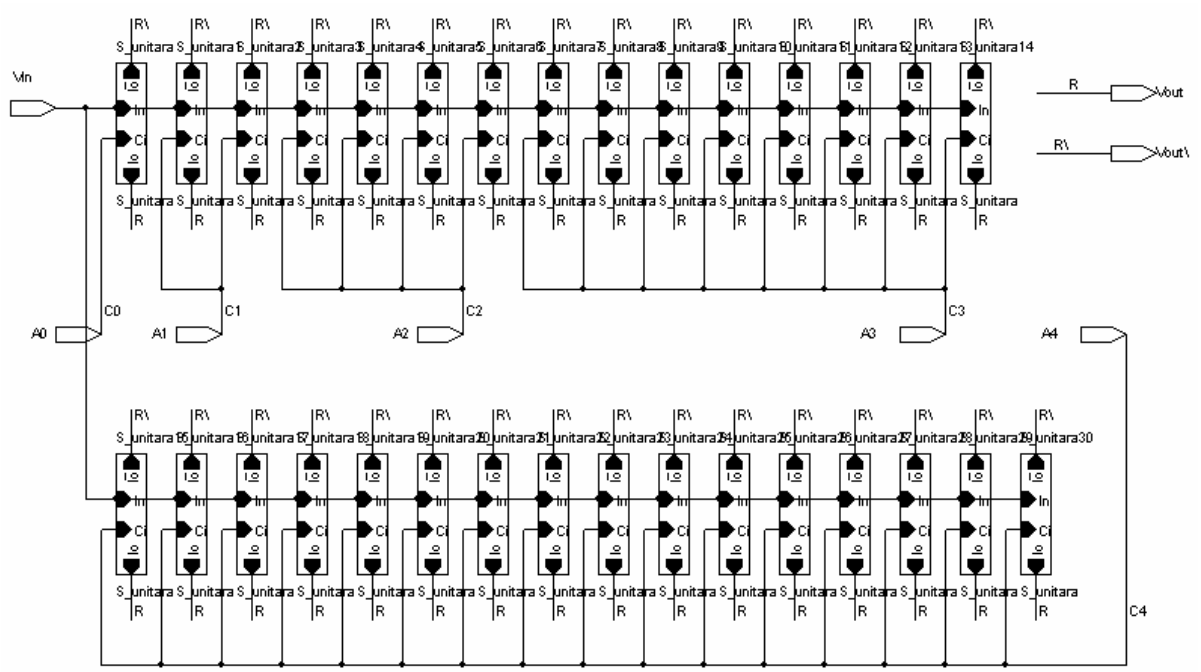

Fig.3 Structure of "Surse" blocks from fig.2

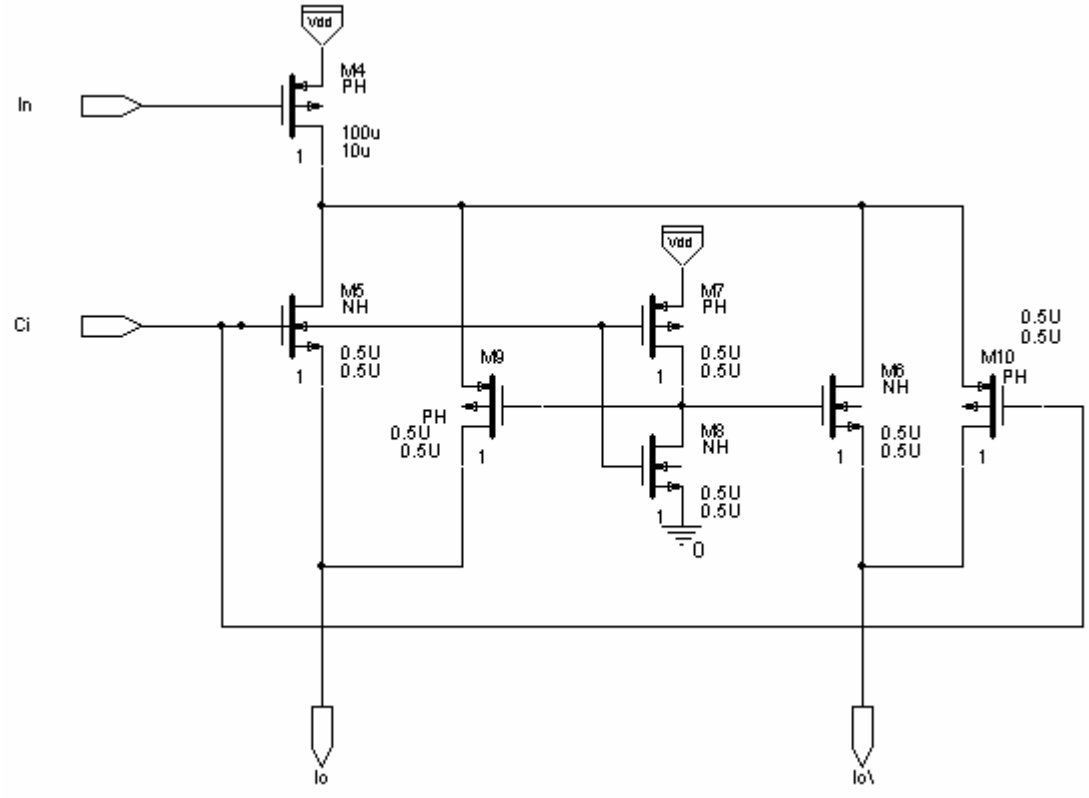

Fig.4 Structure of "S_unitara" block from fig.3 which includes a unit current source (M4) and the corresponding switch

In order not to affect the control voltage V_{GS} of the transistor M4 through which the reference current is imposed, the current switch was placed in its drain and it was made with two transmission gates M5, M9 respectively M6, M10 controlled in opposite-phase conditions to ensure a permanent conduction for transistor M4. The use of transmission gates instead of simple transistors is compulsory because the circuit works with low supply voltage and because a variable potential can appear at the outputs Io and Io/. In this way at least one transistor (out of M5, M9) is perfectly "on" and M4 is maintained saturated.

At the same time, the control with opposite-phase signals minimises the clock feedthrough. On the other hand the charge injection is also minimised because of the small dimensions of the switch transistors. The opposite-phase control is ensured by the inverter M7, M8.

The necessary digital stimuli for the simulation of the converter are provided by the block "NumMath". This is a counter built with elements that present ideal mathematical models of some circuit functions and which allows the generation of consecutive binary sequences in which all the bits are switched simultaneously. This block was designed according to [7].

The converter was simulated using OrCAD programme version 10.3 in which the models of the components correspond to 0.35µm CMOS process.

In the sub-bandgap reference we used an ideal model of the operational amplifier, but in which the gain was set at 1000 that corresponds to a real case, easy to obtain in design using only two amplifier stages. To ensure the stability of the circuit it was necessary to integrate a capacitance of 2pF between the inverting input and the output of the operational amplifier. As we can see in fig.5 the output voltage is set to 0.5V and it vary with only 1mV if the temperature changes from -30°C to 100°C.

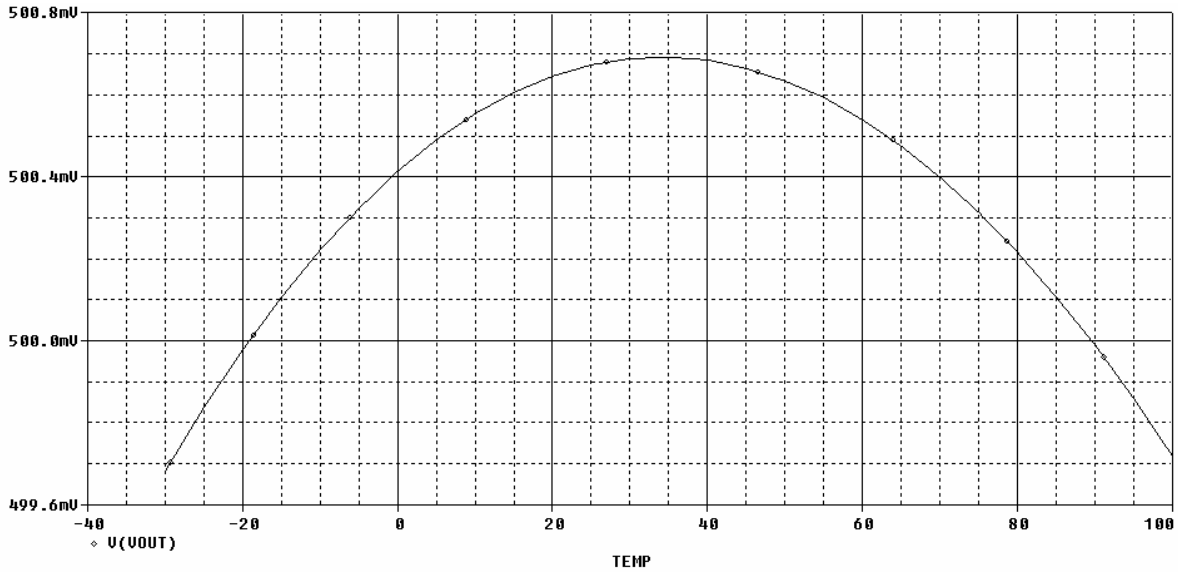

Fig.5 Simulation results of sub-bandgap voltage reference

The simulation of the whole converter was made by using a supply voltage of 3V, as we can see in fig.6, but similar results were obtained for lower supply voltages like 2V or 1V. This confirmed that the pMOS transistors of the unit current sources remained in the saturation region. As we can observe from fig.6.b the converter works very good at 10MHz because, despite the glitches that appeared, the settling time of the converter is not so much affected. If we examine the cursors, we can observe that the voltage step corresponds to the resolution of the converter and a DNL of about 15µV.

V. CONCLUSIONS AND PERSPECTIVES

In this paper we proposed a 10-bit current-steering DAC overlapping a sub-bandgap voltage reference. The converter is controlled by a split digital input code (2×5b) that allows a drastic diminishing of the number of unit current sources.

The solution presented here can be an excellent starting point to design a DAC with very good static and dynamic performances. Our future research will focus on:

-the second order correction for the sub-bandgap voltage reference for improving the thermal behaviour of the converter, as in [9];

-design of a high-speed operational amplifier that will be connected as follower with the inputs at the complementary outputs of the converter; this will diminish the effect of parasitic capacitance switching towards the nodes which don't have different potential anymore. We expect an important reducing of the glitches and an increasing of the converter speed;

-introducing a thermometer code (easy for the two 5-b sections of the digital input code) and a randomiser that would minimise the effect of the matching errors which affect the pMOS transistors of the unit current sources.

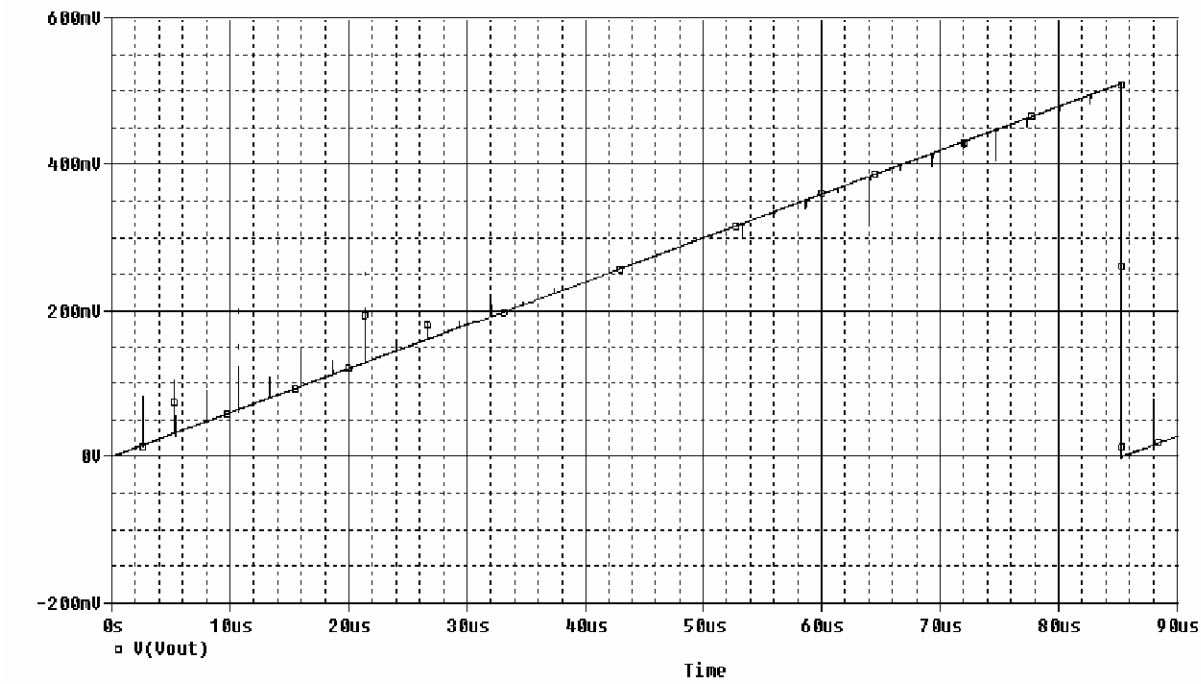

Fig.6.a Simulation results of DAC for all digital input combinations

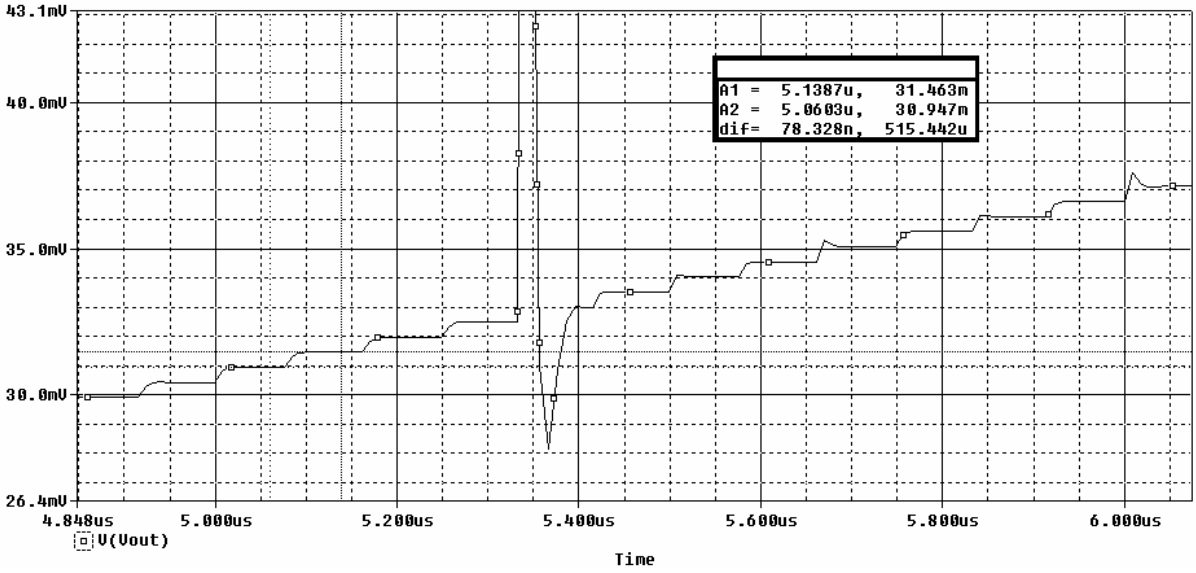

Fig.6.b Simulation results of DAC; detail of glitch

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Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

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Analysis and modeling of rain characteristics

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Abstract – Realistic modeling of rain characteristics is important in several domains, such as meteorology, agriculture and transportation. Rain generators need to have reproducible characteristics, while being able to simulate variability existing in natural rains. In the present work, several characteristics of natural rains were analyzed, then several working parameters of a rain generator were proposed and simulated.

Keywords: rain generator, rain modeling, statistics

I INTRODUCTION

The main objective of this work is modeling rain generators with controlled and reproducible characteristics. This leads to the problem of characterizing rains, and to decide which characteristics of natural rains have to be measured and controlled by the rain generator.
To this end some relevant papers modeling rain characteristics are briefly reviewed and it is shown how the desired characteristics can be obtained for artificially generated rain.

II. DEFINITIONS OF DIFFERENT RAIN TYPES

According to the Romanian National Institute of Meteorology (INMH) [1], rainfall can be classified as follows:

a) Light rainfall = precipitation in the form of rare, isolated drops, which leave traces on surfaces, and that lasts for a period longer than 2 minutes. The noise produced by the falling of the drops is small. This type of rain doesn't abase visibility under 10km; nevertheless, a decrease in visibility can be observed when the light rain starts falling again after a temporary discontinuity of rainfall, or by the diminishing of a heavier previous rainfall; fog is created under these conditions, by evaporating water from wet surfaces.
b) Moderate rainfall = in the form of compact drops, that can be isolated easily and which wet the surface quickly. The noise produced by this type of rainfall on roofs, spouts, leaves can be very well distinguished. Horizontal visibility is reduced below 10km, but is usually more than 4km.
c) Heavy rainfall = type of precipitation that falls in the form of waves, individual drops are no longer observable and water gathers quickly on surfaces. The noise produced by this type of rainfall is similar to a loud rattle. Horizontal visibility is reduced to less than 4 km.
Rainfall classification by rain rates according to INMH [1] is summarized in Table 1.

Table 1.
Rainfall classification according to INMH [1]:

Type of Rainfall	**Rain Rate [liters/m^2]**
Moderate	5 during 3h
Heavy	15 during 3h
Very heavy	15 in less than 3 hours
Maximum rainfall: 25l/m^2/1h	

II. RAINFALL PARAMETERS

The most important parameter of the rain is the amount of rainfall. The amount of rainfall is measured using a rain gauge. The most common intervals of measuring rainfall are: per hour, per 30 minutes and per 3 hours. It is expressed as the depth of water that collects on a flat surface, and can be measured to the nearest 0.25 mm. It is sometimes expressed in liters per square meter (1 L/m² corresponding to 1 mm).
Closely related to the amount of rainfall is the rain rate, measuring the amount of the rainfall in a time unit. Usually the time unit is one hour or one minute. The rain rate depends on several parameters of the rain, like raindrop equivalent diameter, or raindrop concentration. Raindrop diameter is in relation with the falling speed, or velocity.
Raindrops generally have a diameter greater than 0.5 mm. Precipitation with raindrops of less than 0.5 mm in diameter is called drizzle and often severely restricts visibility, but usually does not produce significant accumulations of water.

III. RAIN MODELING

In the following, some methods of modeling rain are presented, as found in literature.

a) Velocity studies

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The velocity-diameter relation has been modeled by the equations [2]:

$$v(D) = 3.78 \cdot D^{0.67} \quad (1)$$

where the velocity v is measured in [m/s] and the diameter D in [mm].

Some studies [3] use a different equation:

$$v(D) = 9.65 - 10.3 \cdot e^{-0.6 \cdot D} \quad (2)$$

b) Raindrop size distribution

The distribution of sizes in a rain usually contains a wide range of drop diameters. Small drops generally outnumber large drops, but as the intensity of the rainfall increases, the number of larger drops grows. The largest drops are found only in downpours with rainfall rates greater than 5 cm per hour. The size of raindrops can be classified as in table 2, according to [4].

Table 2.
The size of raindrop, [3]

Typical Particle Type	Typical Diameter (mm)
Cloud droplet	0.012
Large cloud droplet	0.1
Mist droplet	0.5
Drizzle Drop	1.2
Raindrop	3.0
Large Raindrop	6.0

Rain size distributions have been modeled by several authors. The most popular model remains the Marshall-Palmer model of the size distribution [5]:

$$n(D_d) = 8.0 \cdot 10^{-2} \cdot e^{-4.1 \cdot R^{-0.21} \cdot D_d} \quad (3)$$

R: rain intensity,
Dd: raindrop diameter,
n(Dd): the probability density function of the raindrop diameter.
According to probability theory, the mean drop diameter is [6]:

$$D_{mean} = \frac{1}{4.1 \cdot R^{-0.21}} \quad (4)$$

where D_{mean} is measured in mm and R in mm/h.

The log-normal distribution [7] is another widely used model:

$$y = f\left(\frac{x}{\mu}, \sigma\right) = \frac{1}{x \cdot \sigma \cdot \sqrt{2 \cdot \pi}} \cdot e^{-\frac{(\ln x - \mu)^2}{2 \cdot \sigma^2}} \quad (5)$$

For the log-normal distribution model, the geometric mean diameter is found to be [7]:

$$D_{dg} = 0.72 \cdot R^{0.23} \quad (6)$$

The above models lead to significantly different results. Also experimental data reported in the literature [8, 9, 10] show large differences. Such differences can be related to different environmental conditions (oceans, continent temperature, pressure etc.). However, all estimations lead to the conclusion that the mean diameter of the raindrop is increasing with the rain intensity. The variance of the diameter is of the same order of magnitude as the diameter itself. This is also in agreement with the theoretical models.
Note that the distribution measured with a modern disdrometer in experiments [2] is obtained at (real) variable rain intensity.

IV. RAIN SIMULATION

The objective is to obtain the volumetric contributions of raindrops with different diameters in relation with the total amount of the rain, assuming a constant rain rate. No study of this kind has been found in literature. All the studies found in literature focus on rainfall intensity, raindrop size distribution and velocity studies. In the hypothesis of creating an artificial rain generator, the volumetric contributions of raindrops with different diameters is a very important statistic for the user.
The rain generator under design has to be able to generate several types of rain. For each type of rain, it is important to control the raindrop size distributions expressed in volumetric contributions to the total volume of rain. The proposed rainfall parameters are presented in the table below:
Table 3
Proposed rainfall parameters

Nr	Type of rainfall	Volume of rainfall
IV	Very heavy	> 16 mm/h
III	Heavy	7.5 – 16 mm/h
II	Moderate	< 7.5 mm/h
I	Light	< 2.5 mm/h

The simulation of equation (1), resulting in Figure 1:

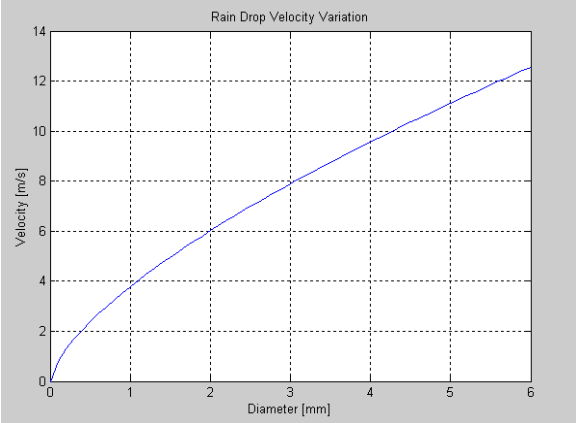

Figure 1. Rain Drop Velocity Variation.

The differences between the velocity equation given by (1) and (2) were studied.
The results of the simulation are given in Figure 2:

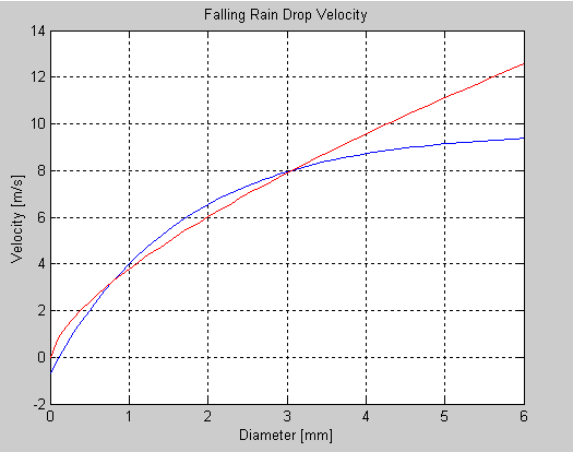

Figure 2. Comparison between the results obtained by using equation (1) - red and equation (2) - blue

In a further study, three types of rains with different intensities and mean diameters were simulated. For each type of rain, three percentages from the number of drops were defined. For each percentage and rain type, the diameter ranges were calculated, using the Palmer-Marshall distribution (3). The results are shown in table 4.

Table 4.
Diameters of different percentages of rain drops for given mean diameters

D_{mean}=1	D_{mean} =2	D_{mean} =3
40% (0.5-1.5mm)	40% (1-3mm)	40% (1.5-4.5mm)
60% (0.1-1.9mm)	60% (0.4-3.6mm)	60% (0.6-5.4mm)
80% (0.1-1.9mm)	80% (0.2-3.8mm)	80% (0.3-5.7mm)

The Palmer-Marshall distribution law better expresses the reality for big and medium raindrop diameters, which is why it offers not so accurate results for small and medium rain intensity. It tends to generate raindrops with smaller diameters than those that can be found by measurements in reality [11, 12]. This result is in part a consequence of the limitations of the measuring devices for small size drop diameters.

For given rain rates, the mean diameter values were determined with the Palmer Marshall distribution. The results, given in Table 5, show that the diameters are very small. On the other hand, for given diameters, very large rain rates resulted when calculated with equation (3).

Table. 5
Mean diameters for given rain rates

Rain Intensity	R=2.5mm/h	R=7.5mm/h	R=16mm/h
Mean Diameter	D_{mean} =0.3mm	D_{mean} =0.375	D_{mean} =0.44

Using a log-normal diameter distribution model, the volumetric contributions to the amount of the rain have been computed for raindrops with different diameters, assuming a constant rain rate. The results are shown in Figure 3.

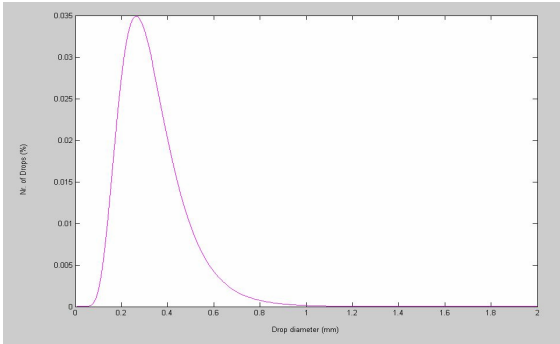

Figure 3. Total amount of the rain with the diameter distribution

The cumulative volume probability function, based on similar simulations is illustrated in figure 4.

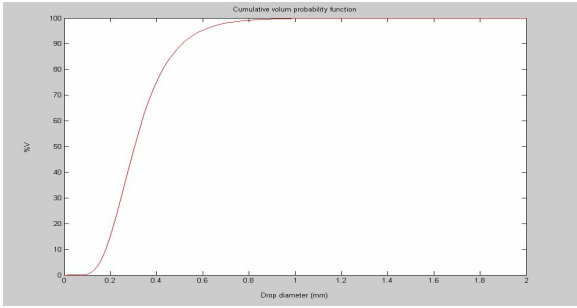

Figure 4. Cumulative volume probability function

Based on the same simulations, the contributions of several diameter ranges, covering 50%, 60% and 80% of the total amount of the rain, for the rain types defined in Table 4 were found. The volumetric contributions of raindrops with different diameters to the amount of the rain, assuming a constant rain rate are illustrated in figure 5. This result is a basic step toward to goal of generating artificial rains with features controlled and similar to natural rainfalls, using devices with narrower drop size distributions.

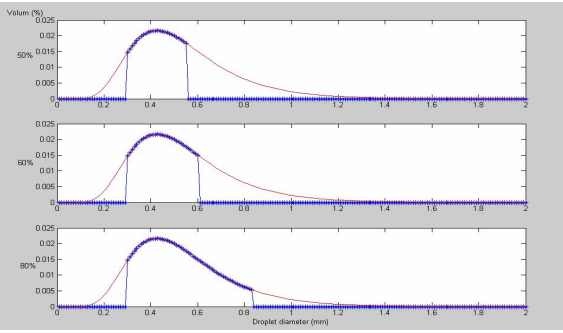

Figure 5. Volumetric contributions of raindrops with different diameters to the amount of the rain, assuming a constant rain rate.

V. CONCLUSIONS

Natural rains are characterized by a high degree of variability. Variability means that rain rate changes in time and space. So do the statistics of the rain. The phenomenon is non-stationary from a statistical point of view. Physical models and statistical analysis reveal several relations and correlations between rain parameters. Many environmental factors tend to influence the underlying laws, resulting in a chaotic behavior of the real rain system.

The present work proposed and simulated several working parameters of a rain generator being designed. Computer simulations carried out in the present work are a basic step toward generating artificial rains with controlled statistical parameters

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Two – Quadrant Converter with RNSIC Analysis having Capacitors on the AC side

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Abstract – A new topology for a two – quadrant converter is presented. In the AC/DC transfer mode the converter works as a rectifier with near sinusoidal input currents (RNSIC), while in the DC/AC transfer mode it works as a square-wave pulse switching inverter. Some suggestions for the converter design are given and a comparison with two–quadrant PWM converter is made.

Keywords: power quality, two-quadrant converter, square-wave pulse switching inverter.

I. INTRODUCTION

Most of the applications use three – phase converters, for two – quadrant operation in AC power supplies where the objective is to produce sinusoidal current waveforms on the AC side. For example, in motor drives with regenerative braking, the power flow through the utility interface converter reverses during the regenerative braking while the kinetic energy associated with the inertias of the motor and load is recovered and fed back to the utility system [1, 2]. Usually, the three – phase converters for two – quadrant operation use PWM switching techniques in order to reduce higher current harmonics on the AC side. Governments and international organizations have introduced new standards (in the United States, IEEE 519, and in Europe IEC 61000 – 3) which limit the harmonic content of the current drawn from the power line by rectifiers [3, 4].

Figure 1a presents the most popular topology used in adjustable speed drives (ASD), uninterruptible power supplies (UPS), and more recently in PWM rectifiers. This topology has the advantage of using a low – cost three – phase module with a bi-directional energy flow capability.

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Due to the rapid changes in voltages and currents of a switching converter, a PWM rectifier is a source of EMI. The PWM rectifier, even though it has near sinusoidal input currents, has important disadvantages as compared with the inexpensive three –phase rectifiers with diodes: larger switching losses, high per – unit current rating, poor immunity to shoot – though faults, higher cost and less reliability [1, 2].

II. NEW CONVERTER CONFIGURATION

A new converter for two – quadrant is presented in this paper; it is equipped with 6 transistors (e.g. IGBT) having square-wave pulse switching (that is not PWM) operation, as shown in Fig. 2a. When the energy is transferred from the AC side to DC side, the transistors are off and the converter works as a RNSIC (Rectifier with Near Sinusoidal Input Currents), as described in [5-7]. When the energy is transferred from the DC side to the AC side, the transistors are controlled to conduct for θ angles (square-wave pulse switching) and the converter works as inverter, as show in Figs. 2b and 3.

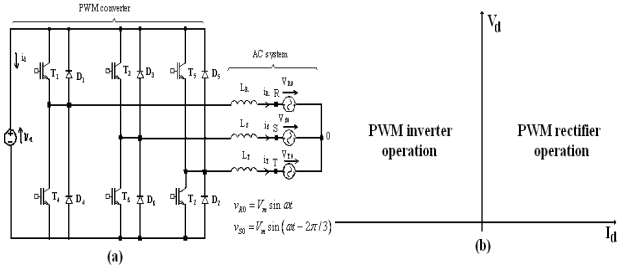


Fig. 1 Converter for two – quadrant based on PWM principle; (a) Configuration; (b) Operation modes

Inductors L_2 have values several times smaller than L_1. For the case of operation in inverter mode, the voltage V_d is considered to be 15-25 % greater than for the case of rectifier system operation. Diodes $D_1^{'} - D_6^{'}$ are chosen according to the RNSIC component design specification, while the diodes $D_1 – D_6$ are rated for much smaller average currents.

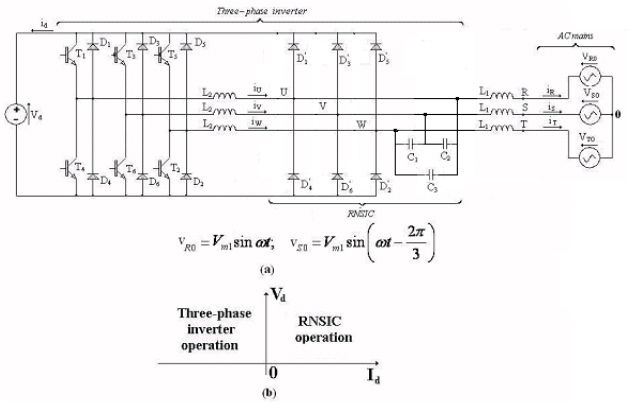


Fig. 2 Converter for two – quadrant with RNSIC; (a) Configuration; (b) Operations

Capacitors C_1 – C_3 have the same capacity, C, fulfilling the condition, [5– 7]:

$$0,05 \le L_1 C\omega^2 \le 0,10 \tag{1}$$

The switch of the converter in Fig. 2a from the inverter mode operation to the rectifier mode operation and reverse can be rapidly accomplished during a utility grid cycle $T = \frac{2\pi}{\omega}$.

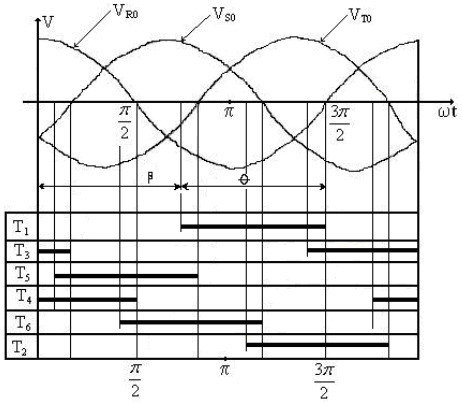


Fig. 3 Control program of the transistors.

According to the phasor diagram in Fig. 4b, current i_R is given by :

$$i_R = \frac{v_{U0} - v_{R0}}{j\omega L_1} \tag{2}$$

while its active value, i_{Ra} , is given by :

$$i_{Ra} = \frac{V_{m2}}{\omega L_1}\left[\sin(\omega t + \alpha) - \frac{V_{m1}}{V_{m2}}\sin\omega t\right] \tag{3}$$

The active power transferred to the AC source is given by:

$$P = \frac{3}{2\pi}\int_0^{2\pi} i_{Ra} V_{m1}\cos\omega t\, d\omega t = \frac{3V_{m1}V_{m2}}{2\omega L_1}\sin\alpha \tag{4}$$

In order to obtain a unity power factor at the AC source, from (3) it implies that:

$$\cos\alpha = \frac{V_{m1}}{V_{m2}} \tag{5}$$

It results that the value of the power transmitted to the AC source could be varied by modifying the amplitude V_{m2} (thus the angle θ) and the angle α (thus the angle β), as show in Fig.3.

Possible applications of the converters for two – quadrant operation with RNSIC are their usage in static frequency converters with DC voltage link, designed for supplying variable voltage and frequency to the three – phase induction motor drives, as shown in Fig. 5.

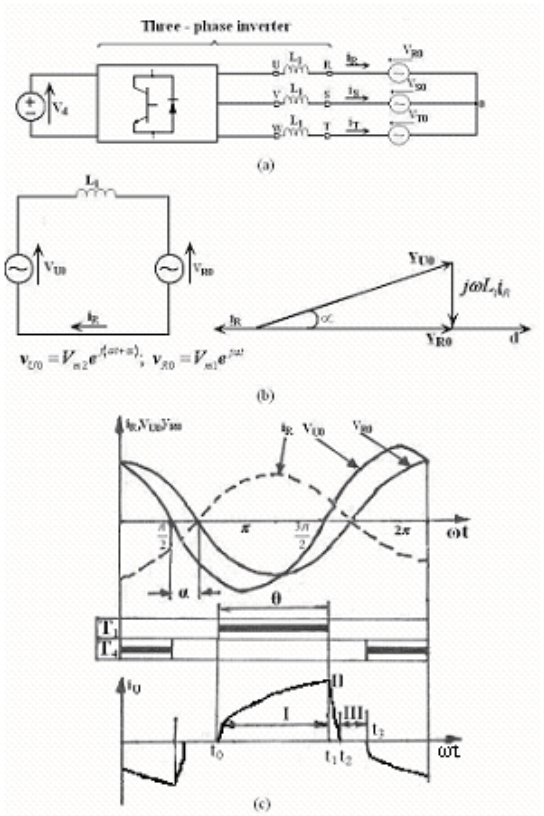


Fig. 4 Inverter mode operation of the two – quadrant converter with a RNSIC ; (a) Simplified representation; (b) Phasor diagram at unity power factor; (c) Waveforms of the currents and voltage.

For the time intervals when the induction motor drive is in the motoring regime, the input converter becomes a RNSIC converter. For this case the transistors T_1 – T_6 are off. The output switch – mode converter operates as a PWM inverter. The energy is transmitted from the power supply to the motor and the voltage on the filtering

capacitor C_0 is less than $V_{d0} = \sqrt{3}V_m\left(1-2L_1C\omega^2\right)$.

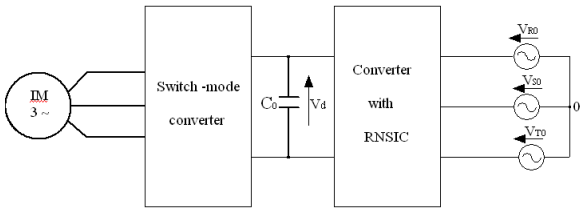


Fig. 5 Static frequency converter for two – quadrant with RNSIC

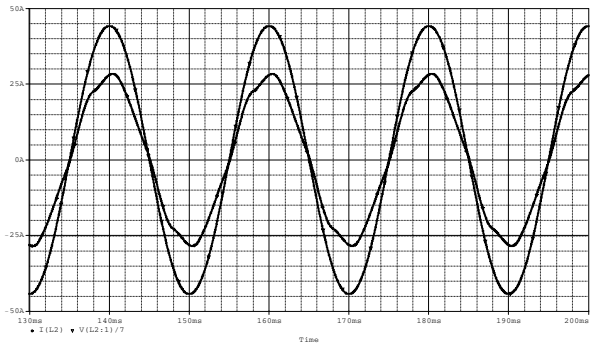
During the time interval while the induction machine (IM) is operating in breaking mode, the energy received from the motor is transmitted to the power supply. The switch – mode converter operates as a rectifier and the voltage across C_0 is greater than $(15-25\%)V_{d0}$. Further on, the energy is transmitted into AC mains by means of a three – phase inverter made up of transistors $T_1 – T_6$, three inductors L_2, diodes $D_1 – D_6$ and RNSIC. One must observe also the fact the total duration of operation as a generator for the asynchronous machine is much smaller as compared with the total motor functioning duration.

III. EXPERIMENTAL AND SIMULATION RESULTS

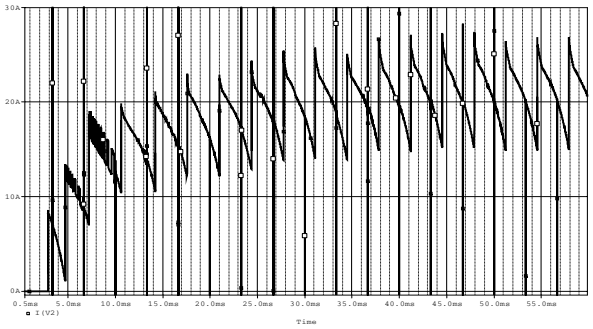
Laboratory experiments and simulations results have proved the effectiveness of the proposed converter in Fig. 2a. The laboratory prototype consists of a three – phase voltage source (with $V_m = 311V$ and f = 50 Hz) and a RNSIC converter. The RNSIC is composed of six diodes, three inductors L_1 with inductance 25 mH and three DC capacitors $C_1 – C_3$ with capacitance 20 μF. For the three inductors L_2 we have adopted the value 25 mH.

Figures 6 and 7 show the simulations results. In Figs. 6a and 6b the waveforms of the phase current i_R and the DC current i_d are shown, for the case of the induction machine operating in motoring regime.

For power circulation in the opposite direction, Figs. 7a and 7b show the waveforms of the phase current i_R, the transistor current i_{T1} and the DC current i_d, when the induction machine is operating in breaking mode. The value of the power transmitted to the AC source can be varied by modifying the angles θ and β, as suggested in Fig. 3.

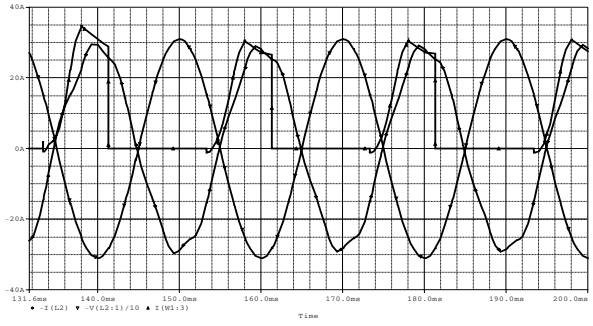


(a)

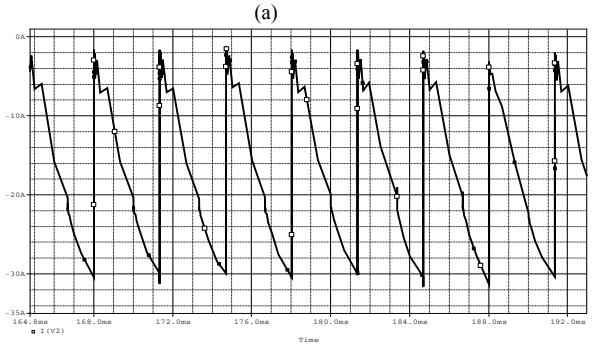


(b)

Fig. 6 Rectifier operation mode of the proposed converter with RNSIC for V_d = 600V; (a) Waveforms of the phase current i_R and the phase voltage v_{R0}; (b) Waveforms of the DC current i_d



(a)



(b)

Fig. 7 Inverter mode operation of proposed converter with a RNSIC for V_d = 800 V; (a) Waveforms of the phase current i_R, the transistor current i_{T1} and the phase voltage v_{R0}; (b) Waveforms of the DC current i_d.

IV. CONCLUSIONS

Comparing the two – quadrant PWM converter with the converter proposed in this paper one can make the following considerations:

- The proposed topology reduces the commutation losses and EMI problems. Transistors $T_1 – T_6$ begin to conduct only once in a utility grid cycle, at zero currents i_U, i_V and i_W (that is according to ZCS – Zero Current Switching principle).
- One of the advantages of the continuous functioning of the controllable switches (in square-wave pulse and not PWM switching), is that each inverter switch changes its state only twice per cycle, which is important at high power levels where the solid – state switches generally have slower turn – on and turn – off speeds.
- The proposed converter has increased safety due to the fact that controllable switches have much smaller total conducting durations, being blocked while the converter operates as RNSIC.
- In the case of DC to AC conversion, for the same values of the voltage V_d and AC inductances, the proposed converter provides larger output voltages V_{U0}, V_{V0} and V_{W0} and thus allows a more efficient energy transfer (obviously, at the PWM inverter, the fundamentals of the output voltages are smaller and so the transferred energy is smaller).

The simulation and experimental results proved that the fifth current harmonic is the most significant one generated in the AC mains and that its value is within the limits imposed by the IEEE Standard 519/1992.

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On the Precision in the Determination of the Movement Features by Doppler Radio–Telemetry

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Abstract – For determining the features of a movement at low speed in the atmosphere, the authors have proposed a Doppler radio-telemetry system with active fixed referential. This paper deals with the precision in the determination of the movement features at low speed in the atmosphere, using electromagnetic waves. The establishing of the systematic errors and the appreciating of the random errors, represents the authors' contribution in this paper.

Keywords: Doppler signal, systematic errors, random errors.

I. INTRODUCTION

The authors have proposed the structure of a Doppler radio-telemetry system with active fixed referential for the determination of the movement features at low speed in the atmosphere, using electromagnetic waves. The authors' contributions in the establishing of this structure, presented in Fig.1, are detailed in [1]. The main contribution consists in the selection of the movement to be evaluated from other movements taking place simultaneously in the same space by the activation of the fixed referential in that it produces the change of frequency f_1 into f_2 and its modulation in DSB-SC with the low frequency f_j.

The signal $s_{e1}(2\pi f_1 t+\varphi_0)$, generated by the frequency synthesizer with PLL1, is emitted by the antenna A1 on the mobile referential (MR) to the active fixed referential (AFR). The signal received by the antenna A2, on the AFR, is phase modulated by the longitudinal Doppler effect caused by the movement of the MR in relation to the AFR; the Doppler shift in frequency, $\pm\Delta f_1$, is retrieved into the signal $s'_2[2\pi(f_2\pm\Delta f_2)t+\varphi_0]$ through $\Delta f_2 = (f_2\cdot\Delta f_1)/f_1$. The signal $s_{e2}[2\pi(f_2\pm\Delta f_2)t\pm 2\pi f_j t\pm\varphi_j+\varphi_0]$ is emitted by the antenna A2 to the antenna A1 and the signal received by the antenna A1 is again phase modulated by the longitudinal Doppler effect. At the output of the Doppler signal extractor, DSE, the signals: s_D - Doppler signal and s_{axi} - Doppler shift in frequency axing signal are obtained. The two signals are represented by the relations:

$$s_D = A_D \sin(8\pi\Delta f_2 t) \tag{1}$$

$$s_{axi} = 2A_m \cos\left[2\pi\left(f_j \pm 2\Delta f_2\right)t + \varphi_j\right] \tag{2}$$

The movement features – instant speed, average speed and distance covered in the time interval Δt are determined by indirect measurement based on the relations:

$$v = \frac{v_f}{f_2}\cdot\frac{1}{8\pi}\cdot\frac{\partial}{\partial t}\left[\arcsin\left(\frac{s_D}{A_D}\right)\right] \tag{3}$$

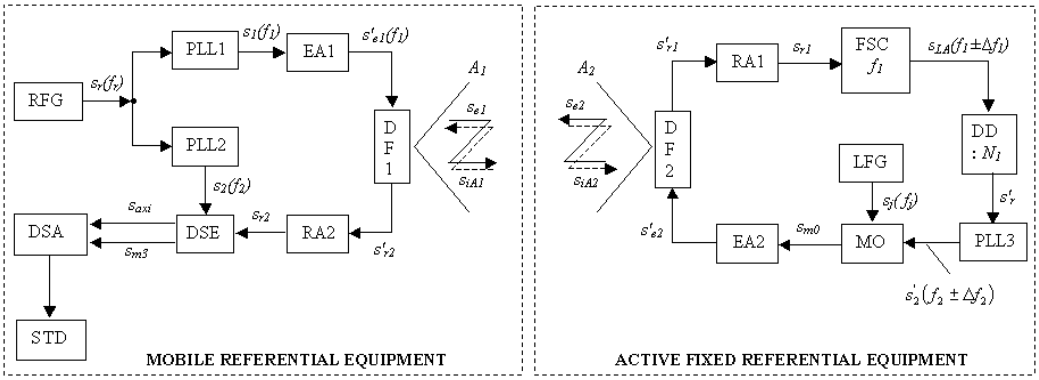

Fig.1. The structure for the Doppler radio-telemetry system with active fixed referential: RFG – reference frequency signal generator; LFG – low frequency signal generator; PLL1, 2, 3 – frequency synthesizers; EA1, EA2 – emission amplifiers; DF1, DF2 – diplex filters; RA1, RA2 – reception amplifiers; FSCf_1 – f_1 frequency selection circuit; DD – digital frequency divider; MO – DSB-SC modulator; DSE – Doppler signal extractor; DSA – Doppler signal analyzer; STD – block for showing and transmitting data.

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$$v_{\text{med}} = \frac{1}{T}\int_0^{\Delta t} v \cdot \mathrm{d}\, t \quad \text{and} \quad D = v_{\text{med}} \cdot \Delta t \qquad (4)$$

The movement sense related to the AFR, approach or getting away, is indicated by the increase of the f_j frequency with $2\Delta f_2$ for approach and the decrease of the f_j frequency with $2\Delta f_2$ for removing from the fixed referential. The determination of these frequencies is made based on the axing signal s_{axi} of the Doppler shift in frequency in the Doppler signal analyzer, DSA.

The structure of the Doppler radio-telemetry system with active fixed referential for the determination of the movement features, presented in Fig.1, can be reduced to the block diagram given in Fig.2.

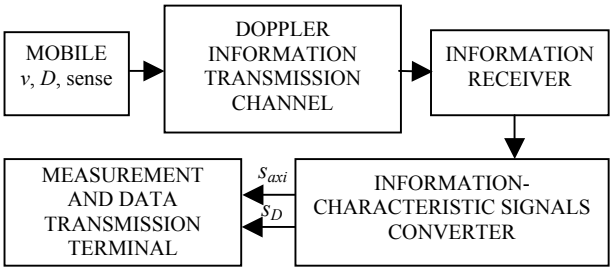

Fig. 2. The block diagram of the telemetering process of the movement features with a Doppler radio-telemetry system with an active fixed referential

The transmission channel of the Doppler information contains the whole chain, presented in Fig.1, from the f_1 frequency signal generator to the antenna A2 which plays the role of receiving the electromagnetic signal with the f_2 carrier frequency. In other words, the transmission channel of the Doppler information contains:

- the blocks on the mobile referential with the role of emitting electromagnetic signal with f_1 frequency (noted in Fig.1 with RFG, PLL1, EA1, DF1, A1);
- the propagation space of the electromagnetic signal with the f_1 carrier frequency from the antenna A1 to the antenna A2;
- the blocks on the active fixed referential with the role of receiving, frequency changing and emitting electromagnetic signal with f_2 carrier frequency (noted in Fig.1 with A2, DF2, RA1, FSCf_1, DD, PLL3, LFG, MO, EA2, DF2, A2);
- the propagation space of the electromagnetic signal with the f_2 carrier frequency from the antenna A2 to the antenna A1.

The information receiver contains the blocks on the mobile referential which plays the role of receiving the electromagnetic signal with the f_2 carrier frequency. The information–characteristic signals converter is, in fact, the extractor of Doppler signal, DSE, and the measurement and data transmission terminal is the Doppler signal analysis block, DSA.

The Doppler information transmission channel, the information receiver, the information–characteristic signals converter and the measurement and data transmission terminal contain professional and fast electronic blocks, meaning that the response speed of the electronic circuits is very high, resulting a very short response time, less than 10 ns. In these conditions it can say that the speed at certain moment can be considered constant during τ_p of a measurement series with the duration of one measurement $\tau_m \ll \tau_p$.

The measurement error Δv_i is defined as

$$\Delta v_i = v_i - v_0 \quad (i = 1, 2, \ldots, n) \qquad (5)$$

where v_i is the value obtained by the measurement i, while v_0 is real value of the physical parameter measured, generally unknown.

An estimate of the real value using a n measuring number can be the arithmetic mean value:

$$\bar{v} = \frac{1}{n}\sum_{i=1}^{n} v_i \cong v_0 \qquad (6)$$

If the errors are random and uncorrelated it is demonstrated that by mediation the dispersion of the measurement error is reduced by n times.

Between the errors that occur from the measurements and the parameters that characterize the measurement physic process appear bindings with functional and random character. Therefore, the measuring error Δv_i must be perceived as a sum of systematic, random and sometimes even rough errors.

In conclusion, the determination precision of the movement features is given by establishing the systematic and random errors that occur.

II. SYSTEMATIC ERRORS

The systematic errors can be: *instrumental*, *methodical*, *exterior* and *rough*. They have a cumulative character and therefore it is necessary to establish carefully and accurately the components and to take measures for eliminating or at least reducing their substantially.

The **instrumental errors** are due to, on the one hand, that it is made an indirect measurement of the velocity by using an electromagnetic wave phase-modulated by longitudinal Doppler effect, and, on the other hand, the relations (3) and (4) are numerically solved in the block DSA.

The instrumental error due to the indirect measurement depends on the form of the electromagnetic wave and the signal-to-noise ratio at the output of the reception amplifiers RA1 and RA2. The electromagnetic signal is generated by the frequency synthesizer with PLL1, respective, PLL3 and has a correct sinusoidal waveform. Through the quality diplexer filters, through the band-pass amplifiers RA1 and RA2 and through the band-selector filters of the modulators and demodulators, the signal waveform remains sinusoidal, the distorting components being insignificant.

The signal-to-noise ratio at the output of the reception amplifiers being of minim 40 dB, so, the influence of the noise is, also, insignificant.

The instrumental errors due to the DSA block refer to: a) the quantization error of the analog/digital conversion of the signal s_D; b) the error in knowing the f_2 frequency and of its stability in time and with temperature; c) the error in knowing the propagation speed of the electromagnetic wave in the atmosphere, v_f; d) the error in knowing the time interval Δt; e) the error of the digital/analog conversion of parameters v, v_{med}, D.

The propagation speed v_f of the electromagnetic wave in the atmosphere is known with an accuracy γ_{vf} = 0.033 %. The carrier frequency f_2, due to the frequency synthesizer with PLL3, is known with the accuracy of the assigned frequency f_r; this is given by a quartz oscillator and it is known with an accuracy of more than 0.05 %, by using a quartz resonator of 10 MHz with three decimals.

Taking into account the quantization errors γ_{qd}, the accuracy of the analog/digital conversion γ_{ad} and the solving by digital method of the equation of the movement speed (relation (3)), results γ_v - the precision in determination of the instant speed of the mobile (mobile referential):

$$\gamma_v = \gamma_{vf} + \gamma_{f2} + \gamma_{qd} + \gamma_{ad} < 0.5\,\% \tag{7}$$

When determining the covered distance D we also must consider the error in knowing the time interval Δt. As Δt is determined digital, considering the tact frequency given by the reference frequency f_r, it can appreciate that the distance D can be determined with an accuracy better than 0.5 %.

For estimating the error due to the temperature variation, greater than the error in knowing the time interval, we must take into account that:

$$v = F\left(v_f, f_2, s_D, A_D\right) \tag{8}$$

The influence of the temperature θ on the measurement accuracy can be determined taking into account the variation of these parameters with temperature [2, 3, 4]. This leads to:

$$v_\theta = F\left(v_{f0}, f_{20}, s_{D0}, A_{D0}\right) + \gamma \cdot \theta \tag{9}$$

where

$$\gamma = \alpha \cdot v_{f0}\frac{\partial F}{\partial v_f} + \beta \cdot f_{20}\frac{\partial F}{\partial f_2} + \\ + \delta \cdot s_{D0}\frac{\partial F}{\partial s_D} + \mu \cdot A_{D0}\frac{\partial F}{\partial A_D} \tag{10}$$

representing the coefficient of temperature for the block Doppler signal analyzer, DSA. The parameters - v_{f0}, f_{2o}, s_{Do} and A_{Do} are the values for normal temperatures, and α, β, δ, μ are the temperature coefficients of these parameters.

The variation with temperature of the propagation speed of the electromagnetic waves in the atmosphere is less than 0.1 % and therefore it is insignificant [3, 4]. The variation with temperature of the frequency f_2 is given by the variation with temperature of the quartz resonator, which is kept at the same temperature. So, we can say that the variation with temperature of the frequency f_2 is insignificant. The other two terms , δ and μ, are also very low due to using the professional integrated circuits with a good rejection of the temperature influence.

However, as a preventive measure, the electronic equipment on the RM is shelters into a temperature-controlled oven, and the electronic equipment on the RFA is build in compact construction and maintained within certain limits of temperature.

In these conditions, it can consider that the influence of the temperature on the precision in the determination of the movement parameters is insignificant.

The **methodical errors** are due to the fallibility of the measurement method used and they appear especially when the measurement is indirect. It is consider theoretical that the method of measurement is described by the function

$$y = F\left(v, l, m, ..., q\right) \tag{11}$$

where v is the measuring parameter, y is the result of the measurement and l,m,…,q are physical parameters which can vary during the measurement process, and this leads to the methodical errors.

When calibrating the Doppler radio-telemetry system with active fixed referential, it is considering the reference values l_0, m_0,..., q_0 such as

$$y_0 = F\left(x, l_0, m_0, ..., q_0\right) \tag{12}$$

$$y = y_0 + \Delta y = \\ = F\left(x, l_0 + \Delta l, m_0 + \Delta m, \ldots, q_0 + \Delta q\right) \tag{13}$$

and by the development in Taylor series and neglecting the infinitely minute of superior order of 1, the methodical errors Δy is obtained:

$$\Delta y = \frac{\partial F}{\partial l}\cdot\Delta l + \frac{\partial F}{\partial m}\cdot\Delta m + \ldots + \frac{\partial F}{\partial q}\cdot\Delta q \tag{14}$$

The relation (14) shows that the value of the methodical error is determined both the offsets Δl, Δm,…,Δq of the physical parameters taken into account and the character of the variation of the function F in respect with these parameters.

In the event of the Doppler radio-telemetry system with active fixed referential these parameters are: the linearizing action of the Doppler effect; the Doppler shift of the low frequency f_j of the signal s_{e2}; the directivity of the antennas on the two referentials; the quality of the diplexer filters; the parasitic signals from the official frequency field near of the working frequencies f_1 and f_2; the offset of the reference frequency f_r due to the Doppler shift in frequency $\Delta f_1/N_1$ in PLL3 on AFR. The first two parameters are more important and they will be studied below.

The methodical error due to the linearizing action of the Doppler effect appears by using relation (16) instead of relation (15):

$$\Delta f_1 = f_1\left(\sqrt{\frac{1-v/v_f}{1+v/v_f}}-1\right) \quad (15)$$

$$\Delta f_1 = -f_1 \cdot \frac{v}{v_f} \quad (16)$$

At low speeds, $v \le 62$ m/s, the speed ratio $v/v_f \le 2.07 \cdot 10^{-7} << 0.02$. In [1] it is shown that for $-0.02 < v/v_f < +0.02$, the dependence of the Doppler shift in frequency on the movement speed is linear; this means that, for low speeds taken into consideration, the error due to the linearizing action of the Doppler effect is insignificant.

The methodical error due to the Doppler shift for the frequency f_j given the situation for f_2, can be appreciated taking into account the usual values for f_j and f_2 presented in [1]. From relation (14), for $f_j = 400$ Hz and $f_2 = 160$ MHz, it obtains $\Delta f_j / \Delta f_2 = f_j / f_2 = 2.5 \cdot 10^{-6}$, so that, it can consider the methodical error by the neglect of Δf_j as being insignificant.

In the choice of the structure presented in Figure 1 and the electronic equipment on the two referentials it kept in view also the minimization of the methodical errors due to the other parameters mentioned above. Therefore it can say that methodical errors in the proposed telemetering system are very small compared to instrumental errors.

The **external errors** are due to the external factors of the Doppler radio-telemetry system, such as atmospheric changes. These do not change the propagation speed of the electromagnetic waves, the longitudinal Doppler effect and the work of the electronic equipment. When the wind speed is considerable (winds are powerful), the movement speed of the mobile is higher or lower, depending on the direction in which the wind blows: whether it's in the direction of the motion or in the opposite direction. In these conditions the movement of the mobile is strong affected by the external factors.

The **rough errors** are caused by some break-downs in the electronic equipment, in the transmission and reception aerials or the encroachment of the general measurement principles. The identification criterion of these errors is based on the fact that the measurement results are very different from the results of the other measurements.

These values must be eliminated from the performed-measurement series. If they persist, it must fix the problem with the electronic equipment.

III. RANDOM ERRORS

The random errors are due to different causes whose individual influence is not easy to see, the experiments putting into evidence only their random appearance. These errors may be positive or negative, grouped around the zero value, and they are according to the known statistical laws [3, 4]. The random errors are very important in the telemetering precision of the movement features and this is why they have been carefully researched..

The parameter that must be measured is the movement speed v, which can be considered practically constant during τ_v of a measurement series with the duration of a measurement $\tau_m << \tau_v$. Consequently, it can admit that during τ_v there are made n individual measurements v_i with $v_i \in R$ ($i = 1, 2,\ldots, n$). Due to the random errors, the most probable value of the speed v it is considered as being v_p and the random errors in the n individual measurements can be estimated by $\alpha_i \in R$ ($i = 1, 2,\ldots, n$), where

$$\alpha_i = v_i - v_p \quad (17)$$

It is considered ξ as being the stochastic-continuous variable, with the repartition function F and the repartition density f. It is very important to define the variation limits of the random errors α_i and the probability that α_i to be between these limits; in these conditions it can take into account the random errors, the causes of their appearance and it can give solutions for diminishing them. In order to do that, it must determine the repartition function F and the density of the random errors repartition f.

It is established an infinitesimal variation h and it is considered the probability P as to the stochastic variable to be find in the interval $[v, v + h)$. It can say that:

$$P(v \le \xi < v + h) = \int_v^{v+h} f(v)\mathrm{d}v \quad (18)$$

which means that, the stochastic variable being in the variation interval of the speed, the density function of the stochastic-variable repartition becomes the density function of the speed repartition, $f(v)$, and the repartition function $F(\xi)$ becomes $F(v)$.

For h low enough and for the continuity of the function $f(v)$, in the conditions in which $\alpha_i \in (v, v + h)$ with $i = 1, 2,\ldots, n$, it can appreciate that the probability P as to the stochastic variable ξ to be find in interval $[v, v + h)$ is:

$$P(v \le \xi < v + h) = h \cdot f(v) \quad (19)$$

The probability p as to the n random errors α_i to be determined with an error $\beta \in (\alpha_i, \alpha_i + h_i)$ with $i = 1, 2,..., n$, it can put in the relation:

$$p = \prod_{i=1}^{n} h_i \cdot f(\alpha_i) \quad (20)$$

where $f(\alpha_i)$ is the repartition density of the random errors α_i.

Because $h_i > 0$, but very small (infinitesimal), p may represent, concomitantly, the probability as the speed v to be near of the most probable value v_p. Therefore:

$$p(v) = \prod_{i=1}^{n} h_i \cdot f(v_i - v_p) \qquad (21)$$

In hypothesis that the function $f(v_i - v_p)$ is derivable, the probability p is maximum if the derivative of the function $p(v)$ in report with h_i is nullified for $v_p = v_0$, where v_0 is expressed with relation (6).
The repartition density function of the random errors $\alpha_i = u_i = v_i - v_0$ [2], is:

$$f(u_i) = f(\alpha_i) = \frac{1}{r\sqrt{2\pi}} \cdot \exp\left(-\frac{u_i^2}{2r^2}\right) \qquad (22)$$

It is noted that de relation (22) represents, in fact, the density of normal repartition $N(0, r)$. The function of normal repartition $N(m, r^2)$ is the same with $F(v)$, namely

$$F(v) = \frac{1}{r\sqrt{2\pi}} \int_{-\infty}^{\infty} \exp\left(-\frac{(t-m)^2}{2r^2}\right) \mathrm{d}t \qquad (23)$$

with $m = \int_{-\infty}^{+\infty} v \cdot f(v) \mathrm{d}v$

and it satisfies the Laplace and Gauss Theorem. The function

$$\overline{\Phi}(v) = \frac{2}{\sqrt{\pi}} \int_{0}^{v} \exp\left(-u_i^2\right) \mathrm{d}u \qquad (24)$$

is called the error function, and the constant h, from the relation (19), takes the value

$$h = \frac{1}{r\sqrt{2}} \qquad (25)$$

and is called the measurement precision (precision module) from the point of view of the random errors.
For the evaluation of the dispersion of variable v, noted with r^2, are used the n individual values v_i, obtained thorough the measurement, keeping account of the definition of the dispersion r^2 as the dispersion in report with the mean value m. It results [2, 3]:

$$r^2 = \sum_{i=1}^{n} P(v = v_i) \cdot (v_i - v_0)^2 = \\ = \frac{1}{n} \sum_{i=1}^{n} (v_i - v_0)^2 \qquad (26)$$

With r thus obtained is determined the precision h and the probability as the absolute value of the apparent error to be contained in the interval $[a_0, b_0)$ with $a_0 \geq 0$ is calculated with the relation

$$P(a_0 \leq |\alpha_i| < b_0) = \overline{\Phi}(hb_0) - \overline{\Phi}(a_0) \qquad (27)$$

For a number n of sufficient great measurements ($n \to \infty$) it can be appreciated as good the equalization of the probable value of the measuring parameter with the mean value of measurements.

Practically speaking, however, the number of measurements is finite, and as result, the arithmetic mean v_0 is departed off the probable value v_p with an random error. On the basis of the previous relations, it may be deduced relations for the parameters that characterize this real state, the error S_r on the result, the probable error R of the result, the average error T and the value of the value of the limit random error α_{lim}. These relations are:

$$S_r = \pm\sqrt{\sum_{i=1}^{n} \frac{u_i^2}{n(n-1)}}, \qquad R = \frac{2}{3} S_r \qquad ,$$

$$T = \pm\sqrt{\frac{2}{\pi}} \cdot S_r \ , \qquad \alpha_{lim} = 3S_r = 4{,}5R \qquad (28)$$

Choosing the interval for the variation of the random error $[-3r, +3r)$, the probability that this error to be inside this interval will be obtained by the integration of the relation (27) between these limits. It results:

$$P(-3r \leq \alpha_i < +3r) = 0.9972$$

This means that the random errors will be inside the interval $[-3r, +3r)$ with a probability of 99.72 %.
The dispersion r of the measured value, of the speed v around the average value v_0, is, concomitantly, also the random error calculated with the little squares method. According to this method of determination of the measured error, the best estimate of the parameter v is the value for which the sum of the squares of the random errors is minimum. This means that the derivative of the sum of the squares of the random errors in report with the probable random value v_p is zero.
In these conditions, $v_p = v_0$ and $\alpha_i = u_i = v_i - v_0$. It is seen that the value v for which the sum of the squares of the random errors is minimum represents the arithmetical mean v_o of the n experimental values v_i. The mean square error of the measurements, taking into account the random variable ξ, is

$$\sigma_v = \sqrt{\frac{1}{n} \sum_{i=1}^{n} (v_i - v_0)^2} = r \qquad (29)$$

and it can be appreciated that, the limits between which are situated the true value of the instant movement speed is given by the relation:

$$v = v_0 \pm r \qquad (30)$$

In reality, the speed v is not directly determined, but through the measurement of the Doppler signal s_D and of its amplitude A_D (relation (3)). Because it has been supposed that for an instant speed v, n individual measurements are made, it is possible to say that the n values of the speed have been obtained through measuring directly n signals s_{Di} and n amplitudes A_{Di}, with $i = 1, 2, ..., n$. In this case the calculation of the random errors is modified.

First of all, it has to determined the arithmetic mean value for each one of the two measurable variable directly:

$$s_{D0} = \frac{1}{n}\sum_{i=1}^{n} s_{Di} \quad \text{and} \quad A_{D0} = \frac{1}{n}\sum_{i=1}^{n} A_{Di} \qquad (31)$$

and then the mean square errors of the random errors are determined with the relations:

$$\sigma_{SD} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(s_{Di} - s_{D0}\right)^2} \quad \text{and}$$
$$\sigma_{AD} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(A_{Di} - A_{D0}\right)^2} \qquad (32)$$

According to relation (3), the dependency of v to the two measurable variable, s_D and A_D, is not a linear function but unlinear one (arcsin); in these conditions:

$$v = V\left(s_D, A_D\right) \qquad (33)$$

where

$$V\left(s_D, A_D\right) = \frac{v_f}{f_2}\cdot\frac{1}{8\pi}\cdot\frac{\partial}{\partial t}\left[\arcsin\left(\frac{s_D}{A_D}\right)\right] =$$
$$= \mathrm{C}\cdot\frac{\partial}{\partial t}\left[\arcsin\left(\frac{s_D}{A_D}\right)\right] \qquad (34)$$

because the parameters v_f, f_2 are not related to any random errors, they are determined from the beginning with a very good precision.
The errors at the two measurable variable directly are noted with

$$\alpha_i = s_{Di} - s_{D0} \quad \text{and} \quad \beta_i = A_{Di} - A_{D0} \qquad (35)$$

with the mention as that $\Sigma\alpha_i = \Sigma\beta_i = 0$.
It results:

$$v_i = V\left(s_{Di},\ A_{Di}\right) \quad \text{and}$$
$$V\left(s_{D0} + \alpha_i,\ A_{D0} + \beta_i\right) \qquad (36)$$

and developing in Taylor series the relation (36), in hypothesis that the α_i and β_i errors have values smaller than 1, it is obtained :

$$\sigma_{pv} = \sqrt{s_{D0}^2\cdot\sigma_{pSD}^2 + A_{D0}^2\cdot\sigma_{pAD}^2} \qquad (37)$$

So, in the conditions of indirect measuring of momentary speed using the two measurable variable directly, s_D and A_D, the value of the speed is:

$$v = V\left(s_{D0}, A_{D0}\right) \pm \sigma_{pv} \qquad (38)$$

IV. CONCLUSIONS

The theoretical consideration of the systematic and random errors, through experimentation proved to be correct and it demonstrated the good knowledge of the performing electronic equipment used, as well as the correct choice of the structure of the Doppler radio-telemetry system with active fixed referential for the telemetering of the small speed movements characteristics.

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Controlling a Hi-Fi Audio Amplifier on I^{2}C Bus Using Microcontroller AT89S8252

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Abstract – The paper presents the hardware structure of a Hi-Fi audio amplifying chain consisting of a sound fader control circuit and a power amplifier, both digitally controlled by microcontroller AT89S825 on I2C bus.
The authors have built in practice this application within the university's laboratory. The user is able to control the operation the audio amplifier using switches and a LCD.
The command program that the authors wrote in assembly language, operates in real-time and presents the user with an interactive way to activate various features and to adjust the amplifier's parameters.
Keywords: Hi-Fi audio amplifier, sound fader control circuit, ATMEL microcontroller, I^{2}C bus.

I. INTRODUCTION

The basic structure of a Hi-Fi audio amplifier digitally controller using a microcontroller is shown in fig.1.
The notes have the following meanings: S – stereo audio signal source from compact disc player (CD), digital versatile disc (DVD), radio receiver (Tuner), television set (TV), cassette player (CAS), video cassette player/recorder (Video) and microphone (Mic); SFCC – sound fader control circuit; FPA – final power amplifier; I – interface of the control unit to the audio amplifier; UCC – command and control unit; AS – the audio speaker system, including both filters and loudspeakers (FLS – front left speaker, FRS – front right speaker, RLS – rear left speaker, RRS – rear right speaker); PS – the power supply unit.

II. SOUND FADER CONTROL CIRCUIT

The audio signal is processed using a sound fader control circuit TEA6320, which is an integrated circuit designed for Hi-Fi play of stereo sound. The main features of this circuit are:
- possibility to select from four stereo signal sources and one mono source;
- interface for noise reduction circuits;
- interface for the use of an external equalizer;
- volume, balance and fader control;
- special loudness characteristics automatically controlled in combination with volume setting;
- bass and treble control;
- command of functions available on I^{2}C bus;
- mute function, controlled by audio signal zero crossing, using I^{2}C bus and an external pin of the integrated circuit;
- internal power supply with power-on initializing circuit, etc.

The basic structure of the TEA6320 circuit is shown in figure 2; notes have the following meanings: SM - input audio source selection multiplexer; V1LLC – V1 volume and loudness left control circuit; V1LRL – V1 volume and loudness right control circuit; BLC - bass left control circuit; BRC - bass right control circuit; TLC - treble left control circuit; TRC - treble right control circuit; MFZCD - mute function zero cross detector; V2BFRLC – V2 volume, balance and fader rear left control circuit; V2BFRRC – V2 volume, balance and fader rear right control circuit;

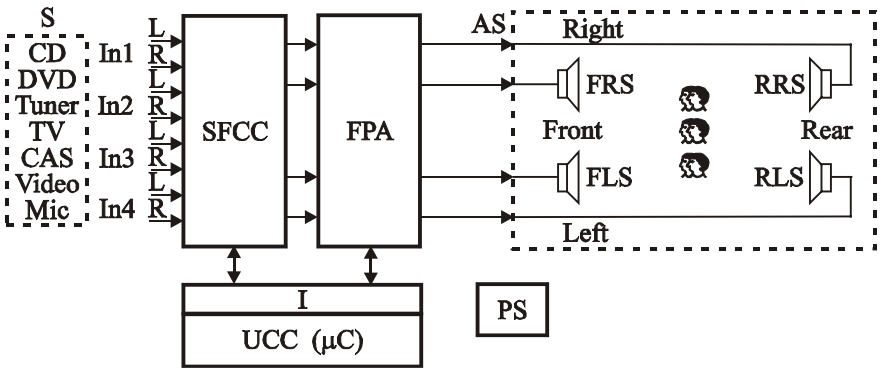

Fig. 1.

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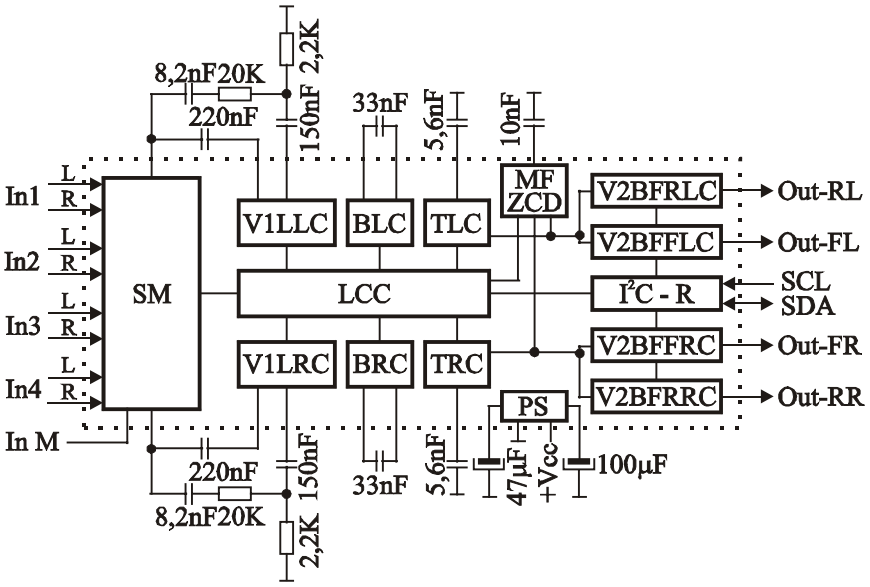

Fig. 2.

V2BFFLC - V2 volume, balance and fader front left control circuit; V2BFFRC - V2 volume, balance and fader front right control circuit; I^2C-R - I^2C bus receiver; LCC – circuit command and control logic; PS – power supply.

The maximal voltage level of the stereo signal input must not exceed 2 V for normal operation.

The volume control function is distributed on two sections, in the volume control block V1 of the first stage and in the volume control block V2 of the second stage. The volume control block of the first stage performs an amplification/attenuation of the audio signal ranging from +20 dB to –31 dB, with 1 dB step. The volume control block of the second stage performs an attenuation of the audio signal going from 0 dB to –50 dB, also with 1 dB step. Theoretically, the volume can be controlled from +20 dB to –86 dB, thus a dynamic range of 106 dB, but the producer only recommends a range between +20 dB and –66 dB, the dynamic range being limited to 86 dB.

The V1 volume control block includes also a loudness correction that uses an external RC filter, its characteristics depending on the values of the external components (20 KΩ, 8.2 nF, 2.2 KΩ, 150 nF). The loudness correction varies the frequency response of the first stage amplifier in order to obtain optimal audition at various volume levels. This feature is necessary because the sensibility of the human ear has non-linear variation in the audio frequency range. For a 20 dB amplification of the first stage amplifier, the filter is linear. The characteristics rises in the 32 dB range and reaches a maximum for a level of –12 dB, where it becomes constant even if the volume continues to drop.

The bass correction block requires only one 33nF capacitor for each channel. The capacitors, combined with the block's internal resistors, constitute a correction filter. The range of the bass corrector is between –15 dB and +15 dB with 1.5 dB step for a 40 Hz input signal.

The treble correction block requires a 5.6 nF capacitor for each channel that, in combination with the internal resistors, constitute the correction filter. The range of the treble corrector is between –12 dB and +12 dB with 1.5 dB step for a 15 KHz input signal.

The last control section for the audio signal is the second volume control stage. This section includes four independent attenuators, each on every of the following outputs: rear-left, front-left, front-right and rear-right. The functions performed by this block are volume, balance and fader control.

The mute function of the circuit has three operation modes:

- enable when connecting the corresponding circuit pin to a logical 0 level;
- quick enable through a command placed on I^2C bus by the command and control unit;
- enable by I^2C bus when audio signal crosses zero; the maximal delay for audio signal zero crossing is 100 ms.

III. THE FINAL POWER AMPLIFIER

It consists of four Hi-Fi power amplifiers. Each one is built using the TDA2613 integrated circuit.

This circuit insures an audio signal pre-amplification, delivers the excitation currents for the final levels, performs a current amplification in the final levels, suppresses unwanted input signals which appear during power-on and power-off, insure thermal protection for the final levels and offers the possibility of symmetric or asymmetric voltage supply.

The structure of a power amplifier using symmetric voltage supply is shown in figure 3.

IV. THE COMMAND AND CONTROL UNIT

The command unit is equipped with the AT89S8252 microcontroller which includes, on a single chip, the following resources: a processor optimised for command and control applications, the 8 Kbytes

FLASH program memory, the 256 bytes RAM data memory, the 2 Kbytes EEPROM date memory, a memory space for special functions registers, four 8-bit parallel ports, three 16-bit counters, programmable hard watchdog timer, a unit for the serial asynchronous data communications (UART), serial peripheral interface (SPI), nine interrupt sources on two priority levels , internal oscillator (f_{max}=24MHz), etc.

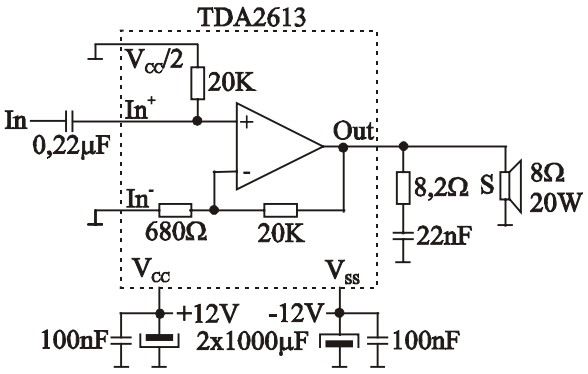

Fig. 3.

From the previous enumeration one can notice that the microcontroller has a large number of inputs and outputs that allow a simple interfacing with other circuits.

The command unit (fig.4) includes around the microcontroller chip: a 20 MHz quartz crystal and two 30 pF capacitors for the clock oscillator, an RC group (10 KΩ and 10 µF), a 1N4148 diode and a switch K for initialization, and two capacitors (100 nF and 10 µF) for decoupling.

The command of the sound fader control circuit is made by microcontroller AT89S8252 through the serial interface I^{2}C. But the microcontroller does not feature this interface and it must be therefore implemented by software.

The communication between the microcontroller AT89S8252 as master and the sound fader control circuit as slave is made using port P0, that has open-drain lines, and two 10 KΩ resistors (fig.5).

The START condition is obtained by a high-to-low transition for the data signal SDA, while clock signal SCL is maintained in high. The STOP condition is determined by a low-to-high transition of the data signal, during which the clock signal is held in high.

The unidirectional line P0.0 of the microcontroller delivers the clock signal SCL. Connecting the microcontroller's output line P0.1 and input line P0.2 obtains the bidirectional data line SDA. When I^{2}C communication is not used, the clock and data lines are held in logical 1.

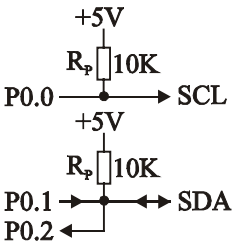

Fig. 5.

A data transfer on bus I^{2}C starts by generating the START condition, then continues by transmitting data and ends by generating the STOP condition by the master, as depicted in fig.6.

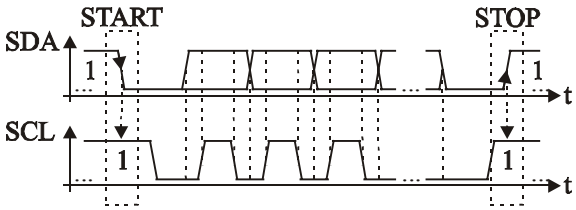

Fig. 6.

The data bits transmitted change during the low level of the clock signal. On the high level of the clock signal, the data is maintained stable. The data transmitted on I^{2}C bus is eight-bit long, the most significant bit being transmitted first. After transmitting eight data bits, the receiving circuit generates an acknowledge bit. Using a low level, the receiver informs the transmitter that it has received the data byte. During the acknowledgement bit, the master circuit generates the clock and its data line is maintained in the high level.

The slave receiver generates the acknowledgement bit after receiving each data byte and will not generate this bit if it is not able to receive data. In this situation, the master transmitter will initiate the STOP condition.

The data format on I^{2}C bus when the master microcontroller transmits towards the slave sound fader control circuit is depicted in fig.7; the notes are:

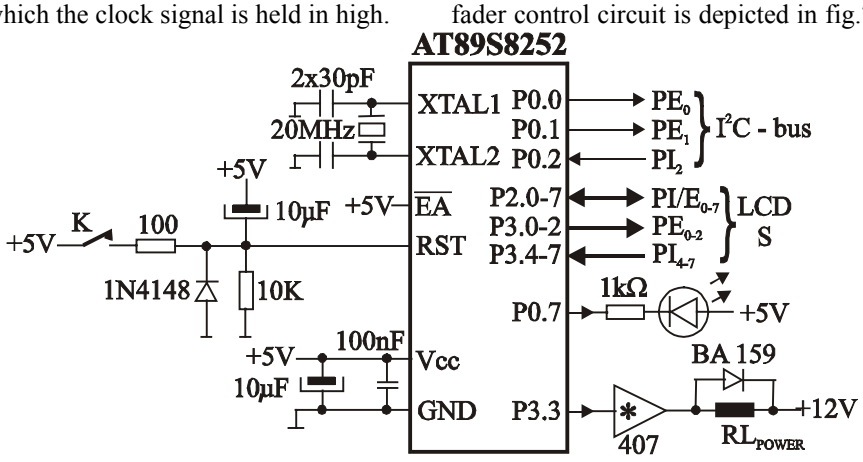

Fig. 4.

Fig. 7.

START - transmission initiation condition; MAD - slave address byte; A – acknowledgement bit; SAD - sub-address byte; DATA - data byte; STOP - transmission termination condition.

The slave address byte of the sound fader control circuit has the value 80H=1000 0000B.

The sub-address byte has the role to select one function for the sound fader control circuit from the following: general volume control (V); fader control front right (FFR); fader control front left (FFL); fader control rear right (FRR); fader control rear left (FRL); bass control (B); treble control (T) ; sound selector control (S).

Table 1 contains the binary values of the functions from the sub-address byte. The five most significant bits are zero logical and the three last significant bits constitute the binary value of the function.

Table 1

Functions	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
V	0	0	0	0	0	0	0	0
FFR	0	0	0	0	0	0	0	1
FFL	0	0	0	0	0	0	1	0
FRR	0	0	0	0	0	0	1	1
FRL	0	0	0	0	0	1	0	0
B	0	0	0	0	0	1	0	1
T	0	0	0	0	0	1	1	0
S	0	0	0	0	0	1	1	1

The data byte for each selected function has the structure detailed in table 2; the notes in the table stand for: ZCM – zero crossing mode; LOFF – switch loudness on/off; GMU – mute control for all outputs.

Table 2

Functions	bit7	bit6	bit5	bit4	bit3	Bit2	bit1	bit0
V=00	ZCM	LOFF	V5	V4	V3	V2	V1	V0
FFR=01	-	-	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
FFL=02	-	-	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
FRR=03	-	-	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
FRL=04	-	-	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
B=05	-	-	-	B4	B3	B2	B1	B0
T=06	-	-	-	T4	T3	T2	T1	T0
S=07	GMU	-	-	-	-	S2	S1	S0

Bits GMU and ZCM provide the mute function as follows:

- GMU=0 and ZCM=0 for direct mute off;
- GMU=0 and ZCM=1 for mute off delayed until next zero crossing;
- GMU=1 and ZCM=0 for direct mute on;
- GMU=1 and ZCM=0 for mute on delayed until next zero crossing;

LOFF bit switches the loudness control as follows:

- LOFF=0 - V1 volume control using loudness;
- LOFF=1 - linear V1 volume control.

The control bits for V1 general volume have binary values from 111111B to 001100B in order to provide a level gain ranging between +20 dB and –31 dB with 1 dB step (table 3).

Table 3

G V1	V5	V4	V3	V2	V1	V0
+20 db	1	1	1	1	1	1
+19 db	1	1	1	1	1	0
……	……					
0 db	1	0	1	0	1	1
……	……					
-31 db	0	0	1	1	0	0

When loudness is on, the increment of the loudness characteristics is linear at every volume step in the range from +20 dB to –11 dB. The loudness characteristics stays constant for a gain ranging from –12 dB to –31 dB. For the binary values of the volume ranging from 001011B and 00000B, the gain steps between –28 dB and –31 dB are repeated.

The control bits for the second stage volume V2 provide on each separate channel i.e. fader front right, fader front left, fader rear right and fader rear left. The binary values from 111111B to 001000B provide a gain ranging from 0 dB to –55 dB with 1 dB step (table 4).

Table 4

G V2	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
0 db	1	1	1	1	1	1
-1 db	1	1	1	1	1	0
-2 db	1	1	1	1	0	1
……	……					
-55 db	0	0	1	0	0	0

The binary values from 000111B to 000000B for the volume control of second stage from any channel enable mute function. By soft volume may vary on each channel and left-right or front-rear balance function may be implemented.

The control bits for bass have binary values from 11011B to 00110B for a gain ranging from +15 db and –15 db with 1.5 db step (table 5).

Table 5

G B	B4	B3	B2	B1	B0
+15 db	1	1	0	1	1
+13.5 db	1	1	0	1	0
……	……				
+1.5 db	1	0	0	1	0
0* db	1	0	0	0	1
0 db	1	0	0	0	0
-1.5 db	0	1	1	1	1
……	……				
-13.5 db	0	0	1	1	1
-15 db	0	0	1	1	0

The binary values of the bass control ranging from 11111B to 11100B provide the +15 dB and +13.5 dB level, by means of repetition, while the values between 00101B and 00100B provide the –13.5dB and –15 dB levels. The numeric range between 00011B and 00000B disables the bass corrector.
The control bits for treble have binary values from 11001B to 01000B for a gain ranging from +12dB and –12dB with 1.5 dB step (table 6).
Table 6

G T	T4	T3	T2	T1	T0
+12 db	1	1	0	0	1
+10,5 db	1	1	0	0	0
……	……				
+1,5 db	1	0	0	1	0
0* db	1	0	0	0	1
0 db	1	0	0	0	0
-1,5 db	0	1	1	1	1
……	……				
-10,5 db	0	1	0	0	1
-12 db	0	1	0	0	0

Gain levels of +12 dB and +10.5 dB are obtained using repeatedly binary values of the treble control between 11111B and 11010B. The binary value range between 00111B and 00000B disables the treble corrector.
The binary value 00000B for bass and treble control is intended for the use of an external equalizer.

The input selection bits S connect one of the four stereo signals or the mono one, as detailed in table 7.
Table 7

Functions	S2	S1	S0
Input stereo In 1	1	1	1
Input stereo In 2	1	1	0
Input stereo In 3	1	0	1
Input stereo In 4	1	0	0
Input mono In M	0	-	-

The commands of the Hi-Fi amplifier such as on/off, input selection, setting the audio source, the first stage volume control, the left-right, front-rear balance and the fader control are all displayed on a LCD.
A M1632, two rows, 16-characters/row display module is used. The circuit HD44780 included in the module performs the display control.
The display module is connected to the microprocessor using parallel input/output ports as in figure 8; characters having ASCII codes from 20H to 7FH can be displayed (uppercase and lowercase letters, digits and punctuation marks) but also a series of special characters having ASCII codes ranging from A0H to FFH. The main features of the display module are: internal character generator, display data memory, read/write memory access and various functions for clearing, moving the cursor in the upper-left corner, enabling/disabling the display or the cursor, cursor and display shifting, blinking display and so on.

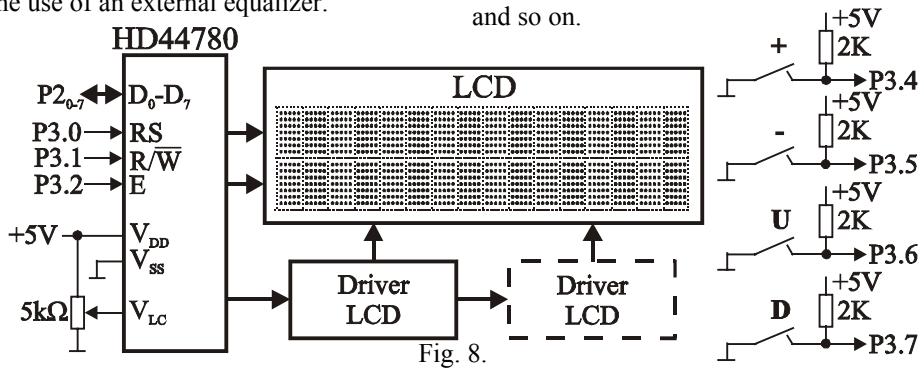

Fig. 8.

The input and edit of certain commands are made using four switches (figure 8).
Two switches (‘**U**’ - up and ‘**D**’ - down) select the current command from a list, while the other two switches (‘**+**’ increment, ‘**-**’ decrement) are used to set the current numeric value.
The command program is interrupt-based and consists of a main program and a program sequence for interrupt requests treating.
The main program detects the switches’ status, updates the software image of the process in the internal data memory of the microcontroller and displays the commands from a list on the display module.
The command list is:

1. POWER
OFF
ON
2.INPUT SELECT
In 1
In 2
In 3
In 4
(In M)
3. SOURCE SELECT
CD
DVD
Tuner
TV
CAS
Video
MIC
4. AUDIO CONTROL

Volume	*+3db*
Balance left-righ	*0 db*
Balance front-rear	*0 db*
Fader front right	*-3 db*
Fader front left	*-3 db*
Fader rear right	*-3 db*
Fader rear left	*-3 db*
Treble	*+12 db*
Bass	*+9 db*

The EEPROM data memory of the microcontroller contains the updated values of the commands set by the user, which are not to be lost at power-off.
The program sequence for handling interrupt requests, issued every 0.1 ms, performs the communication on I^2C bus between the sound fader control circuit and the microcontroller.

V. CONCLUSIONS

The hardware structure of the Hi-Fi audio chain that the paper presents, consisting of the sound fader control circuit and the power amplifier, is digitally controlled by microcontroller AT89S8252.
This structure has a minimal hardware volume thanks to the circuit selected for the application, that present many integrated features.
The authors have built in practice this application within the "The Architecture of Systems Based on Microprocessors and Microcontrollers" university laboratory.
The microcontroller selected has an EEPROM non-volatile data memory where the user settings for the audio chain functions are stored and updated, feature that compensates for the down-side of the missing I2C interface, since this interface was implemented by software.
The command program, written by the authors using machine code language, operates in real-time and takes up to 4 Kbytes of Flash program memory, while the user data structure requires some 500 bytes of the data EEPROM memory.
The software designed by the authors gives the user access to an interactive solution, based on switches and LCD, to select functions with desired operating features and parameters.

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Logic Analyzer for Development Systems Equipped with AT89C51 Family Microcontroller

Petruţ Duma[1]

Abstract – The paper describes the hardware structure of the interface used by a logic analyzer for testing development systems equipped with AT89C51 family microcontroller. The interface is connected to a command and control unit equipped with I80C51 microcontroller and to a personal computer. The command program perform execution and testing functions for instructions run on a tested system, instruction display functions at instruction cycle, semi-cycle, state, phase and clock levels, initialisation function for the tested microcontroller, as well as other general purpose functions.
Keywords: logic analyzer, development system, ATMEL microcontroller, command software.

I. INTRODUCTION

The basic structure of a logic analyzer for a development system equipped with a microcontroller from AT89C51 family is shown in fig.1.

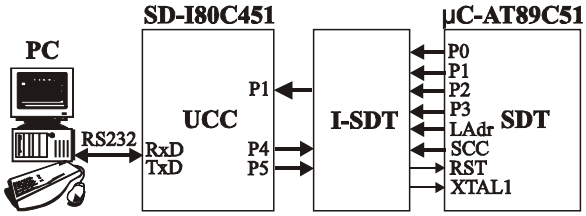

Fig. 1.

The logic analyzer consists of a command and control unit (UCC) - basically a development system (SD) equipped with microcontroller INTEL 80C51, the interface for the tested development system (I-SDT) and the tested development system itself (SDT), equipped with a microcontroller from AT89C51 family. The command and control unit communicates through the serial interface with a personal computer (PC).

II. THE STRUCTURE OF THE TESTED DEVELOPMENT SYSTEMS

The development system based on the AT89C51 microcontroller has the structure shown in fig.2
Microcontroller AT89C51 is connected to a circuitry including a 11,0592 MHz quartz crystal and two 30pF capacitors for the clock oscillator, an RC group (10 KΩ and 10 µF), a 1N4148 diode and a switch K for initialisation, and two capacitors (100 nF and 10 µF) for decoupling.
The system has external program memory and data memory, the pin /EA being therefore connected to logical 0. In order to address the external memory, the P2 port contains the high part of the address bus, while port P0 holds the low part of the address bus, multiplexed with the data bus. The low part of the address bus is latched using an 8-bit external register (74373), on the descending edge of the ALE signal. In this way the low part of the address bus is de-multiplexed from the data bus, port P0 standing subsequently for data bus. The EPROM memory (27256) has a 32 KB capacity and is addressed in the memory space ranging from 0000H to 7FFFH by connecting the address bus BA_{15} to /CE and the signal /PSEN./RD to /OE. This is designed to make sure that programs are executed from the external memory and that data is also read from that memory.
The SRAM (55257) has a capacity of 32 KB and is addressed in the memory space from 8000H to FFFFH by connecting the inverted address line BA_{15} to /CE and the signal /PR./WR=/PSEN./RD./WR to /OE. This connection scheme is designed to allow the execution of the programs from the external SRAM memory, but also the storage/retrieval of data from that same memory.
The logical levels from input (RxD)/output (TxD) of the serial interface are converted using circuit MAX232 in order to perform communication on a line with a personal computer.

III. THE INTERFACE FOR THE TESTED DEVELOPMENT SYSTEM

The tested development system has a large number of digital signals that are to be processed by the command and control unit through interface I-SDT; these digital signals are:
- port P0 – provides the low part of the address bus multiplexed with the data bus;
- port P1 – used as input/output port;
- port P2 – provides the high part of the address bus;

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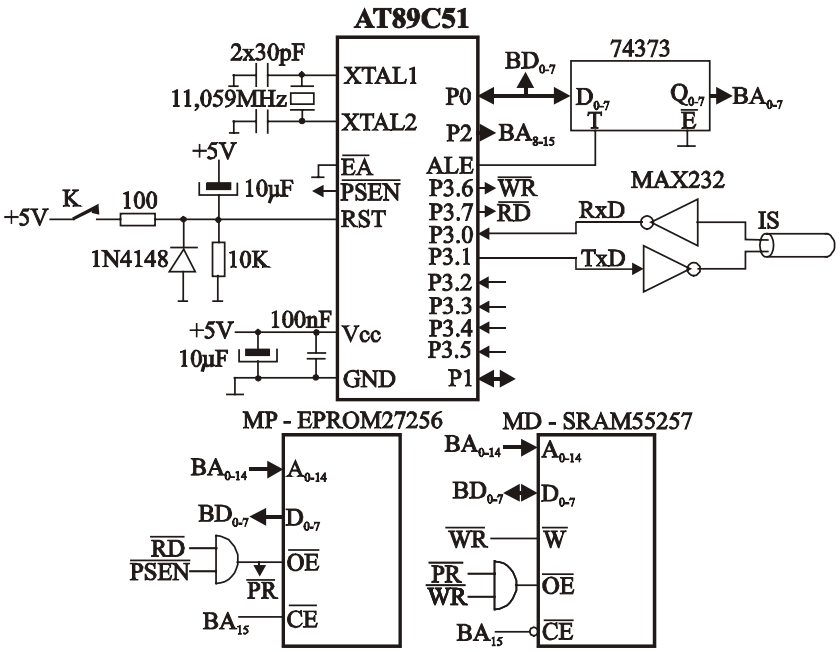

Fig. 2.

- port P3 – provides input RxD and output TxD of the serial interface, inputs for external interrupts /INT0, /INT1, inputs of counters T0, T1, outputs for the command signals /RD (read from the external data memory) and /WR (write in the external data memory);
- the low part of the address bus LAdr;
- the command and control signals SCC of the tested microcontroller: /EA (external program memory selection), ALE (de-multiplex of the low part of address bus from data bus), /PSEN (read the instruction code from the external program memory), XTAL1, XTAL2 (the test oscillator signals), Vcc and GND (microcontroller power supply).

Other tested development systems equipped with other types of microcontrollers from the same family might have in addition two ports, P4 and P5, used as input/output ports.

The command and control unit processes these signals using a 64-input analog multiplexer (fig. 3.).

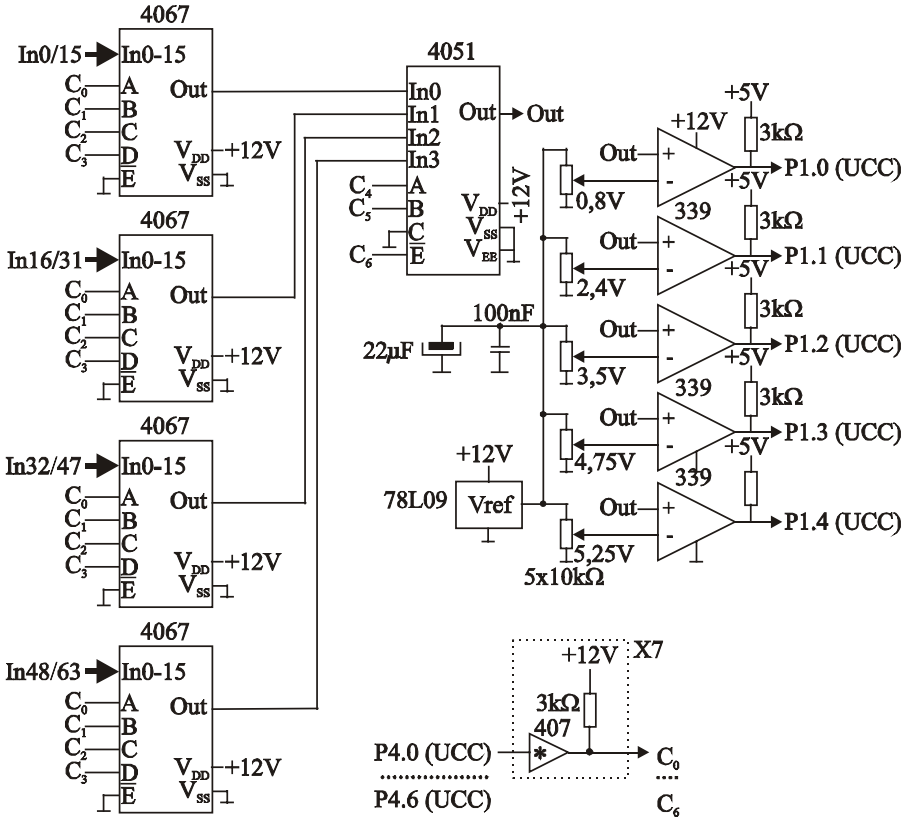

Fig. 3.

The multiplexer consists of four 4067 analog multiplexers with 16 outputs and one 4051 analog multiplexer with 8 inputs. The address of the 64-input analog multiplexer is provided by port P4 of the command and control unit through buffer 7407 that have the role to translate voltage levels. The multiplexer inputs are connected to the digital signals of the tested development system according to table 1.

Table 1

	Input MUX	Digital signal
1	In 0	P0.0 = BA_0 / BD_0
2	In 1	P0.1 = BA_1 / BD_1
…	…..	…….
8	In 7	P0.7 = BA_7 / BD_7
9	In 8	P1.0
10	In 9	P1.1
…	……	……
16	In 15	P1.7
17	In 16	P2.0 = BA_8
18	In 17	P2.1 = BA_9
…	…….	……..
24	In 23	P2.7 = BA_{15}
25	In 24	P3.0 = RxD
26	In 25	P3.1 = TxD
27	In 26	P3.2 = /INT0
28	In 27	P3.3 = /INT1
29	In 28	P3.4 = T0
30	In 29	P3.5 = T1
31	In 30	P3.6 = /WR
32	In 31	P3.7 =/RD
33	In 32	BA_0
34	In 33	BA_1
…	……	……
40	In 39	BA_7
41	In 40	SCC.0 = /EA
42	In 41	SCC.1 = ALE
43	In 42	SCC.2 = /PSEN
44	In 43	SCC.3 = XTAL2
45	In 44	SCC.4 = XTAL1
46	In 45	SCC.5 = RST
47	In 46	SCC.6 = Gnd
48	In 47	SCC.7 = Vcc
49	In 48	P4.0
50	In 49	P4.1
…	……	……
56	In 55	P4.7
57	In 56	P5.0
58	In 57	P5.1
…	……	……
64	In 63	P5.7

The digital signals can have correct or incorrect voltage levels; specifically, the logical 0 level must be lower that 0.8 V, logical 1 level must generally be higher that 2.4 V, except for logical 1 of signals RST and XTAL1 which should be no less than 3.5 V, while the power supply voltage must range between 4.75 V and 5.25 V.

In order to validate these conditions, the hardware structure required must compare the output Out of the analog multiplexer to voltage levels 0.8 V, 2.4 V, 3.5 V, 4.75 V and 5.25 V (fig.3).

This hardware structure consists of 339 comparators that have their inputs In+ connected to output Out of the analog multiplexer, and the In- inputs the standard comparison voltages delivered by a voltage reference adequately divided using multi-tour potentiometers.

The comparators' outputs are connected to port P1 of the command and control unit, and the logical levels obtained can be interpreted as in table 2.

Table 2

P1.4	P1.3	P1.2	P1.1	P1.0	Describe
0	0	0	0	0	0 logical (< 0.8V)
0	0	0	1	1	1 logical (>2.4V)
0	0	1	1	1	1 logical (> 3.5V)*
0	1	1	1	1	4.75V < Vcc < 5,25V
any other combination					wrong level

* for RST and XTAL1 signals

The interface must provide the clock signal and the initialisation signal for the tested development system (fig.4).

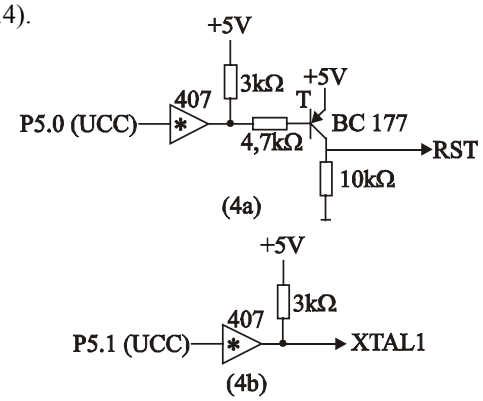

Fig. 4.

An open-collector buffer (7407) is used in order to provide the clock signal, delivering a logical 1 voltage higher that 3.5 V. The command of the clock oscillator from the tested system is applied to XTAL1 using bit P5.1 of the command and control unit.

The quartz crystal must be removed from the tested development system in order to apply a software-generated clock.

The initialisation of the tested development system is made using an open-collector buffer (7407) and a transistor BC177. A logical 0 to the buffer's input, applied by bit P5.0 of the command and control unit determines transistor T to saturate and a voltage level of +5V-U_{CEsat} (higher than 3.5V) is applied to input RST of the microcontroller. It is required that the initialisation signal is active for at least 24 clock periods. A logical 1 applied to the buffer's input determines transistor T to block and a logical 0 to be delivered to input RST after 10 µF capacitor C of the

initialisation circuit is loaded. The microcontroller of the tested development system terminates the initialisation cycle, and then starts the execution of the program from address 0000H of the external program memory.

IV. THE EXECUTION OF THE INSTRUCTIONS STORED IN THE EXTERNAL PROGRAM MEMORY

After the microcontroller of the tested development system is initialised based on the signals software-provided by the command and control unit, the instructions stored in the external program memory are executed starting from address 0000H. The AT89C51 microcontroller family has one, two or three-byte long instructions. The first byte always consists of the instruction code, while the following one or two represent data, an address, a relative displacement, etc. An instruction is executing during an instruction cycle (CI) that consists of one, two or four machine cycles (CM) (table 3).

Table 3

No. bytes	No. machine cycles
1	1
1	2
1	4
2	1
2	2
3	2

Any machine cycle consists of six states (S1, S2,... S6), each of them including two phases (P1 and P2). A phase corresponds to one clock period. The command and control unit provides the clock of the tested system by software, and for each level of the clock signal, it loads in the system's memory all the digital signals through the analog multiplexer and the comparators.

The general time diagram including all the command signals for the execution from the program memory of a one, two or three-byte instruction in one, two or four machine cycles is shown in fig. 5. This diagram does not cover the MOVX instruction that addresses the external data memory.

The time diagrams with all command signals for the execution of an instruction stored in the external program memory, that reads or writes data in the external memory (MOVX) are shown in fig. 6 and fig.7.

V. THE COMMAND PROGRAM COMMANDS

The command program is loaded into the command and control unit from the personal computer, through the serial interface and is executed automatically. First it is executed the initialization sequence, which loads the system variables, defines the data memory zone, clears the console screen and displays a program launch message.

The program then enters a loop designed to interrogate the keyboard, during which various user commands may be input. The program collects the user command, tests the command syntax and then executes it. After the user command execution, the keyboard interrogation loop is resumed, waiting for a new command.

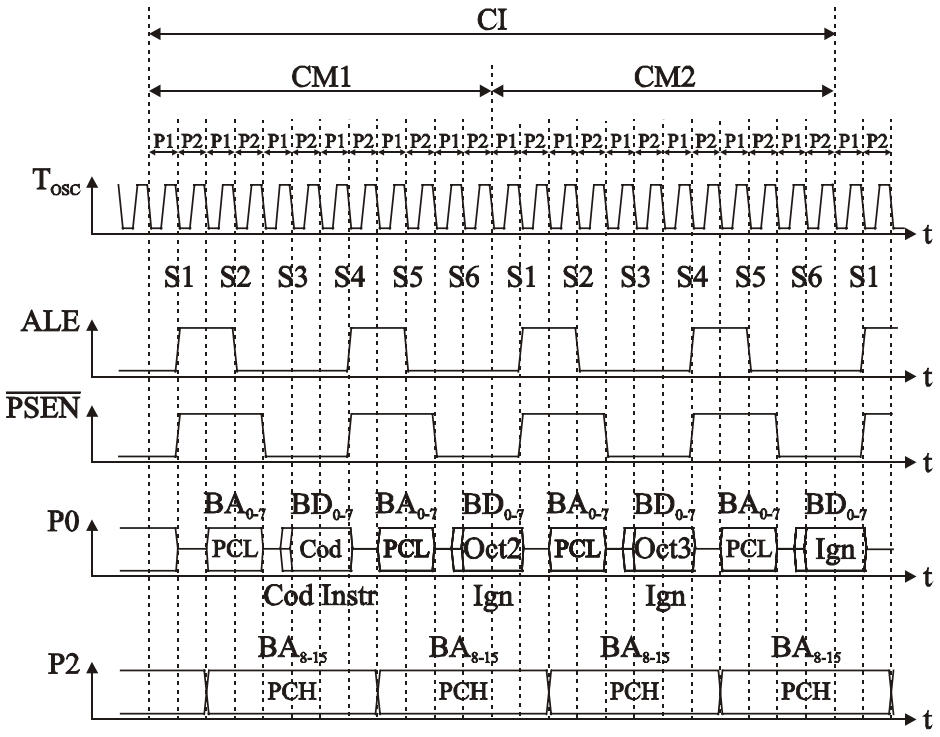

Fig. 5.

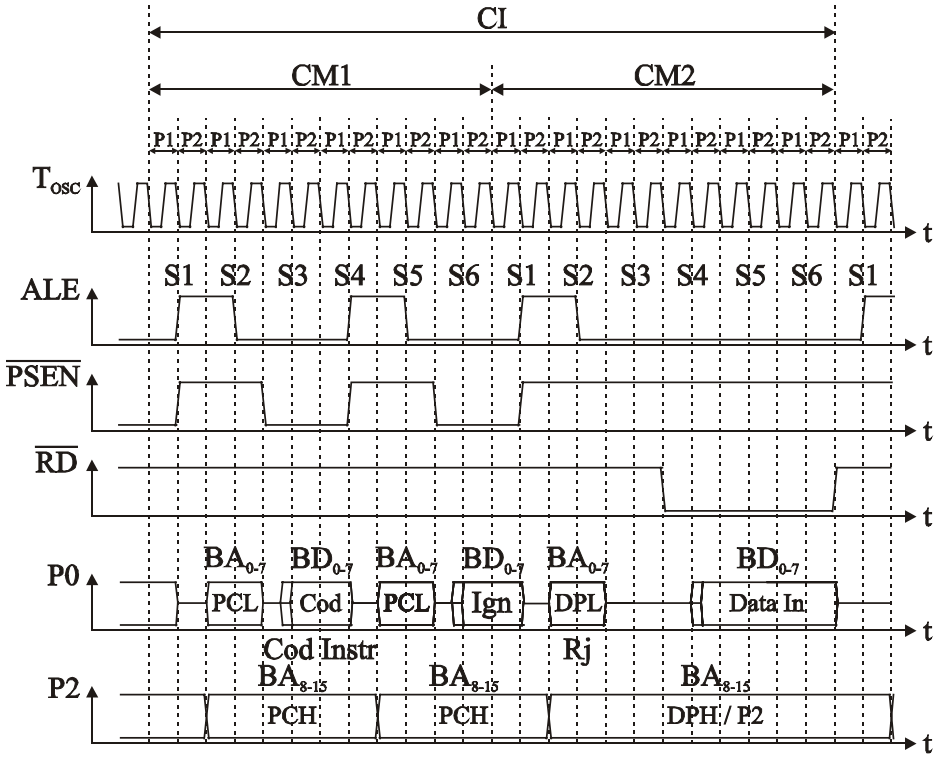

Fig. 6.

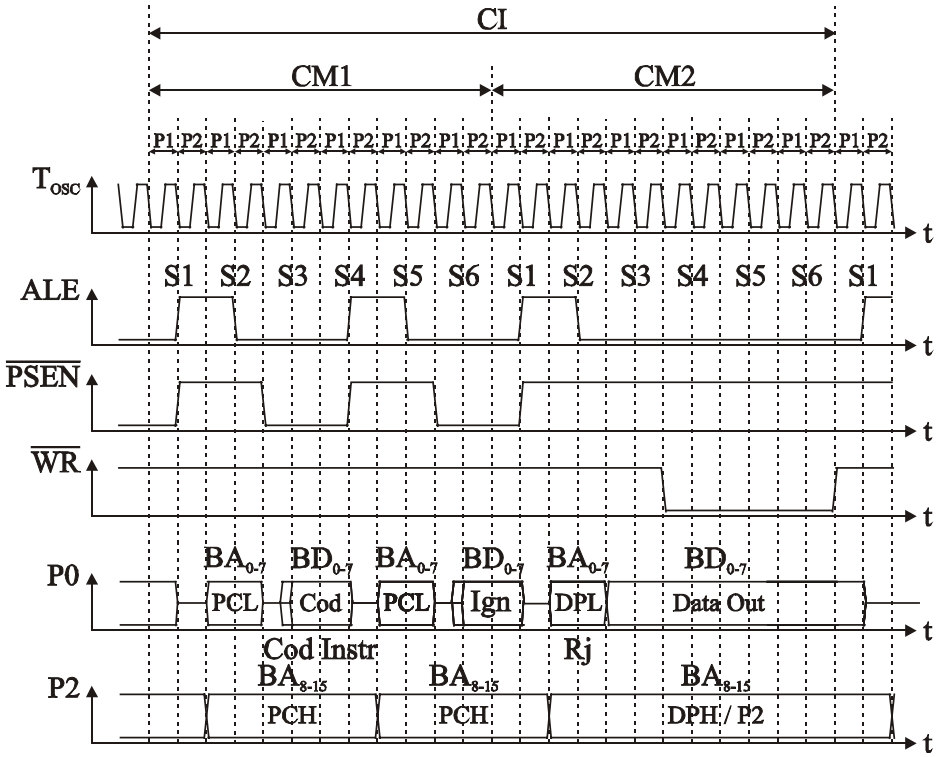

Fig. 7.

The logic analyzer commands syntax and their summary description are briefly presented below.

A. – displays on the console the list of commands accepted by the logic analyzer;

B. – selects the resources of the tested microcontroller that are to be displayed also at bit level;

DI. – displays the last instruction executed (address, instruction code, the second and the third instruction byte, mnemonic);

DC – displays the last instruction executed at semi-cycle level;

DS. - displays the last instruction executed at state level;

DP. - displays the last instruction executed at phase level;
DX. - displays the last instruction executed at clock level;
GX. – executes the current instruction at clock level;
GP. – executes the current instruction at phase level;
GS. – executes the current instruction at state level;
GC. – executes the current instruction at semi-cycle level;
GI. - executes integrally the current instruction;
GNp1 – executes p1 instructions on the tested system;
GAp1 – executes instructions on the tested system up to address p1;
Q. – exits the command program to the monitor program;
R. – initialises the tested microcontroller and executes the instruction stored at address 0000H.
The command program signalises incorrect voltage levels of any signal from the tested system and incorrect activation/de-activation logic of these signals.

VI. CONCLUSIONS

The interface of the logic analyzer described has a minimal hardware structure, it was build in practice and has proven itself a useful testing tool for development systems equipped with microcontroller AT89C51. Development systems can be tested if they are based on microcontrollers from this family and have no more than 6 parallel ports.
The command program uses a memory area of some 10 KB and features particularly useful functions.
The logic analyzer described can also be used to test application systems equipped with any AT89C51 family microcontroller, requiring adequate adjustment of the command program.

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Index of Authors