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Experimental results regarding the using of the UC3854 circuit for power factor correction in the drives with asynchronous motors

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Abstract – In this paper are presented experimental results obtained by simulation, using PSpice model of the UC3854 circuit and the average model of the boost converter, and by measurements on experimental stand, regarding the manner in which the capacitor from voltage control loop affects the dynamic response of power factor circuit at voltage supply changes. Also, it was studied the manner in which the values of this capacitor affects the power factor and the total harmonic distortion factor. The efficiency of power factor circuit depending on output power and power factor modification depending on asynchronous motor speed were experimental determined.
Keywords: UC3854, boost converter, power factor

I. INTRODUCTION

The static frequency converters with dc voltage link used for asynchronous motors drives contain in their structure rectifiers for changing the ac voltage given by the utility grid into dc voltage. Once with the development and increasing the performances of the electronic equipments, new performances of rectifiers are required. As a result, modern rectifiers have many of the de-dc converters principle. The reason is the low power factor and unexpected current harmonics that appear in classical rectifiers.
In the first part of the paper is developed an average model for boost converter available both in continuous conduction mode CCM and in discontinuous conduction mode DCM, model which will be used for modeling and simulating the circuit for power factor correction using UC3854 as command circuit.
In the second part it is presented the way of modeling and simulating in PSpice for UC3854. To realize the power factor correction PFC circuit is necessary to simulate before with one of the programs for computer-aided design like Orcad, Protel, Caspoc etc. These programs must contain libraries with models for all the components that are in the electronic circuit that is simulated. So, to simulate the PFC circuit, to see how it works and its performances, is necessary to simulate the control circuit UC3854, as this is not in the libraries for simulation programs. In this part it was analyzed by simulation how the capacitor from voltage control loop influences: the dynamic response of PFC circuit to the modifying input voltage, power factor PF and total harmonic distortion THD factor.
In the third part there are presented the laboratory experimental results. It was experimental determined the efficiency to the PFC circuit regarding to output power and power factor regarding to the speed of asynchronous motor.

II. AVERAGE MODEL FOR BOOST CONVERTER

Because state-space averaging model for boost converter taking into account the working conditions, CCM or DCM, in the next will be developed an average model unchanging in time, valid regardless of working conditions.
For boost converter from Fig.1 the PWM switch formed by active switch S and the diode D changes his topology in time. In this way appears the idea to mediate only this element.

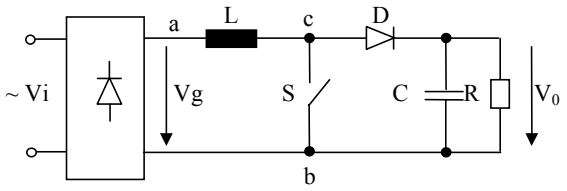

Fig.1. Circuit of the boost converter

In DCM, when S is open and through L passes current in time T_{off}, like in Fig.2, between points c and d is applying the output voltage V_0. When the current from L is breaking, D is blocking and between c and d is applying the rectified voltage V_g in time $T-T_{on}-T_{off}$. T_{on} is switch S conduction time. The average value of

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the voltage between c and d in time switching period T will be:

$$V_{cb,med} = V_0 D_{off} + V_g (1 - D_{on} - D_{off}), \quad (1)$$

where: $D_{on}=T_{on}/T$, and $D_{off}=T_{off}/T$.
In CCM the last term of (1) will de zero.
In Fig.2 is presented the wave shape of inductor current in DCM.

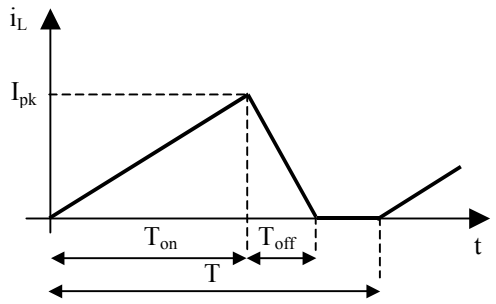

Fig. 2. Inductor current in discontinuous case

The average value of inductor current depending on peak current I_{pk} is [1]:

$$i_L = I_{pk}(D_{on}+D_{off})/2. \quad (2)$$

The average value of diode current is [1]:

$$i_D = I_{pk}D_{off}/2. \quad (3)$$

From (2) and (3) yields:

$$i_D = i_L D_{off}/(D_{on}+D_{off}). \quad (4)$$

Average model of the boost converter is obtained by (1) and (3). This model is presented in Fig.3 and it is valid regardless working mode CCM or DCM.

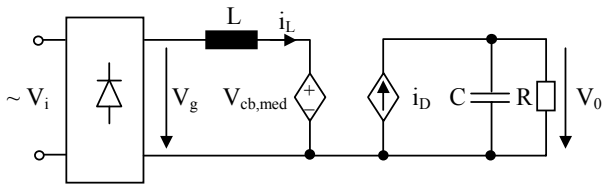

Fig. 3. Average model of boost converter

From [2], in DCM, i_d is:

$$i_D = V_g D_{on} D_{off} T/2L. \quad (5)$$

The last two equations give:

$$D_{off} = (2 i_L L/V_g D_{on} T) - D_{on}. \quad (6)$$

In CCM:

$$D_{off} = 1 - D_{on}. \quad (7)$$

Because the average model of boost converter must be valid in DCM and CCM, D_{off} is choosing:

$$D_{off} = \min\{(2 i_L L/V_g D_{on} T) - D_{on}, 1 - D_{on}\}. \quad (8)$$

This model was implemented in PSpice using voltage source voltage controlled and current source voltage controlled. The duty factors D_{on} and D_{off} appear like voltages accordingly nodes D_{on} and D_{off} as can be shown in Fig. 4.

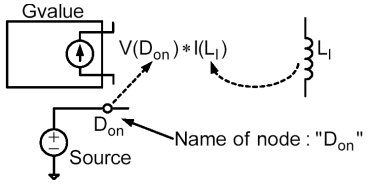

Fig. 4. PSpice representation of duty factor D_{on}

Pspice implementation of average model for boost converter is presented in Fig. 5.

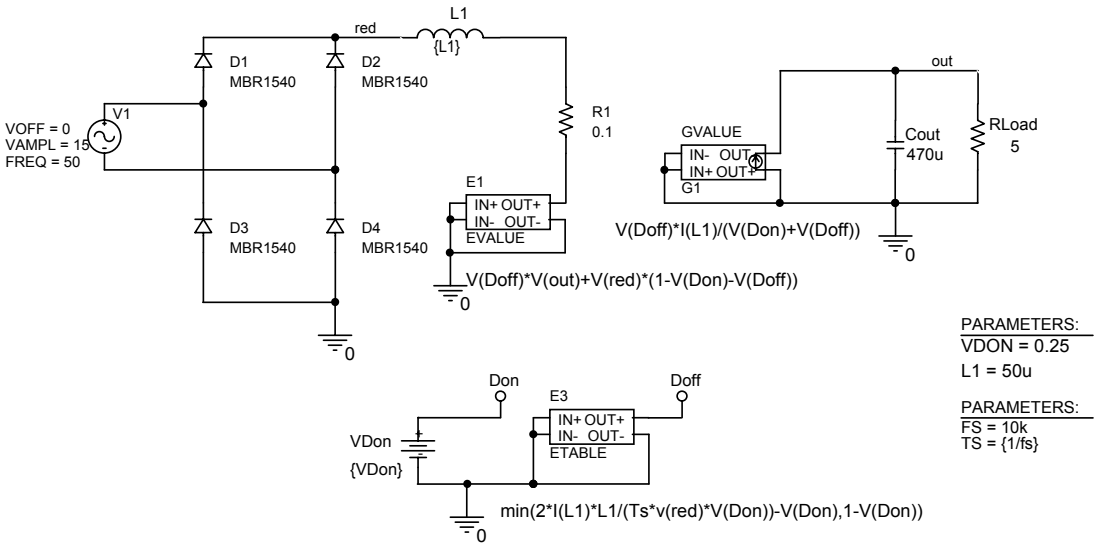

Fig. 5. PSpice implementation of average model for boost converter

In Fig. 6 are presented wave shapes for output voltage and current through inductance when is used average model and real model that contains the power transistor and the diode. As can we see, the wave shapes obtained using average model is mean values for real case. The simulation time for average model is ten times lower than for real case.

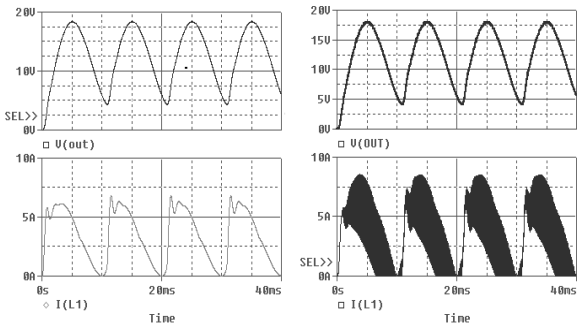

Fig. 6. Wave shapes for average model a) and for real model b)

III. PSPICE MODEL FOR UC3854

The UC3854 provides active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC3854 contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC3854 contains a power MOSFET compatible gate driver, 7.5V reference, load-enable comparator, low-supply detector, and over-current comparator. The UC3854 uses average current-mode control to accomplish fixed frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

For UC3854 will be implemented only principal blocks: multiplier-divider-square, current error amplifier, voltage error amplifier and PWM modulator.

PSpice model of multiplier, divider and squarer MDS is presented in Fig. 7.

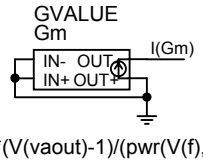

Fig. 7. PSpice implementation of multiplier-divider-square block

MDS block keep the current loop gain constant [3]. This circuitry makes it possible to operate a boost PFC stage over a 3:1 input voltage range and still get excellent voltage loop bandwidth and fast response to input voltage variations. The output of the voltage error amplifier V(vaout) is divided by the square of the average input voltage V(f) before it is multiplied by the rectified input signal I(V_Iac). I(Gm) is output quantity of the MDS and it is given by [4]:

$$I(Gm)=I(V\_ac)\cdot[V(vaout)-1]/V(f)^2 \qquad (9)$$

Equation (9) is modeled with part GVALUE from Analog Behavioral Model ABM library.

Current error amplifier is a large bandwidth amplifier. Feedback loop part has been designed like in [5]. PSpice implementation of current error amplifier and Bode plots obtained by simulation are presented in Fig. 8 and Fig. 9.

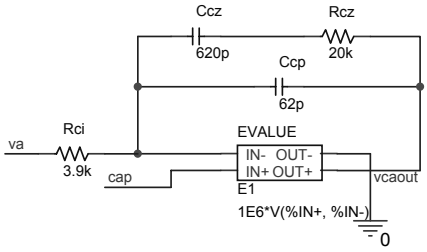

Fig. 8. Current error amplifier

In flat zone of frequency characteristic of current error the zero corresponds to 12,38 kHz, while the pole to 141,18 kHz. The crossover frequency is 15,7 kHz and it is in the flat zone. The phase margin is $46{,}2^0$, being an acceptable value.

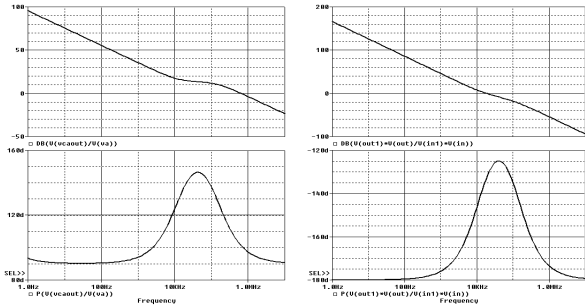

Fig. 9.a) Frequency characteristics for error amplifier b) transfer function in open loop

PSpice implementation of voltage error amplifier and its frequency characteristic are presented in Fig. 10 and Fig. 11.

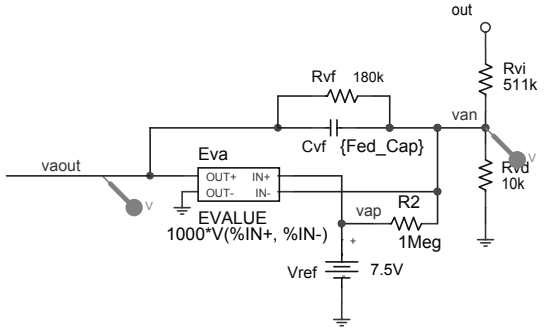

Fig. 10. PSpice model of voltage error amplifier

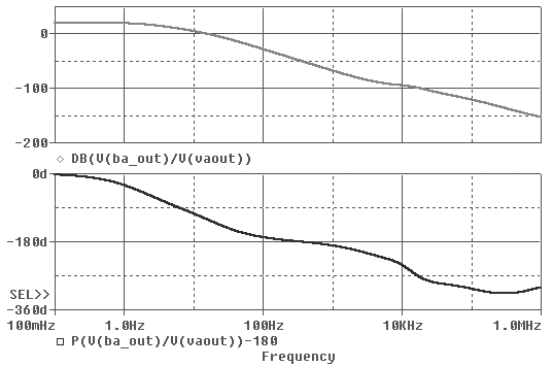

Fig 11 Voltage error amplifier

The voltage control loop must be compensated for stability but because the bandwidth of the voltage loop is so small compared to the switching frequency the requirements for the voltage control loop are really driven by the need to keep the input distortion to a minimum rather than by stability. The bandwidth of the voltage control loop is determined by the amount of input distortion to be contributed by the output ripple voltage. If the output capacitor is small and the distortion must be low then the bandwidth of the loop will be low so that the ripple voltage will be sufficiently attenuated by the error amplifier. Transient response is a function of the loop bandwidth and the lower the bandwidth the slower the transient response and the greater the overshoot. The output capacitor may need to be large to have both fast output transient response and low input current distortion.

Feedback loop part has been designed like in [3].

The crossover frequency is 19,14 Hz and phase margin is 61^0, being an acceptable value.

PSpice model of PWM is presented in Fig.12. The PWM signal is obtained by comparison between a triangular signal and output of current error amplifier. For UC3854, the triangular signal has a minimal value V_{PP}= 1,1V and a maximal value V_{PP}=5,2V [4]. The relationship between output signal of PWM block V_{cauot} and duty factor D_{on} is given by [6].

$$D_{on} = (V_{caout}\text{-}V_{min})/V_{pp} \qquad (10)$$

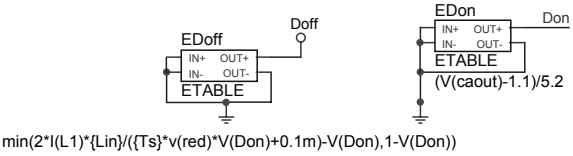

Fig.12. PWM modulator

PWM block was implemented in PSpice with voltage source ETABLE from ABM library. The voltage source EDoff is necessary because is work with average model of boost converter.

PSpice model of PFC circuit with UC3854 and average model of boost converter is presented in Fig.13.

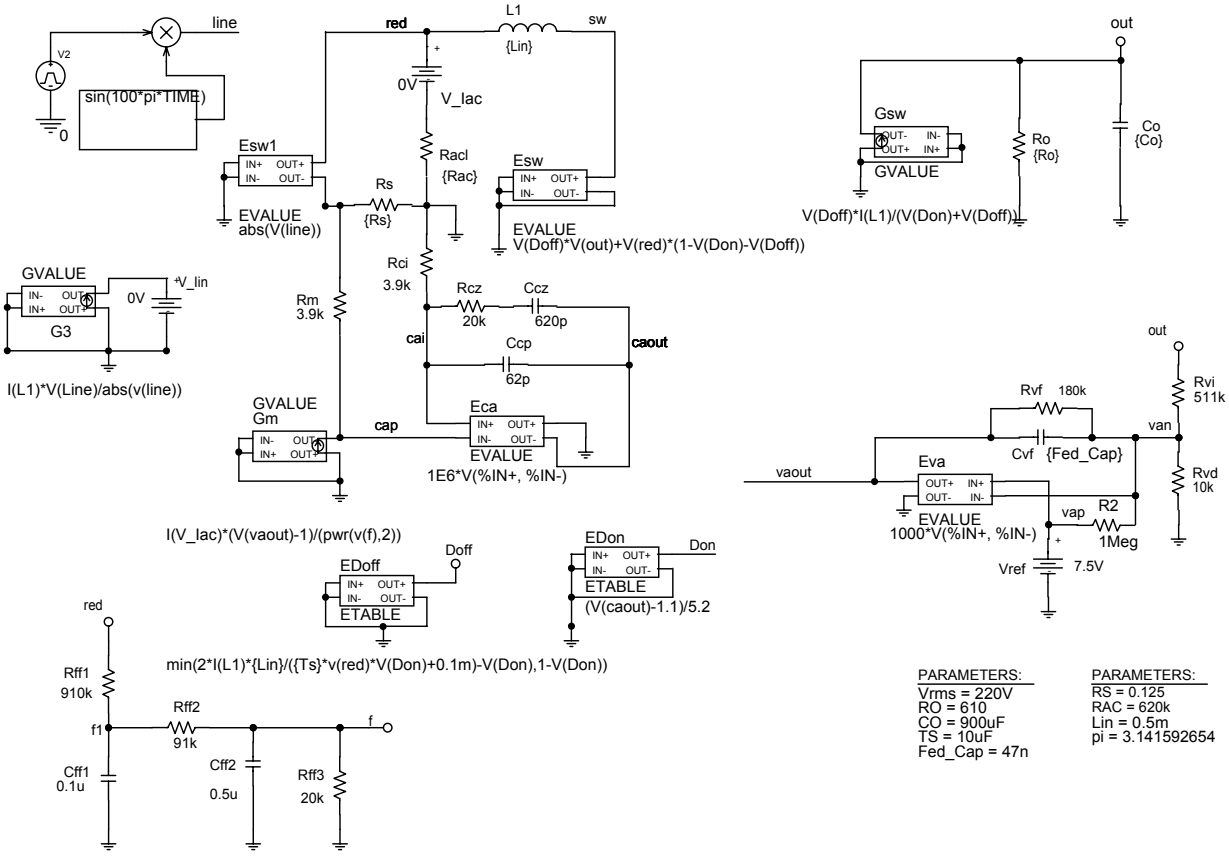

Fig. 13. PSpice model of PFC circuit

Have been supposed that at time t=0,5 seconds the utility grid was changed from115V rms at 220V rms. As can be seen from Fig. 14a, the average value of output voltage V(out) remain constant round about 400V and input current I(G3) is in phase with input voltage V(LINE). It was studied how C_{vf} from voltage control loop influences the step response at changes of utility grid and distortions introduced in input current. Were analyzed the situations when C_{vf} is0,1nF, 47nF and 300nF. Have been observed that when values of C_{vf} arise, the distortions of input current decrease, because the gain of error amplifier decreases but, the time response is slower.

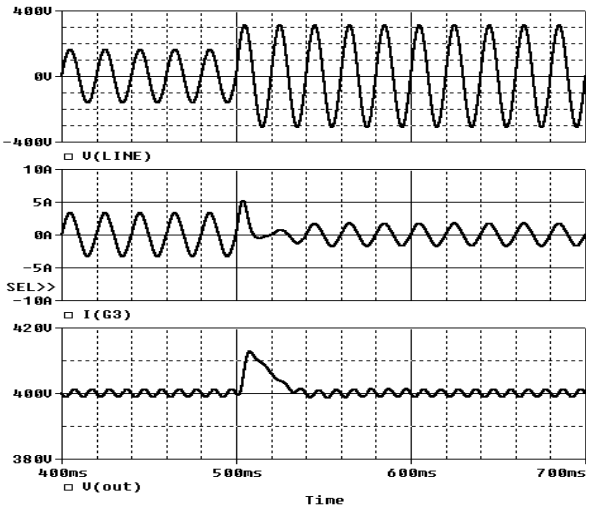

Fig.14a Simulation results obtained when input voltage changes from 155V at 220V rms for C_{vf}=47nF

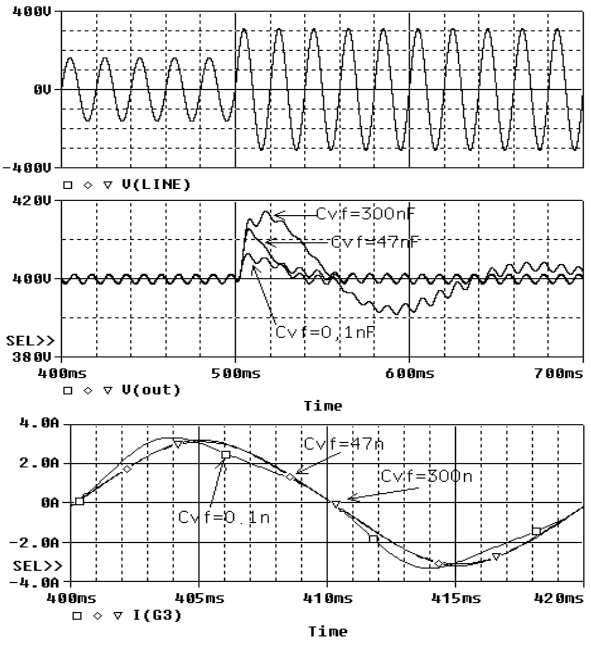

Fig 14b Dynamic response of PFC for 0,1nF, 47nF and 300nF

In Fig. 15 is presented THD and PF depending on C_{vf} values. A trade-off value of C_{vf} between small time response and high PF is C_{vf}=47nF.

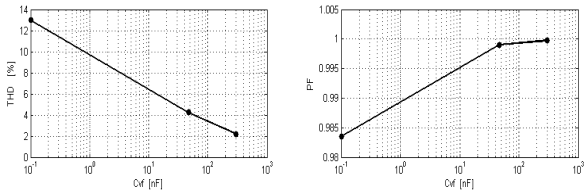

Fig. 15. THD and PF of PFC

IV. EXPERIMENTAL RESULTS

PFC circuit was designed for output power P_{out}=500W, input voltage V_{in}=220V and output voltage V_{out}=400V.

Wave shapes of acquisitioned signals and Fourier component depending on C_{vf} are presented in Fig. 16.

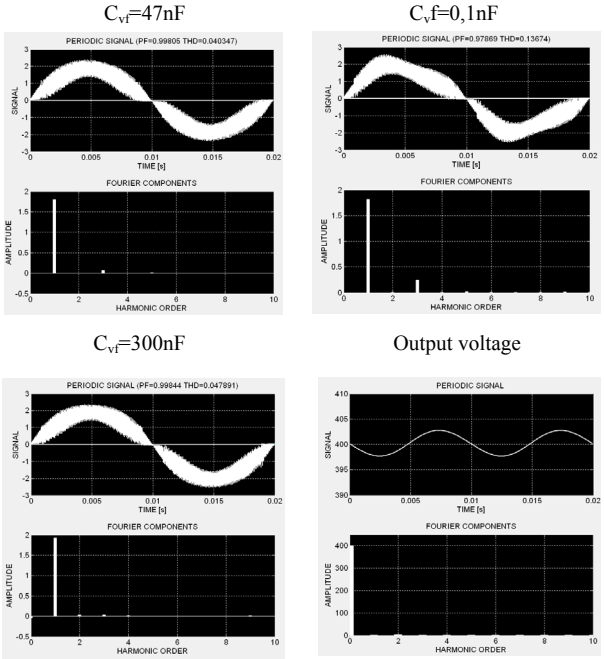

Fig. 16. Acquisition signal of input current and output voltage

Fourier components of input current obtained by acquisition and processed in Matlab are presented in Table1.

Table1 Fourier components of input current

C_{vf} harmonic no.	47nF	0,1nF	300nF
1	1,8295	1.7922	0.9174
2	0.0001	0.0001	0.0397
3	0.0289	0.2359	0.0464
4	0	0	0.0076
5	0.0476	0.0234	0.0053
6	0.0001	0	0.004
7	0.0191	0.007	0.0656
8	0.0001	0	0.0025
9	0.0136	0.0082	0.0067
10	0.0001	0	0.0016
PF	0.9980	0.9786	0.9984
THD	0.0403	0.1367	0.0478

The efficiency of PFC circuit depending on output power and PF depending on speed motor were experimental determined. The results are presented in Fig. 17 and Fig. 18.

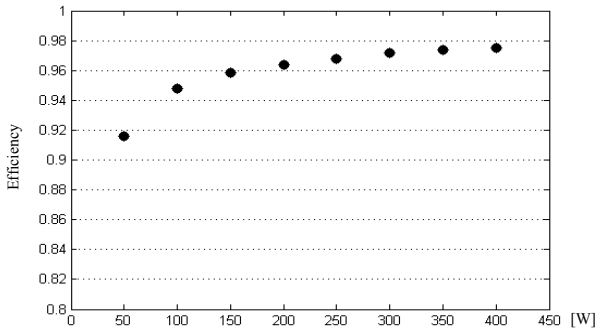

Fig. 17. Efficiency of PFC circuit

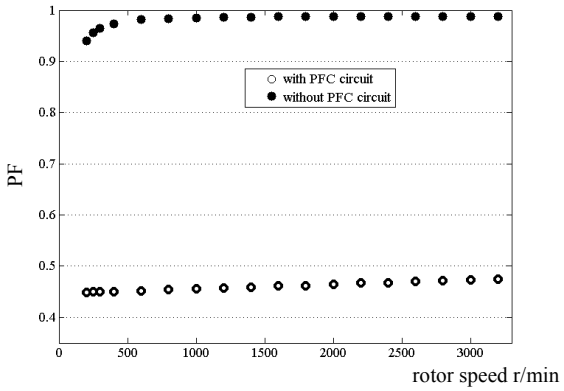

Fig. 18. Power factor with and without PFC circuit

By using PFC circuit PF rises from about 0,46 to 0,98. The speed motor was modified by 50 rotation/min between 200 and 400 r/min where was observed a more rising of PF, and by 200 r/min between 400 and 3200r/min. PF rises with motor speed. This fact is explicated by raising the input current, so, sinusoidal reference voltage of UC3854 is closely follows.

V. CONCLUSIONS

As we said at the beginning, the major disadvantages of rectifying circuits is it the low power factor and the harmonic problems that appear being necessary the usage of PFC circuits. The PFC circuit used in simulating and experiments uses the average current mode control and is realized with Unitrode part UC3854. Before the practical realization of the PFC circuit it is recommended to simulate it first. For simulating the PFC functioning it is necessary to do a model for the control circuit. Has been implemented the average model of boost converter in PSpice environment using voltage controlled voltage source and voltage controlled current source. The duty cycles D_{on} and D_{off} occur as voltage corresponding to the nods. The model shown has advantage, different than other models seen in the specific literature, that uses two controlled sources not four as the [1]. The wave shapes obtained with the average model represents the medium values of the wave shapes obtained in real model. As well, the simulation time when used the average model is ten times lower than when used real model.

It was made the PSpice model of control circuit for PFC. To realize UC3854 model it suggests a model which could be applied to a average model of boost converter. It will use parts from Analog Behavioral Model. In this case the simulation time will be lower.

It has been studied the way in which the values of capacitor in voltage regulation loop cause the modification of the PF and THD. The study was done through simulations and laboratory experiments, the results were very similar, confirming thus validity of the proposed and simulated model.

It has been determined the efficiency of PFC circuit and PF for different values of motor speed. The PF of asynchronous motor drives is substantially improved when using PFC circuit.

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