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Superior-Order Curvature-Corrected Voltage Reference with Improved Performance

Cosmin Popa, Anca Manolescu, Anton Manolescu[1]

Abstract - A new curvature-correction technique for improving the temperature behavior of a CMOS voltage reference will be presented. The reducing of the temperature coefficient for the reference voltage will be realized compensating the nonlinear temperature dependence of the gate-source voltage for a MOS transistor working in weak inversion with the difference between two gate-source voltages. These MOS transistors are polarized at drain currents with different temperature dependencies ($PTAT$ and $PTAT^{\alpha}$, respectively), α parameter being selected to the optimal value for the implementing technology. The $PTAT$ voltage generator will be designed using an original Offset Voltage Follower block, with the advantage that matched resistors are replaced by matched transistors and, in consequence, with a relatively smaller degradation of the circuit temperature behavior caused by devices' mismatches. SPICE simulation reports $TC = 1.95\,ppm/K$ for an extended temperature range, $273K < T < 363K$, without considering the parameters spread.

Keywords: Offset Voltage Follower block, subthreshold operation, superior-order curvature-correction technique, temperature coefficient

I. INTRODUCTION

The voltage reference represents a very important stage in applications such as A/D and D/A converters, data acquisition systems, memories or smart sensors.

There are two important classes of voltage references. The first class includes low-voltage low-power voltage references, with medium performances, but with the main goal of a very small minimal supply voltage and supply current. The second class is focusing to the high performances voltage references, which are mainly characterized by a very small value of the temperature coefficient for a relatively large temperature range, with the price of increasing the minimal required supply voltage, current consumption and complexity.

[1] Faculty of Electronics, Telecommunications and Information Technology Bucharest, 1-3 Iuliu Maniu

Because of the superior performance of bipolar references with respect to the circuits using MOS transistors, the first approaches of high-performance voltage reference were implemented in bipolar technology.

However, due to the nonlinear temperature dependence of the base-emitter voltage [1], there exists a theoretical limit for improving the temperature stability of a simple BGR. Basic bandgap references, with a temperature coefficient of about hundred ppm/K, useful only for applications that do not require a very good accuracy of the reference voltage, have been extensively presented in literature. In order to improve the temperature behavior of the bandgap reference, a lot of curvature-correction techniques have been developed.

The first group of these techniques is based on the correction of the nonlinear temperature dependence of the base-emitter voltage by a suitable polarization of the bipolar transistor. A polarization at a $PTAT^3$ + $PTAT^4$ collector current was proposed in [1], allowing a simulated temperature coefficient in the range of $4-8\,ppm/K$. The curvature-correction technique from [2], based on the polarization of the bipolar transistor at a $PTAT^n$ current, reports a TC about $20\,ppm/K$ without trimming and thermal stabilization of the chip.

The second possibility to improve the temperature dependence of a BGR is to compensate the nonlinear temperature characteristic of the base-emitter voltage by a correction voltage, which is added to the basic reference voltage [3], or by a correction current added to the PTAT current [4], [5]. The reference voltage presented in [3] has a relatively large temperature coefficient, about $30\,ppm/K$ for a limited temperature range, due to the MOS parameters mismatches. The compensation technique based on the correction current decreases the temperature dependence under $10\,ppm/K$, but it has the disadvantages of a large silicon occupied area and of the incompatibility with CMOS processes.

In CMOS bandgap references that are still using bipolar transistors, the required bipolar devices are realized as parasitic vertical or lateral transistors,

available in CMOS technology. The result will be a small degradation of the temperature behavior of the circuit due to the poorer match of MOS devices' parameters with respect to those of bipolar transistors.

Another approaches of CMOS references, using exclusively MOS devices and (or without) resistors implements the *CTAT* (ComplemenTary with Absolute Temperature) voltage reference using a threshold voltage extractor circuit, which generates at its output the MOS device threshold voltage, with a negative linear temperature dependence. The disadvantage of this class of CMOS references is that the exact temperature dependence of V_T is not so simple to estimate, so a curvature correction technique for improving its thermal behavior is relatively difficult to design.

The proposed realization of a CMOS voltage reference uses a gate-source voltage of a MOS transistor working in weak inversion as *CTAT* voltage generator. The negative linear dependent term from $V_{GS}(T)$ expression will be compensated by a complementary term implemented using an *OVF* (Offset Voltage Follower) block. The new curvature-correction technique is based on the compensation of the nonlinear temperature dependence of the gate-source voltage by using the difference between two gate-source voltages for MOS transistors with different temperature dependencies of theirs drain currents (*PTAT* and $PTAT^{\alpha}$, respectively), α being a constant parameter that will be further analyzed.

II. THEORETICAL ANALYSIS

A. The temperature dependence of the gate-source voltage

Similarly with the bipolar approach, the gate-source voltage represents the simplest implementation in CMOS technology of a *CTAT* voltage with the great advantage of a very good controllability through the temperature dependence of the operating drain current.

Considering a subthreshold operation of the MOS transistor, the temperature dependence of the gate-source voltage could be expressed as:

$$V_{GS}(T) = V_{FB} + E_G + \frac{V_{GS}(T_0) - V_{FB} - E_G}{T_0} T + \\ + \frac{nkT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_0} \qquad (1)$$

where T_0 is the reference temperature, γ is a technological constant and α models the temperature dependence of the drain current that biases the MOS device (it was supposed that $I_D(T) = ct.T^{\alpha}$). The first term is a constant term, the second one is a linear term, which will be compensated by a complementary linear voltage summed with the gate-source voltage and the last term models the nonlinearity of the gate-source voltage temperature dependence. This term will be compensated by a suitable logarithmic dependent on temperature term, also added to $V_{GS}(T)$.

B. The superior-order curvature-corrected voltage reference

The gate-source voltage (1) represents the zero-order compensated reference voltage. Its temperature dependence is primarily represented by the linear term, which will be cancel out (the first-order compensation) using an *OVF* (Offset Voltage Follower) block, having two important advantages: an improved accuracy achieved by replacing matched resistors by matched MOS transistors and a reduced silicon occupied area obtained by removing any resistor from the circuit. In order to remove the additional superior-order errors introduced by the last logarithmical term from (1), a curvature-correction technique will be implemented.

The superior-order curvature-corrected voltage reference is presented in Fig. 1.

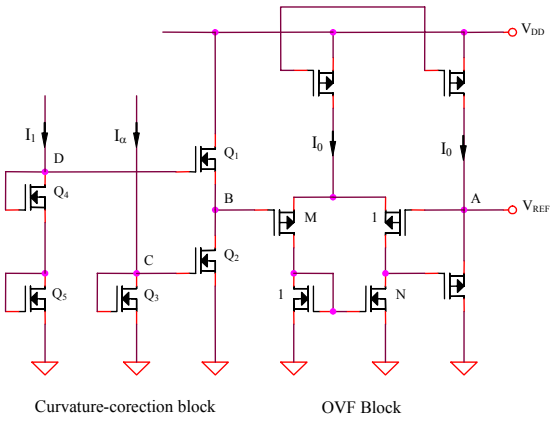

Fig. 1. The superior-order curvature-corrected voltage reference

The temperature dependence of the gate-source voltage for a MOS transistor in weak inversion is strongly increased by the linear temperature dependent term from relation (1). In order to cancel it, an original technique for implementing a complementary *PTAT* voltage will be presented, using an *OVF* (Offset Voltage Follower) block [6]. The output voltage of the *OVF* block is $V_{AB} = nV_t \ln(MN)$. For a proper choice of the aspect ratios M and N, the linear dependent term from expression (1) will be cancel out by the complementary *PTAT* voltage V_{AB}, resulting the first-order compensated reference voltage expression:

$$V_{GS}(T) = V_{FB} + E_G + \frac{nkT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_0} \qquad (2)$$

Because of the nonlinear temperature dependence (2) of the gate-source voltage for a MOS transistor working in weak inversion, the original idea is to obtain a correction term having a temperature dependence complementary to the logarithmic dependent on temperature term from (1). This correction term, summed with the zero-order compensated voltage reference (1), is represented in Fig. 1 by V_B potential and it will be obtained by subtracting a gate-source voltage (V_{GS_3}) from two summed gate-source voltages (V_{GS_4} and V_{GS_5}). The resulting expression of the reference voltage (after first- and superior-order compensations) will be:

$$V_{REF}^{(SUP)} = V_{AB} + V_B = E_G + V_{FB} + \frac{nKT}{q}(\gamma - \alpha)\ln\frac{T}{T_0} \quad (3)$$

In conclusion, the linear term from the expression of the gate-source voltage temperature dependence has been cancel out by using an OVF block, while the logarithmic dependent on temperature term from (1) could be minimized for $\alpha \cong \gamma$. The constant γ is a technological parameter, strongly dependent on the current technology. The original idea for reducing the circuit temperature dependence by minimizing the logarithmical term from (3) is to design a circuit that must be able to compute the proper value of α for the current used technology. The core of the circuit that generates a current having a $PTAT^{\alpha}$ temperature dependence (α value being optimally selected in a fixed range) is represented by a current-mode squaring circuit which must compute the function $I_B = I_C^2 / I_A$. Choosing $I_C = I_1$ (with a $PTAT$ variation) and $I_A = I_O$ (in a first-order approximation, independent on temperature), it results an output current I_B proportional to the square of the absolute temperature. For obtaining a $PTAT^3$ output current, another identical squaring circuit will be used, having $I_C = I_B^{(O)}$ and $I_A = I_1$. In the same manner, $I_B^{(n)}$ current will be $PTAT^{n+2}$, $I_B^{(I)} = I_1^3 / I_O^2$. In conclusion, all the possible integer values for the exponent α of the absolute temperature in the output current dependence have been obtained. In the following lines, the method for obtaining the non-integer values of the same exponent will be presented. For example, in order to obtain 0.5 value of the exponent, relation (6) will be used, choosing $I_A = I_1$ and $I_B = I_O$. For 0.25, $I_A = \sqrt{I_1 I_O}$ and $I_B = I_O$.

The total value of the exponent is obtained by multiplying the proper partials currents, resulting the desired value of parameter α.

III. SIMULATED RESULTS

The curvature-corrected voltage reference was implemented in $0.35\mu m$ CMOS technology. The SPICE simulation $V_{REF}(T)$ based on previous mentioned technology parameters is presented in Fig. 2.

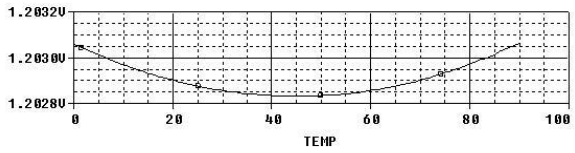

Fig. 2. SPICE simulation $V_{REF}(t)$ for the curvature-corrected voltage reference

The supply voltage is $V_{DD} = 2.5V$. The most important MOS parameters used in the previous simulation are: $V_{T_n} = 0.4V$, $V_{T_p} = -0.5V$. The simulated temperature coefficient of the reference voltage is $TC = 1.95\,ppm/^o C$ for an extended temperature range, $0 < t < 90^o C$. For sub micron processes, channel-length modulation effect will affect the bandgap reference performances, imposing the use of cascode current mirrors (having the disadvantage of increasing the minimal supply voltage of the circuit).

IV. CONCLUSIONS

A new curvature-correction technique for improving the temperature behavior of a CMOS voltage reference has been presented. The reducing of the temperature coefficient for the reference voltage has been realized compensating the nonlinear temperature dependence of the gate-source voltage for a MOS transistor working in weak inversion with the difference between two gate-source voltages. These MOS transistors were polarized at drain currents with different temperature dependencies ($PTAT$ and $PTAT^{\alpha}$, respectively), α parameter being selected to the optimal value for the implementing technology. The $PTAT$ voltage generator has been designed using an original Offset Voltage Follower block, with the advantage that matched resistors are replaced by matched transistors and, in consequence, with a relatively smaller degradation of the circuit temperature behavior caused by devices' mismatches. SPICE simulation reports $TC = 1.95\,ppm/K$ for an extended temperature range, $273K < T < 363K$, without considering the parameters spread.

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