Linearity Considerations for Adaptively Biased Transconductors with Applications in Continuous Time Filters

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Abstract – This paper discuses the approach of increasing the linearity of transconductor cells using adaptive bias currents. Adaptive biasing proves to be a powerful technique that may be used to obtain a very linear voltage-to-current conversion. The advantages of this method are its simplicity and its applicability in designing current-mode circuits that can handle wide dynamic range signals without introducing significant (harmonic) distortions. In this paper a 6th order, gm-C, Chebyshev band-pass filter is designed to demonstrate the excellent linearity of adaptively-biased transconductors.
Keywords: transconductor, adaptive bias current

I. INTRODUCTION

Current mode signal processing techniques have been in the last years the first choice for hardware designers when designing high performance analog circuits. Current mode circuits offer significant advantages when compared with voltage mode circuits: simpler structures that often lead to higher operating frequencies, higher dynamic range and lower supply voltages. Transconductor-based circuits have found applications in designing filters for wireless applications, current-mode amplifiers and other circuits that claim simplicity and high linearity at moderate frequencies (of the order of tens of MHz). Design specifications for high performance transconductor circuits include: no internal dominant parasitic poles, high linearity and low bias currents. Programmability or tunability or are also at high prize, since there are numerous applications where the transconductor cell must feature a digital control over the value of g_m [17], [18] or a precise values of transconductance is needed.
Linearity and dynamic range are two closely related parameters that measure the performance of a transconductor in terms of large signal handling capabilities; for example, the linearity of the transconductor cells that are used to build filters for wireless applications plays an important role in the overall performance of a transceiver. Harmonics that are introduced by nonlinear circuits may be seen as distortion that disrupts the process of accurate demodulation.
In what follows, this paper analyses and discusses the technique of adaptive biasing to improve the linearity of MOS transconductance elements. Adaptive biasing refers to circuits which use signal dependent bias currents, in contrast to circuits that use current sources uncorrelated in magnitude to the input signal. Although other efficient techniques have been proposed for the linearization of transconductor circuits, among which current differencing, source degeneration and class AB configuration [3], adaptively biased transconductors offer simpler basic g_m cells at greater performance in terms of linearity.

II. THE PRINCIPLE OF ADAPTIVE BIASING

A. Simple differential pair transconductor
The simplest differential voltage-to-current converter circuit is shown in Fig. 1a. It consists of one pair of source-coupled MOS devices biased – at this point – with a constant current I_{bias}. The relationship between the differential input voltage and the two gate-source voltages is described by (1); this equation also shows the relationship between the two drain currents and the total bias current.

$$\begin{cases} v_{id} = v_{gs1} - v_{gs,2} \\ i_{d1} + i_{d2} = I_{bias} \end{cases} \quad (1)$$

Using the square law of a saturated transistor, we can write the drain currents for transistors M_1 and M_2 as:

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$$i_{di} = k\left(v_{gsi} - V_{th}\right)^2, i = \overline{1,2} \qquad (2)$$

where $k=0.5\mu_n C_{ox}W/L$ defines the transconductance of an n-type MOS transistor and μ_n, C_{ox}, and W/L stand for the surface mobility, capacitance per unit area and channel geometrical parameters, respectively; v_{gs} is the gate-source voltage and V_{th} is the threshold voltage. Replacing (2) in (1), after some simple computations we obtain that the differential output current is:

$$i_{out} = i_{d1} - i_{d2} = \pm v_{id}\sqrt{2I_{bias}k}\sqrt{1 - \frac{k}{2I_{bias}}v_{id}^2} \qquad (3)$$

under the condition:

$$|v_{id}| \le \sqrt{\frac{I_{bias}}{k}} \qquad (4)$$

Eq. (4) shows that the current-voltage conversion of the simple differential MOS pair is linear only over a limited domain of the differential input voltage. Also, the nonlinear term in (3) is a square function of v_{id}; as the signal level increases the function becomes more nonlinear. Therefore, large input signals will result in harmonic distortion, thus limiting the dynamic range of the circuit. Nonlinearity is understood in this paper as the percent deviation of (3) from the ideal (and linear) conversion shown in (5) due to harmonic components:

$$i_{out} = \pm v_{id}\sqrt{2I_{bias}k} = g_m v_{id} \qquad (5)$$

where g_m defines the transconductance of the differential pair. The harmonic components are computed from the MacLaurin[2] development of (3).

B. Adaptive biasing principle
A significant increase in the linearity domain of the circuit in Fig. 1a can be obtained by employing an adaptive bias current [1], [2], [12]. Referring again to Fig. 1a, if we replace the dc bias current I_{bias} with a voltage dependent bias current as shown bellow, we obtain that the voltage-current conversion of (3) becomes of the form given in (7).

$$I_{ad} = I_{bias} + av_{id}^2 \qquad (6)$$

$$i_{out} = i_{d1} - i_{d2} = \pm v_{id}\sqrt{2I_{bias}k}\sqrt{1 - \frac{k-2a}{2I_{bias}}v_{id}^2} \qquad (7)$$

under the condition given by (8), and where a is a constant measured in $\mu A/V^2$. The previous equation results in a perfectly linear $i_{out}=f(v_{id})$ conversion, if we impose that $a=k/2$.

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[2] Taylor development around the operating point where $v_{id}=0$.
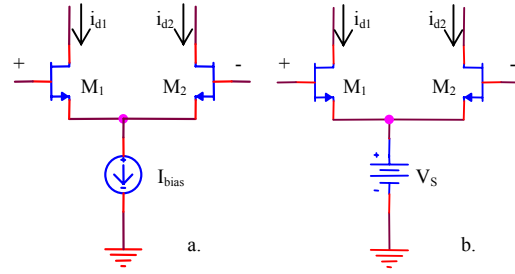

Fig. 1. Simple differential pair transconductor; current biased (a) and voltage biased (b)

$$|v_{id}| \le \sqrt{\frac{2I_{bias}}{k}} \qquad (8)$$

It must be noted from (8) that the range of the input voltage has increased by $\sqrt{2}$, in comparison to the circuit using non-adaptive current; this results in an increase of the large signal handling capability for 1% THD (Total Harmonic Distortion) of approximately 11dB [1].

C. Generation of adaptive bias current
The simplest way to generate a signal-dependent bias current proportional to the square of the input voltage signal as described by (6) is to use the square law model of MOS saturated transistors. This law was shown in (2); starting from the differential transistor pair in Fig. 1a in which we replace the bias current source at the common source node with a constant voltage source, we obtain the circuit shown in Fig. 1b. Writing the gate-source voltage as in (9) and assuming that the two transistors are perfectly matched and that the input signal is fully balanced around a common-mode voltage (V_{CM}), we derive that the sum of the two drain currents depends on the square of the input differential voltage; this relationship is shown in (10).

$$\begin{cases} v_{GS1} = V_{CM} + \dfrac{v_{id}}{2} - V_S \\ v_{GS2} = V_{CM} - \dfrac{v_{id}}{2} - V_S \end{cases} \qquad (9)$$

$$I_{sum} = I_{d1} + I_{d2} = 2K\left(V_{CM} - V_S - V_{th}\right)^2 + \frac{K}{2}v_{id}^2 \qquad (10)$$

By comparing (10) with (6), the two equations are equal provided that:

$$\begin{cases} I_{bias} = 2K\left(V_{CM} - V_S - V_{th}\right)^2 \\ a = \dfrac{K}{2} \end{cases} \qquad (11)$$

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Fig. 2. Differential cross-coupled squarer

Fig. 3. Adaptively biased transconductor using the squarer circuit
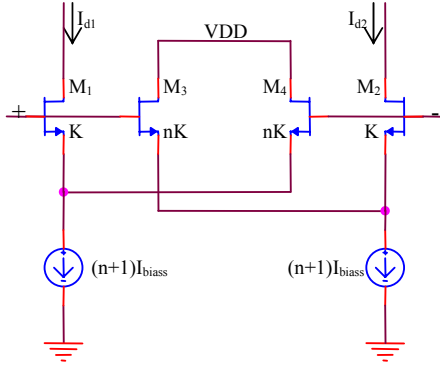
In (10) and (11), K stands for the transconductance parameter of the voltage pair in Fig. 1b. Another commonly used circuit for the generation of adaptive currents is shown in Fig. 2; it is based on two unbalanced differential pairs, with the inner pair transistors n times larger than the other transistors. In comparison to the previous circuit, this configuration increases the linearity of the quadratic equation by eliminating most of the third order harmonics of the adaptive current [1], [2], [3]. If we assume that all the transistors are operating in the saturation region, the sum of the two drain currents I_{d1} and I_{d2} is given by:

$$I_{d1} + I_{d2} = 2I_{bias} + 2K\frac{n(n-1)}{(n+1)^2}v_{id}^2 \quad (12)$$

under the condition that:

$$|v_{id}| \le \sqrt{\frac{n+1}{n}\frac{I_{bias}}{k}} \quad (13)$$

Comparing (12) to (10) we obtain that the following relationship must hold between the equation parameter a and the transconductance K of transistors M_1-M_4 from the circuit in Fig. 2:

$$a = 2K\frac{n(n-1)}{(n+1)^2} \quad (14)$$

In what follows the two methods described above are used for the generation of adaptive currents that are further applied as bias currents to differential pair transistors.

III. COMPLETE ADAPTIVELY BIASED TRANSCONDUCTOR CELLS

The complete transconductor circuit that is made of the two current and voltage-biased pairs shown in Fig. 1a and b is presented in Fig. 3; the transistor pair M_3M_4 generates the voltage dependent bias current that is applied at the common source node of the differential pair M_1M_2. Neglecting nonidealities of the square-law model of the transistors, from (11) we
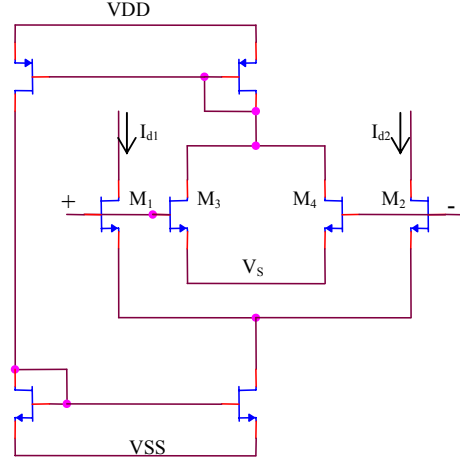
obtain that the nonlinear term in equation (7) is cancelled when M_1-M_4 are matched. However, mobility reduction in the channel of transistors M_1-M_4 determines third order distortions that reduce the linearity of the circuit.

The effect of this mobility reduction can be modeled by:

$$\mu = \frac{\mu_0}{1+\theta(v_{GS}-V_{th})} \quad (15)$$

where μ defines the surface mobility, μ_0 is the zero-field carrier mobility and θ is the carrier mobility degradation factor. Including these effects, (7) becomes:

$$i_{out} = \pm v_{id}\sqrt{2I_{bias}k}\sqrt{1-\frac{k-2a}{2I_{bias}}v_{id}^2} - \\ -\theta v_{id}\left[I_{bias}-(K-a)v_{id}^2\right] \quad (16)$$

Writing the MacLaurin series of the previous equation (only the third harmonic is shown), we obtain the transfer function:

$$i_{out} = \left(\sqrt{2I_{bias}K}-\theta I_{bias}\right)v_{id} - \\ -\left[\sqrt{\frac{K}{8I_{bias}}}(K-2a)-\theta(K-a)\right]v_{id}^3 \quad (17)$$

This equation clearly indicates a deviation from the relationship given in (7) due to mobility degradation; we obtain that mobility reduction introduces third order harmonics and also a decrease of the small signal transconductance. Imposing that the third order term cancels, we compute that the optimum value for a is:

$$a = K\left(\left(\theta-\sqrt{\frac{K}{8I_{bias}}}\right)\bigg/\left(\theta-\sqrt{\frac{K}{2I_{bias}}}\right)\right) \quad (18)$$
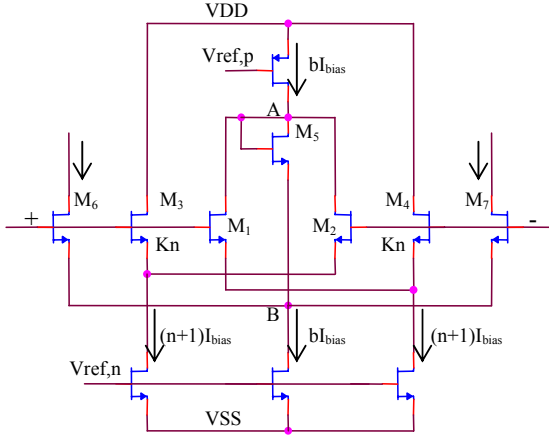
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Fig. 4. Cross coupled adaptively biased transconductor

Fig. 5. THD versus differential input voltage

Fig. 6. THD versus differential input voltage

This new value for *a* is less than K/2 (see (11)); using level 7 SPICE transistor models, the previous equation provides a value of *a=K/2.32*, for a bias current of 200μA; V_S was chosen 400mV, the supply voltage is 1.8V with the common mode voltage 1.2V and the channel geometrical parameters for transistors M1-M4 are 10μm/1μm. Fig. 5 shows the measured performance of the complete transconductor cell; the percent nonlinearity measured as total harmonic distortion is plotted versus the differential input voltage (peak-to-peak). An important improvement in linearity may be observed in Fig. 6 (curves A and B) after taking into account the effects of mobility reduction with the value of *a* estimated by (18). The above analysis assumes that a perfect quadratic bias current can be generated, according to the expression predicted by (10). While good linearity performance can be obtained with the circuit described above, its main penalty is the frequency response [2]; this is caused by the current mirrors that are used to propagate the adaptive current to the common source node of M_1M_2.

An alternative to this implementation that makes use of the squarer circuit presented in Fig. 2 is discussed further. The complete transconductor cell is shown in Fig. 4. Instead of the current mirrors we used an additional transistor and two current sources to deliver the summed squared current of M_1 and M_2 from point A to point B. According to (11), if we choose a=K/2 we obtain from (14) that n=2.155. This is the optimum value for *n* in order to eliminate the nonlinear component from the differential output current. Mobility reduction has not been taken into account in this analysis. Instead of using current mirrors, this circuit uses an additional transistor (M_5) and the two current sources that generate the current bI_{bias}. It can be shown [1] that a value of b>4n/(n+1) is needed to maintain transistor $V_{ref,p}$ conducting over the input range given by (13). Replacing (12) in (7), with n=2.155 we obtain the transfer function of the circuit described above:

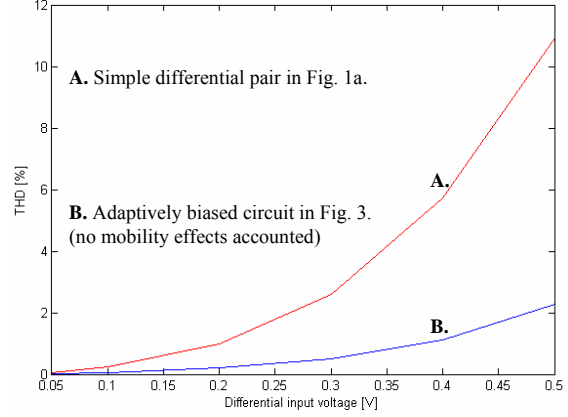$$i_{out} = i_{d6} - i_{d7} = \pm 2\sqrt{KI_{bias}} \qquad (19)$$
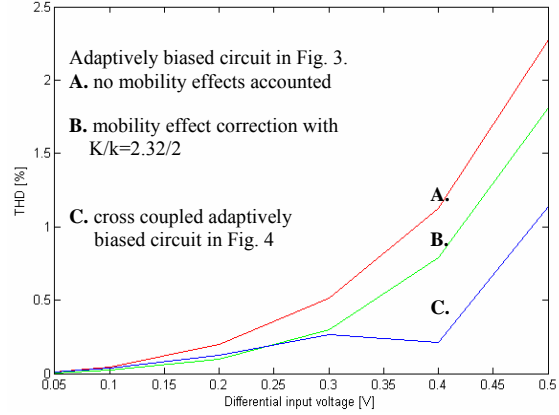
The small signal transconductance is now $\sqrt{2}$ times the value from the previous circuit, due to the DC bias current which is twice as much, as shown in (12). For *b* chosen equal to 4, the gate source voltages of transistors M_1-M_7 are equal. For this value of *b*, the circuit described in Fig. 4 was simulated and the THD versus differential input voltage is plotted in Fig. 6. Compared to the previous implementation, this circuit offers an improved voltage range over which the nonlinearity is maintained bellow 1%. Also, the frequency response is improved since no current mirrors are needed to propagate the adaptive current to the common source node of the differential pair.

IV. FILTER IMPLEMENTATION

The basic cell of the filter designed to demonstrate the high linearity of the transconductor cells discussed in the previous sections is shown in Fig. 7; the entire filter is constructed of three such g_m-C biquads in cascade, each biquad based on the g_m cell shown in Fig. 4. The adaptive biasing technique was used to linearize the transconductor cells. This filter is intended to be the IF (intermediate frequency) filter in a digital-IF wireless receiver with the IF stage at 50 MHz. A folded cascade was used as load to the basic cell in Fig. 4 as it ensures reasonably high output resistance; for an integrator constructed with one g_m
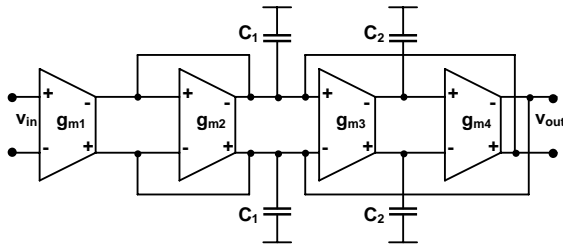
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Fig. 7. Transconductor-based differential second-order section

cell loaded with this output stage and a load capacitor of 5 pF, the measured DC gain is of approximately 34 dB, while the phase shifts from -89° at 200 kHz and -91° at 420 MHz. Q-compensation techniques to boost the DC gain were not used, although negative resistor cells (g_m-based resistors) connected at the output of each transconductor cell may be used [5]. The gain of the 6th order, 0.1 dB, Chebyshev band-pass filter was set to 0 dB, the central frequency at 50 MHz, with a bandwidth of 5 MHz (Q=10). All the simulations were performed using SPICE, with Level 7, 130nm CMOS transistors. The filter draws 2.8 mA from a 3 V power supply. The linearity of the filter was determined using the „equivalent 3rd order input Intercept Point", IP_3; the measured value of the IIP_3 is of -6.5 dBm. Compared to other results (in [17] and in [18] the measured values are of -9.2 dBm and -8 dBm, respectively), this value indicates that the adaptive bias approach offers an improvement in terms of linearity.

V.   CONCLUSIONS

The concept of adaptive biasing has been discussed in the context of increasing the linearity domain for transconductor cells. Two complete circuits have been presented and their performance in terms of linearity has been discussed and compared. The adaptive biasing method discussed was used to design a very linear CMOS filter using transconductor cells. The designed IF filter intended for use in the intermediary stage of a wireless receiver features high linearity (measured in terms of 3rd order Intercept Point), as required to implement high performance transceiver front-ends.

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