4 SWITCH Z PWM CONVERTERS IN INDUCTION MOTOR DRIVES

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4 Switch Z PWM converters in induction motor drives

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Abstract,

The thesis presents a general overview of the Z-source converters and the main formulae describing the operation of a Z-source inverter. Several topologies for connecting impedance network to three-phase four-switch inverter are analyzed. It has been shown that some of the topologies are not capable of boost compared to three-phase four-switch inverter without front end impedance network.

A V/f close loop speed control of three phase induction motor fed by a six-switch Z-source inverter from low to high motor speed. The V/f control is implemented based on Space Vector PWM voltage modulation. The Z-source inverter with controlled peak dc link voltage is used to drive the three phase induction motor.

The four-switch three-phase z-source inverter with induction machine with full load torque ventilator proportional to speed square is described analytically. The algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive is proposed. The proposed algorithm has been verified in simulation and experiments.

The improved Z-source inverter with four switches and induction motor drive obtained from the re-arrangement of the Z-Source topology elements presented in chapter three is described with the algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive

The experimental setup of the four switch three phase Z-source inverter for induction motor drive. The hardware system contains a personal computer, a digital control system with a Digital Signal Processor (DSP), a ZSI and other hardware.

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OBJECTIVES

The main objectives of the thesis are:

- To present an overview of the four-switch three-phase Z-Source converters;
- To presents a closed loop speed control of induction motor fed by Space Vector Pulse Width Modulation Six-switch Z-source inverter based on close loop Volts/Hertz control strategies;
- To describe analytically, through digital simulations and experiments the four-switch three-phase z-source inverter with induction machine with full load torque ventilator proportional to speed square;
- To propose the algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive;
- To describe analytically, through digital simulations and experiments the improved four-switch three-phase z-source inverter with induction machine with full load torque ventilator proportional to speed square;
- To propose the algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive;
- To build and test small power, configurable laboratory setup, in order to validate the theoretical results;

OUTLINE

The thesis is organized in 6 chapters:

- Chapter 1 presents a general overview of the Z-source converters and the main formulae describing the operation of a Z-source inverter. Several topologies for connecting impedance network to three-phase four-switch inverter are analyzed. It has been shown in this chapter that some of the topologies are not capable of boost compared to three-phase four-switch inverter without front end impedance network.
- In Chapter 2 is presented a V/f close loop speed control of three phase induction motor fed by a six-switch Z-source inverter from low to high motor speed. The V/f control is implemented based on Space Vector PWM voltage modulation. The Z-source inverter with controlled peak dc link voltage is used to drive the three phase induction motor. In order to verify the close loop speed control and peak dc-link voltage control strategies, simulations are carried out using PSIM software for a 1.8 kW induction motor.
- In Chapter 3 the four-switch three-phase z-source inverter with induction machine with full load torque ventilator proportional to speed square is describe analytically. The algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive is proposed. The proposed algorithm has been verified in simulation and experiments.
- In Chapter 4 the improved Z-source inverter with four switches and induction motor drive obtained from the re-arrangement of the Z-Source topology elements presented in chapter three is described with the algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive
- In Chapter 5 is presented the experimental setup of the four switch three phase Z-source inverter for induction motor drive. The hardware system contains a personal computer, a digital control system with a Digital Signal Processor (DSP), a ZSI and other hardware. The software package developed for the four switch three phase Z-source inverter for induction motor drive contains the ZSI drive project. It is developed in C++ language and assembler for the eZdsp F28335 platform and implements the proposed control algorithm for the real drive. The program is based on object-oriented technology. This code is developed for stand-alone, real-time execution.
- In Chapter 6, the overall conclusions, the main contributions are presented.

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CHAPTER 1. Z-SOURCE INVERTERS

1.1. Introduction

Due to rising energy costs and environmental aspects, high efficiency of electric drives is increasingly considered to be very important. With electric motors, this is taken into account by the definition of the premium efficiency motor programme and the definition of the efficiency class EFF1, respectively. However, the efficiency of the induction motor is very badly affected if its terminal voltage is lowered compared to its rated value. Fig. 1 shows, that under-voltage in the normal tolerance of the mains voltage (-10%) can cause additional losses, so that the efficiency is lowered by 2–3 per cent.

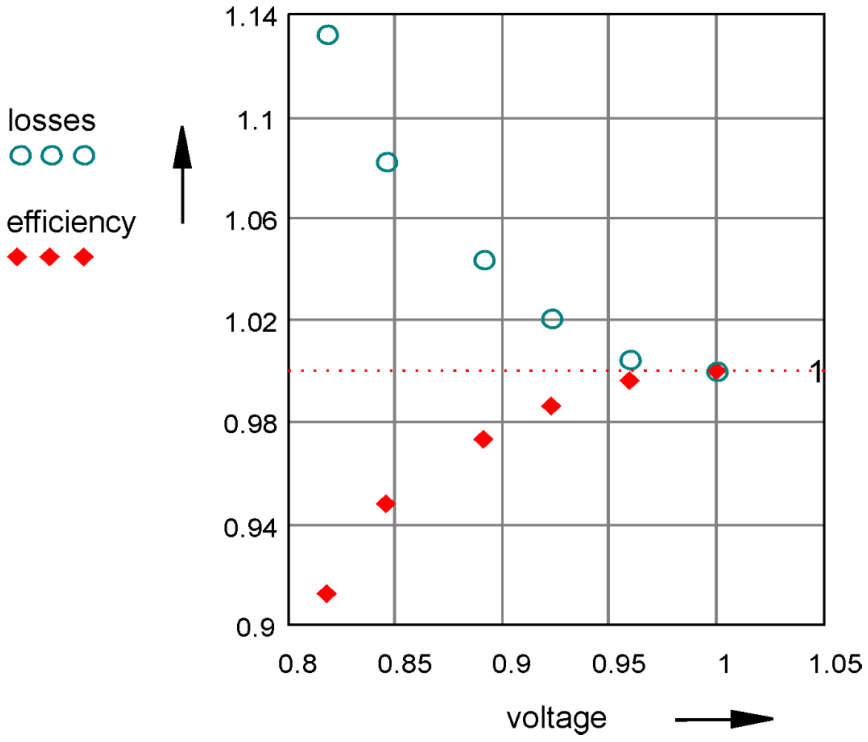

Figure 1.1 Effect of under-voltage on losses and efficiency of an 11 kW induction motor (measurements, all values are referred to their rated values)

Further reasons for low voltage on the motor terminals can be voltage drops in the converter and the voltage ripple in the DC link caused by the limited size of the DC link capacitor. The bottom line is that the operation of the motor with its

rated values is out of reach. By means of the step-up effect of the Z-source inverter, under-voltage on the terminals of the motor can be avoided regardless of its cause. In comparison to converters with a step-up converter in the DC link or a line-side inverter with step-up choke (active front end), no additional power electronic components are needed.

The passive Z-source network as a filter and self-boost network was proposed by F. Z. Peng in 2003 [1]. Up to today several studies have been carried on Z-source network inverters with fuel cells, photovoltaic panels, ultracapacitors, wind turbines or combination of these [5][7]-[10][14][18]. All these studies are related to the field of renewable energy or hybrid vehicles. In the aforementioned studies the Z-source network is in the main power flow path from the input to the output but it can be also used for voltage sag/swell compensation [19] or even for electronic loads [21].

The majority of the studied topologies are for the three-phase output voltage and just a few for single phase [9],[15]-[17]. The single-phase Z-source inverter for uninterruptable power supplies (UPS) proposed in [15] pointed out the competitive efficiency compared to traditional UPS topologies.

New topologies [4], [12], [20] were derived from the Z-source network proposed by Peng.

Details regarding the voltage control in the Z-source network based on PI and hysteresis controller can be found in [6], [11].

The main reasons the Z-source network seems to be a good choice for the intermediate circuit between the dc-link voltage and the inverter are the followings:

- It provides a greater voltage than the dc link voltage if it is necessary
- It makes the inverter immune to short circuits produced by the conduction of both transistors on the same phase leg(caused by EMI or bugs in the control software of the transistors)
- It forms a second order filter and handles the undesirable voltage sags of the dc voltage source [1]-[11].

1.2. Z-source Inverter Principle of operation

Figure 1.2 presents the electrical circuit of the Z-source network connected to a three-phase full bridge inverter. The diode D at the front end of the Z-source network makes the circuit unidirectional. The electrical energy flows from the DC voltage source to the load.

The Z-source inverter has two main operating states: one active state (also called the non-shoot through state) characterized by the modulation of the dc-link voltage V_i by the six switches T_1-T_6 to obtain a desired voltage waveform and frequency at the U, V and W output terminals and one shoot-through state characterized by the conduction of at least both transistors in one phase leg to boost the average dc-link voltage Vi. The two equivalent circuits corresponding to the two operating states of the three-phase Z-source inverter are shown in Figure 1.3.

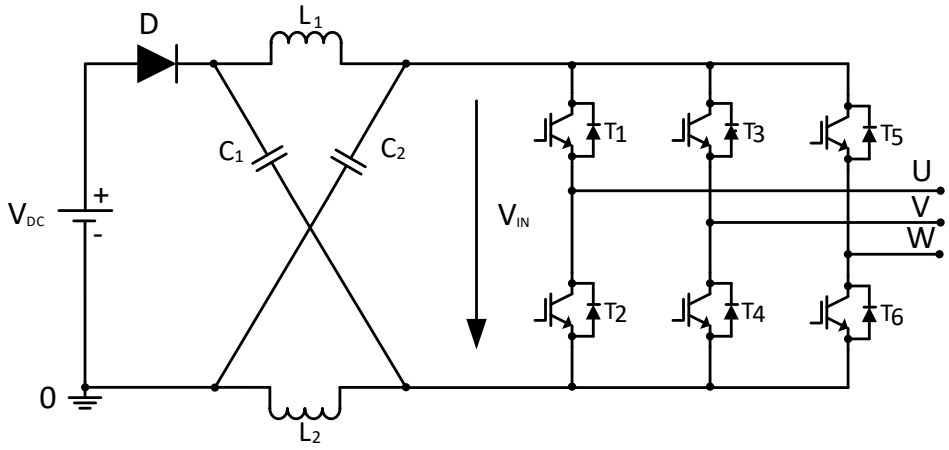

Figure 1.2 Six-switch three-phase Z-source inverter

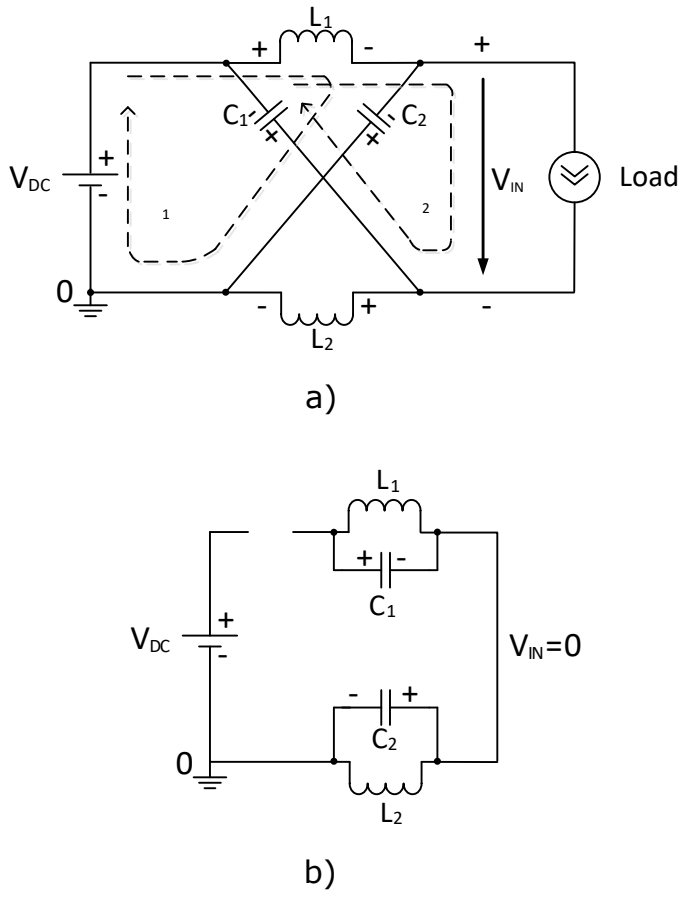

Figure 1.3 Equivalent schemes of the six-switch three-phase Z-source inverter in (a) active state (non-shoot through state) and (b) shoot-through state.

In the active state the load is symbolized by a current source. Now assume that the load is large enough and the average current of the load goes through the diode D which was substituted with a wire. In this state the desired output voltage waveform and voltage frequency can be obtained by applying one of the well-known PWM modulation techniques: unipolar pulse width modulation or bipolar pulse width modulation. During this state in steady-state operation mode the average V_{in} voltage is equal with the average voltage across capacitors C_1 and C_2.

Assuming $C_1=C_2=C$ and $L_1=L_2=L$ ($V_{C1}=V_{C2}=V_C$ and $V_{L1}=V_{L2}=V_L$) in the equivalent schemes and applying Kirchhoff's voltage law in Figure 1.3a on the voltage loops 1 and 2 (drawn with dotted line) we get:

$$V_L = V_{DC} - \overline{V_C} \tag{1.1}$$

$$V_{IN} = \overline{V_C} - V_L \tag{1.2}$$

Substituting the expression of V_L from (1.1) into (1.2) the dc-link voltage will be

$$V_{IN} = \overline{V_C} - \left(V_{DC} - \overline{V_C}\right) = 2\overline{V_C} - V_{DC} \tag{1.3}$$

In the shoot-through state in Figure 1.3b the Z-source network voltages across the inductors are equal with the voltages across the capacitors

$$V_L = \overline{V_C} \tag{1.4}$$

A line appearing over a term indicates the average value of that term, terms written with small letters and capital subscript indicate instantaneous values of that term and terms written with capital letters and capital subscript indicate that we are dealing with continuous terms.

Both terms of the six-switch three-phase Z-source inverter are present during one switching period. Now, with t_{ST} being the time duration of the shoot-through state and T_S-t_{ST} the time duration of the active state the average voltage across the inductors during one switching period T_S can be expressed as

$$\overline{V_L} = \frac{\left(T_S - t_{ST}\right)\left(V_{DC} - \overline{V_C}\right) + t_{ST}\overline{V_C}}{T_S} \tag{1.5}$$

Knowing that in steady state the average voltage across the inductors is zero

$$\overline{V_C} = 0 \tag{1.6}$$

With the duty ratio of the shoot-through state

$$D_{ST} = \frac{t_{ST}}{T_S} \tag{1.7}$$

from equation (1.5) we get the relationship between the average voltage on the capacitors $\overline{V_C}$ and the input dc voltage V_{DC} and the shoot-through time t_{ST}

$$\overline{V_C} = \frac{1 - D_{ST}}{1 - 2D_{ST}} V_{DC} = K V_{DC}$$
$$D_{ST} = \frac{\frac{\overline{V_C}}{V_{DC}} - 1}{2\frac{\overline{V_C}}{V_{DC}} - 1} \quad (1.8)$$

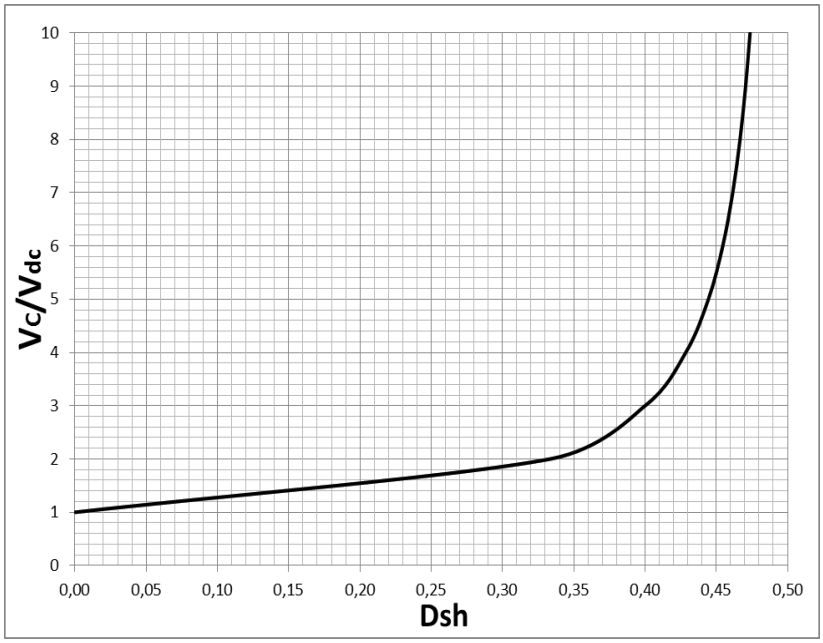

Figure 1.4 Relationship between capacitor voltages $\overline{V_C}$ /dc input V_{DC} and shoot-through time duty ratio D_{ST}

Figure 1.4 and (1.8) clearly show that at a 0.5 shoot-through duty ratio the voltage across the capacitors is infinite, theoretically. In practice measures should be taken to avoid excessive increase of the shoot-through time.

In Figure 1.3b the front-end diode D does not conduct due to the series connection of the inductors which are in parallel with the capacitors thus the diode is inversely polarized.

Eq. (1.8) shows that the average voltage across the capacitors increases as the shoot-through duty ration increases but on the other hand the average dc-link voltage $\overline{V_{IN}}$ decreases in the first few switching periods as the duty ratio increases because during the shoot-through time the dc-link voltage is zero. So the average dc-link voltage over one switching period is

$$\overline{V_{IN}} = (1 - D_{ST})\left(2\overline{V_C} - V_{DC}\right) \quad (1.9)$$

From (1.9) is obvious that the maximum voltage stress of the six-switch bridge is equal with $2\overline{V_C} - V_{DC}$. Now to reduce the current stress of the inverter

bridge the first would be to drive all the switches simultaneously in the transistor full bridge during the shoot-through time. That is why throughout the whole thesis only this shoot-through state will be considered and any shoot-through state involving only two switches in one or a number less than the total phase legs in the used transistor bridge will not be considered.

For a given shoot-through duty ratio the maximum modulation index is

$$M_{\max} = 1 - D_{ST} \tag{1.10}$$

Therefore the maximum average dc-link voltage can be expressed as

$$\overline{V_{IN}} = \left(1 - D_{ST}\right)^2 \left(2\overline{V_C} - V_{DC}\right) \tag{1.11}$$

The peak dc-link voltage across the inverter bridge can be written as (see Figure 1.3a)

$$\hat{V}_{IN} = \overline{V_C} - V_L = 2\overline{V_C} - V_{DC} \tag{1.12}$$

Substituting (1.8) into (1.12) the peak dc-link voltage can be written as

$$\hat{V}_{IN} = \frac{1}{1 - 2D_{ST}} V_{DC} = BV_{DC} \tag{1.13}$$

Where

$$B = \frac{1}{1 - 2D_{ST}} \geq 1 \text{ and } \quad 0 \leq D_{ST} \leq \frac{1}{2} \tag{1.14}$$

is the boost factor from the shoot-through zero state. Further, the output peak load voltage from the inverter can be expressed as

$$\hat{V}_{ac} = M \frac{\hat{V}_{IN}}{2} \tag{1.15}$$

where M is the modulation index. Using (1.13) and (1.15) the load peak voltage will be

$$\hat{V}_{ac} = BM \frac{\hat{V}_{DC}}{2} \tag{1.16}$$

where the product BM is the buck-boost factor. By choosing an appropriate buck-boost factor BM the output voltage can be stepped up or down.

1.3. Z-source network inrush current

At the moment of the connection of the dc source to the Z-source inverter the capacitors of the Z-source network are discharged thus a great inrush current exists, which charges the capacitors to half the input dc voltage. After that the resonance between the Z-source network capacitors and inductors take place with large current and voltage surge. At last the capacitors get charged to the input dc voltage level. The current path of the inrush current is illustrated in Fig. 1.5.

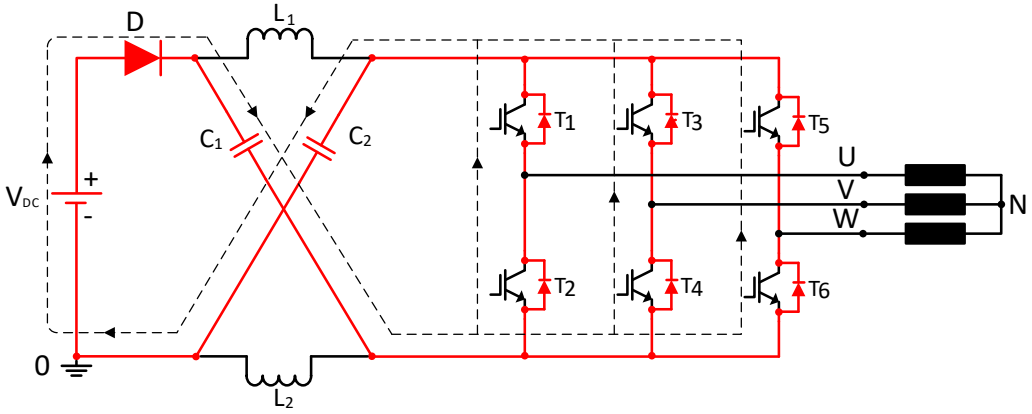

Figure 1.5 Inrush current path at start-up

The inrush current goes through the front-end diode, the Z-source network capacitors and the freewheeling diodes of the inverter bridge. A simulation was made to show the inrush current with the following circuit parameters
$L=L_1=L_2=$ 10mH; $R_L=$ 0.6Ω; $C=C_1=C_2=$2800μF; R_C=0.05Ω; V_{DC}=350V
And the resistance of each inverter leg was considered $R_{Phase\ leg}$=0.1Ω

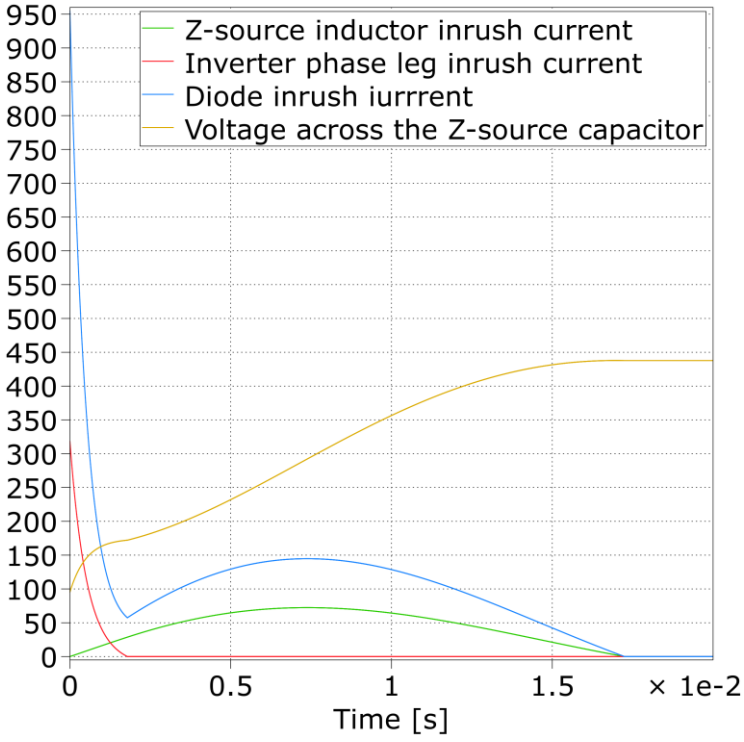

Figure 1.6 The diode, Z-source network inductor, inverter phase leg inrush currents and the voltage across the Z-source network capacitor

The inrush currents and voltages are illustrated in fig. 1.6. The inherent property of the Z-source topology is that it cannot be soft-started without additional circuitry and these high currents could destroy the front-end diode or the inverter bridge.

1.4. Z-Source Three-Phase Four-Switch Inverters

Nowadays, voltage source inverters (VSI) have been found many in the industries with different topologies depending on particular application. Generally, traditional six switch inverter can satisfy most applications such as motor drives, renewable energy conversion systems and active filters. However in some low power range applications, reduced switch count topologies is considered by both users and vendors to reduce volume and cost [22]-[27]. In order to achieve this goal, three-phase four-switch inverter was proposed by Van der Broeck as shown in Fig.1.7 [24]. In this inverter DC link is split into two voltage sources and to the middle of them one load phase is connected. From another point of view, the three-phase four-switch inverter can be used as a fault tolerant six switch inverter, when in one phase leg of six switch inverter short circuit fault has occurred.

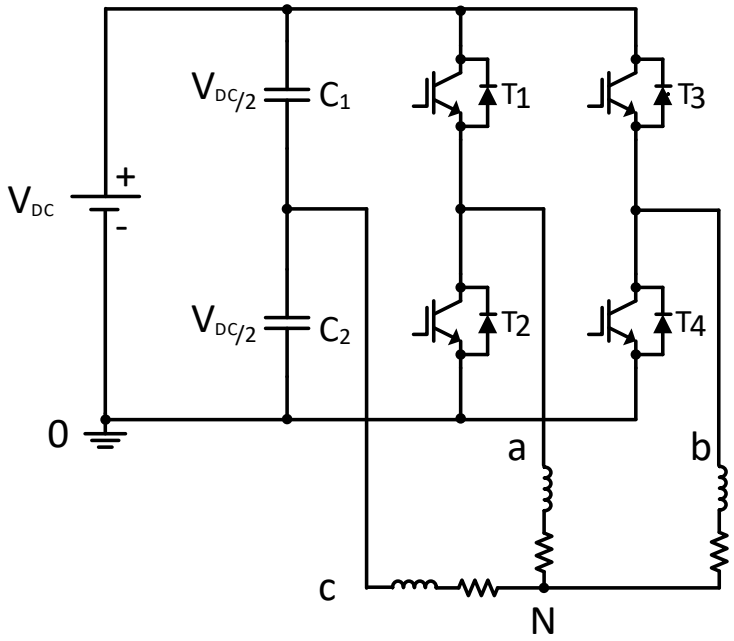

Figure 1.7 Three-phase four-switch inverter

Similar to traditional six switch inverter, three-phase four-switch inverter only performs buck operation. Compared to conventional six switch inverter, output voltage of three-phase four-switch inverter is decreased by a factor of $\sqrt{3}$. Consequently, to remedy this problem, the most straight forward solution is to insert a DC-DC boost converter between DC source and three-phase four-switch

inverter or the three-phase six switch inverter. But from cost reduction point of view, this solution is not recommended because boost converter needs active switch. Comparatively, another approach is using a z-source network [1] (Figure 1.2). Using impedance network has special advantages such as enhanced reliability of the inverter because the shoot-through caused by EMI noise can no longer damage the inverter. Moreover inrush current and harmonics is reduced due to impedance network. Also eliminating dead-time improves output voltage total harmonic distortion.

Z-source network can also be used for three-phase four-switch inverter [29, 30]. However there are some points to apply a z-source network into three-phase four-switch inverter: A) Despite conventional six switch inverter in which shoot-through is applied during inactive vectors, three-phase four-switch inverter does not have inactive vector [31] as a result there is a challenge where shoot-through times should be applied to the inverter. B) According to analysis in [28], there are different strategies for place and type of the solid-state switches of Z-source network. C) Also another challenge is the connection point of load phase C for which there is two approaches: 1) Similar to three-phase four-switch inverter, one load phase is connected to middle of DC link [29] 2) One load phase is tied to middle of impedance network capacitors [30]

1.4.1. Review of three-phase four-switch inverter Modulation

There are two switching patterns for three-phase four-switch inverter: Carrier Based Pulse Width Modulation (CBPWM) and Space Vector Modulation (SVM). CBPWM utilizes two modulating functions to generate balanced line to line voltages across the load as follows [32]:

$$V_{ref,ac} = m \cdot \sin(\omega t), \qquad V_{ref,ac} = m \cdot \sin(\omega t + \frac{\pi}{3}) \qquad (1.17)$$

Where m is modulation index and ωt is the desired fundamental angular frequency. Using defined functions in a typical switching cycle, three distinct active states are generated as shown in Figure 1.8. Therefore no null state is produced by this modulation, but an average null state totally produced by equal time durations of (0, 1) and (1, 0) or (1, 1), (0, 0) per load frequency can be generated.

The SVM is implemented using basic voltage vectors based on possible switching states (Table 1.1). It is depicted in Figure 1.9 that the three-phase four-switch inverter can only produce four basic nonzero vectors. As Figure 1.9 shows, the reference vector in the space diagram of three-phase four-switch inverter can be placed in four different sections and should be implemented using four basic nonzero vectors. This fact leads to two types of sequences for generating the resultant zero vectors [32]. For example assume that reference vector is in sector I, thus two types of sequences are as follows:

Sequence I: $V_1 - V_2 - V_3 - V_2 - V_1$ Sequence II: $V_4 - V_1 - V_2 - V_1 - V_4$

Time duration of each vector in desired sequence is presented here and will be used in next sections as follows:

Sequence I & Sector I:

$$t_{v1} = \frac{1}{2}T_S - \frac{\sqrt{3}T_S V_{ref}}{V_{DC}}\sin\left(\theta - \frac{\pi}{3}\right), t_{v2} = \frac{\sqrt{3}T_S V_{ref}}{V_{DC}}\sin(\theta)$$
$$t_{v3} = \frac{1}{2}T_S - \frac{\sqrt{3}T_S V_{ref}}{V_{DC}}\sin\left(\theta + \frac{\pi}{3}\right) \quad (1.18)$$

Sequence II & Sector I:

$$t_{v1} = \frac{\sqrt{3}T_S V_{ref}}{V_{DC}}\cos(\theta), t_{v2} = \frac{1}{2}T_S + \frac{\sqrt{3}T_S V_{ref}}{V_{DC}}\sin\left(\theta - \frac{\pi}{3}\right),$$
$$t_{v4} = \frac{1}{2}T_S - \frac{\sqrt{3}T_S V_{ref}}{V_{DC}}\sin\left(\theta + \frac{\pi}{3}\right) \quad (1.19)$$

Maximum phase output voltage (V_{max}) is the same as CBPWM and is given by:

$$V_{\max} = \frac{1}{\sqrt{3}}\frac{V_{DC}}{2} \quad (1.20)$$

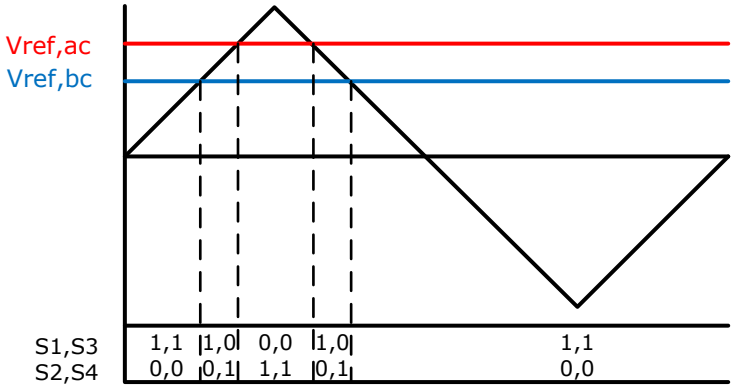

Figure 1.8 PWM modulation strategy of three-phase four-switch inverter

S1,S3	Voltage Vector	Vector Symbol
00	$\frac{1}{3}V_{DC}$	V_1
10	$\frac{1}{\sqrt{3}}jV_{DC}$	V_2
11	$-\frac{1}{3}V_{DC}$	V_3
01	$-\frac{1}{\sqrt{3}}jV_{DC}$	V_4

Table 1.1 Three-phase four-switch inverter space vectors

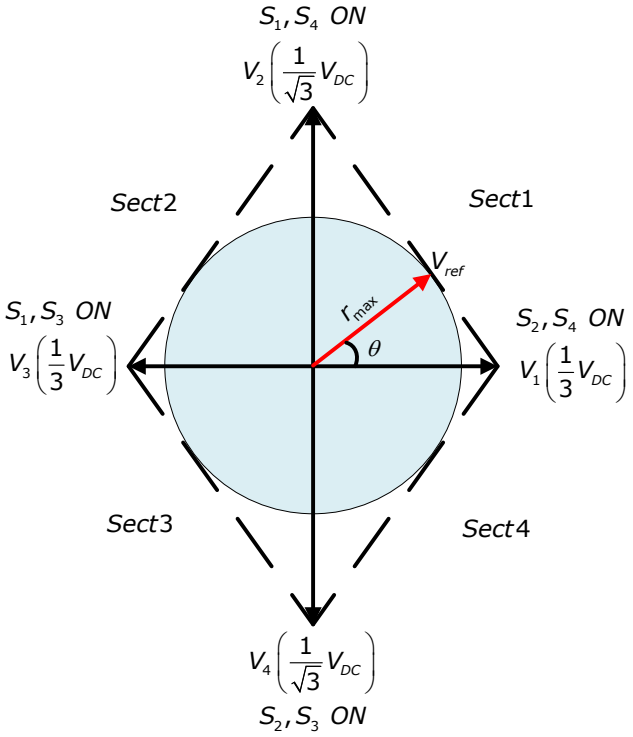

Figure 1.9 Space diagram and vectors of three-phase four-switch inverter

1.4.2. Z-Source three-phase four-switch inverter with upper diode

Figure 1.10 shows the configuration of Z-Source three-phase four-switch inverter with upper diode topology inserting diode to upper DC rail. In this topology, the shoot-through vector V_{ST} (S_1, S_2, S_3 & S_4: On) and active vector V_3 (S_1&S_3: On, S_2&S_4: Off) generate similar phase voltages $V_{an}=V_{bn}=V_{i(NST)}/2$, $V_{cn}=0$. In other words, from viewpoint of inverter, there is no difference between V_{ST} and V_3. Thus required shoot-through vector for desired boost level can be inserted in the switching pattern instead of V_3. This can easily be implemented via adding a lower constant signal V_N into the conventional CBPWM switching method of three-phase four-switch inverter to generate shoot through time interval Figure 1.11. Maximum boost occurs when:

$$V_N = m \tag{1.21}$$

And $D_{ST\,MAX}$ is given by:

$$D_{ST} = \frac{1-m}{2} \tag{1.22}$$

Consequently peak ac output voltage of inverter is given by:

$$V_{ac,\max} = \frac{2\left(\frac{\frac{m}{2}+\frac{1}{2}}{m}\right)-1}{2} mV_{DC} = \frac{V_{DC}}{2} \Rightarrow G = 1 \qquad (1.23)$$

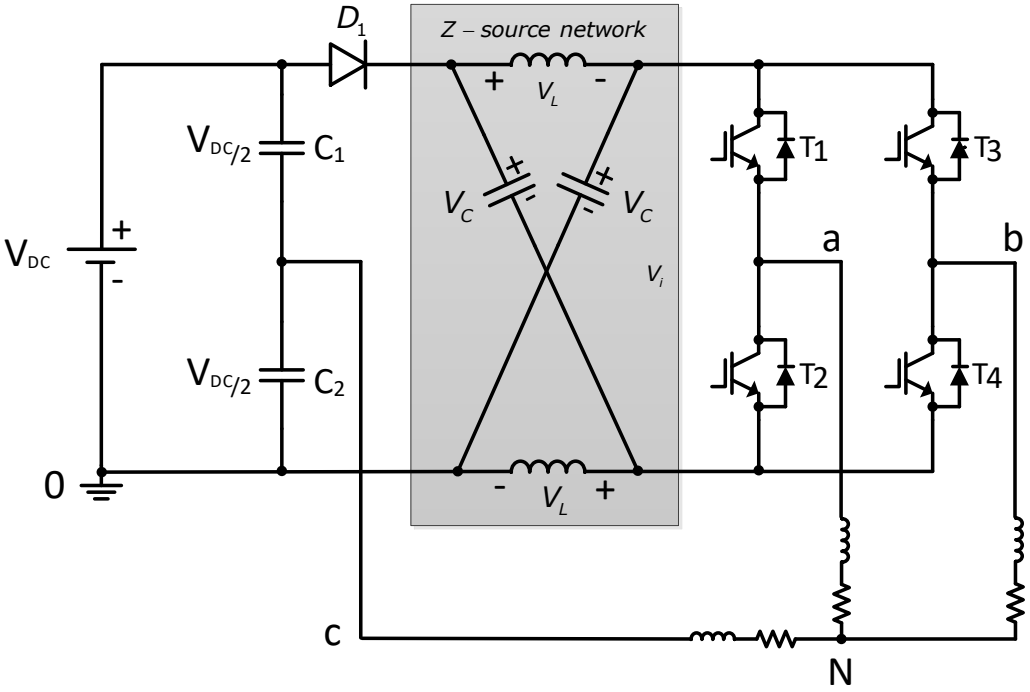

Figure 1.10 Z-source three-phase four-switch inverter with upper diode

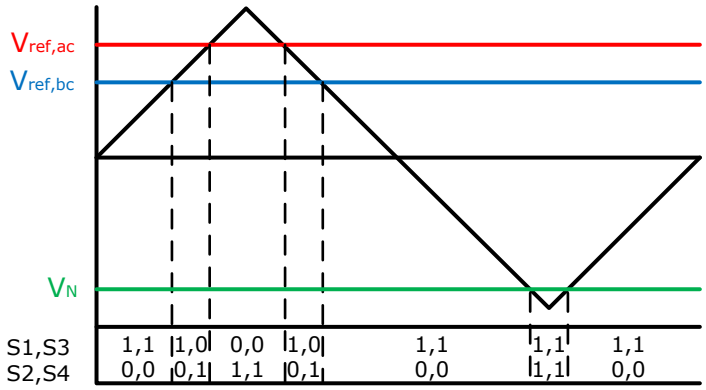

Figure 1.11 PWM strategy for Z-source three-phase four-switch inverter with upper diode

It is clear from (1.25) that this topology with CBPWM pattern is not capable of boosting the input voltage.

Another switching method is space vector modulation (SVM), space voltage vectors of Z-source three-phase four-switch inverter in a αβ plane are shown at Figure 1.12 There is a difference between three-phase four-switch inverter vectors and Z-source three-phase four-switch inverter vectors amplitude. All vectors in Z-source three-phase four-switch inverter converter are multiplied by a factor of 2K-1, where K is defined at (1.8), which is equal to boost factor B (1.13). As mentioned before, two sequences can be used for three-phase four-switch inverter. However for four-switch three-phase Z-source inverter, one of the sequences, may not be applicable, because of not presence of V_3 and consequently non-applicable shoot through. Therefore only sequence I is considered that V_3 is always available in all sectors. Now the required shoot-through vector can be used instead of V_3. For determination of maximum boost, the minimum time of V_3 should be calculated:

$$\frac{\partial V_3}{\partial t} = \frac{-\sqrt{3}T_S V_{ref}}{V_{DC}} \cos\left(\theta + \frac{\pi}{3}\right) = 0 \Rightarrow \theta = \frac{\pi}{6} \tag{1.24}$$

So the amount of t_{v3} which is available at whole of sector is equal to:

$$t_{v3} = T_S\left(\frac{1}{2} - \frac{m}{2}\right) \Rightarrow D_{ST,\max} = \frac{1}{2} - \frac{m}{2} \tag{1.25}$$

The calculated shoot-through time for SVM is just similar to CBPWM. So this topology is not capable of boosting the input voltage in both SVM and CBPWM switching method.

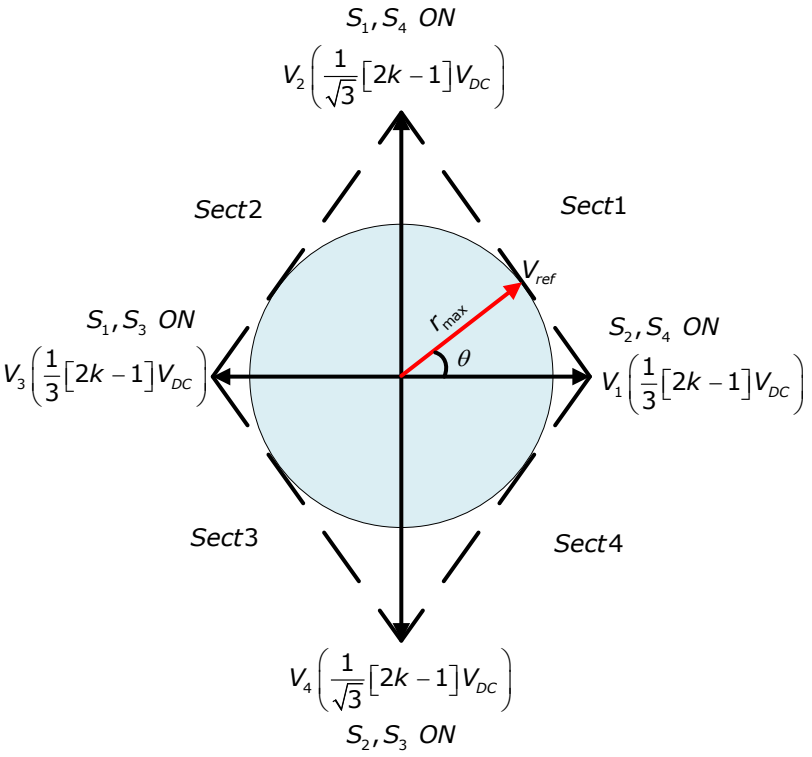

Figure 1.12 Space diagram of Z-source three-phase four-switch inverter with upper diode

1.4.3. Z-Source three-phase four-switch inverter with upper diode

Instead of inserting diode D_1 to the upper DC rail, another possible choice is to insert diode D_2 to lower DC rail as shown in Figure 1.13 [29]. In this topology, the shoot-through states should be applied when V_1 is available. There is a little modification in both CBPWM and SVM. Instead of lower constant in CBPWM method, upper constant signal V_P should be used. In SVM method, V_{ST} is aligned with V_1 vector. It can be proved that this topology similar to the Z-Source three-phase four-switch inverter with upper diode topology, Figure 1.10, is not capable of boosting output voltage in comparison to traditional three-phase four-switch inverter.

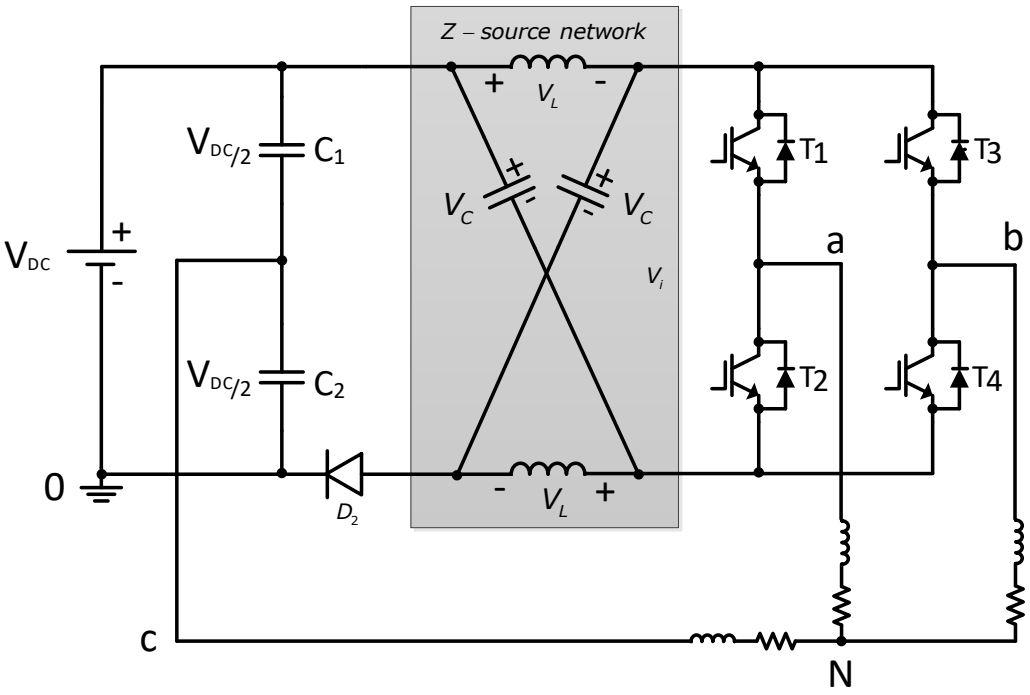

Figure 1.13 Z-source three-phase four-switch inverter with lower diode

1.4.4. Z-Source three-phase four-switch inverter with active switches

In the previous topologies, in each switching cycle, only one vector is aligned with the shoot-through vector. By adding two active switches Figure 1.14 it is possible to align two active vectors with the shoot-through vector and consequently increasing the duty of shoot-through vector. CBPWM for this topology is the combination of the topologies A and B Figure 1.15 [26]. So if $V_P = V_N$, $D_{ST,max}$ is given by:

$$D_{ST,\max} = 1 - m \Rightarrow V_{ac} = \frac{\frac{2m}{2m-1} - 1}{2} m V_{DC} \Rightarrow$$
$$V_{ac} = \frac{m}{2m-1}\frac{V_{DC}}{2}, \qquad G = \frac{m}{2m-1},\ m > 0.5 \Rightarrow G > 1 \tag{1.26}$$

Although the voltage gain of topology C can be greater than one, required two extra switches is not desirable.

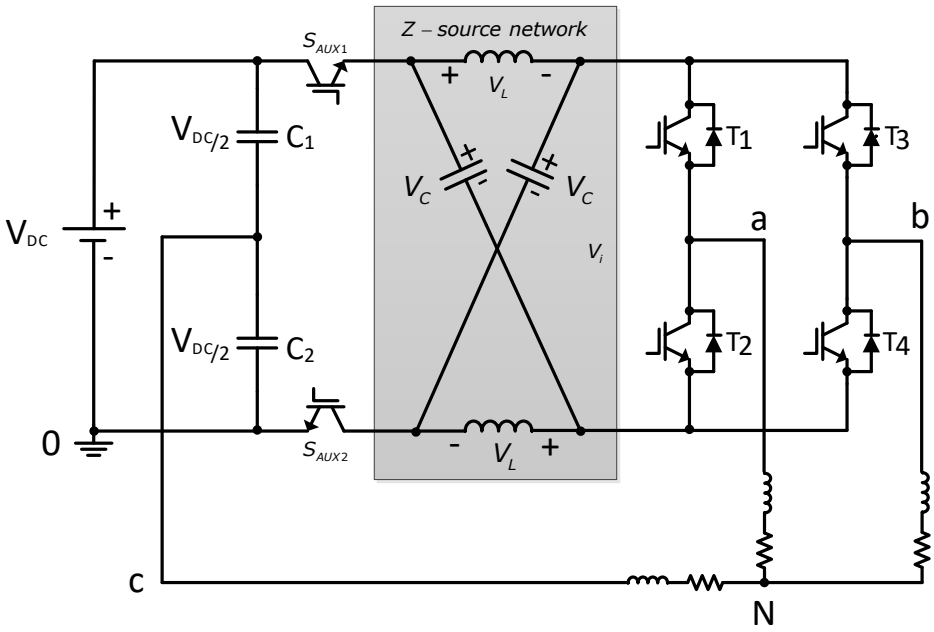

Figure 1.14 Z-source three-phase four-switch inverter with active switches

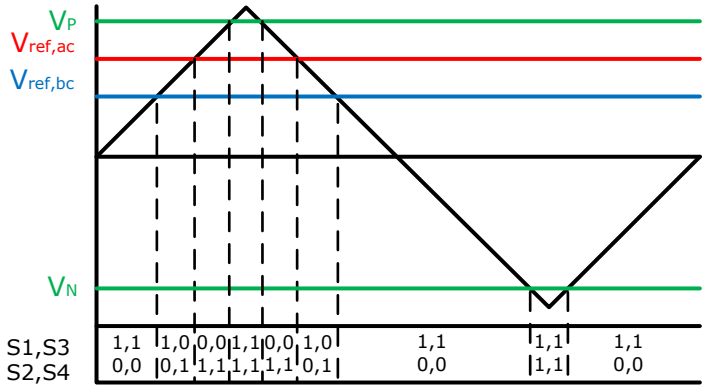

Figure 1.15 PWM Switching strategy of Z-source three-phase four-switch inverter with active switches

1.4.5. Z-Source three-phase four-switch inverter with only passive elements

To keep advantage of four-switch three-phase Z-Source inverter with active switches topology Figure 1.14, but suppress its disadvantage, topology of Figure 1.16 was presented in [28]. In this topology two active switches are replaced with four passive diodes. In the shoot-through state, D_1 and D_2 conduct and D_3 and D_4 are found to have no influence on the inverter. On the other hand, in a shoot-through state, D_1, D_2 are naturally reversely biased to disconnect DC source form inverter and D_3 and D_4 are used as clamping diode to 0V potential. Any rise in potential is compensated by D_4 and any fall in potential is compensated by D_3. So in this topology, one new inactive vector is generated. But unfortunately this state doesn't match with any active state.

Besides topology of Figure 1.16, there is another variant called, inverted Z-source three-phase four-switch inverter with only passive elements shown in Figure 1.17. Unlike the former, this topology utilizes two shunt split inductor and series capacitor. Operation principle and voltage gain is similar to the former.

CBPWM switching of Figure 1.15 whit both upper and lower constants can be used for both topologies D. Since with this switching strategy equal duration of (1, 1) and (0, 0) is applied and no volt-sec error happens, consequently maximum shoot-through duty ratio is similar to (1.28).

In case of SVM, minimum time of V_1 and V_3 available in each sector is devoted to shoot through. Consequently no volt-sec error happens, due to equal time of V_3 and V_1. The voltage gain of this topology in both CBPWM and SVM is similar to the topology with active switches.

Main problem of topologies D is the requirement of fast and high power diodes. Unfortunately high power diodes are slow and have sensible forward voltage. Consequently these features cause unbalanced output voltage and low efficiency.

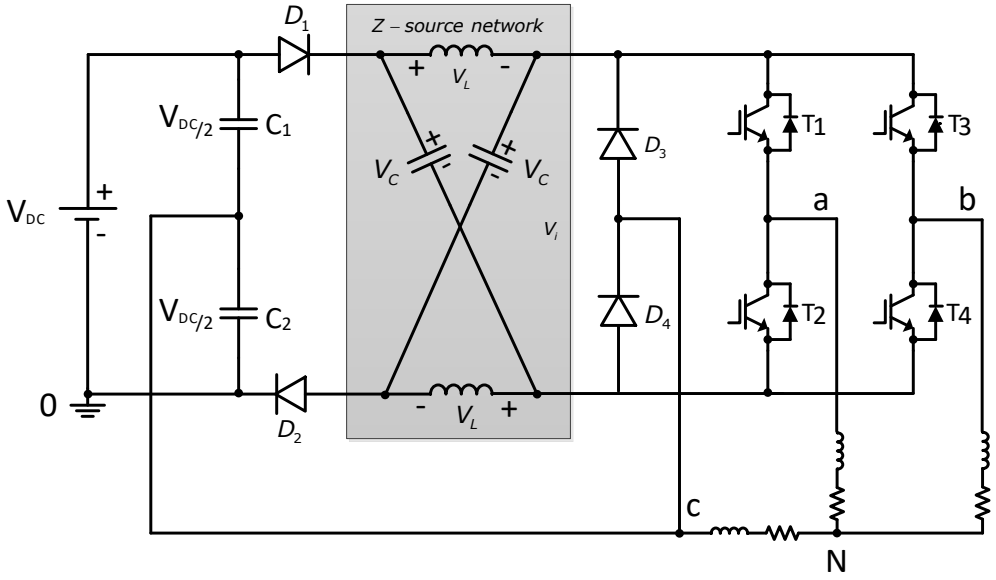

Figure 1.16 Z-source three-phase four-switch inverter with passive elements

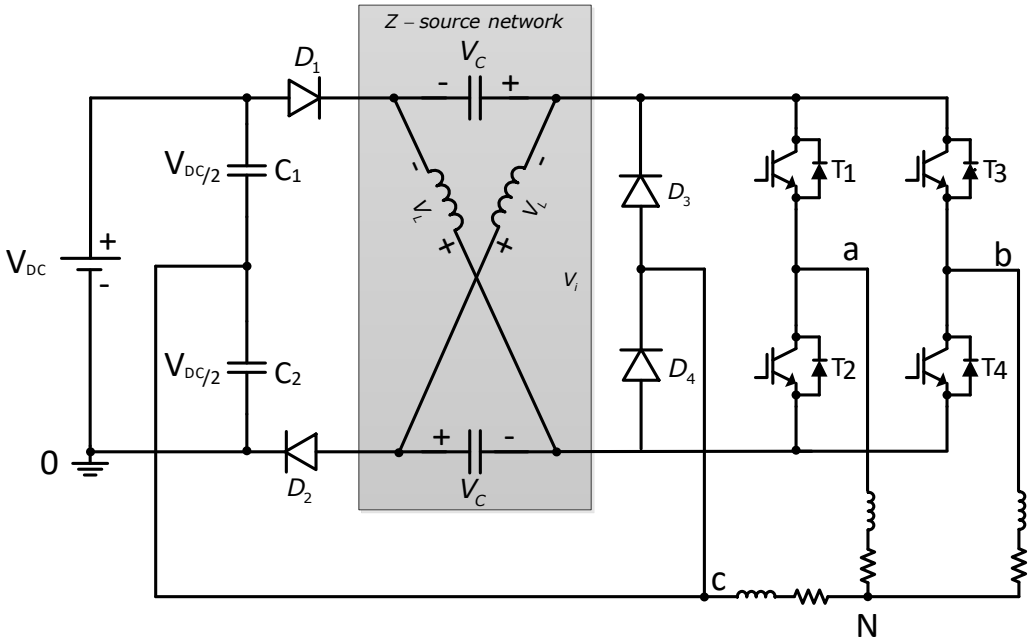

Figure 1.17 Z-source three-phase four-switch inverter source with passive elements

1.4.6. Four-switch three-phase Z-source inverter with split impedance network capacitors

In this topology one of the capacitors of impedance network is split into two and one load phase is connected to middle point Figure 1.18 [30].

Space vectors of this topology in αβ plane are depicted in Figure 1.19 (Table 1.2). It is seen that V_3 has limited output voltage regard to other active vectors. Value angle γ in Figure 1.19 is independent of K and always is equal to 60°. Consequently, maximum obtainable voltage is equal to:

$$\sin 60 = \frac{r}{\frac{k}{3}} \Rightarrow r = \frac{k}{2\sqrt{3}} \tag{1.27}$$

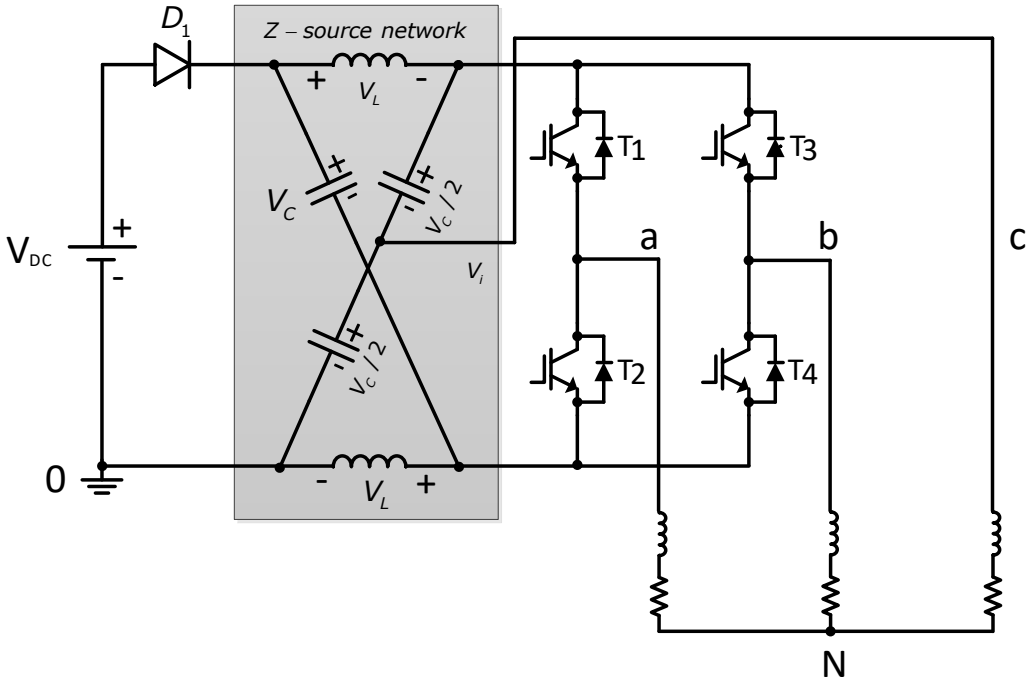

Figure 1.18 Four-switch three-phase Z-source inverter with split impedance network capacitors

From vectors depicted in Figure 1.18, it seems that only during V_3 a shoot-through vector can be inserted just like Z-Source three-phase four-switch inverter with upper diode topology. In the four-switch three-phase Z-Source inverter with upper diode topology, applying a shoot-through vector during V_1 adds a DC offset into output line voltages. However this is not the case for this topology, because by applying shoot-through vector during both V_3 and V_1, using both upper & lower constant signals, DC offset is automatically eliminated from line voltages. Consider $V_P = V_N$ at Figure 1.15, line to line voltage is given by:

$$V_{ac} = \frac{V_{DC}}{T}\left\{\left[\left(1-\frac{3}{2}K\right)\frac{T}{2}\left(1-V_{ref,ac}\right)-\frac{T_{ST}}{2}\right]+\frac{K}{2}\left[\left(1+V_{ref,ac}\right)\frac{T}{2}+\frac{T_{ST}}{2}\right]\right\}$$
$$V_{ac} = \underbrace{\frac{2k-1}{2}V_{ref,ac}}_{AC\ TERM} + \underbrace{\left(1-\frac{3}{2}K\right)\frac{1}{2}-\frac{D_{ST}}{2}\left(1-\frac{3}{2}K\right)+\frac{K}{4}+\frac{KD_{ST}}{4}}_{DC\ TERM} \quad (1.28)$$

Considering (1.11)-(1.16) and (1.28), DC term automatically omits and maximum output voltage is equaled to:

$$V_{ac} = \frac{2k-1}{2}mV_{DC}\sin(\omega t),\ D_{ST,\max} = 1-m \Rightarrow V_{ac,\max} = \frac{k}{2}V_{DC} \quad (1.29)$$

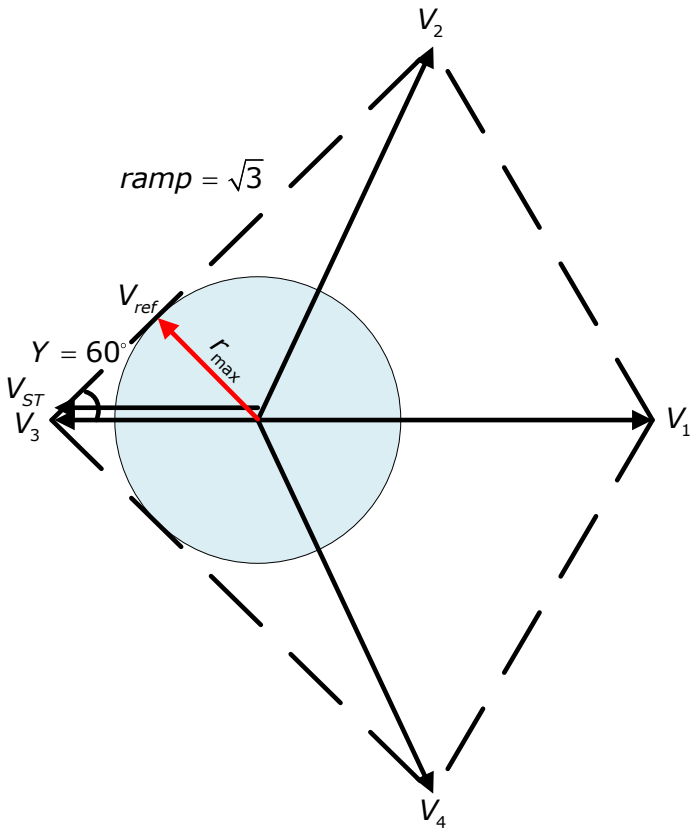

Figure 1.19 Vectors of four-switch three-phase Z-source inverter with split impedance network capacitors

S1,S3	Voltage Vector	Vector Symbol
00	$\left(k-\frac{2}{3}\right)V_{DC}$	V_1
10	$\left[\frac{1}{3}(k-1)+j\frac{1}{\sqrt{3}}(2k-1)\right]V_{DC}$	V_2
11	$-\frac{1}{3}kV_{DC}$	V_3
01	$\left[\frac{1}{3}(k-1)+j\frac{1}{\sqrt{3}}(-2k+1)\right]V_{DC}$	V_4

Table 1.2 Space vectors of Four-switch three-phase Z-source inverter with split impedance network capacitors

1.5. Hardware Implementation of the varying shoot-through pulses with the four-switch three-phase Z-source inverter active V3 voltage vector pulses

The shoot-through signals can be generated in two ways: in the control program in the signal processor or hardware by extra gates added between the signal processor which generates the gating signals for the four switches of the inverter bridge and the drives of the switches.

Usually the four PWM outputs of a digital signal processor used to control an inverter bridge are set to the complementary mode, meaning that if one transistor on a phase leg is on the other one is off. Briefly one way to generate the shoot-through signals in the control program is to override the complementary PWM outputs during the V_3 voltage time intervals which means that at least one extra timer (or extra PWM output synchronized with the 4 PWM signal generation internal unit) should be used, besides the PWM generation internal module of the signal processor, to determine the moments in time when the PWM outputs has to be overridden. Therefore the traditional space vector PWM generation algorithm has to be modified.

Without modifying the traditional space vector PWM algorithm the shoot-through signals can be generated by extra hardware. The schematic of the extra hardware needed between the DSP and the drivers of the inverter bridge is shown in Fig.1.19.

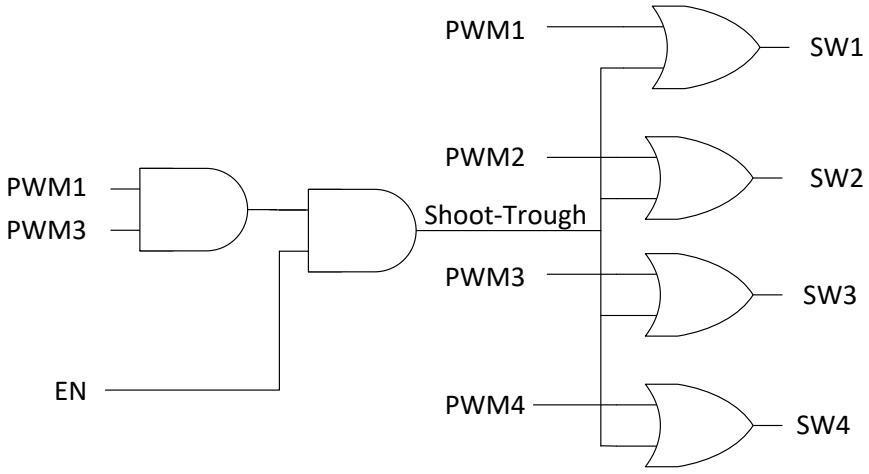

Figure 1.20 Hardware implementation of the varying shoot-through pulses with the four-switch three-phase Z-source inverter into active V3 voltage vector pulses

After the complementary initialization of the PWM module in the DSP the PWM output signals of the DSP for the lower switches PWM2 and PWM4 are on while the PWM signals for the upper switches PWM1 and PWM3 are off. This state could be set well before the SVPWM algorithm starts. Thus the enable bit has to be kept low until the SVPWM algorithm starts in order to avoid a long shoot-through state which could lead to the failure of the inverter. The AND gate for the upper switches PWM1, and PWM3 monitors the active V_3 voltages generated by turning on all the upper

switches and outputs one if all of them are on. The or gate multiplies the two outputs and if the AND gate's enable is on it sends the resulting shoot-through state signals to the output 2 input OR gates which override the PWM input ST is on.

The enable pin can be used to switch of the boost action of the control algorithm if the prescribed output voltage level is lower than the input dc voltage. Thereby the voltage stressed of the inverter bridge will be reduced.

1.6. Conclusions

In this chapter several topologies for connecting impedance network to three-phase four-switch inverter, have been investigated. Despite conventional six switch inverter, three-phase four-switch inverter does not have inactive vectors. This fact cause two challenges in four-switch three-phase Z-source inverters: 1) connection point of load phase C 2) place of input Z-source diode. In order to solve these challenges several topologies were investigated. It has been shown in this chapter that some of the topologies are not capable of boost compared to three-phase four-switch inverter without front end impedance network.

The four-switch three-phase Z-source inverter with split impedance network capacitors topology has some excellent advantages however it needs modification in structure of z-source network. This modification will not be desirable, while in the most cases, z-source network is modular and modification of it is tough and also these modifications disturb the symmetrical topology and can lead some problems such as EMI and EMC effects. In addition, four-switch three-phase Z-source inverter with split impedance network capacitors topology removes split dc link, while in AC/DC/AC configurations is selected to reduce ripple and fault tolerant capability.

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CHAPTER 2 SIX SWITCH THREE-PHASE Z-SOURCE INVERTER

2.1. Introduction

The Z-source inverter (ZSI) was introduced in order to overcome limitations of conventional voltage-source (V-source) and current-source (I-source) converters [1]. The ZSI provides special features which cannot be noticed in the traditional inverter; they are as follows:

- The ZSI is a self-boost converter for dc-to-ac power con-version and a desired ac voltage can be obtained, which is greater than the source line voltages.
- A short circuit across any phase leg is allowed, so that the dead time is not a necessary attribute.
- Second-order filters are provided, which are more effective to suppress voltage ripples than the capacitor used in the traditional PWM inverter.
- The in-rush current and harmonics in the current can be reduced due to the inductor.
- Ride-through during voltage sags is provided without any additional energy storage elements.

The general Z-source converter structure, which consists of inductors L1, L2 and C1, C2 capacitors connected in X shape connects the inverter to the dc voltage source, which may be a battery, a diode rectifier, or a fuel cell.

The Z-source network is utilized to boost the DC link voltage to a desired level which could be equal or greater than the DC voltage. A voltage boost is necessary when a voltage-sag occurs in the DC side or the load needs a higher voltage level than the voltage level provided by the DC side.

A standard three-phase voltage-source inverter has six active states and two zero states. A zero state is produced when the three upper or lower switches are turned on at the same time, shorting the output terminals. During these zero state time intervals the so called shoot-through times are introduced when both transistors from one, two or all three phase legs are conducting. In this way two things are realized: the DC link voltage is boosted and the phase-to-phase voltages prescribed by the PWM control technique are not affected by these shoot-through intervals, because during the zero states the voltage prescribed by the inverter to the load is zero [1] [2].

The Z-source inverter intentionally utilizes the shoot through zero states to boost dc voltage and to produce an output voltage greater than the original dc voltage. At the same time, the Z-source structure enhances the reliability of the inverter greatly because the shoot-through states, which might cause by EMI noise, can no longer destroy the inverter.[12]-[21]

The algorithm to control linearly the capacitor voltage is suggested in [9]-[11] in order to improve the transient response for dc boost control of the ZSI. The peak value of the ac output voltage is used to control exactly the ac output voltage to its

desired level and a modified space vector pulse-width modulation scheme is applied to control the shoot-through time for boosting dc voltage.

A detailed analysis on Z-source inverter modulation, showing how various conventional PWM strategies for controlling a conventional VSI can be modified to switch a voltage-type -source inverter either continuously or discontinuously. Through the proper placement of shoot-through states, -source inverter modulation can be made to reproduce the desired performance features of various reported conventional PWM strategies [12],[13].

Induction motors have many advantages compared to DC machines and synchronous machines in many aspects, such as size, efficiency, cost, life span and maintainability. Low cost and easy manufacturing have made the induction machine a good choice for electric drives.

The traditional adjustable speed drives (ASD) system is based on the voltage source inverter (VSI), which consists of a diode rectifier front end, dc link capacitor, and an inverter bridge. It suffers from common limitations and problems, such as: the obtainable output is limited below the input line voltage, the voltage sags can interrupt an ASD system and shut down critical loads and processes and the performance and reliability are compromised by the VSI structure (miss-gating, dead time, common mode voltage)[3][4].

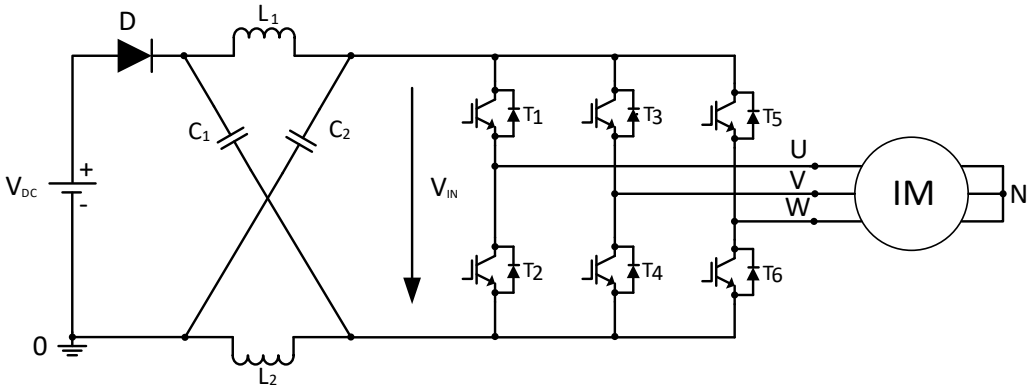

Figure 2.1 Six-switch z-source three-phase inverter with induction machine

The volt per hertz (V/f) induction motor drives with inverters are widely used in a number of several industrial applications promising not only energy saving but also improvement in productivity and quality. The low cost applications usually adopt V/f scalar control. Variable speed pumps, fans and appliances are the examples. Furthermore, these applications usually do not require zero or very low speed operation. The main advantages of V/f control is its simplicity and for this reason it has been traditionally implemented using low cost microcontrollers.

This chapter presents a V/f close loop speed control of three phase induction motor fed by Z-source inverter from low to high motor speed. The V/f control is implemented based on Space Vector PWM voltage modulation. The Z-source inverter with controlled peak dc link voltage is used to drive the three phase induction motor.

2.2. Closed loop V/f controlled induction motor drive

A simplified diagram of the V/f controlled induction motor is shown in Figure 2.2. The closed loop control by slip regulation of combined inverter & induction machine improves the dynamic performance. The speed loop error generates the slip command through a proportional integral (PI) controller and limiter. The slip is added to the speed feedback or observer signal to generate the frequency command. Thus frequency command generates the voltage command through a volts/hertz generator [5]. Volts/Hertz closed loop speed control simulation model is shown in Figure 2.3.

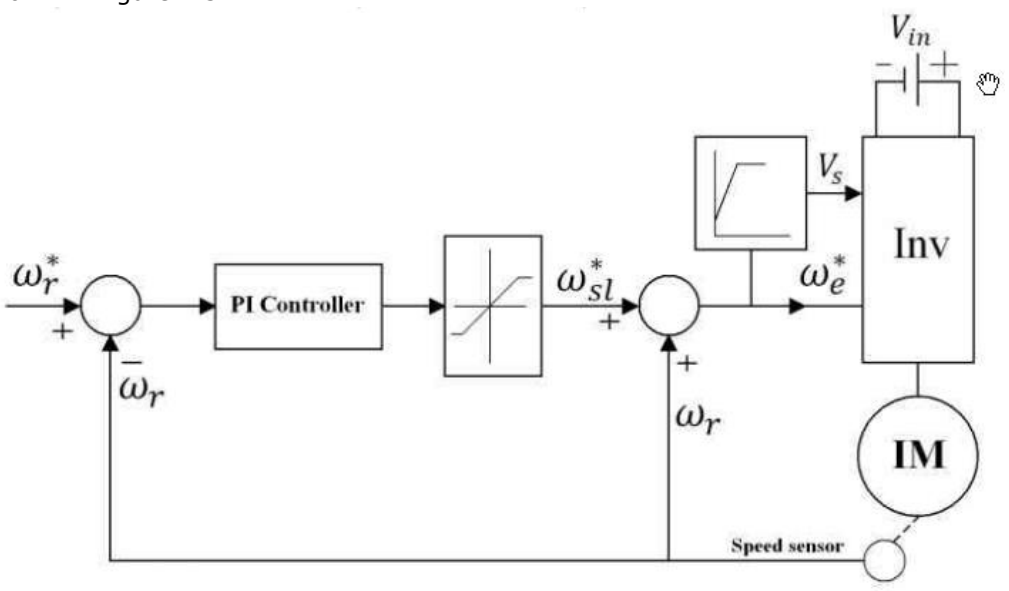

Figure 2.2 General Volts/Hertz based closed loop speed control scheme of induction motor.

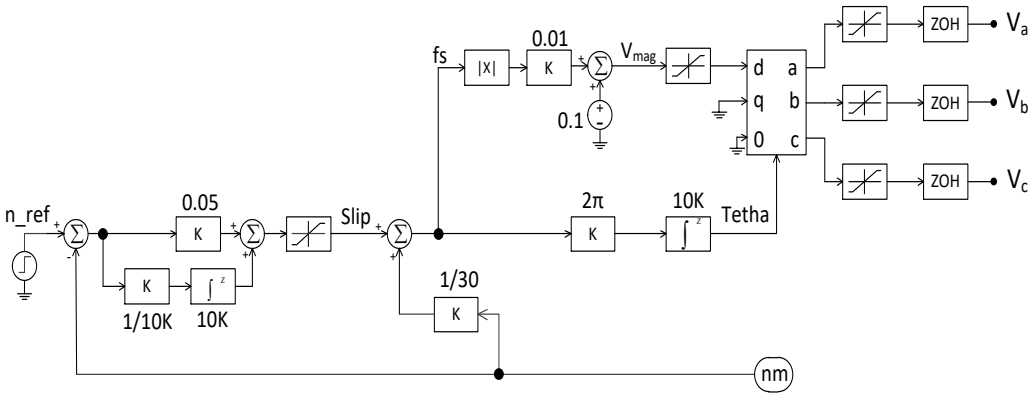

Figure 2.3 Volts/Hertz closed loop speed control

3.3 Space vector pulse width modulation

SVPWM method is an advanced, computation-intensive PWM method and is arguably the best among all the PWM techniques for variable speed applications [6]. Because of its superior performance characteristics, it has found widespread applications in recent years. All existing PWM methods have been implementation on a half bridge of a three phase bridge inverter. If the load neutral is connected to the center tap of the dc supply, all three bridges operate independently, giving satisfactory PWM performance.

With the machine load, the load neutral is normally isolated, which causes interaction among the phases. This interaction was not considered in other PWM techniques. SVPWM considers this interaction of the phases and optimizes the harmonic content of the three phase isolated neutral load. There are not separate modulation signals in each of the three phases in SVPWM techniques. Instead, a voltage vector is processed as a whole. Therefore, it is very suitable to control the shoot-through time Figure 4, the discontinuous inner circle shows the trajectory of voltage space vectors (V) for the traditional three-phase two-level PWM inverters.

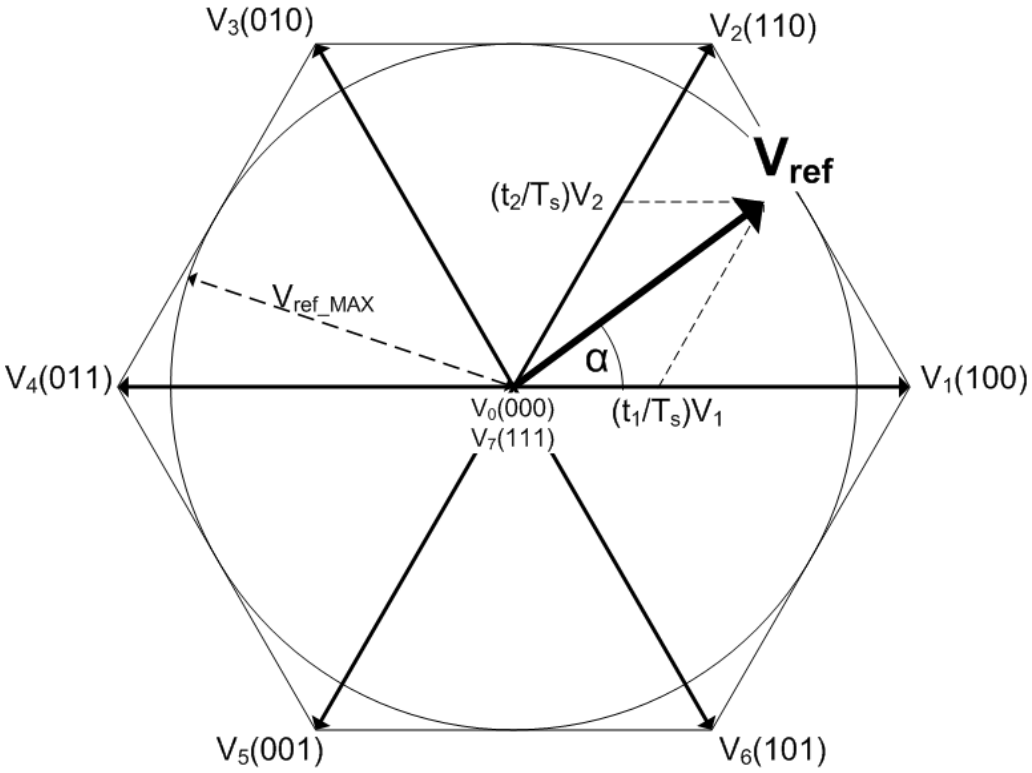

Figure 2.4 Voltage space vectors with shoot through states for Z source inverter.

The output voltage of the inverter is determined by the different voltages between each inverter arm and the time duration in which the different voltages are maintained. Eight voltage vectors $\vec{V}_0, \vec{V}_1, \vec{V}_2, \vec{V}_3, \vec{V}_4, \vec{V}_5, \vec{V}_6, \vec{V}_7$ corresponding to the witching states $\vec{S}_0 = [000]$, $\vec{S}_1 = [100]$, $\vec{S}_2 = [110]$, $\vec{S}_3 = [010]$, $\vec{S}_4 = [011]$,

$\vec{S}_5 = [001]$, $\vec{S}_5 = [101]$, $\vec{S}_7 = [111]$ respectively are available $\vec{V}_1, \vec{V}_2, \vec{V}_3, \vec{V}_4, \vec{V}_5, \vec{V}_6$ are called active vectors $\vec{V}_0$ and $\vec{V}_7$ are the traditional zero vectors. The length of the active vectors is unity and length of the zero vectors is zero. In one sampling interval T_S, the output voltage vector of the traditional inverter $\vec{V}$ is split into the two nearest adjacent voltage vectors. These two nearest active vectors and the traditional zero vectors are used to synthesize the output voltage vector. $\vec{V}_n$ and $\vec{V}_{n+1}$ (Where n = 0……6) vectors are applied at times T_1 and T_2 respectively, and zero vectors are applied at T_Z times.

The trajectory of voltage vector $\vec{V}$ should be circular, while maintaining pure sinusoidal output line-to-line voltages. The boundary of the linear modulation and over modulation is the hexagon. The time duration for the active vectors are kept constant throughout the operation sub-cycle and the zero vector time is conveniently placed depending upon the angle of the space vector (T_Z is decreased when the voltage vector is increased).

The maximum output line-to-line voltage is obtained when the voltage vector trajectory becomes the inscribed circle of the hexagon and $|\vec{V}|$ becomes $\sqrt{3}/2\ V_{DC}$.

This limitation of the length of the active vector affects the smooth operation of loads like motor drives where overdrive is desired [7]. By self-boosting, the output voltage the Z converter can overcome voltage sags or provide wide (larger) speed, torque range in exterior cycle in Figure 4. Space Vector Pulse Width Modulation simulation model is shown in Figure 2.5.

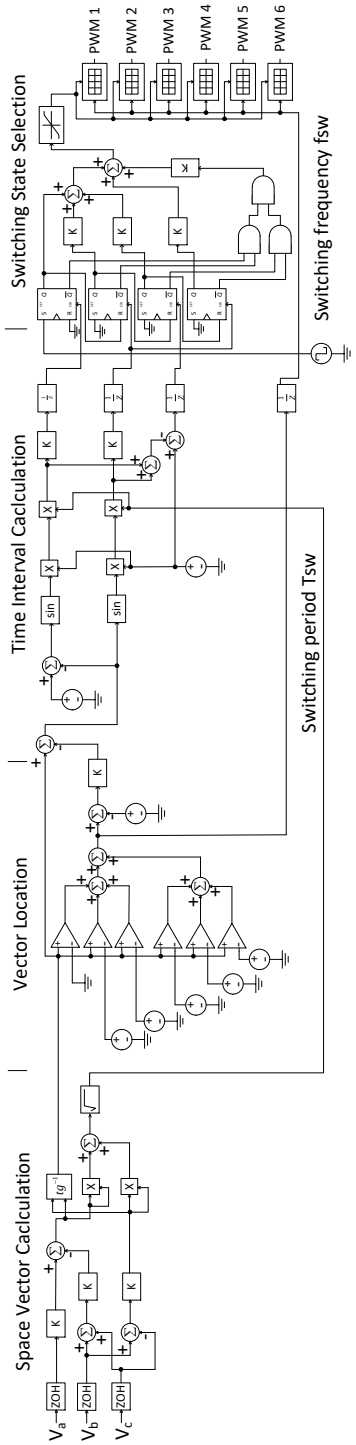

Figure 2.5 Space Vector Pulse Width Modulation

2.4 The peak dc link voltage control

One PI controller was used to control the shoot-through time interval from the Z-source capacitor voltage error. The PI controller can be seen in Figure 6. The input is the error between the prescribed C capacitor voltage and the measured capacitor voltage and the output is the shoot-through interval.

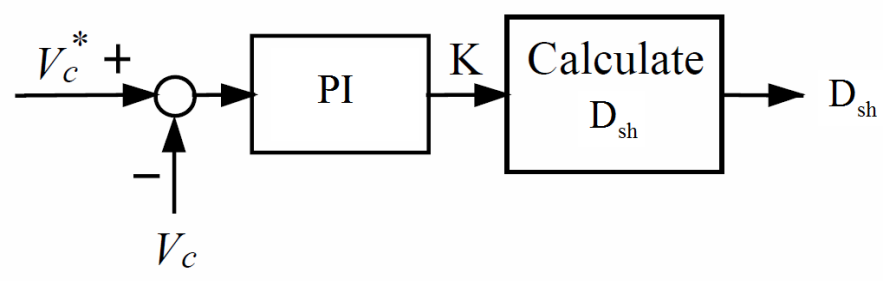

Figure 2.6 PI controller for the Z-source capacitor voltage

Without modifying the traditional space vector PWM algorithm the shoot-trough signals can be generated by extra hardware thanks to the characteristics of the two control algorithms. The schematic of the extra hardware needed between the SVM and the drivers of the inverter bridge is shown in Figure 7. The triple input AND gate for the upper switches PWM1, PWM3 and PWM5 monitors the zero voltage generated by turning on all the upper switches and outputs one if all of them are on while the other three input AND gate does the same thing for the lower switches of the inverter bridge. The two gates together cover the two zero voltage states. The OR gates multiply the two outputs and, if the two input AND gates enable is on, it sends the resulting shoot-through state signal to the output two inputs OR gates, which override the PWM input if shoot-through is on.

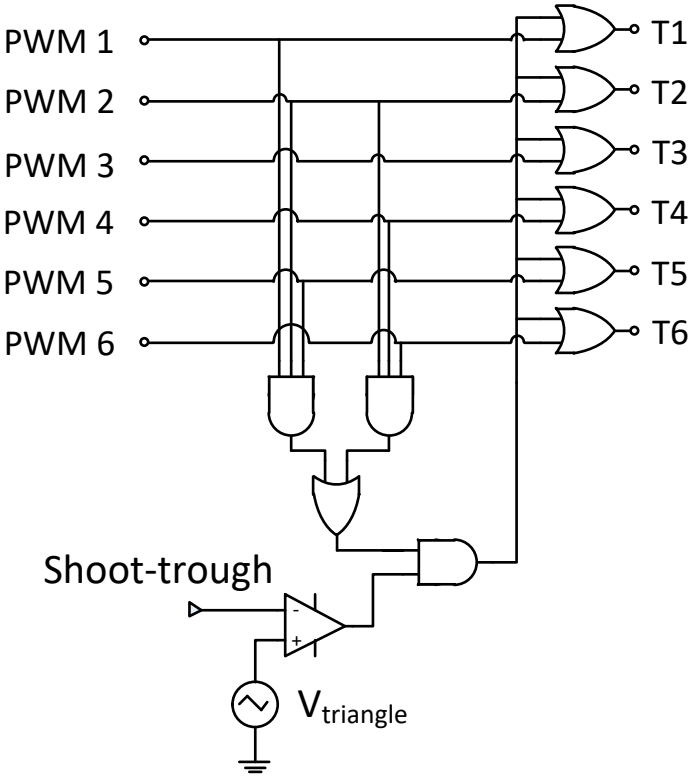

Figure 2.7 Hardware variable shoot-through generation

The standard mode to operation of an ASD is to maintain the DC-link voltage at a constant value and adjust the modulation index M to control the output voltage. In order to obtain the rated 400V rms output voltage, the DC-link voltage is boosted to somewhat higher level, V_{dc}=790V [8].

In this closed loop Z-source inverter ASD system, in order to make the inverter operate with higher modulation index, the dc link voltage is controlled to be constant at VC 790V by the close loop shoot-through control. The modulation index is calculated either by the V/f control with variable operating frequency.

2.5. Simulation Results

In order to verify the close loop speed control and peak dc-link voltage control strategies, simulations are carried out using PSIM software for a 1.8 kW induction motor using parameters in Table 2.1 and for Z-network in Table 2.2. In the simulation model, the modulation index is calculated from the reference voltage of V/f method. In Figure 2.8 the closed loop speed control of three phase induction motor fed by Space Vector PWM Z-source inverter scheme is shown.

Parameter	Value
Output power	1.8kW
RMS line voltage	400 V
Input frequency	50Hz
No. of poles	4
Stator resistance, R_s	2.56 Ω
Rotor resistance, R_r	1.97 Ω
Stator leakage inductance, L_{ls}	0.01472 Ω
Rotor leakage inductance, L_{lr}	0.01124 Ω
Mutual inductance, L_m	0.2815 Ω
Moment of inertia, J	0.012024 $kg{\cdot}m^2$
Rated dc input voltage	500Vdc

Table 2.3 1.8 kW induction motor parameters

Z-SOURCE NETWORK PARAMETERS

Parameter	Value
Capacitors	750μF
Inductors	450μH

Table 2.4 Z-source network parameters

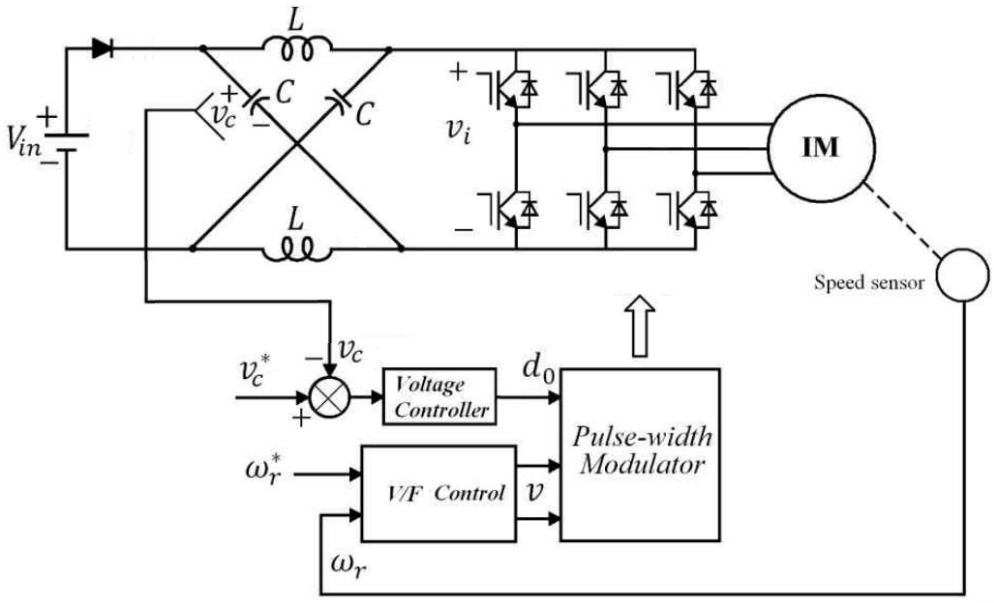

Figure 2.8 Closed loop speed control of three phase induction motor fed by Space Vector PWM Z-source inverter

Figures 2.9 – 2.16 show the simulation results for V/f control of a 1.8 kW induction motor fed by a ZSI. Figure 2.9 expose the motor speed, torque and stator current during motor starting from zero to rated speed with full load torque is proportional to speed square, Figure 2.10 shows the steady state motor filtered voltage and phase current, Figure 2.11 illustrates the reference capacitor voltage, the capacitor voltage, the dc input voltage, the modulation index and actual inductor current.
Figure 2.12 shows the system response during 50% step up load disturbance and Figure 2.13 shows the system response during 50% step down in load disturbance. Also Figure 2.14 illustrates system response for 50% step down in input voltage (V_{dc}) at high load torque (12Nm). It is evident that in this severe case (f_1=50Hz) the machine, for 50% step down in input voltage, is not any more capable to reach the reference speed, but the response is still rather stable. Figure 2.15 shows the system response for 50% step down in input voltage (V_{dc}) with large load at 75Hz; similar behavior with Figure 2.14 is observed in this even more demanding situation. Finally Figure 2.16 shows operation at 5 Hz motor operation frequency. The simulation results in figures 2.9-2.16 can be interpreted as follows:

The machine accelerates to 50 Hz with speed squared proportional load torque in 0.7, seconds with moderately large current peaks while the capacitor voltage is boosted at 790 V and stays there finally (Fig 2.9-2.11); also the inductor current (Fig. 2.11) which is divided between the three inverter legs does not warrant oversizing of the standard inverter.

The machine handles ± 50% step load rather well, with some damped oscillations in capacitor voltage and inductor current (Fig 2.12 and 2.13).

A 50% reduction (sag) in dc input voltage is handled smoothly as the steady capacitor voltage and speed waveforms show (Fig. 2.14), but this sag becomes a problem at 75 Hz motor operating when the motor is overloaded (Fig.15).

Motor operation at 5 Hz, even with the high (constant capacitor voltage reference: 790V) is still acceptable (Fig. 2.16).

The gradual decrease of capacitor reference voltage V_C* with motor frequency should faster improve drive performance. Also faster capacitor voltage control is required.

The voltage self-boost of Z converters can extend the torque/speed range of induction machine drives while maintaining a voltage ceiling reserve for zero voltages timing in all conditions.

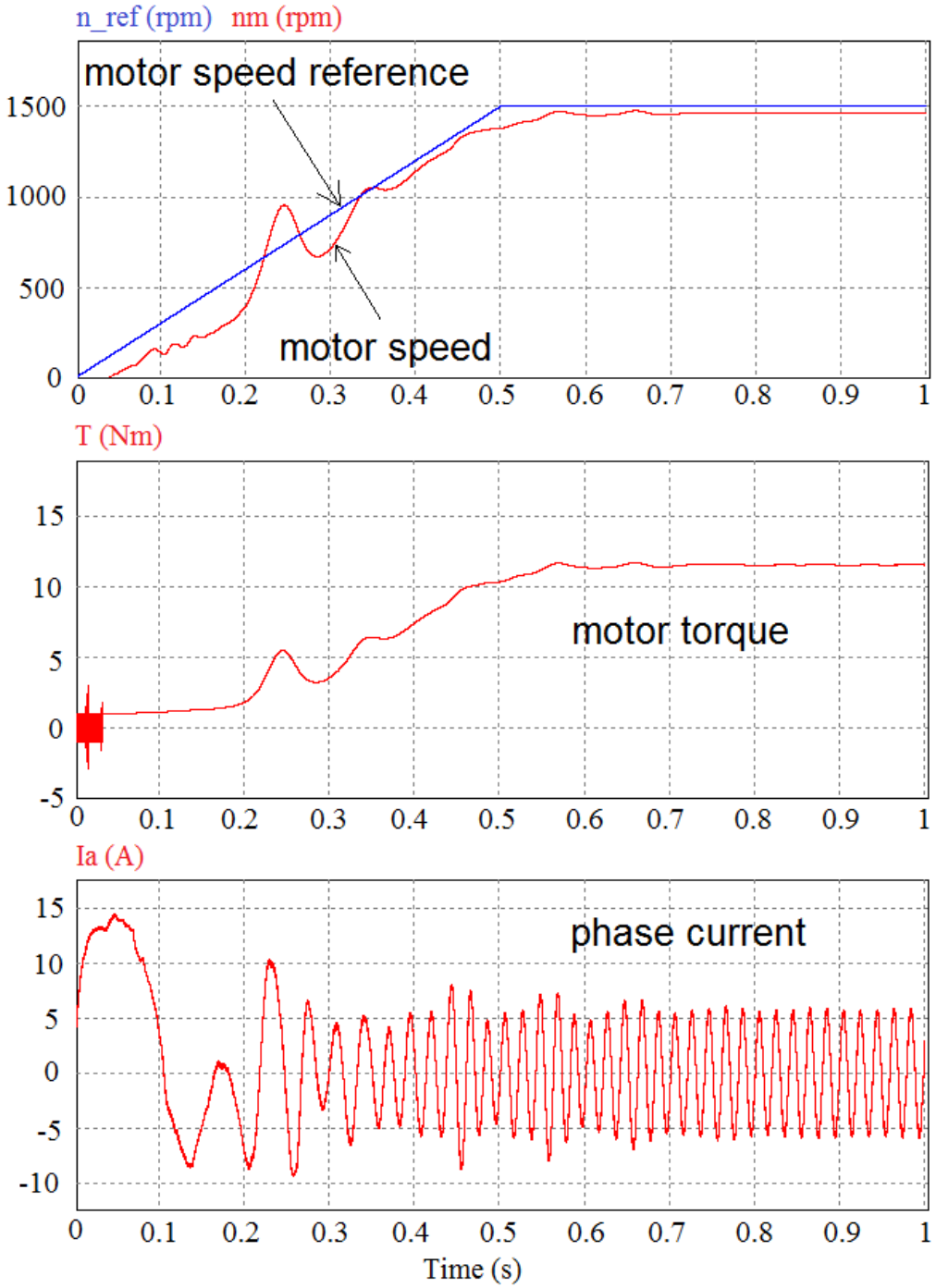

Figure 2.9 Motor speed, torque and stator current during motor starting from zero to rated speed with full ventilator (proportional to speed square) load

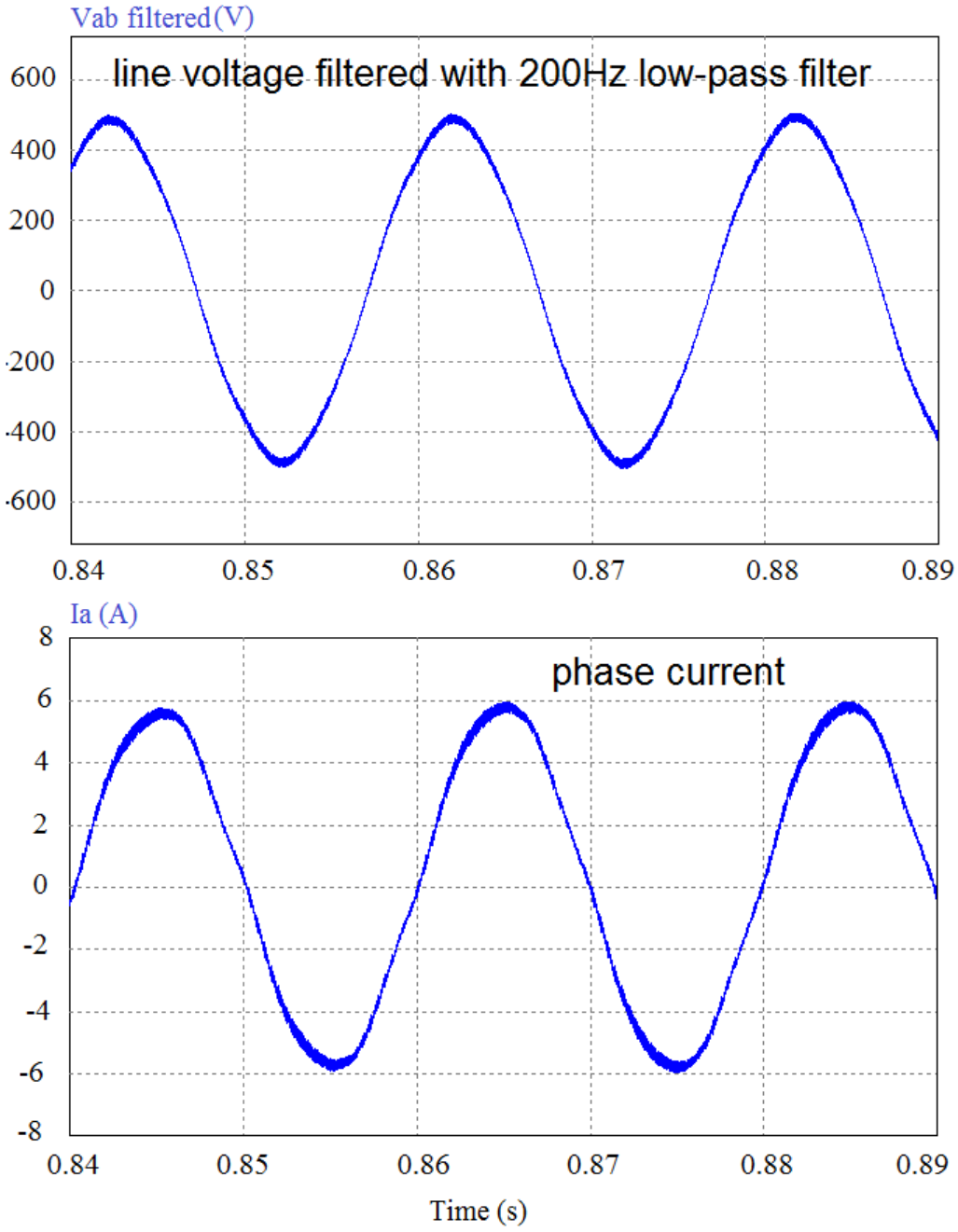

Figure 2.10 The steady state motor voltage filtered with 200Hz low pass filter and phase current

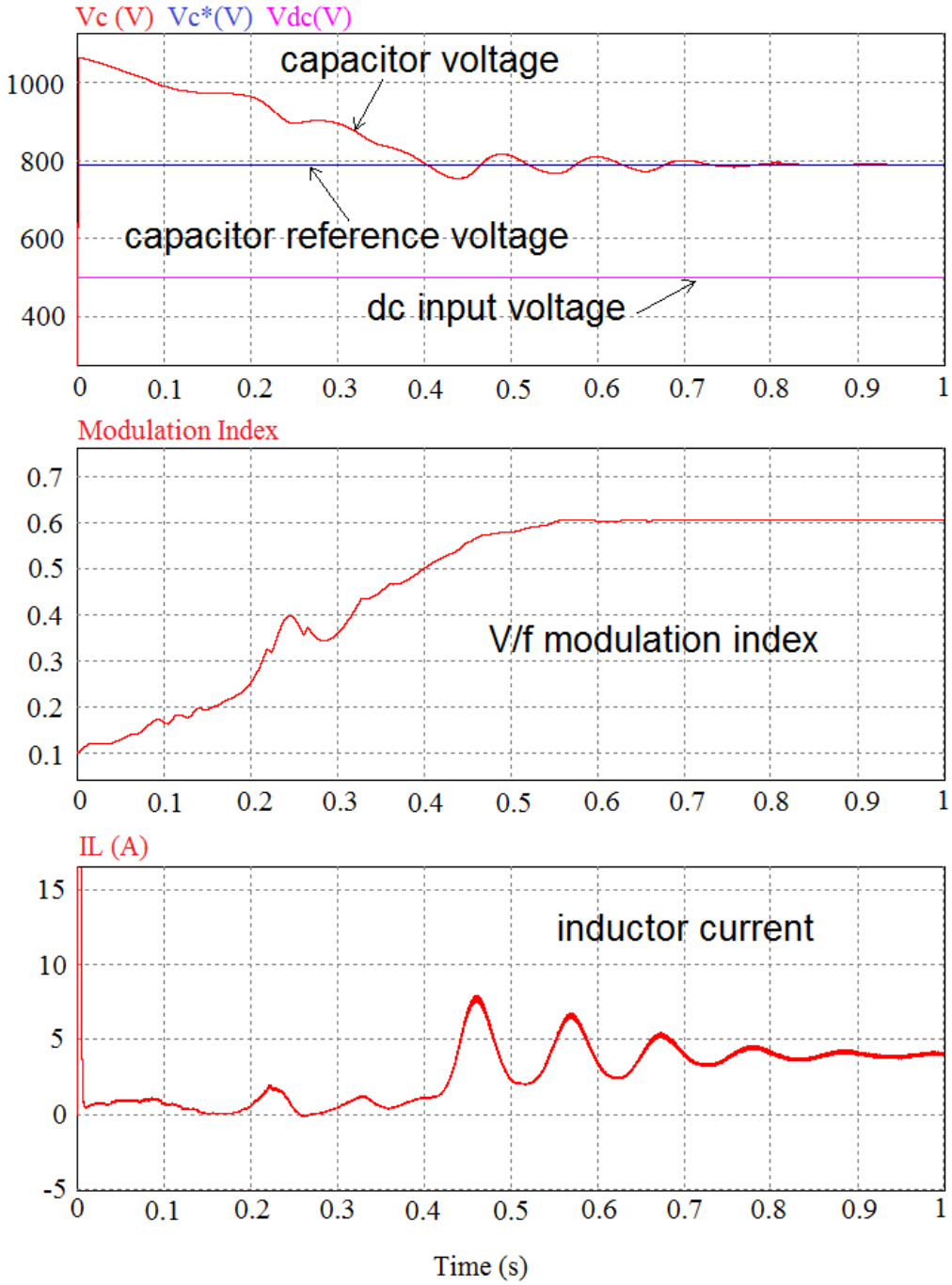

Figure 2.11 The reference capacitor voltage VC*, the capacitor voltage VC, the dc-link voltage V_{DC}, the V/f modulation index and actual inductor current IL

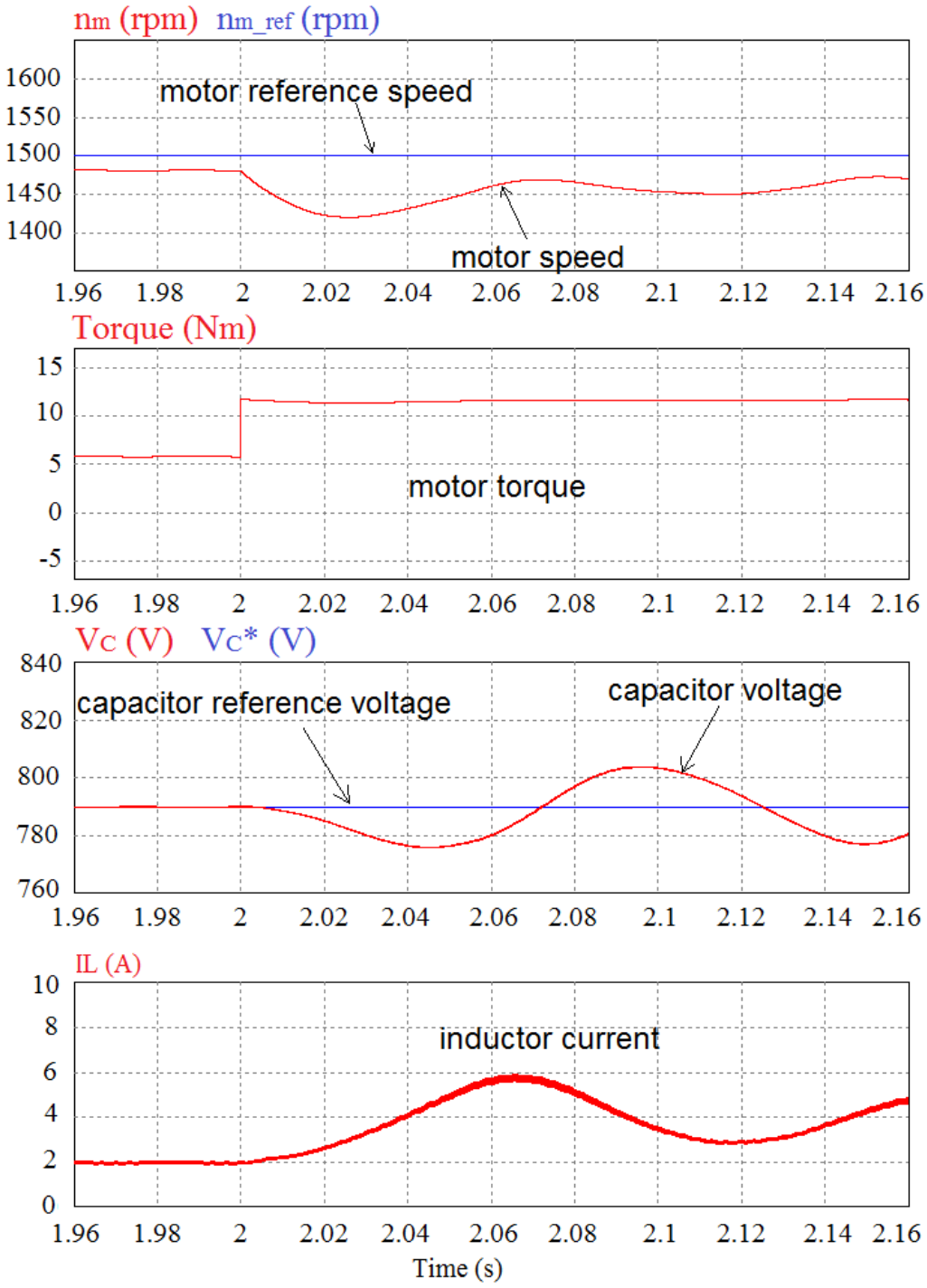

Figure 2.12 The system response during 50% step up load disturbance: motor speed nm, motor torque T, capacitor voltage VC, inductor current IL

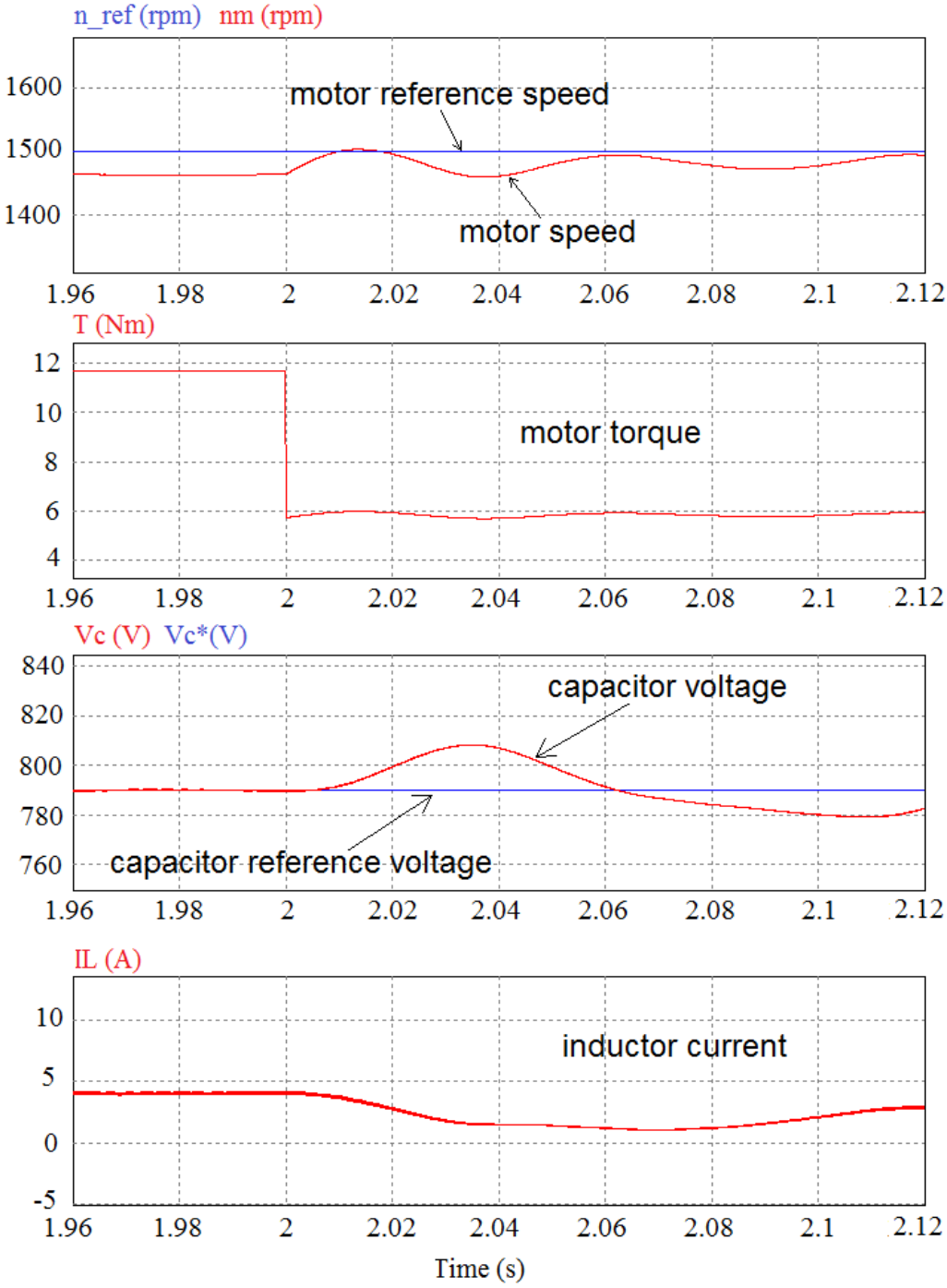

Figure 2.13 The system response during 50% step down load disturbance: motor speed nm, motor torque T, capacitor voltage VC, inductor current IL

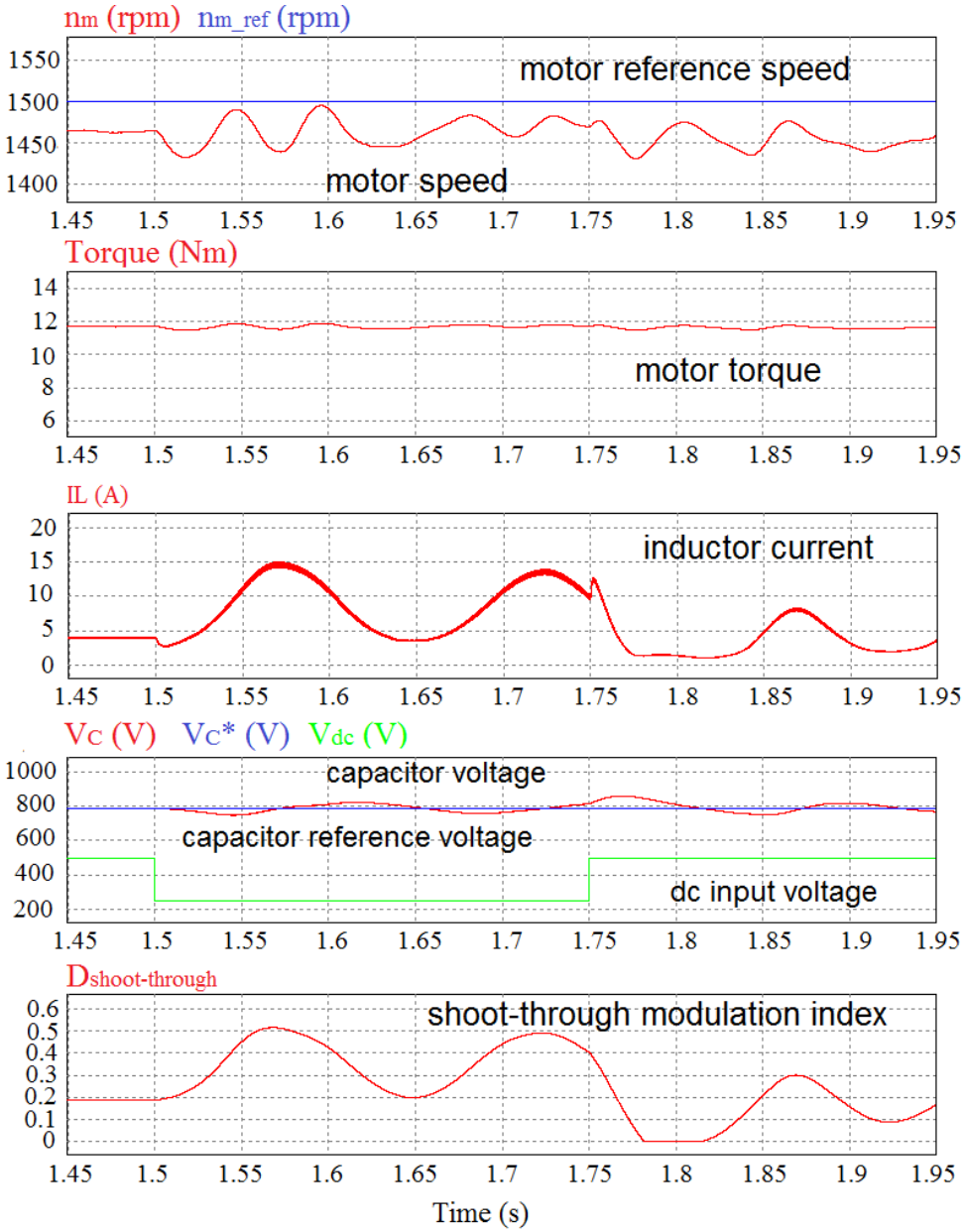

Figure 2.14 The system response during 50% step down in input voltage, at 50 Hz motor frequency

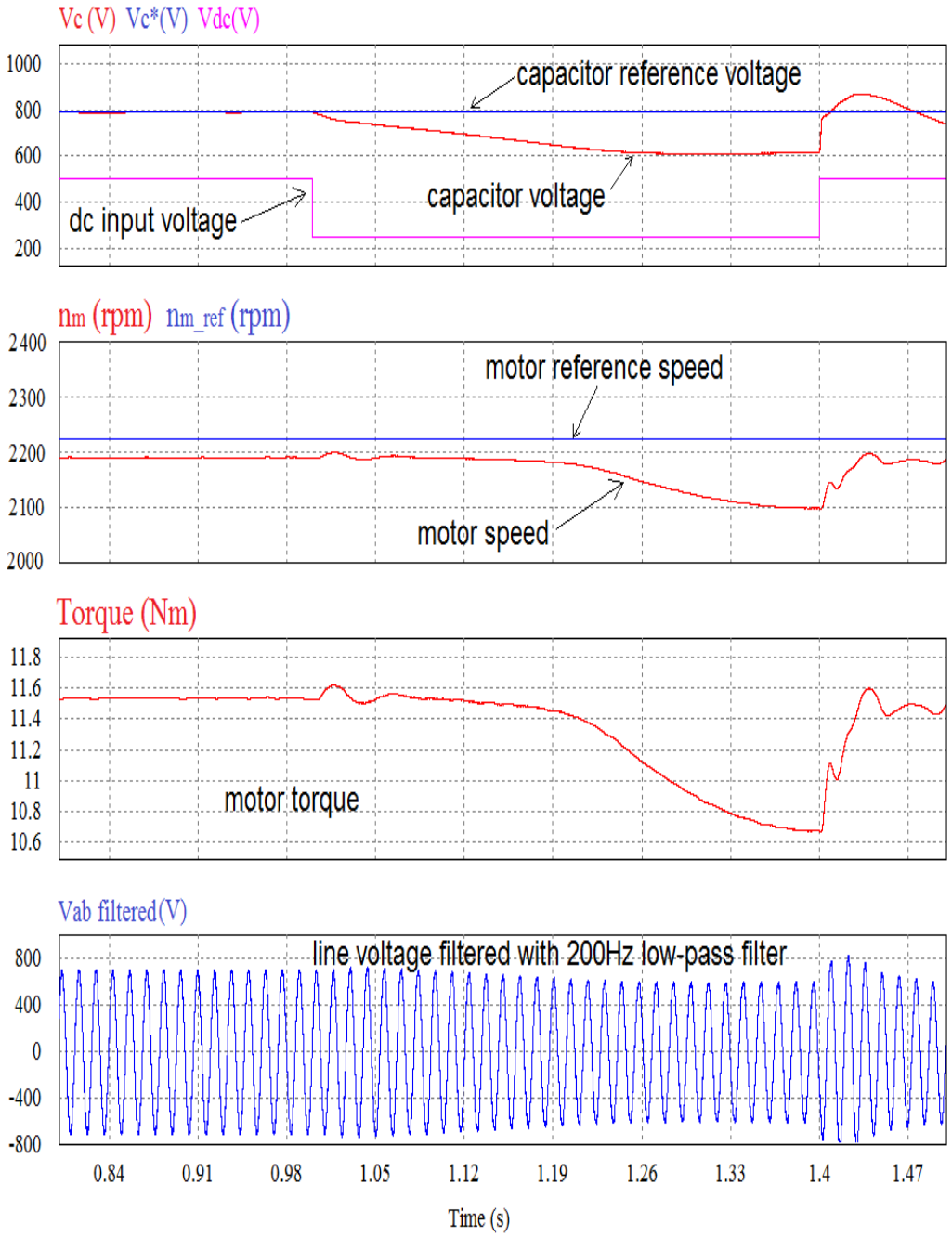

Figure 2.15 Capacitor voltage, motor speed, torque and shoot-through modulation index under full load at 75Hz with 50% step down and up in dc input voltage

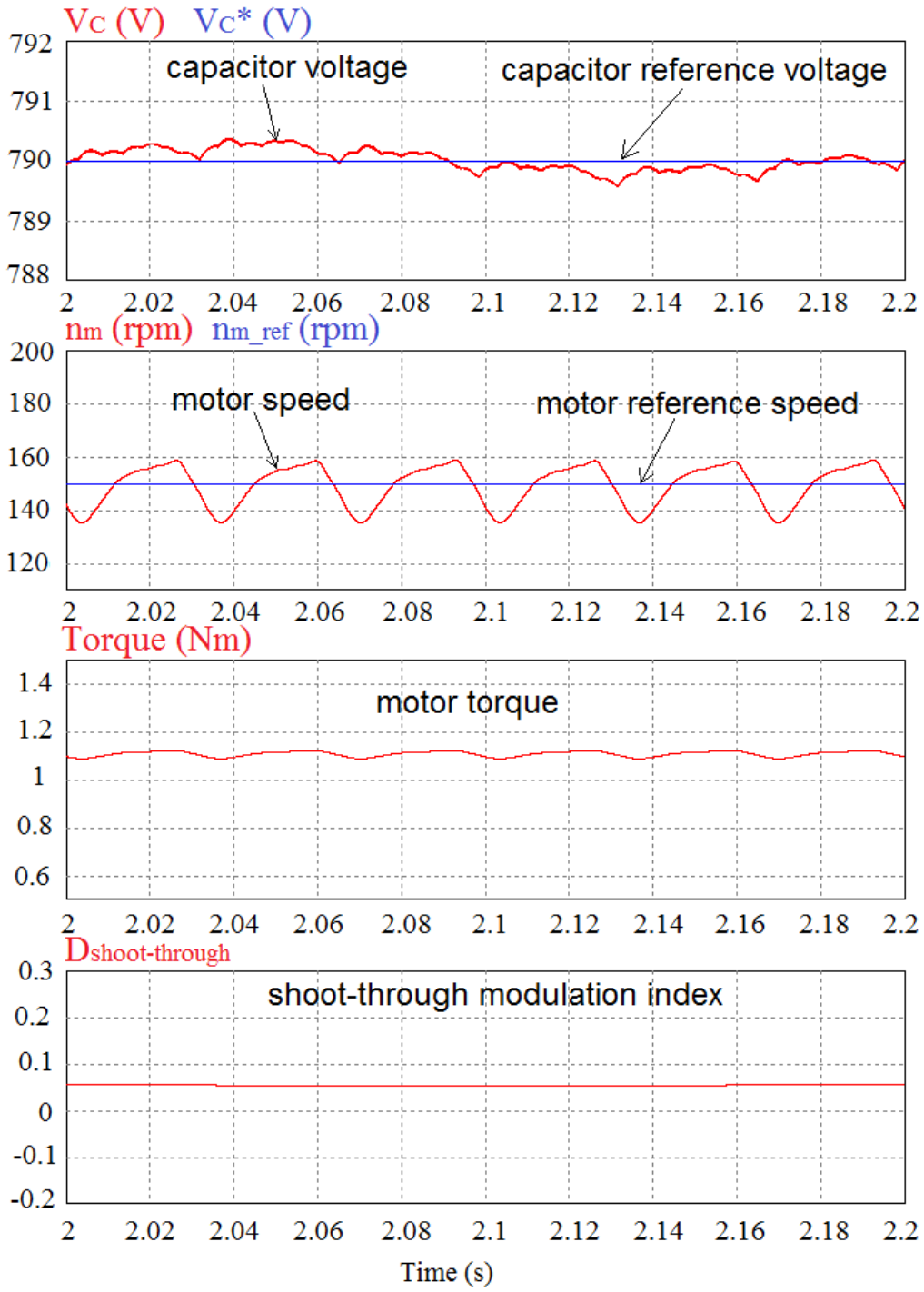

Figure 2.16 Capacitor voltage, motor speed, torque and shoot-through modulation index at 5 Hz operation frequency, for ventilator load(1.1Nm at 5Hz)

2.6. Conclusions

This chapter presents a closed loop speed control of induction motor fed by Space Vector Pulse Width Modulation Z-source inverter based on close loop Volts/Hertz control strategies. The peak dc-link voltage is controlled by a closed loop voltage controller within the period of zero vectors of space vector modulation. The simulation results verified the validity of the close loop speed control method during start up, load disturbance and input voltage changes.

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CHAPTER 3 FOUR SWITCH THREE-PHASE Z-SOURCE INVERTER

3.1. Introduction

The four-switch three-phase Z-source inverter presented in [1] is a single stage buck boost inverter with reduce count switches. In contrast to standard four-switch three-phase inverter [3]–[5] which operates at half dc input voltage the proposed four-switch z-source inverter, by self-boosting, brings the output voltage at same (or higher) value as in six switch standard three-phase inverter [6].

Comprehensive investigation of z-source three-phase four-switch inverters and z-source three-phase four-switch inverter with dc link split capacitor and a new proposed topology with self-boost property that can be used as post-fault topology in the switch redundant fault tolerant Z-source inverter is presented in [2]

A modified z-source single-phase inverter with two switches is introduced in [7]. Besides the topology and the operating principle of the new modified z-source single-phase inverter with two switches, three voltage control methods are presented. Two of them control the average output voltage of the modified z-source and the other one controls the load current as well as the average output voltage of the modified z-source.

The two six-switch three-phase inverters sharing the same Z-source network [17] can be considered also a reduced element count solution because instead of two Z-source network use only one.

In essence they are self-boosting unidirectional dc-ac converters with only six power switches (unless used in multilevel topologies [11][13][17][21]), which are used with some PWM strategies to short-circuit the z-source and thus produce dc voltage boosting.

In the Z-source converters the self-boost attribute implies some voltage and current over rating [12][13]. The average dc-link voltage is equal with the voltage across the capacitors in the Z impedance network but the voltage stress of the inverter bridge is much higher.

3.2. Four-Switch Three-Phase Z-Source Inverter

The today's widely used variable-speed drives for ac motors usually incorporate a six switch inverter bridge. The necessity for further cost reduction of the variable-speed drives can lead to the substitution of the six switch bridge with a four switch bridge. In case of a three-phase four switch inverter one of the three-phase load terminals is at a fixed potential referenced to the ground of the dc supply.

The four-switch three-phase z-source topology combines the advantages of a traditional four-switch three-phase inverter with the advantages of the Z impedance network. This new topology, besides the self-boost property, has low switch count and it can operate as a buck-boost inverter. In contrast to standard four-switch three-phase inverter which operates at half dc input voltage the proposed four-switch z-source inverter, by self-boosting, brings the output voltage

at the same (or higher) value as in six switch standard three-phase inverter. As we could see in case of a z-source inverter with six switches the voltage across the inverter bridge is zero when the voltage boost is applied by short-circuiting at least one of the three inverter legs. So the shoot-through state of the inverter limits the available maximum output voltage, the placing of shoot-through states during the zero voltage vector time intervals (no voltage seen by the load) seems to be a practical solution [8].

3.2.1 Principle of operation

The four-switch three-phase Z-source inverter is shown in Fig. 3.1. In essence, this topology shows that one of the capacitors in the Z network is split into and the middle point is connected to one phase of the load.

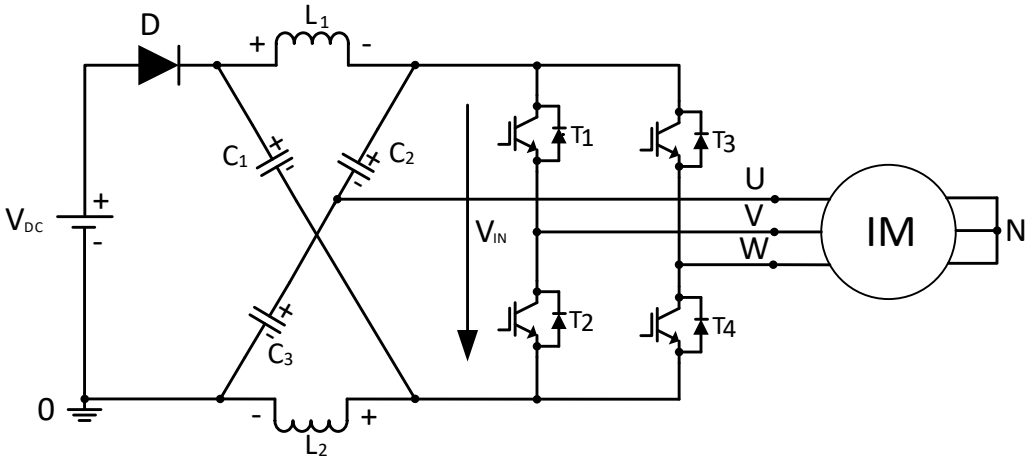

Figure 3.1 Four-switch three-phase z-source inverter with induction machine

The 50% voltage drawback of conventional four-switch three-phase inverter is eliminated by the four-switch Z-source inverter because the shoot through state produce not only the voltage boost but it produce also an active voltage vector, thus generating non-zero output voltage Fig.3.2.

The equivalent scheme of the shoot-trough state of the four-switch z-source three-phase inverter when all four switch are conducting shows that during the shoot-through state the voltage seen by the load is equal with the voltage across capacitor C_2.

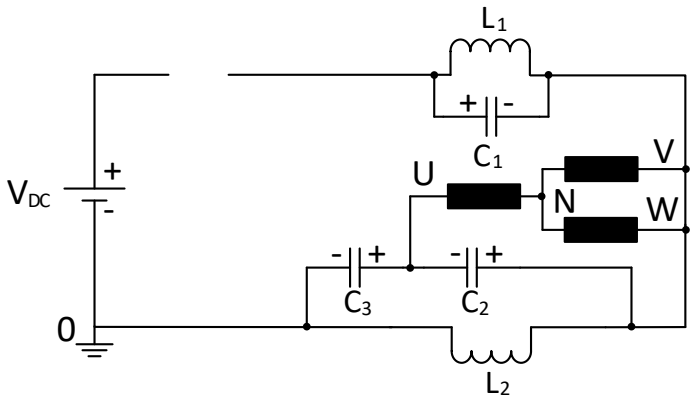

Figure 3.2 Shoot-through state equivalent circuit of the four-switch three-phase z-source inverter

By averaging the voltage across one inductor during one switching period in steady state the same relationship can be obtained between the input dc voltage V_{DC} and the average dc-link voltage V_{in}. The average dc-link voltage is equal with the voltage across C_1 or across C_2 and C_3 as for a three-phase Z-source inverter with six switches or for a single phase Z-source inverter.

3.2.2 Space phasor analysis

The voltage space vector for the three-phase load in Fig. 3.1 can be defined as follows

$$\underline{v}_s = \frac{2}{3}\left(v_{UN} + e^{-j\frac{2\pi}{3}}v_{VN} + +e^{-j\frac{4\pi}{3}}v_{WN}\right) \tag{3.1}$$

where v_{UN}, v_{VN}, and v_{WN} are the instantaneous phase voltages. With the four switches in Fig. 3.1 five voltage vectors can be obtained, as shown in Table 3.1

	T_1	T_2	T_3	T_4
S_1	0	1	0	1
S_2	1	0	0	1
S_3	1	0	1	0
S_4	0	1	1	0
S_{ST}	1	1	1	1

0 – switch off
1 – switch on
S_x – switching state

Table 3.1 Switching pattern

All voltage vectors are active voltage vectors. Although two more shoot-through state can be obtained by turning on T_1 and T_2 or T_3 and T_4 at the same time these states were neglected because the maximum current flowing through the inverter bridge would only flow through one leg of the inverter bridge which would lead to a bigger power transistor bridge. The wey connected three-phase load terminal voltages referenced to the ground are shown with respect to the switching pattern in Table 3.1, in Fig. 3.3.

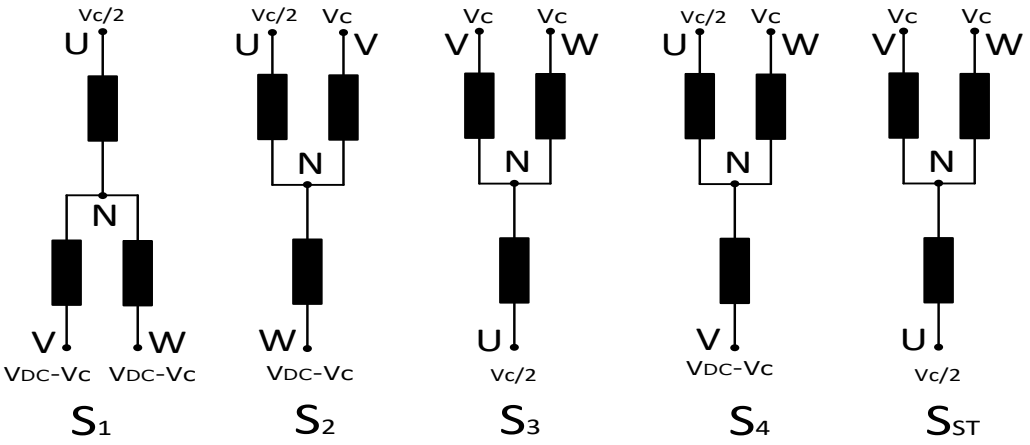

Figure 3.3 Load phase terminal voltages referenced to ground 0

In order to derive the phase voltages we will consider

$$\bar{V}_C = \bar{V}_{C1}; \qquad \bar{V}_{C2} = \bar{V}_{C3} = \frac{\bar{V}_C}{2} \tag{3.2}$$

where $\bar{V}_{C1}, \bar{V}_{C2}$ and $\bar{V}_{C3}$ are the average voltages across C_1, C_2 and C_3 capacitors.
For a symmetrical balanced wye connected three-phase load the phase voltages can be written as

$$\begin{aligned} v_{UN} &= \frac{2}{3}v_{U0} - \frac{1}{3}(v_{V0} + v_{W0}) \\ v_{VN} &= \frac{2}{3}v_{U0} - \frac{1}{3}(v_{W0} + v_{U0}) \\ v_{WN} &= \frac{2}{3}v_{U0} - \frac{1}{3}(v_{U0} + v_{V0}) \end{aligned} \tag{3.3}$$

Substituting V_{U0}, V_{V0} and V_{W0}, from fig. 3.3 into (3.3) and using expression of the space voltage vector (3.1) the five voltage vectors can be derived as

$$
\begin{aligned}
\underline{V_1} &= \bar{V}_C \frac{2}{3} V_{DC} \\
\underline{V_2} &= \left(\frac{1}{3} + j\frac{2\sqrt{3}}{3}\right)\bar{V}_C + \left(-\frac{1}{3} - j\frac{\sqrt{3}}{3}\right)V_{DC} \\
\underline{V_3} &= -\frac{1}{3}\bar{V}_C \\
\underline{V_4} &= \left(\frac{1}{3} - j\frac{2\sqrt{3}}{3}\right)\bar{V}_C + \left(-\frac{1}{3} + j\frac{\sqrt{3}}{3}\right)V_{DC} \\
\underline{V_{ST}} &= -\frac{1}{3}\bar{V}_C
\end{aligned}
\tag{3.4}
$$

The relationship between the average capacitor voltage $\bar{V}_C$ and the input dc voltage V_{DC} can be expressed as

$$\bar{V}_C = k \cdot V_{DC} \tag{3.5}$$

$$k = \frac{1 - D_{ST}}{1 - 2D_{ST}}; \quad k > 1 \tag{3.6}$$

Rewriting (3.4) using (3.6) the voltage vectors can be derived as

$$
\begin{aligned}
\underline{V_1} &= \left(k - \frac{2}{3}\right)V_{DC} \\
\underline{V_2} &= \left[\frac{1}{3}(k-1) + j\frac{\sqrt{3}}{3}(2k-1)\right]V_{DC} \\
\underline{V_3} &= -\frac{1}{3}kV_{DC} \\
\underline{V_4} &= \left[\frac{1}{3}(k-1) - j\frac{\sqrt{3}}{3}(2k-1)\right]V_{DC} \\
\underline{V_{ST}} &= -\frac{1}{3}kV_{DC}
\end{aligned}
\tag{3.7}
$$

Notice that in (3.7) the boost factor k influences the amplitude as well the direction of the five voltage vectors.
For k=2 the five vectors in the complex plane are illustrated in fig. 3.4.

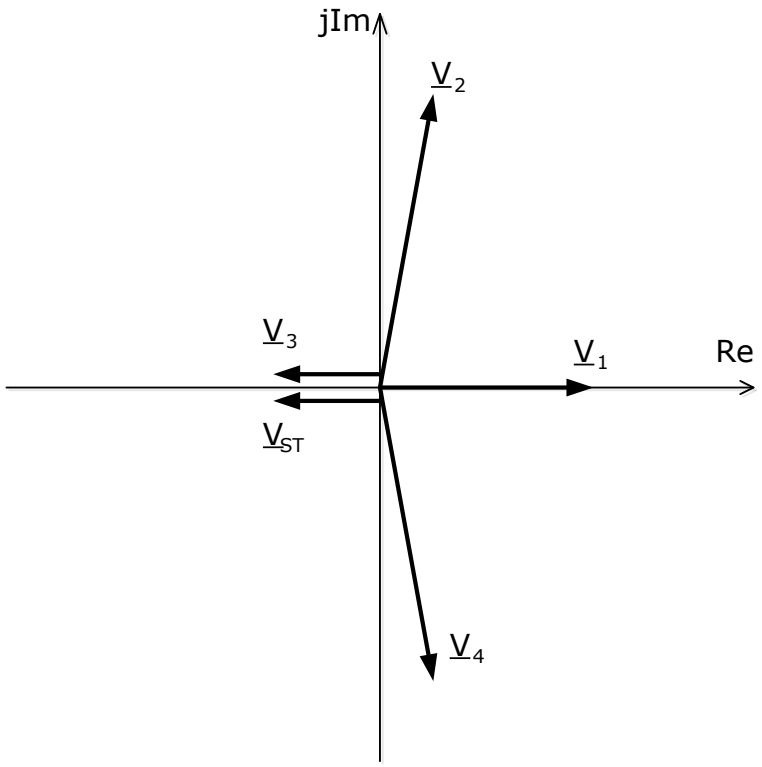

Figure 3.4 Locations of the voltage vectors in the complex plane for k=2

The voltage vector generated by the shoot-through state V_{ST} has the same amplitude and direction as the V_3 voltage vector.

The voltage space vector expressed in (3.1) can be rewritten in the complex plane as

$$\underline{v}_s = v_{s\alpha} + v_{s\beta} \tag{3.8}$$

The average voltage space vector over one switching cycle should be equal with the sum of the five average voltage space vectors (V_1, V_2, V_3, V_4 and V_{ST}) over one switching cycle T_S

$$\bar{\underline{v}}_s = \frac{(t_1 V_1 + t_2 V_2 + t_3 V_3 + t_4 V_4 + t_{ST} V_{ST})}{T_S} \tag{3.9}$$

where

$$T_S = t_1 + t_2 + t_3 + t_4 + t_{ST} \tag{3.10}$$

To obtain the expressions of $v_{s\alpha}$ and $v_{s\beta}$ the expressions of the five voltage vectors (3.7) are introduced in (3.9)

$$V_{S\alpha} = \frac{V_{DC}}{3T_S}\left[t_1(3k-2) + (t_2+t_4)(k-1) - (t_3+t_{ST})k\right]$$
$$V_{S\beta} = \frac{\sqrt{3}V_{DC}}{3T_S}(t_2 - t_4)(2k-1) \tag{3.11}$$

3.3. Control algorithm for DC boost and AC output voltage

The algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive is shown in Fig. 3.5.

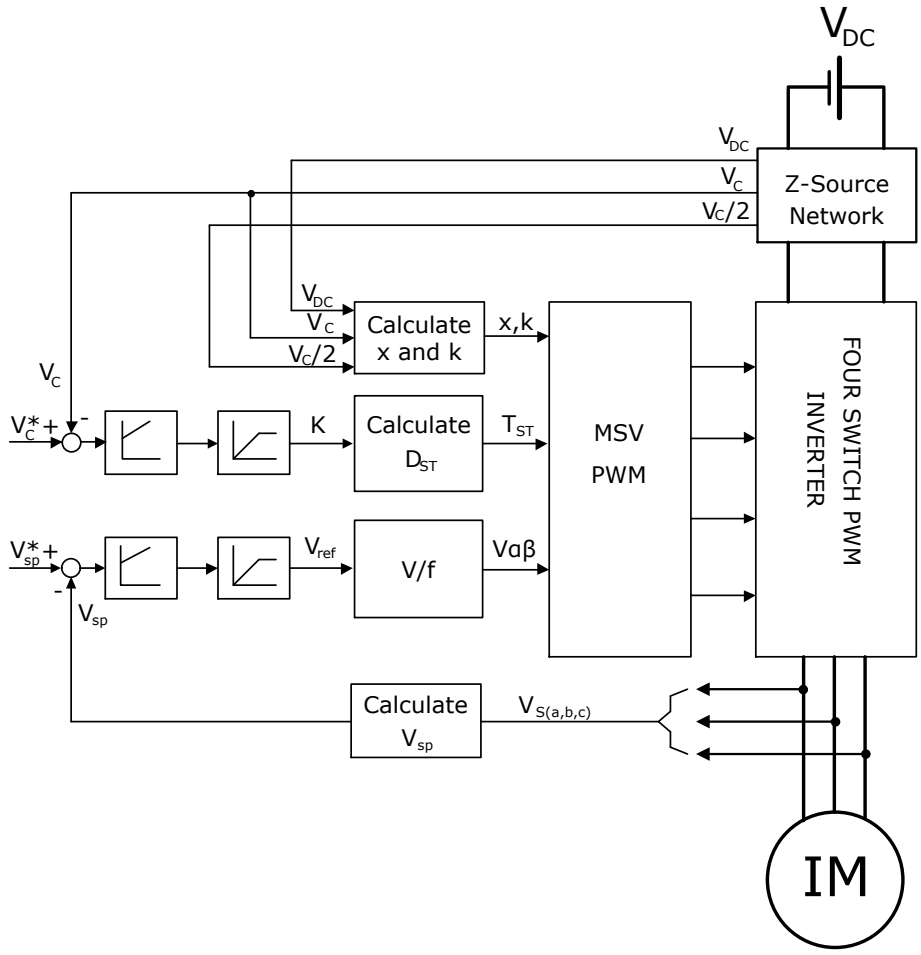

Figure 3.5 Block diagram for voltage control of four-switch three-phase Z-source induction motor drive

3.3.1 Z-source Capacitor Voltage Control

The Z-source utilizes the shoot-through state to step up the dc link voltage by conducting both upper and lower switches of any phase legs. Thus, the Z-source inverter can boost the voltage to the desired ac output voltage, which is greater than the available dc link voltage. The capacitor voltage V_C is equivalent to the dc link shoot- through time duty ratio. Fig. 3.6 shows the relationship between $\frac{V_C}{V_{DC}}$ and the shoot-through time duty ratio D_{ST}. As the relationship has nonlinear characteristics, the shoot-through time cannot linearly control the capacitor voltage.

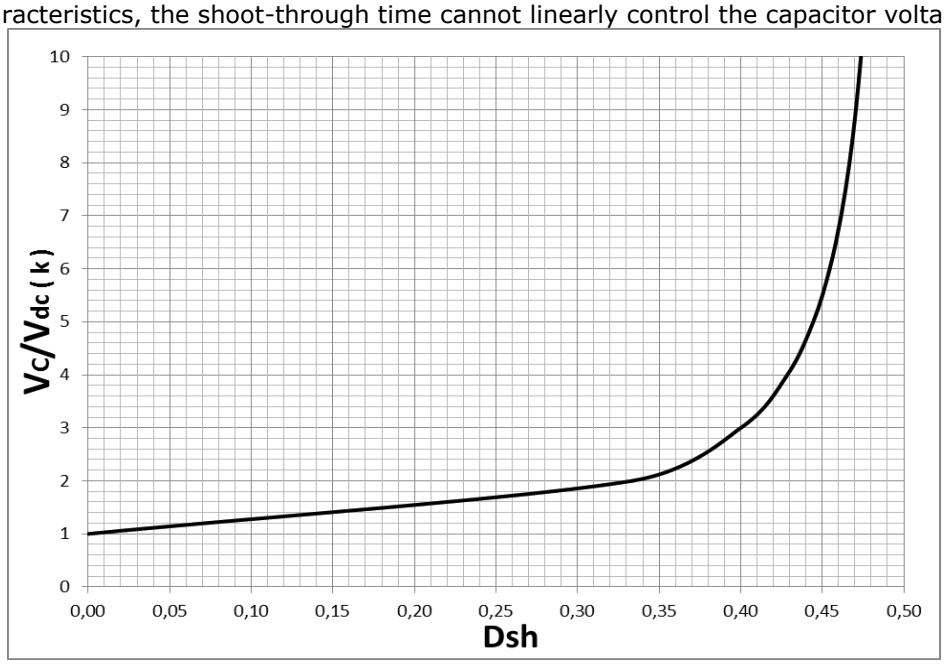

Figure 3.6 Relationship between capacitor voltage and shoot-through time

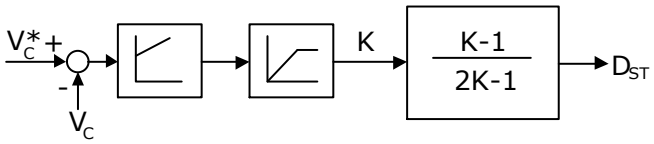

Figure 3.7 Capacitor voltage controller using linearization method

The nonlinearity may deteriorate the transient response of capacitor voltage. In order to overcome the problem, the algorithm for controlling linearly the capacitor voltage is shown in Fig. 3.7. The output of the PI controller of V_C becomes K and can be defined as

$$K = \frac{V_C}{V_{DC}} \tag{3.12}$$

where the K is greater than 1 for stepping up the capacitor voltage. Using (3.6) and (3.12), the shoot-through time D_{ST} is calculated from

$$D_{ST} = \frac{K-1}{2K-1} \tag{3.13}$$

The output of PI controller of VC becomes K and then the D_{ST} can be calculated from K from (3.13). As the capacitor voltage is linearly controlled by K, the good transient performance of capacitor voltage can be obtained.

3.3.2 AC output voltage control

The ac output voltage is assigned as a feedback signal at the output voltage PI controller, the phase delay between the reference ac output voltage and actual ac output voltage is generated due to the integral component in the PI controller. Instead of ac output voltage, the peak output voltage is used to control the ac output voltage, because the peak output voltage is dc value. After detecting 3-phase line voltages, the 3-phase voltages are transformed into 2-axis voltages in the stationary reference frame, V_{ds}^{s} and V_{qs}^{s}, and then the peak output voltage V_{sp} can be derived as follows

$$V_{sp} = \sqrt{\left(V_{ds}^{s}\right)^2 + \left(V_{qs}^{s}\right)^2} \tag{3.14}$$

The output of PI controller V_{sp} becomes the reference voltage for V/f speed control. Block diagram for ac output voltage control is shown in Fig. 3.8.

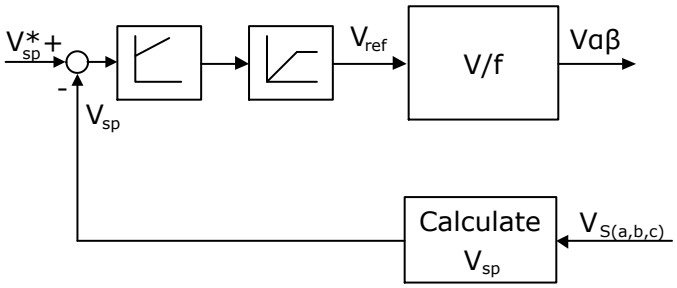

Figure 3.8 Block diagram for ac output voltage control

3.3.3 Split capacitor voltage balance compensation

During the shoot-through state the voltage seen by the load is equal with the voltage across capacitor C_2. This will discharge de C_2 capacitor and move the potential value from the fixed point referenced to the ground of the dc supply, unbalance the split capacitor which affect the inverter performance. To correct this situation the measured voltage on the capacitor C_2 and measured k is introduced in vector calculation.

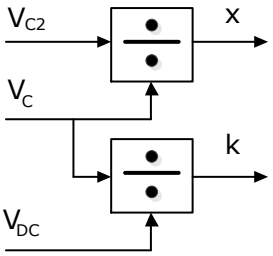

Figure 3.9 Block diagram for voltage balance compensation and boost factor

$$x = \frac{VC_2}{VC} = \frac{1}{2} \tag{3.15}$$

Substituting V_C from (3.5) and using the expression (3.15) the five voltage vectors can be derived as

$$\begin{aligned}
\underline{V_1} &= \frac{2}{3}\left[(x+1)k-1\right]V_{DC} \\
\underline{V_2} &= \left[\frac{1}{3}(2xk-1)+j\frac{\sqrt{3}}{3}(2k-1)\right]V_{DC} \\
\underline{V_3} &= \frac{2}{3}k(x-1)V_{DC} \\
\underline{V_4} &= \left[\frac{1}{3}(2xk-1)-j\frac{\sqrt{3}}{3}(2k-1)\right]V_{DC} \\
\underline{V_{ST}} &= \frac{2}{3}k(x-1)V_{DC}
\end{aligned} \tag{3.16}$$

Finally the expressions of the v_α and v_β components of a desired voltage space phasor $\underline{v_S}$ using can be given by

$$\begin{aligned}
V_{S\alpha} &= \frac{V_{DC}}{3T_S}\left[t_1 2\left((x+1)k-1\right)+(t_2+t_4)(2xk-1)-(t_3+t_{ST})2k(1-x)\right] \\
V_{S\beta} &= \frac{\sqrt{3}V_{DC}}{3T_S}(t_2-t_4)(2k-1)
\end{aligned} \tag{3.17}$$

Given (3.8) – (3.10) and (3.17) calculate the duty ratios for the four transistors and generate the four gating pulses.

Considering $t_4 = 0$ from expression of $V_{S\beta}$ results the time for vector V_2

$$t_2 = \frac{3T_S V_{S\beta}}{(2k-1)\sqrt{3}V_{DC}} \tag{3.18}$$

Substituting t_2 and t_4 in expression of $V_{S\alpha}$ and considering (3.10) derive the time t_3.

$$t_3 = \frac{T_S\left(1-\frac{3V_{S\alpha}}{V_{DC}2\left[(x+1)k-1\right]}+\frac{3V_{S\beta}}{(2k-1)\sqrt{3}V_{DC}}\frac{2xk-1}{2\left[(x+1)k-1\right]}\right)}{\left(1+\frac{k(1-x)}{(x+1)k-1}\right)}-t_{ST}\cdot T_S \tag{3.19}$$

The duty ratios D_V and D_W to generate the two complementary signals for the two phase legs of the inverter bridge and the D_{ST} for the shoot-trough signal are

$$\begin{aligned} D_V &= 1-D_1 = D_{ST}+D_3+D_2 = D_W+D_2 \\ D_W &= D_{ST}+D_3 \\ D_{ST} &= \frac{t_{ST}}{T_S} = \frac{K-1}{2K-1} \\ D_2 &= \frac{t_2}{T_s} = \frac{3V_{S\beta}}{(2k-1)\sqrt{3}V_{DC}} \end{aligned} \tag{3.20}$$

$$\begin{aligned} D_3 &= \frac{t_3}{T_S} = \frac{\left(1-\frac{3V_{S\alpha}}{V_{DC}2\left[(x+1)k-1\right]}\right)+\frac{3T_SV_{S\beta}}{(2k-1)\sqrt{3}V_{DC}}\cdot\frac{2xk-1}{2\left[(x+1)k-1\right]}}{\frac{k(1-x)}{(x+1)k-1}+1}-D_{ST} \\ D_V &= \frac{\left(1-\frac{3V_{S\alpha}}{2\left[(x+1)k-1\right]V_{DC}}\right)+\frac{3V_{S\beta}}{(2k-1)\sqrt{3}V_{DC}}\cdot\frac{2xk-1}{2\left[(x+1)k-1\right]}}{1+\frac{k(1-x)}{(x+1)k-1}} \\ D_W &= \frac{\left(1-\frac{3V_{S\alpha}}{2\left[(x+1)k-1\right]V_{DC}}\right)+\frac{3V_{S\beta}}{(2k-1)\sqrt{3}V_{DC}}\cdot\left(\frac{2xk-1}{2\left[(x+1)k-1\right]}-1\right)}{1+\frac{k(1-x)}{(x+1)k-1}} \end{aligned} \tag{3.21}$$

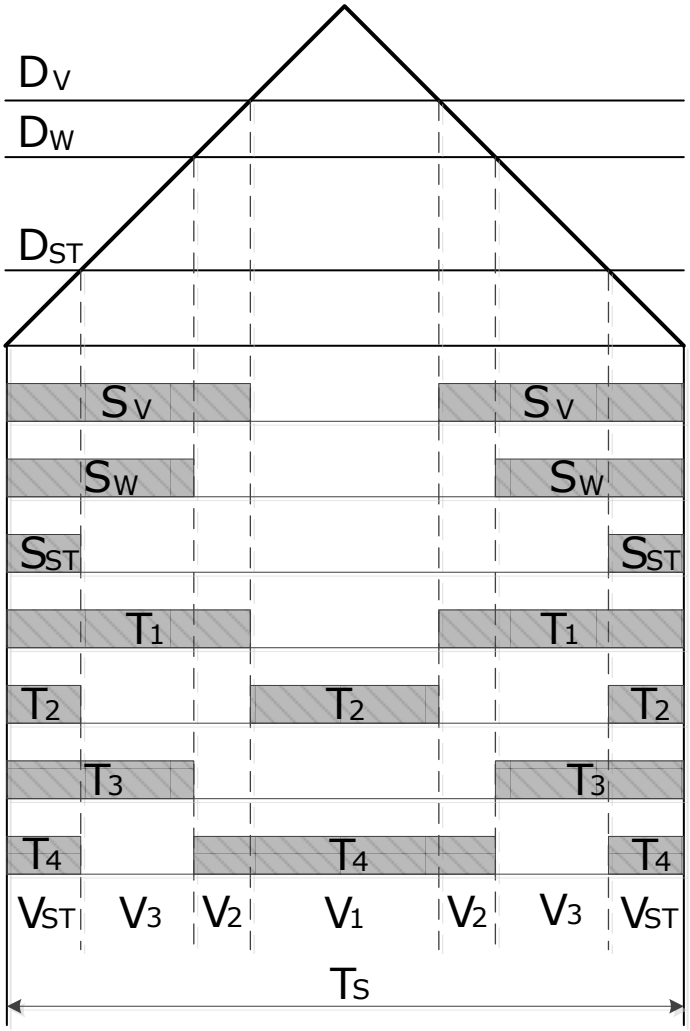

Figure 3.10 PWM signal waveform generation for T_1, T_2, T_3 and T_4

3.4. Simulation Results

The four switch three-phase z-source inverter with induction machine drive and its control algorithms was simulated and validated through experiments. In order to verify the peak dc-link voltage control strategies, simulations are carried out using PLECS software for a 0.5 kW induction motor using parameters in Table 3.2 and for four switch three-phase Z-source inverter network in Table 3.3.

Parameter	Value
Output power	0.5kW
RMS line voltage	400 V
Input frequency	50Hz
No. of poles	4
Stator resistance, R_s	16 Ω
Rotor resistance, R_r	18.5 Ω
Stator leakage inductance, L_{ls}	0.043 Ω
Rotor leakage inductance, L_{lr}	0.043 Ω
Mutual inductance, L_m	0.585 Ω
Moment of inertia, J	0.001 kg·m^2
Rated dc input voltage	350Vdc

Table 3.2 0.5 kW induction motor parameters

Z-SOURCE NETWORK PARAMETERS

Parameter	Value
Capacitors	235μF
Inductors	6.4mH
Inductors resistance	0.9Ω

Table 3.3 Z-source network parameters

Figures 3.11 – 3.18 show the simulation results for V/f control of a 0.5 kW induction motor fed by a four switch three-phase z-source inverter. Figure 3.11 and Figure 3.12 expose the stator current during motor starting from zero to rated speed with full load torque proportional to speed square, Figure 3.13 shows the motor filtered voltage during motor starting from zero to rated speed, Figure 3.14 illustrates the capacitor voltage, the split capacitor voltages and the dc input voltage. Figure 3.15 shows the Z-impedance inductor current IL1 and IL2. Figure 3.16 and Figure 3.17 shows the instantaneous and the dc-link voltage V_i. Motor speed ant torque of the 0.5 kW induction machine are illustrated in Figure 3.18.

The machine accelerates to 50 Hz with speed squared proportional load torque in 0.15 seconds while the capacitor voltage is boosted at 790 V Figure 3.11-3.18; also the inductor current Figure 3.15 which is divided between the two inverter legs does not warrant oversizing of the standard inverter.

Figures 3.19 – 3.26 show the simulation results for V/f control of a 0.5 kW induction motor fed by a four switch three-phase z-source inverter for speed reduced with 25%. Figure 3.19 expose the stator current during motor starting from zero to rated speed with full load torque is proportional to speed square and than speed is reduced with 25%, Figure 3.20 shows the motor filtered voltage during motor starting from zero to rated speed, Figure 3.21 illustrates the capacitor voltage, the split capacitor voltages and the dc input voltage. Figure 3.22 shows the Z-impedance inductor current I_{L1} and I_{L2}. Figure 3.23 and Figure 3.24 shows the instantaneous dc-link voltage V_i. Motor speed ant torque of the 0.5 kW induction machine are illustrated in Figure 3.25. Figure 3.26 shown modulation signals D_V, D_W and D_{ST} in the case of reduced speed with 25%.

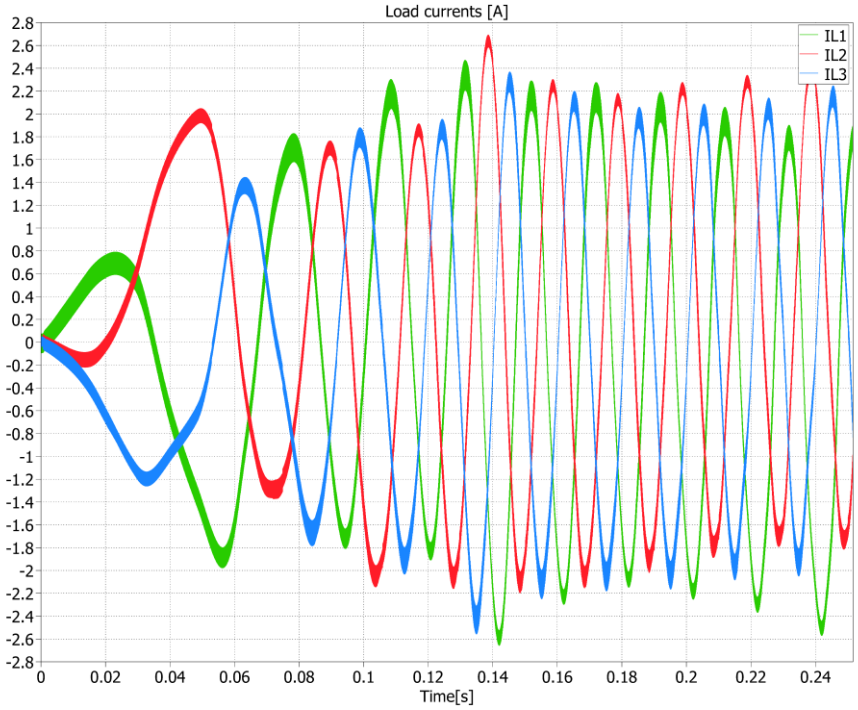

Figure 3.11 Simulated load currents at start-up

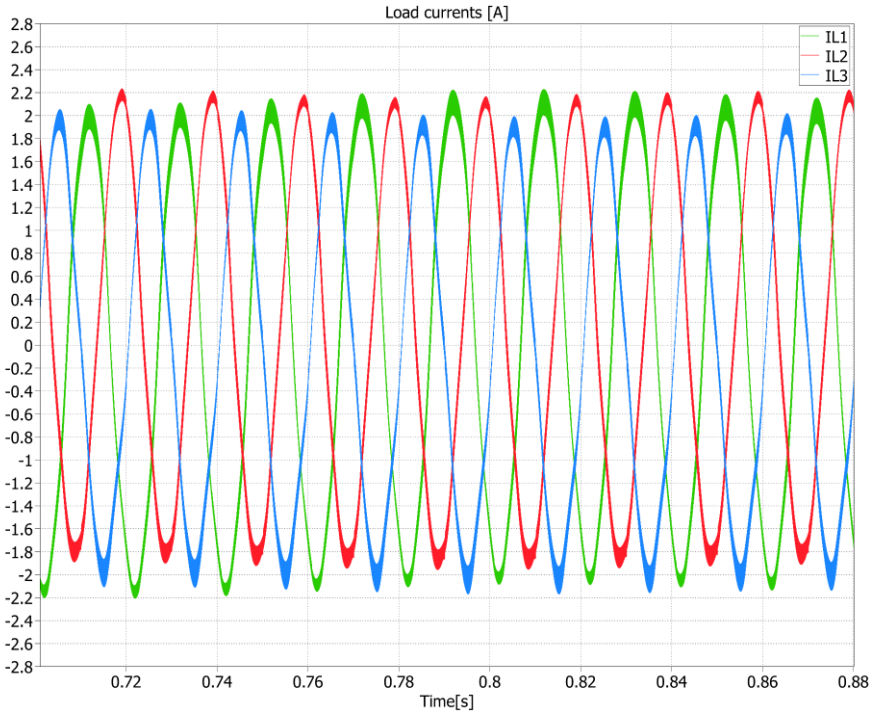

Figure 3.12 Simulated load currents (zoom)

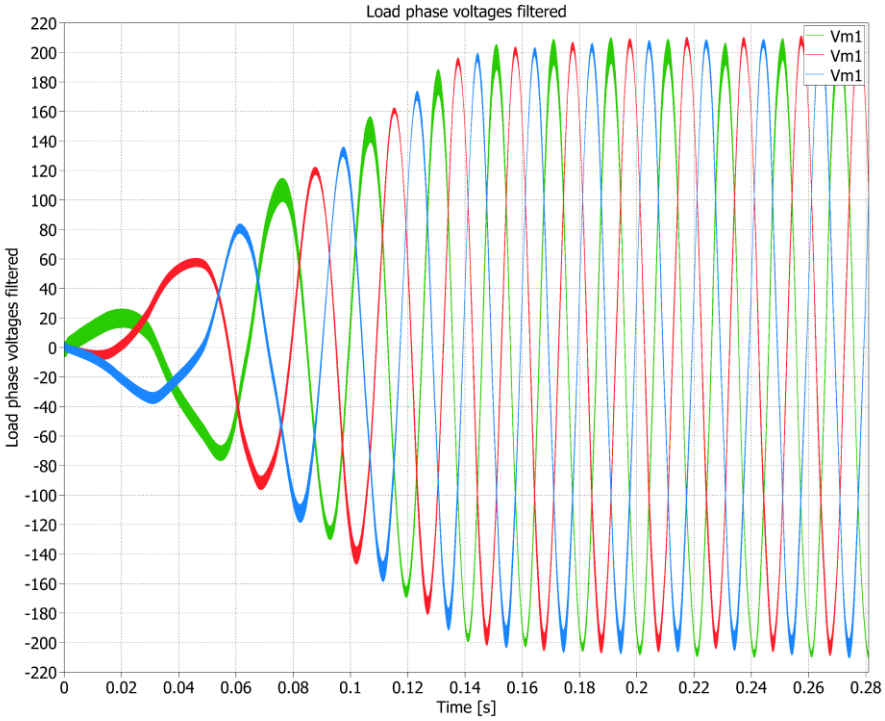

Figure 3.13 Simulated filtered load phase voltages

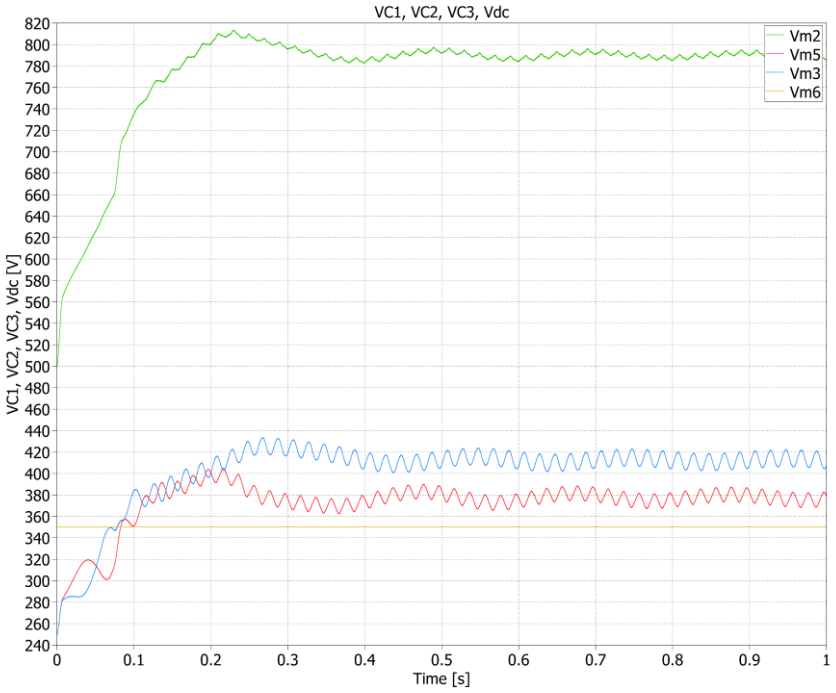

Figure 3.14 Simulated voltage waveforms across C_1, C_2, C_3 and the input dc voltage

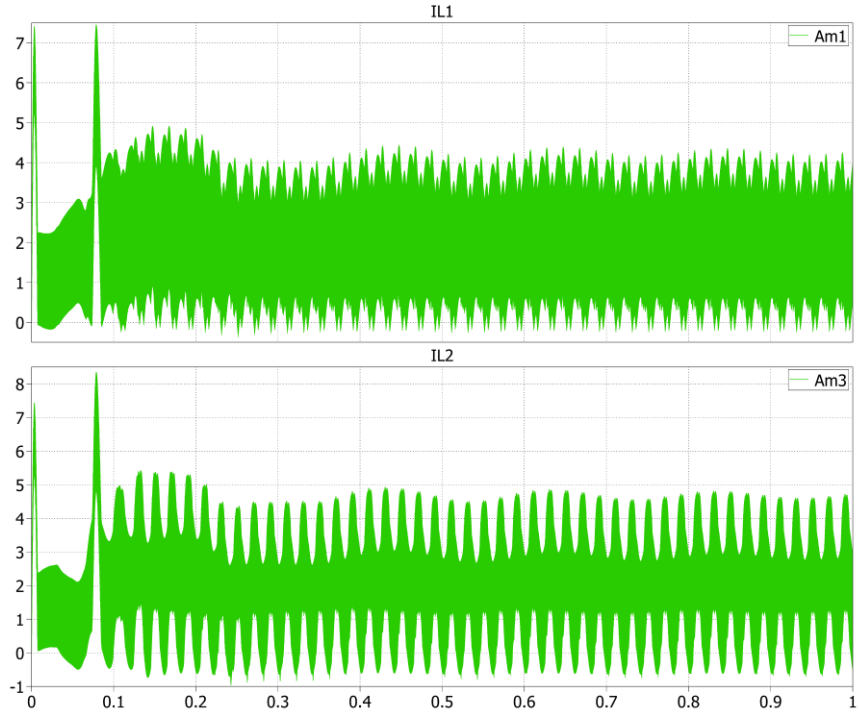

Figure 3.15 Simulated Z-impedance inductor current IL_1 and IL_2

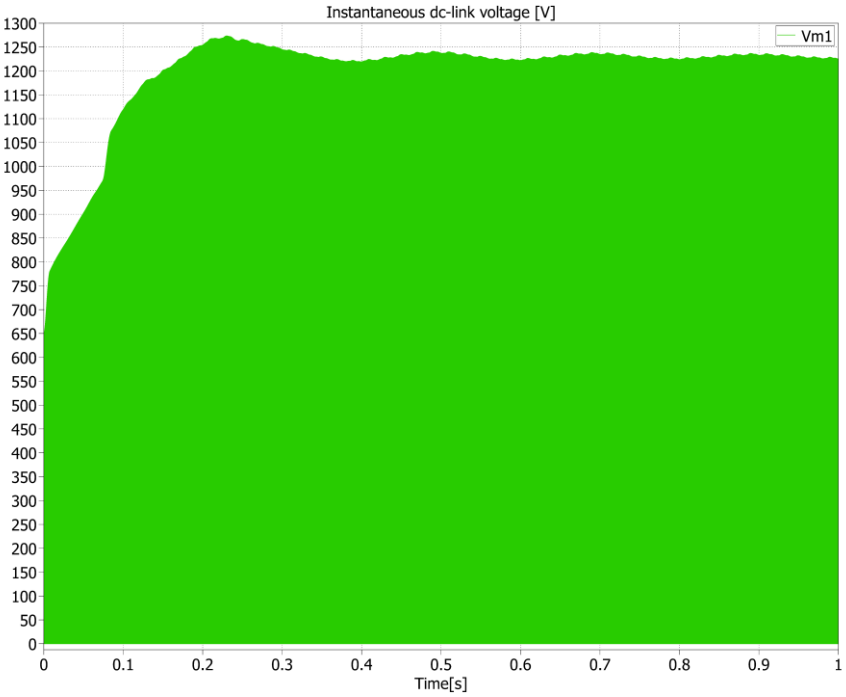

Figure 3.16 Simulated instantaneous dc-link voltage Vi

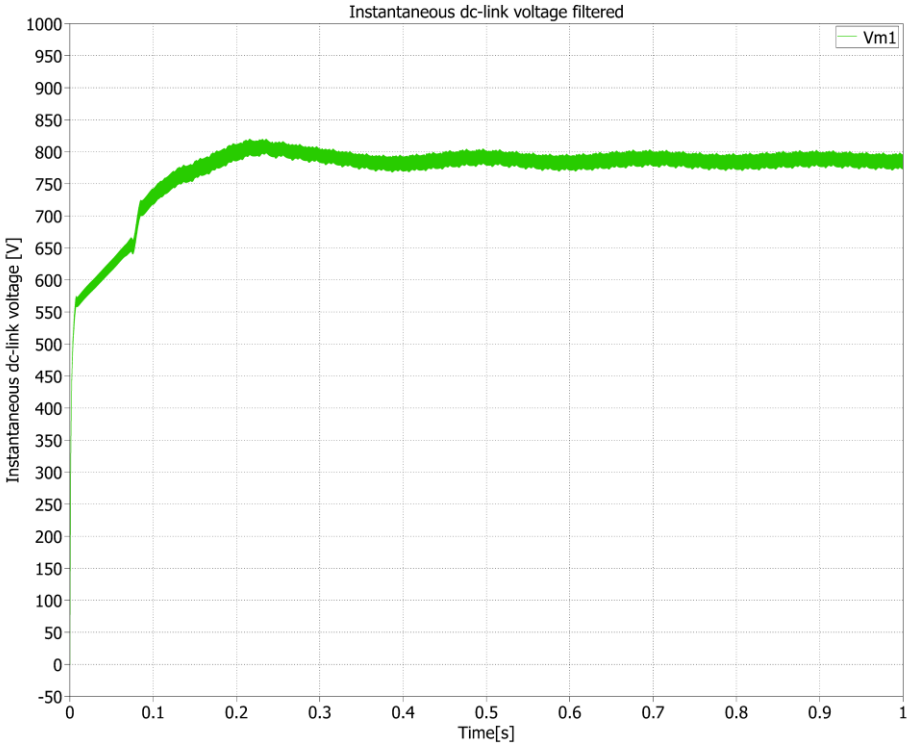

Figure 3.17 Simulated filtered dc-link voltage Vi

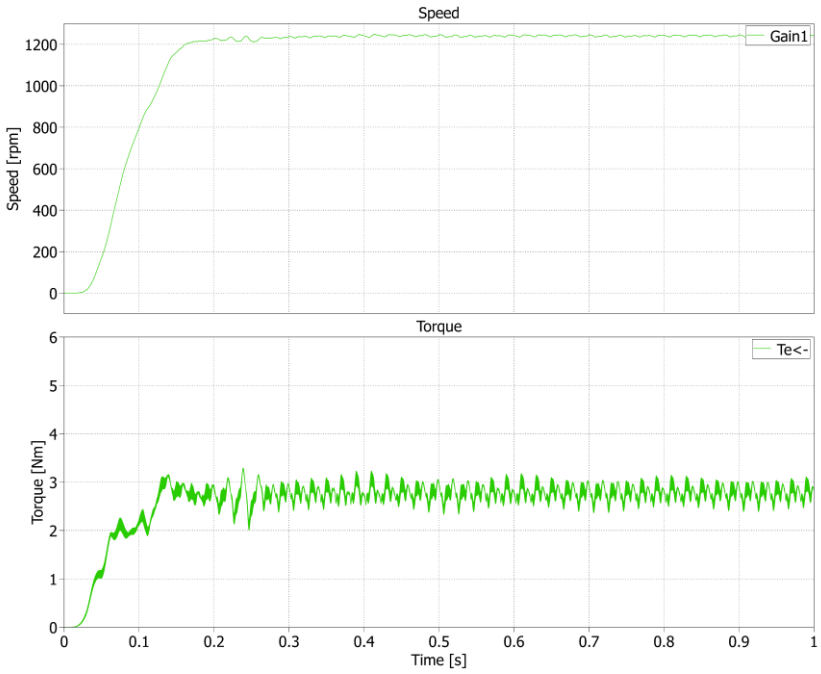

Figure 3.18 Simulated speed ant torque of the 0.5 kW induction machine

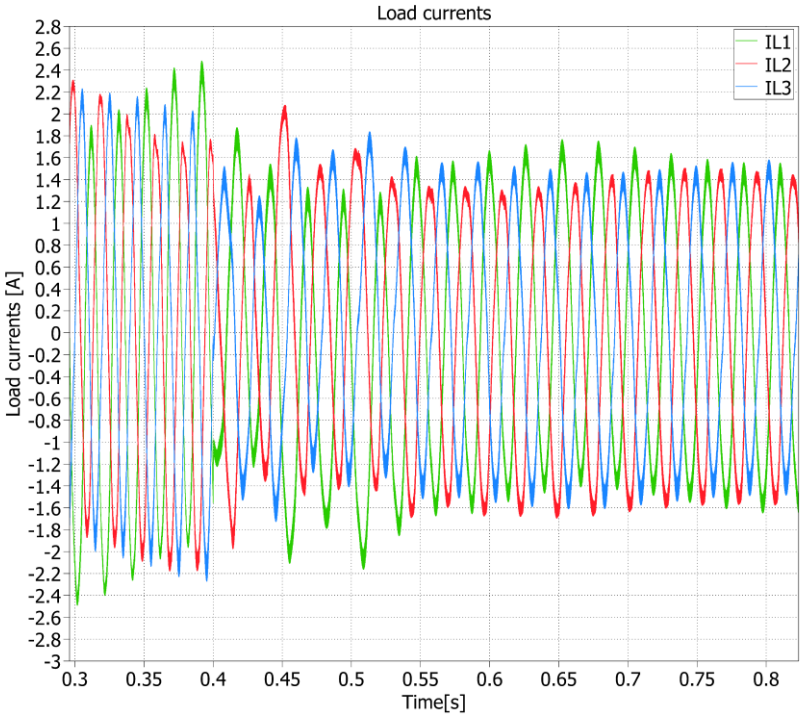

Figure 3.19 Simulated load currents for speed reduced with 25%

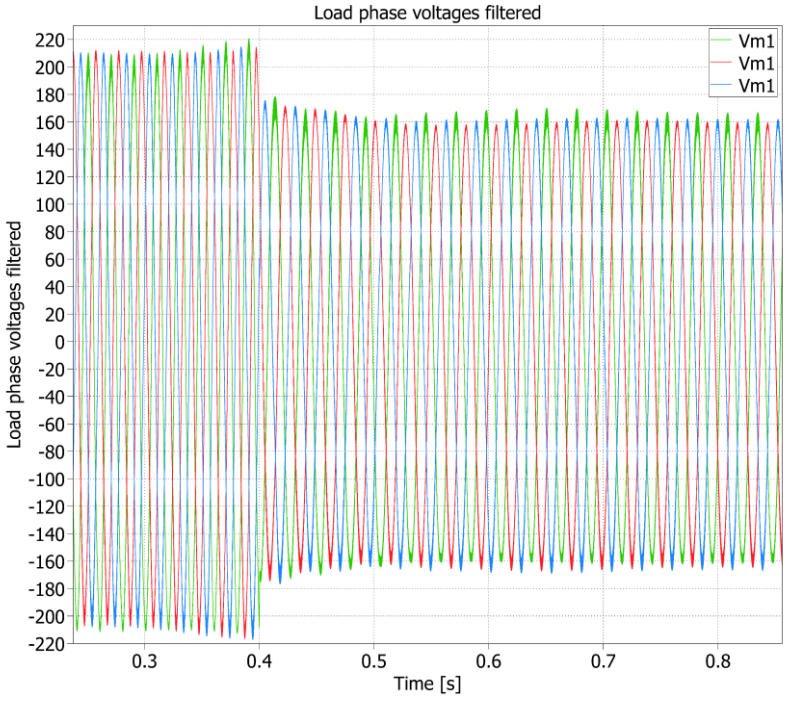

Figure 3.20 Simulated filtered phase voltages for speed reduced with 25%

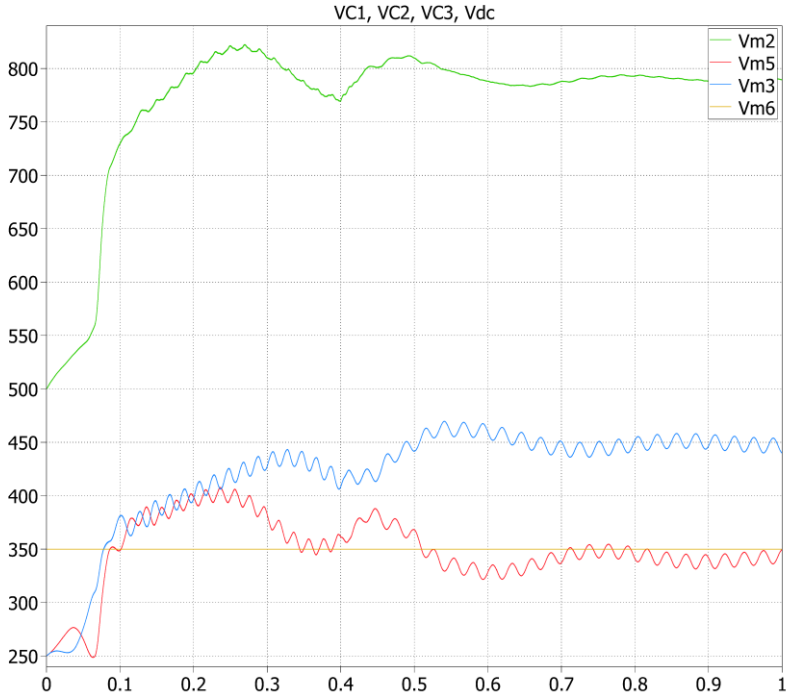

Figure 3.21 Simulated voltage waveforms across C_1, C_2, C_3 and the input dc voltage for speed reduced with 25%

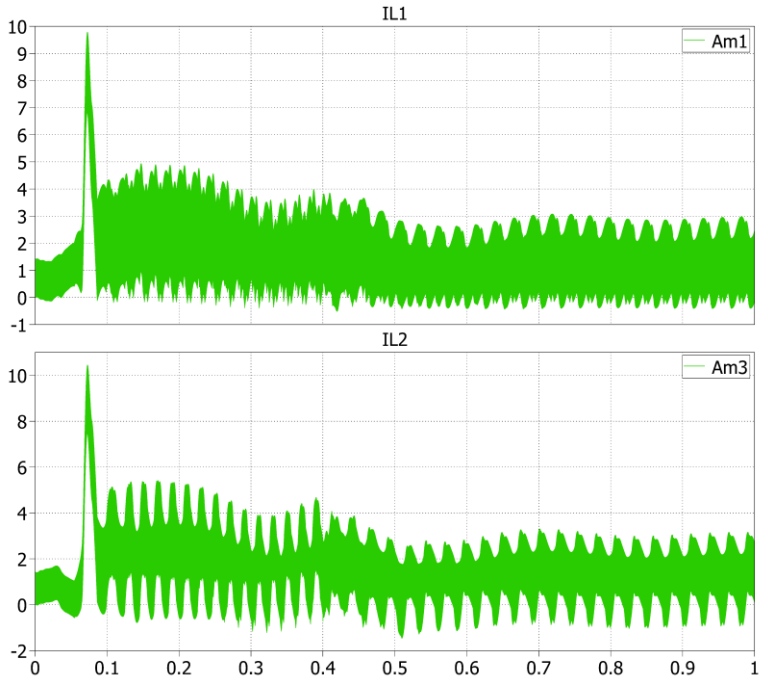

Figure 3.22 Simulated z-impedance inductor current IL_1 and IL_2 for speed reduced with 25%

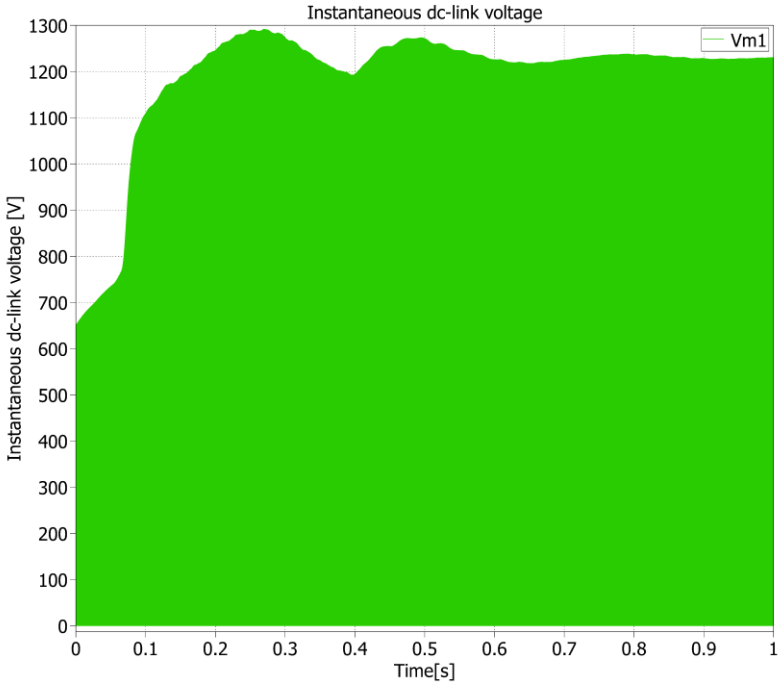

Figure 3.23 Simulated instantaneous dc-link voltage V_i for speed reduced with 25%

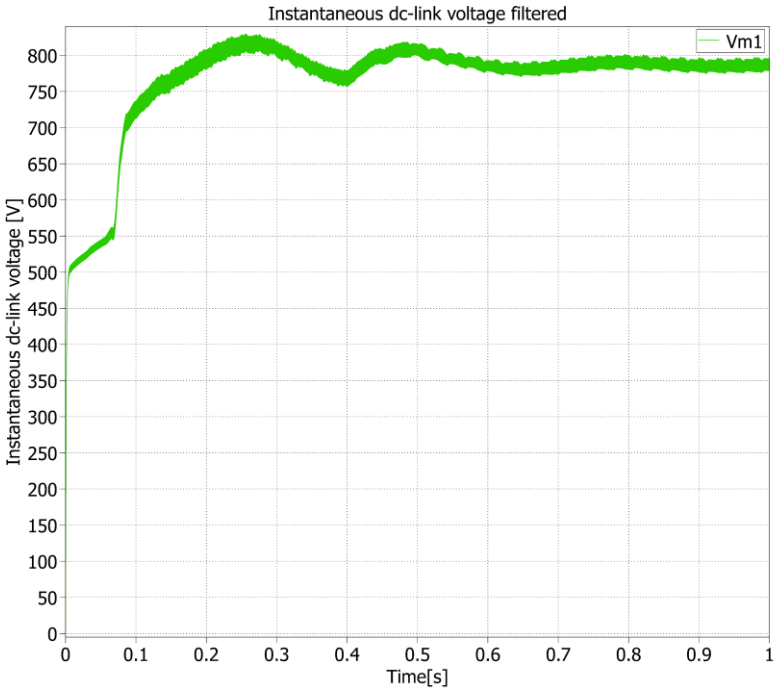

Figure 3.24 Simulated filtered dc-link voltage V_i for speed reduced with 25%

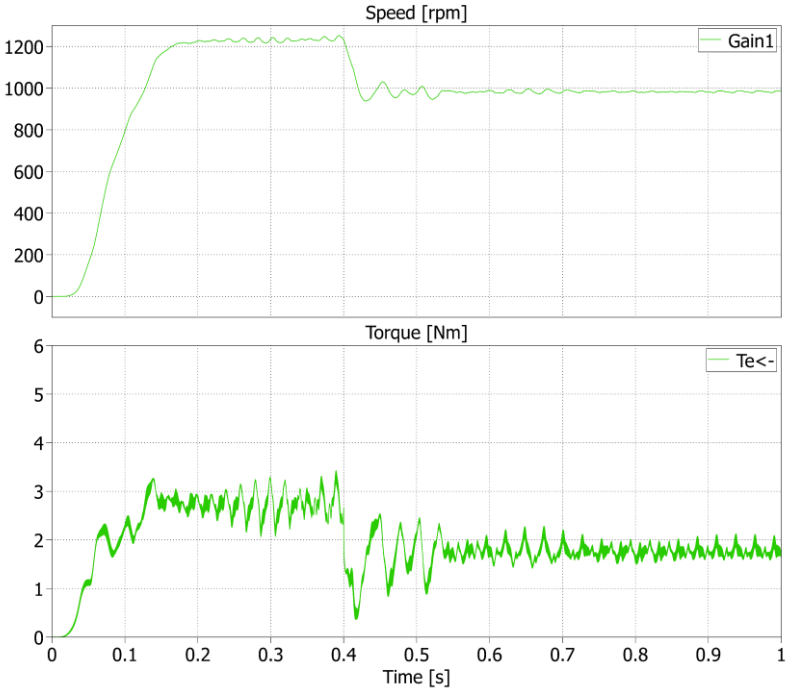

Figure 3.25 Simulated speed ant torque of the 0.5 kW induction machine for speed reduced with 25%

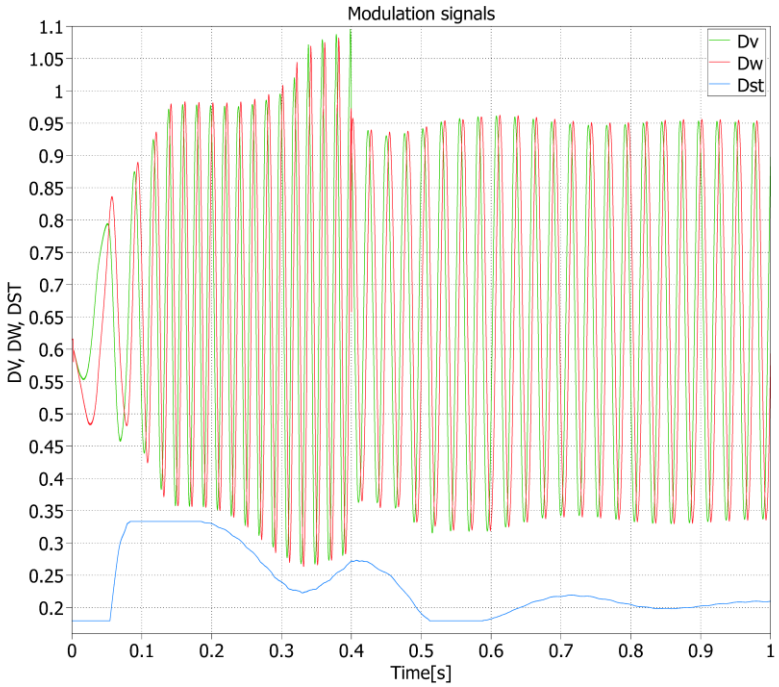

Figure 3.26 Simulated modulation signals D_v, D_W and D_{ST} for speed reduced with 25%

3.4.1 Experimental Results

A laboratory setup was built to validate the proposed four switch Z-source there-phase inverter. The control algorithm based on equations (3.15)-(3.21) was implemented on a TMS 320F28335 digital signal processor from Texas Instruments with a clock frequency of 120MHz. The experimental wave forms are shown in Figure 3.20 – 3.39.

The laboratory Z-Source data are the same as for the digital simulation.

The experimental load currents in Figure 3.28 are close to those from digital simulation (in Figure 3.12) though a bit more asymmetric.

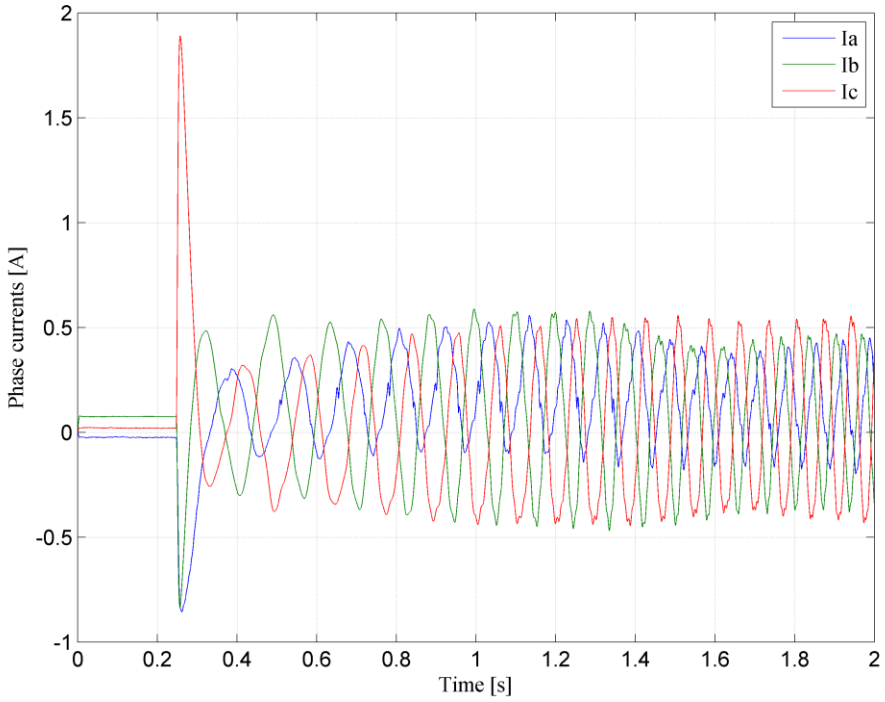

Figure 3.27 Motor stator currents during motor starting from zero to 25Hz rated speed with full ventilator (proportional to speed square) load.

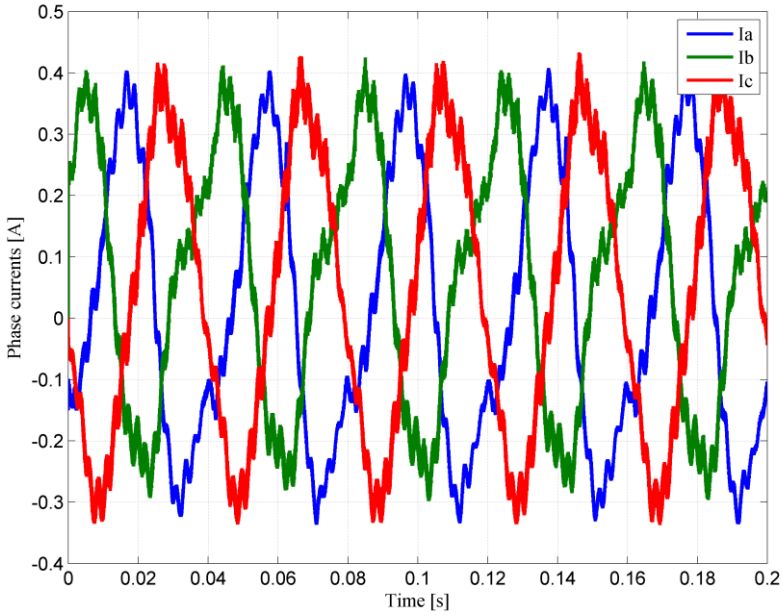

Figure 3.28 The steady state motor stator currents during 25Hz rated speed with full ventilator (proportional to speed square) load

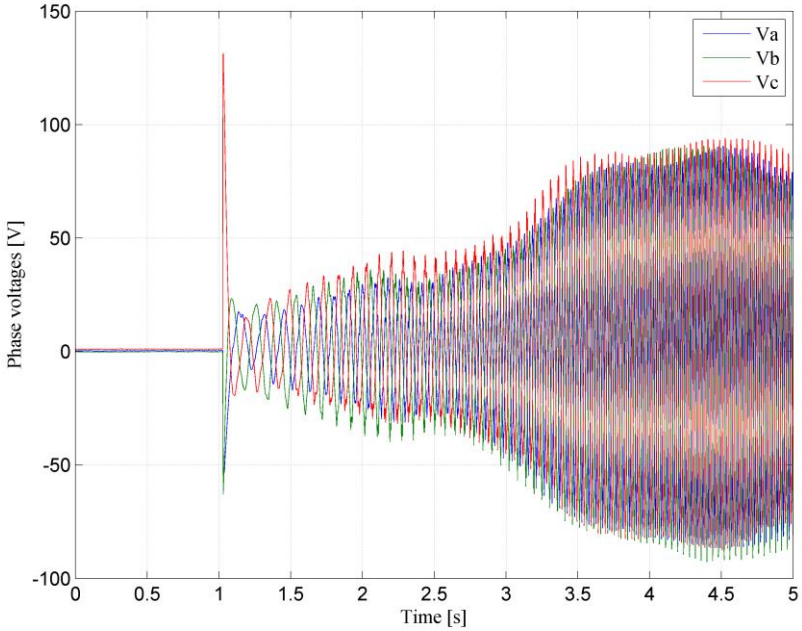

Figure 3.29 The motor voltage filtered with 200Hz low pass filter during motor starting from zero to 25Hz.

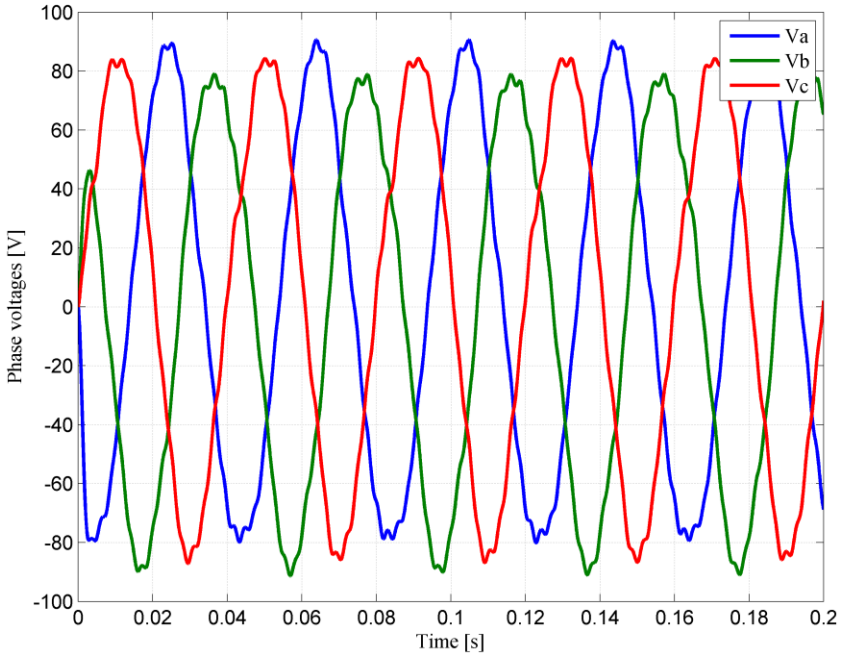

Figure 3.30 The steady state motor voltage filtered with 200Hz low pass filter at 25Hz.

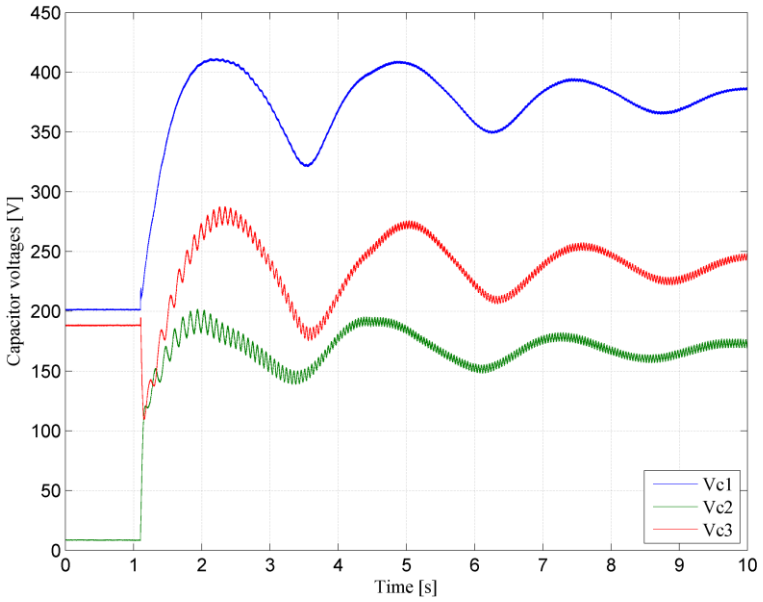

Figure 3.31 The voltage waveforms across C1, C2, C3 during motor starting from zero to 25Hz.

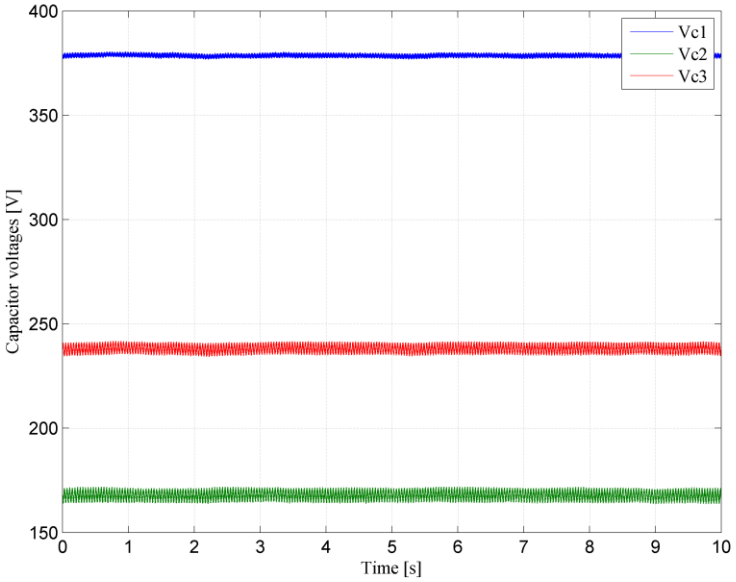

Figure 3.32 The steady state voltages across C1, C2, C3 during motor functioning at 25Hz.

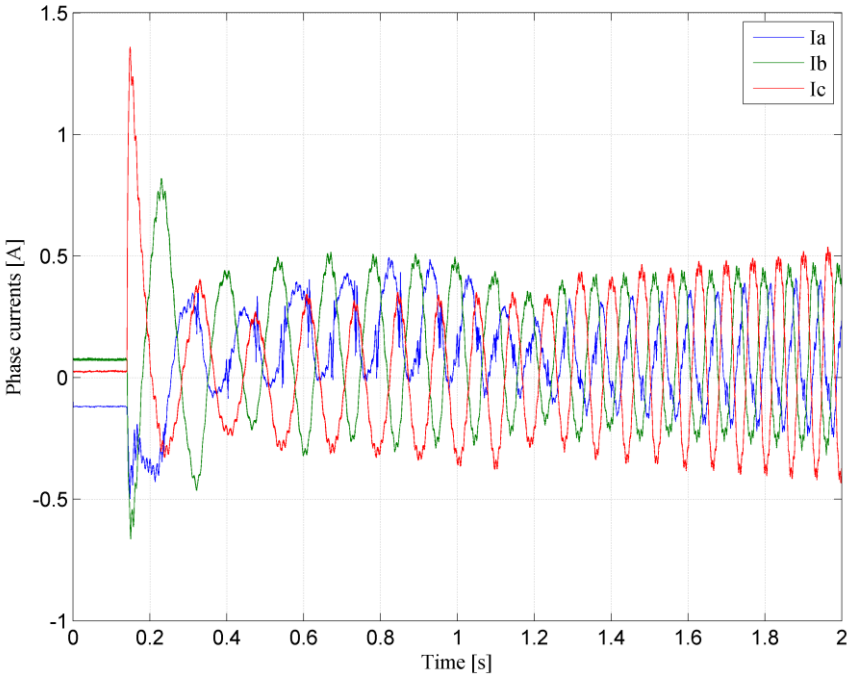

Figure 3.33 Motor stator currents during motor starting from zero to 35Hz rated speed with full ventilator (proportional to speed square) load.

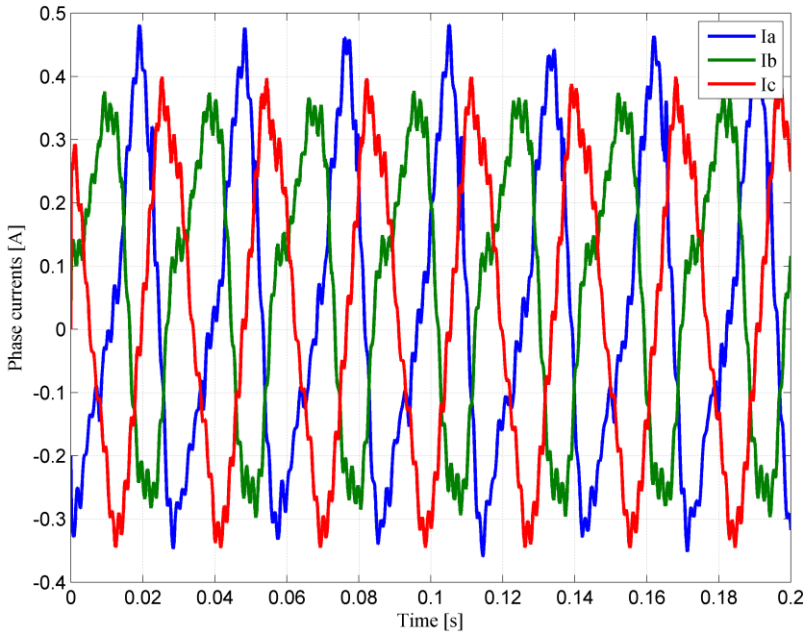

Figure 3.34 The steady state motor stator currents during 35Hz rated speed with full ventilator (proportional to speed square) load

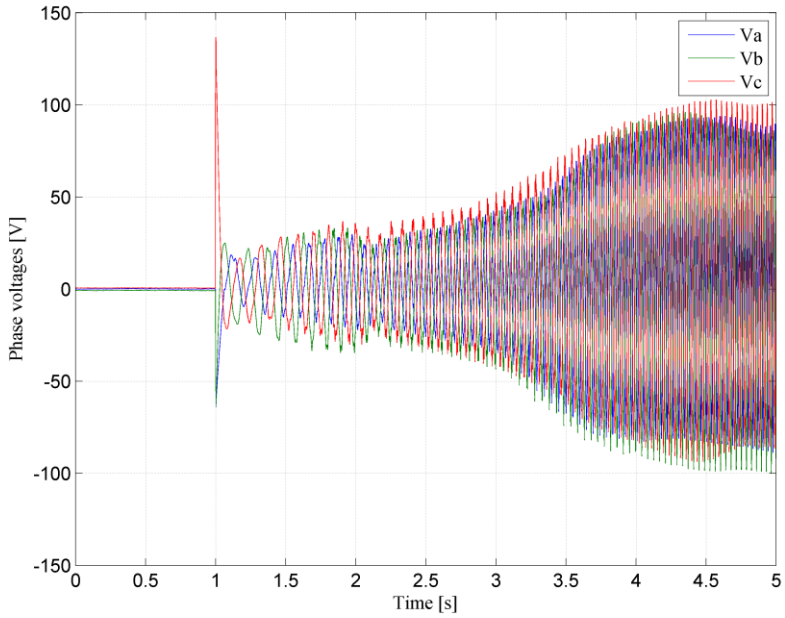

Figure 3.35 The motor voltage filtered with 200Hz low pass filter during motor starting from zero to 35Hz.

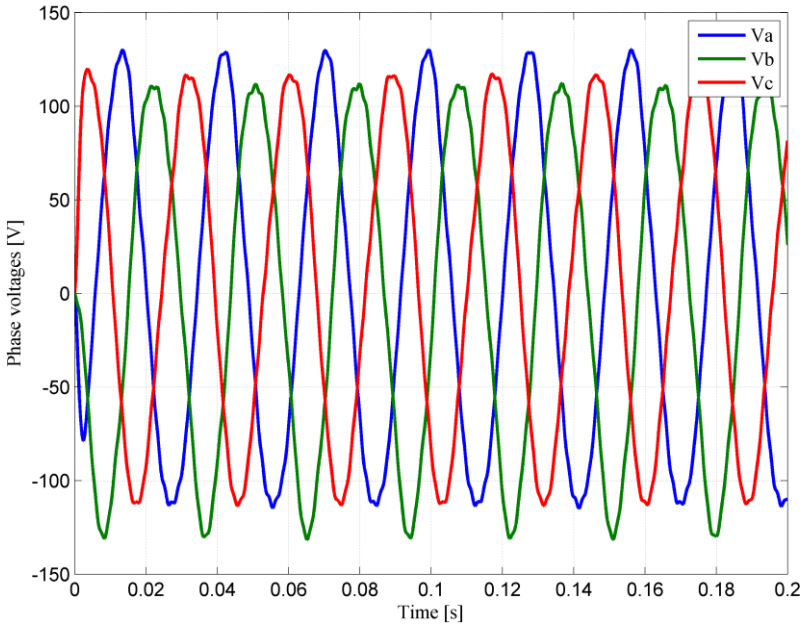

Figure 3.36 The steady state motor voltage filtered with 200Hz low pass filter at 35Hz.

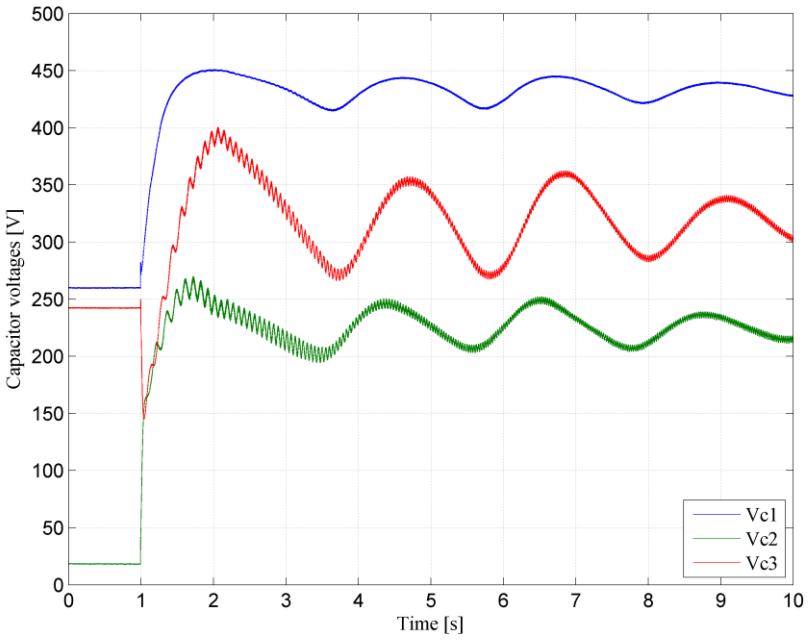

Figure 3.37 The voltage waveforms across C1, C2, C3 during motor starting from zero to 35Hz.

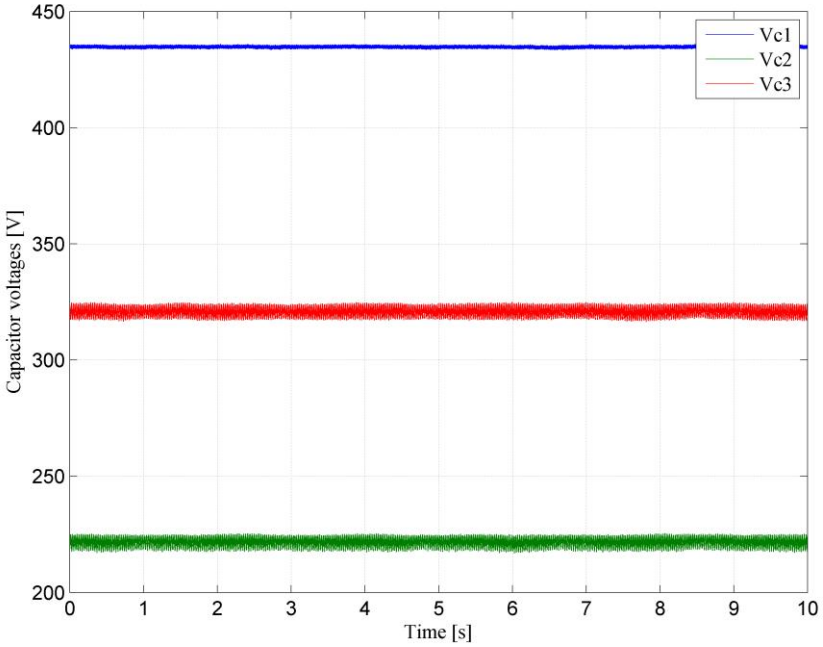

Figure 3.38 The steady state voltages across C1, C2, C3 during motor functioning at 35Hz.

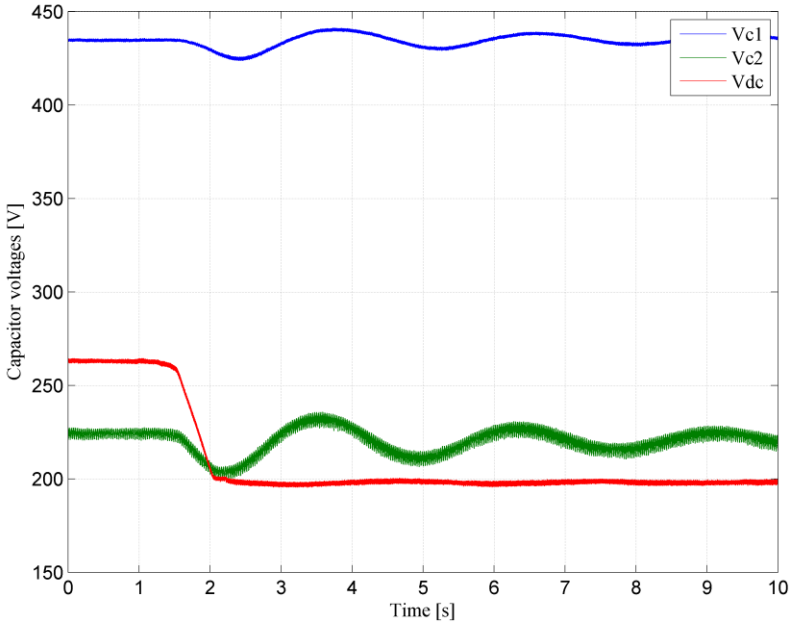

Figure 3.39 The system response during 25% step down in input voltage, at 35 Hz

3.5. Conclusions

This chapter presented the four-switch three-phase z-source inverter with induction machine with full load torque ventilator proportional to speed square.

The algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive has been proposed. The analytical analysis of the proposed algorithm has been verified in simulation and experiments.

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CHAPTER 4 IMPROVED FOUR SWITCH THREE-PHASE Z-SOURCE INVERTER

4.1. Introduction

The improved Z-source inverter was proposed in [1][2] in 2009 is derived from the Z-source inverter presented in [3] and is a single stage buck-boost inverter. The elements used are exactly the same as in the previous one. It consist of the same components: the front end diode, the two port X shaped network form by two identical inductors and two identical capacitors, the six switch inverter bridge and one dc voltage source which it can be a solar panel, fuel cell or the rectified output voltage of a permanent magnet synchronous generator connected to a wind turbine. The difference is that the position of the inverter-bridge and diode is exchanged and their connection direction is reversed, by rearranging the element enhances its properties, Fig 4.1. The two drawbacks which are overcome by the new topology would be:

- the inrush current and the resonance of the Z-source capacitors and inductors at the start-up which could cause failure of the devices
- the high average Z-source capacitor's voltage which is always equal to the average dc-link voltage

Several other current and voltage fed new Z-source topologies to reduce the size of Z-source network and system cost proposed by the same authors can be found in [4].

Simple constant boost control with third harmonic signal injection in the reference sinusoidal signals [5], well-known from the traditional z-source inverter, is used in case of the improved topology in order to increase the modulation index and reduce the voltage and current stress of the inverter bridge.

The feed-forward plus feedback control for the improved Z-source and not only presented in [6] uses only the measured input dc voltage for rough regulation of the shoot through state and the measured peak output voltage is used for load and input voltage variations without taking into account the Z-source network model.

The proposed switched inductor Z-source inverter [7] has a higher voltage gain then the traditional one and the improved Z-source topologies but it has extra diodes and inductors in the Z-source network.

The algorithm to control linearly the capacitor voltage is suggested in [8] in order to improve the transient response for dc boost control of the ZSI. The peak value of the ac output voltage is used to control exactly the ac output voltage to its desired level and a modified space vector pulse-width modulation scheme is applied to control the shoot-through time for boosting dc voltage.

Different operating states (five states) of the Z-source inverter are shown in [9] which depend on the inductance of the Z-source inductor. Even though these states, described by complicated equations, can be considered in the control loop and the size of the Z-source network can be reduced with smaller inductance.

The small signal modeling and mathematical analysis of the improved Z-source inverter are presented in [10]. In particular, the state space averaging method is employed to deduce the transfer functions.

An improved six switch Z-source inverter used to feed and control the speed of an induction motor is presented in [12],[13].

A direct peak dc-link voltage detection method is developed in [14] with a simple sampling circuit, and then controlled directly. Therefore, the constant peak dc-link voltage can be achieved in different input and load conditions. The peak ac output is calculated in real-time by sampling the ac phase voltage, and it is controlled to the desired value without steady-state error. With the proposed direct peak dc-link voltage control and peak ac output control, both the peak dc-link voltage and ac output is controlled to a desired level under different input and load condition.

4.2. Improved Three-Phase Z-Source Inverter

The improved Z-source inverter topology with six switches is shown in Fig 4.1

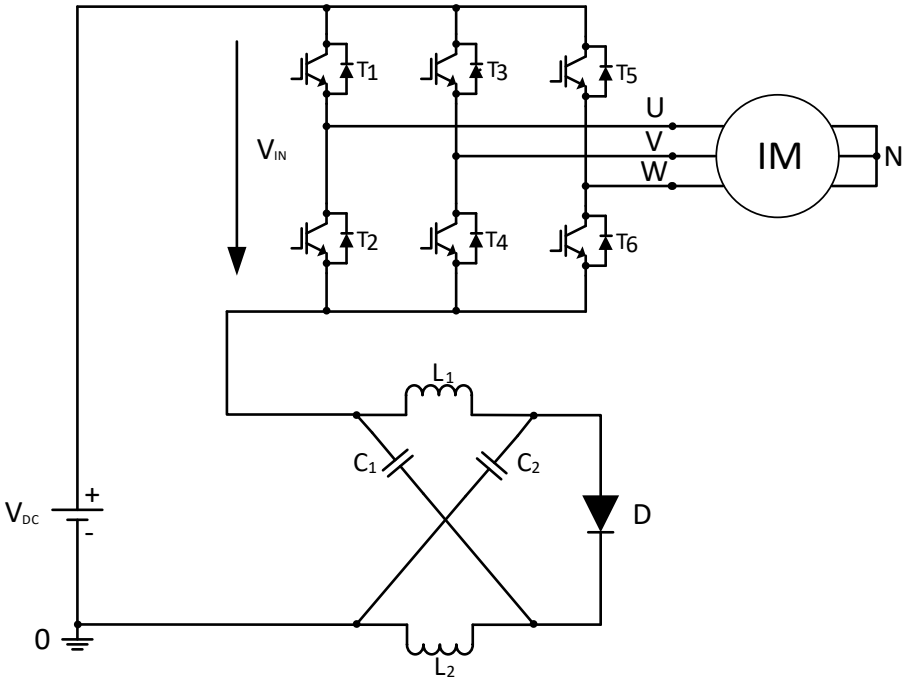

Figure 4.1 Improved Z-source inverter with six switch and induction motor drive

4.2.1 Principle of Operation. Voltage Gain

The improved Z-source topology has two operating states like the traditional Z-source inverter: one shoot-through state generating the desired voltage boost and the one non-shoot-through state when the average dc-link voltage is pulse width

modulated by the inverter bridge. The two equivalent circuits of the two states are show in Fig 4.2.

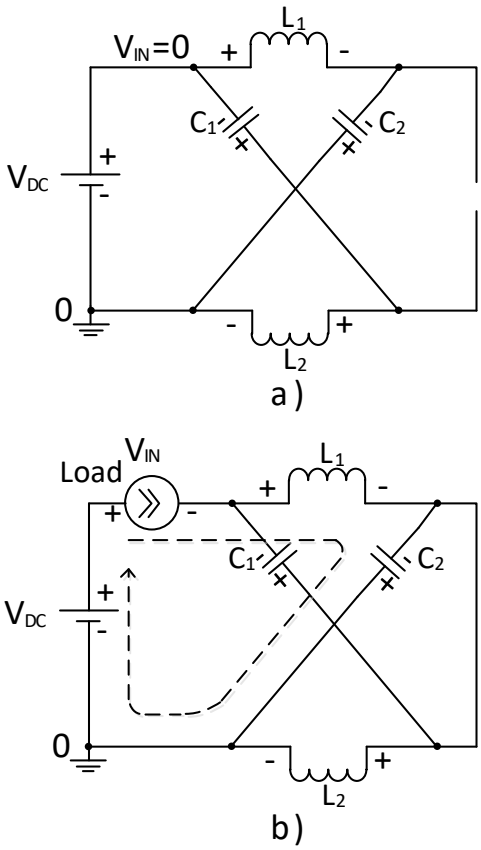

Figure 4.2 Equivalent circuits of the improved Z-source inverter: a) shoot-through state b) non shoot through state

In Fig 4.2 we can see that in both states the voltage across the capacitors changed polarity compared to the traditional Z-source inverter (see chapter 1). In the shoot-through state, the diode stops conducting Fig 4.2a). In the shoot-through state all the switches in the inverter bridge are turned on thus the voltage across the inverter bridge in zero. Writing Kirchhoff's voltage law in the shoot-through state the voltage across the inductor is given by

$$V_L = V_{DC} + \overline{V_C} \tag{4.1}$$

Even through the voltage across the capacitors being zero the voltages across the inductors will be equal with the input voltage and with the polarity of the inductor voltage shown in Fig 4.2a) therefore at the cathode of the diode the voltage potential is $+V_{DC}$ and the anode of the diode is $-V_{DC}$. That is why the diode is not conducting because is inversely polarized.
In the non shoot-through stage the voltage across the inductor can be defined by

$$V_L = -\overline{V_C} \tag{4.2}$$

The non shoot-through state includes the active states as well as the zero voltage states of the inverter bridge.
Through the average voltage across the inductor in steady state during one switching period we get the shoot-thorough duty radio

$$\begin{aligned} \overline{V_L} &= \frac{1}{T_s}\int_0^{T_s} V_L(t) = 0 \\ \overline{V_L} &= \frac{1}{T_s}\left(t_{sT}\left(V_{DC} + \overline{V_C}\right) + \left(T_s - t_{sT}\right)\left(-\overline{V_C}\right)\right) = 0 \\ \overline{V_C} &= \frac{D_{ST}}{1 - 2D_{ST}} V_{DC} \end{aligned} \tag{4.3}$$

In equations (4.3) for zero shoot-through duty ratio the voltage across the capacitor is zero meaning that the voltage across the capacitor can be gradually increased.

As shown in [1] the voltage ripple of the capacitors, the Z-source inductor current ripple, the input current ripple and the inverter bridge peak voltage stress are the same as in case of the traditional Z-source inverter. However, there remains one delicate aspect, which needs further investigation, of the operation in the non shoot-through state: whether the diode is conducting or not in this state. Looking at the currents in the non shoot-through state we can say one thing for sure: the diode is conducting only when the inductor instantaneous current in this state is greater than half the dc-link voltage.

The duty ratio versus the radio of the average capacitors voltage of the Z-source network and the input dc voltage is represented graphically in Fig 4.3.

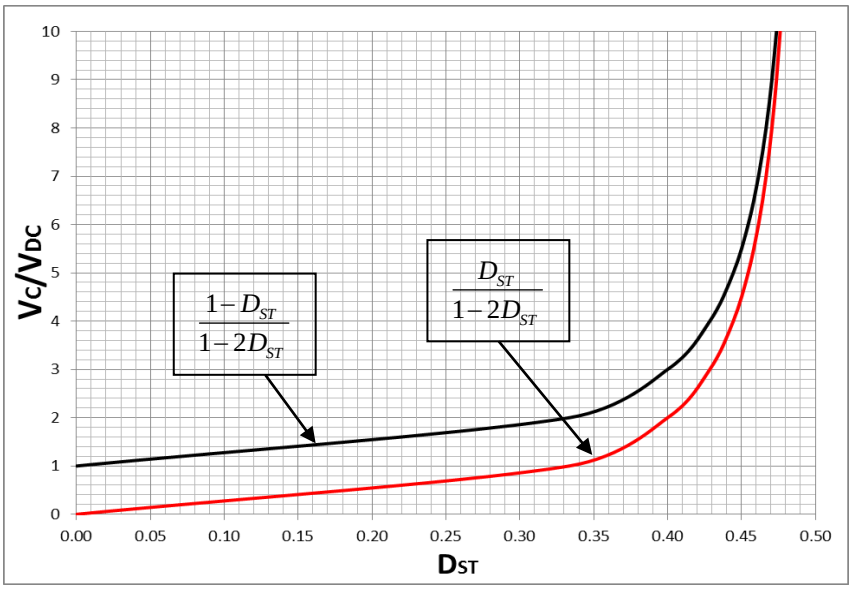

Figure 4.3 V_C/V_{DC} versus D_{ST} for the traditional and the improved Z-source inverter

It can be seen in the Fig 4.3 that the ratio between the average capacitor voltage and the input dc voltage starts from zero or for zero shoot-through duty ratio the capacitor voltage is zero. As a result of the circuit configuration the capacitor voltage can be increased gradually from zero.
The average dc-link voltage is given by (see Fig 4.1)

$$\overline{V_{in}} = V_{DC} + \overline{V_C} + \overline{V_L} \tag{4.4}$$

but the average inductor voltage

$$\overline{V_L} = 0 \tag{4.5}$$

So, the average dc-link voltage, for this improved topology, is greater with the input voltage compared to the average dc-link voltage in traditional Z-source inverter topology

$$\overline{V_{in}} = V_{DC} + \overline{V_C} \tag{4.6}$$

while the average dc-link voltage of the traditional Z-source inverter is the average Z-source capacitor voltage. In other words for the same average dc-link voltage the capacitor voltage stress for the improved topology is lower than for the traditional one thus low voltage capacitors can be used. Still the peak voltage stress across the inverter bridge remains the same.

4.3 Improved Four-Switch Three-Phase Z-source Inverter

The improved Z-source inverter with 6 switches got better properties by the rearrangement of the circuit elements of a traditional Z-source inverter with six switches. One way of the further improved of the characteristics of the Z-source inverters is to reduce the number of switches Fig 4.4. This of course introduces some control difficulties and it has some output limitations but eliminates the cost of two switches and their driver circuits.

4.3.1 Principle of Operation

The improved Z-source inverter with four switches leaves the main elements in the same place as in case of the improved Z-source inverter with six switches. It uses only four switches and the floating load terminal, which was connected to the eliminated inverter leg, is connected at the common point of two capacitors used instead of one of the Z-source network capacitors.

The derivation of the different operating states of the proposed topology and finally the switching times calculation is based on the theory for four-switch three phase inverters presented in [8].

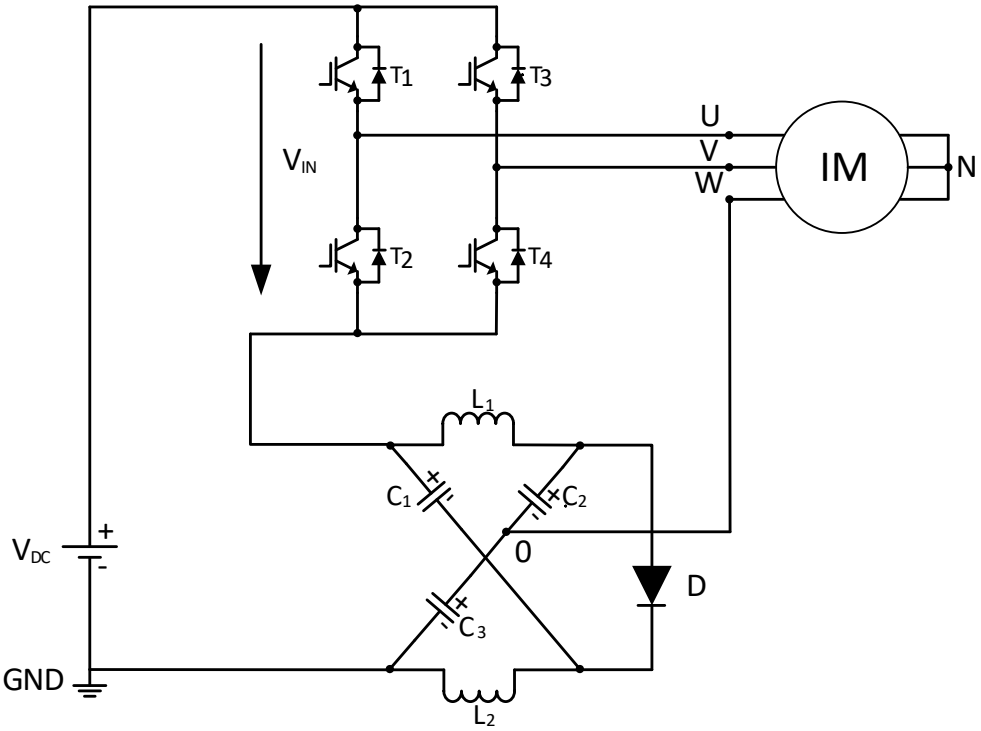

Figure 4.4 Improved Z-source inverter with four switches and induction motor drive

It can be easily demonstrated, by the integration of the voltage across one inductor, that the voltage boost formula (4.3) used at the improved six switch topology is valid for the proposed topology in Fig 4.4 as well. The improved Z-source inverter with four switches has one more operating states, the shoot-through state, compared for the four switch three-phase inverters. The shoot-through state is generated with all the switches on. By interfering in the topology of the Z-source network the shoot-through state become not only a voltage state but also an active state for the inverter at the same time as we will see later. Only the shoot-through state's equivalent circuit will be drawn to point out the duality of this state.

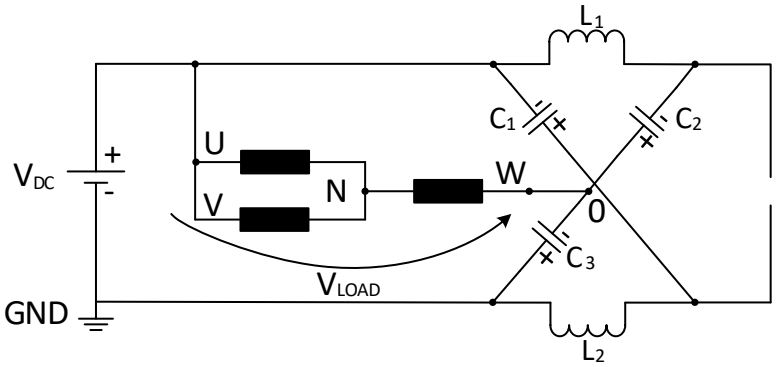

Figure 4.5 Shoot-through state equivalent circuit of the improved Z-source four switch inverter

The load voltage across the load phases is the sum of half the average capacitor voltage and the input dc voltage

$$V_{LOAD} = \frac{\overline{V_C}}{2} + V_{DC} \tag{4.7}$$

4.3.2 Space phasor analysis

For the three-phase load in Fig. 4.4 the voltage space vector can be defined as follows

$$\underline{v}_s = \frac{2}{3}\left(v_{UN} + e^{-j\frac{2\pi}{3}}v_{VN} + +e^{-j\frac{4\pi}{3}}v_{WN}\right) \tag{4.8}$$

where v_{UN}, v_{VN}, and v_{WN} are the instantaneous phase voltages. With the chosen reference potential the common mode of the two capacitors the five possible switching states are illustrated in Table 4.1.

	T_1	T_2	T_3	T_4
S_1	0	1	0	1
S_2	1	0	0	1
S_3	1	0	1	0
S_4	0	1	1	0
S_{ST}	1	1	1	1

0 – switch off
1 – switch on
S_x – switching state

Table 4.1 The five possible switching states

In order to derive the phase voltages we will consider

$$\bar{V}_C = \bar{V}_{C1}; \qquad \bar{V}_{C2} = \bar{V}_{C3} = \frac{\bar{V}_C}{2} \tag{4.9}$$

where $\bar{V}_{C1}, \bar{V}_{C2}$ and $\bar{V}_{C3}$ are the average voltages across C_1, C_2 and C_3 capacitors.
The load terminal voltages referenced to "0" are shown in Fig 4.6 .

The load terminal voltages expressions referenced to "0" for the five switching state

$$V_{V0} = -\frac{3}{2}\overline{V_C}$$

Switching state 1

$$V_{V0} = -\frac{3}{2}\overline{V_C} \qquad (4.10)$$

$$V_{W0} = 0$$

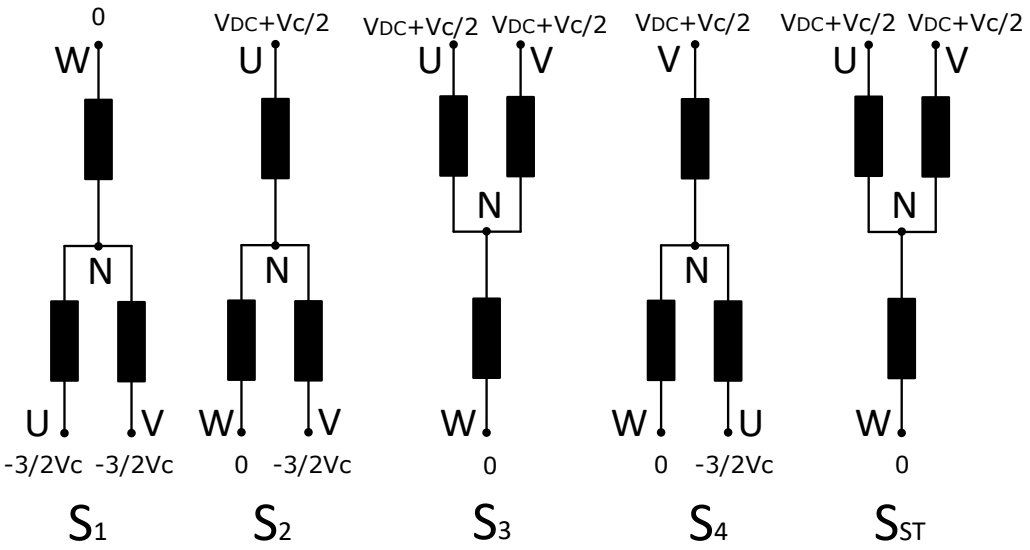

Figure 4.6 Load terminal voltage potentials at different switching states

For a symmetrical balanced wye connected three-phase load the phase voltages can be written as

$$\begin{aligned} v_{UN} &= \frac{2}{3}v_{U0} - \frac{1}{3}(v_{V0} + v_{W0}) \\ v_{VN} &= \frac{2}{3}v_{U0} - \frac{1}{3}(v_{W0} + v_{U0}) \\ v_{WN} &= \frac{2}{3}v_{U0} - \frac{1}{3}(v_{U0} + v_{V0}) \end{aligned} \qquad (4.11)$$

The load terminal to neutral N voltage (the phase voltages) for the five switching states using the voltage potentials in Fig. 4.6 and substituting in into (4.11) can be expressed as

$$V_{UN} = -\frac{\overline{V_C}}{2}$$

Switching state 1

$$V_{VN} = -\frac{\overline{V_C}}{2} \qquad (4.12)$$

$$V_{WN} = +\overline{V_C}$$

Switching state 2

$$\begin{aligned} V_{UN} &= \frac{5}{6}\overline{V_C} + \frac{2}{3}V_{DC} \\ V_{VN} &= -\frac{7}{6}\overline{V_C} - \frac{1}{3}V_{DC} \\ V_{WN} &= \frac{1}{3}\overline{V_C} - \frac{1}{3}V_{DC} \end{aligned} \tag{4.13}$$

Switching state 3

$$\begin{aligned} V_{UN} &= \frac{1}{6}\overline{V_C} + \frac{1}{3}V_{DC} \\ V_{VN} &= \frac{1}{6}\overline{V_C} + \frac{1}{3}V_{DC} \\ V_{WN} &= -\frac{1}{3}\overline{V_C} - \frac{2}{3}V_{DC} \end{aligned} \tag{4.14}$$

Switching state 4

$$\begin{aligned} V_{UN} &= -\frac{7}{6}\overline{V_C} - \frac{1}{3}V_{DC} \\ V_{VN} &= \frac{5}{6}\overline{V_C} + \frac{2}{3}V_{DC} \\ V_{WN} &= \frac{1}{3}\overline{V_C} - \frac{1}{3}V_{DC} \end{aligned} \tag{4.15}$$

Shot-through switching state

$$\begin{aligned} V_{UN} &= \frac{1}{6}\overline{V_C} + \frac{1}{3}V_{DC} \\ V_{VN} &= \frac{1}{6}\overline{V_C} + \frac{1}{3}V_{DC} \\ V_{WN} &= -\frac{1}{3}\overline{V_C} - \frac{2}{3}V_{DC} \end{aligned} \tag{4.16}$$

Note that in the shoot-through state the phase voltage are the same as in state S3.

From the five switching states we will get five voltage space phasors in the complex plane by substituting the three phase voltage expressions from the five switching states (4.12)-(4.16) into the definition of the voltage space phasor (4.8)

$$\begin{aligned} \underline{V_1} &= \left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right)V_C \\ \underline{V_2} &= \left(\frac{5}{6} - j\frac{\sqrt{3}}{2}\right)V_C + \frac{2}{3}V_{DC} \\ \underline{V_3} &= \left(\frac{1}{6} + j\frac{\sqrt{3}}{6}\right)V_C + \left(\frac{1}{3} + j\frac{\sqrt{3}}{3}\right)V_{DC} \\ \underline{V_4} &= \left(-\frac{7}{6} + j\frac{\sqrt{3}}{3}\right)V_C + \left(-\frac{1}{3} + j\frac{\sqrt{3}}{3}\right)V_{DC} \\ \underline{V_{ST}} &= \left(\frac{1}{6} + j\frac{\sqrt{3}}{6}\right)V_C + \left(\frac{1}{3} + j\frac{\sqrt{3}}{3}\right)V_{DC} \end{aligned} \tag{4.17}$$

The relationship between the average capacitor voltage $\bar{V}_C$ and the input dc voltage V_{DC} can be expressed as

$$\bar{V}_C = k \cdot V_{DC} \tag{4.18}$$

$$k = \frac{D_{ST}}{1 - 2D_{ST}}; \quad k > 0 \tag{4.19}$$

Rewriting (4.17) using (4.19) the voltage vectors can be derived as

$$\begin{aligned}
\underline{V_1} &= \left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right) kV_{DC} \\
\underline{V_2} &= \left(\frac{5}{6} - j\frac{\sqrt{3}}{2}\right) kV_{DC} + \frac{2}{3}V_{DC} \\
\underline{V_3} &= \left(\frac{1}{6} + j\frac{\sqrt{3}}{6}\right) kV_{DC} + \left(\frac{1}{3} + j\frac{\sqrt{3}}{3}\right) V_{DC} \\
\underline{V_4} &= \left(-\frac{7}{6} + j\frac{\sqrt{3}}{3}\right) kV_{DC} + \left(-\frac{1}{3} + j\frac{\sqrt{3}}{3}\right) V_{DC} \\
\underline{V_{ST}} &= \left(\frac{1}{6} + j\frac{\sqrt{3}}{6}\right) KV_{DC} + \left(\frac{1}{3} + j\frac{\sqrt{3}}{3}\right) V_{DC}
\end{aligned} \tag{4.20}$$

Notice that in (4.20) the boost factor k influence the amplitude as well the direction of the five voltage vectors.
For k=1 the five vectors in the complex plane are illustrated in fig. 4.7.

The voltage vector generated by the shoot-through state V_{ST} has the same amplitude and direction as the V_3 voltage vector.
The voltage space vector expressed in (4.8) can be rewritten in the complex plane as

$$\underline{v_s} = v_{s\alpha} + v_{s\beta} \tag{4.21}$$

The average voltage space vector over one switching cycle should be equal with the sum of the five average voltage space vectors (V_1, V_2, V_3, V_4 and V_{ST}) over one switching cycle T_S

$$\underline{\bar{v}_s} = \frac{(t_1V_1 + t_2V_2 + t_3V_3 + t_4V_4 + t_{ST}V_{ST})}{T_S} \tag{4.22}$$

Where

$$T_S = t_1 + t_2 + t_3 + t_4 + t_{ST} \tag{4.23}$$

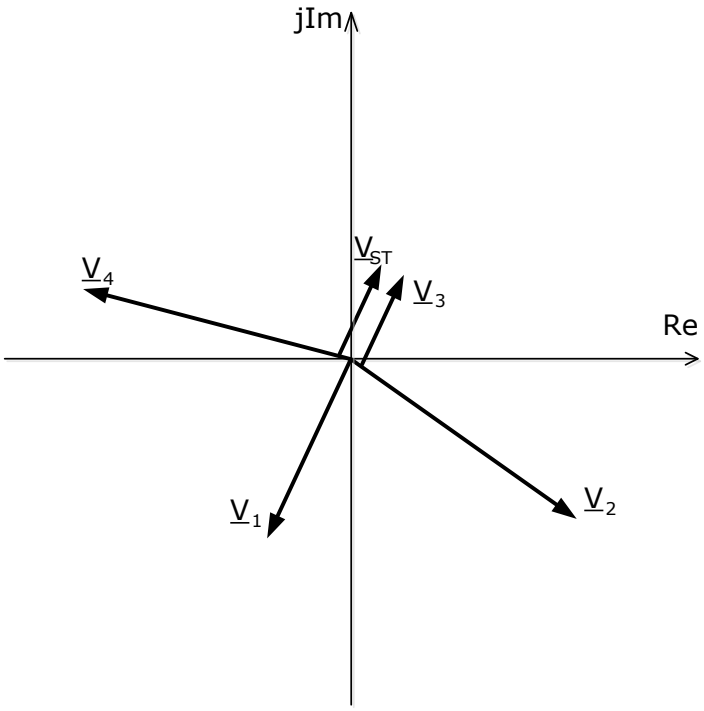

Figure 4.7 Locations of the voltage vectors in the complex plane for k=1

As we could have expected the space voltage phasor corresponding to the shoot-through state and state 3 are identical. Therefore in the complex plane the two space phasors will have the same orientation and amplitude.

Finally the expressions of the v_α and v_β components of a desired voltage space phasor $\underline{v_s}$ using can be given by

$$\begin{aligned} v_\alpha &= \frac{V_{Dc}}{6T_s}\left(2\left(2k+1\right)\left(t_2 - t_1 - 2t_4\right) + T_s\left(k+2\right)\right) \\ v_\beta &= \frac{\sqrt{3}V_{Dc}}{6T_s}\left(2\left(2k+1\right)\left(-t_2 - t_1\right) + T_s\left(k+2\right)\right) \end{aligned} \tag{4.24}$$

With proper control algorithm the desired voltage space-phasor can be generated from the five available in (4.14).

4.4 Control algorithm for DC boost and AC output voltage

The algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the improved four-switch three-phase Z-source inverter feed an induction motor drive is shown in Fig. 4.8.

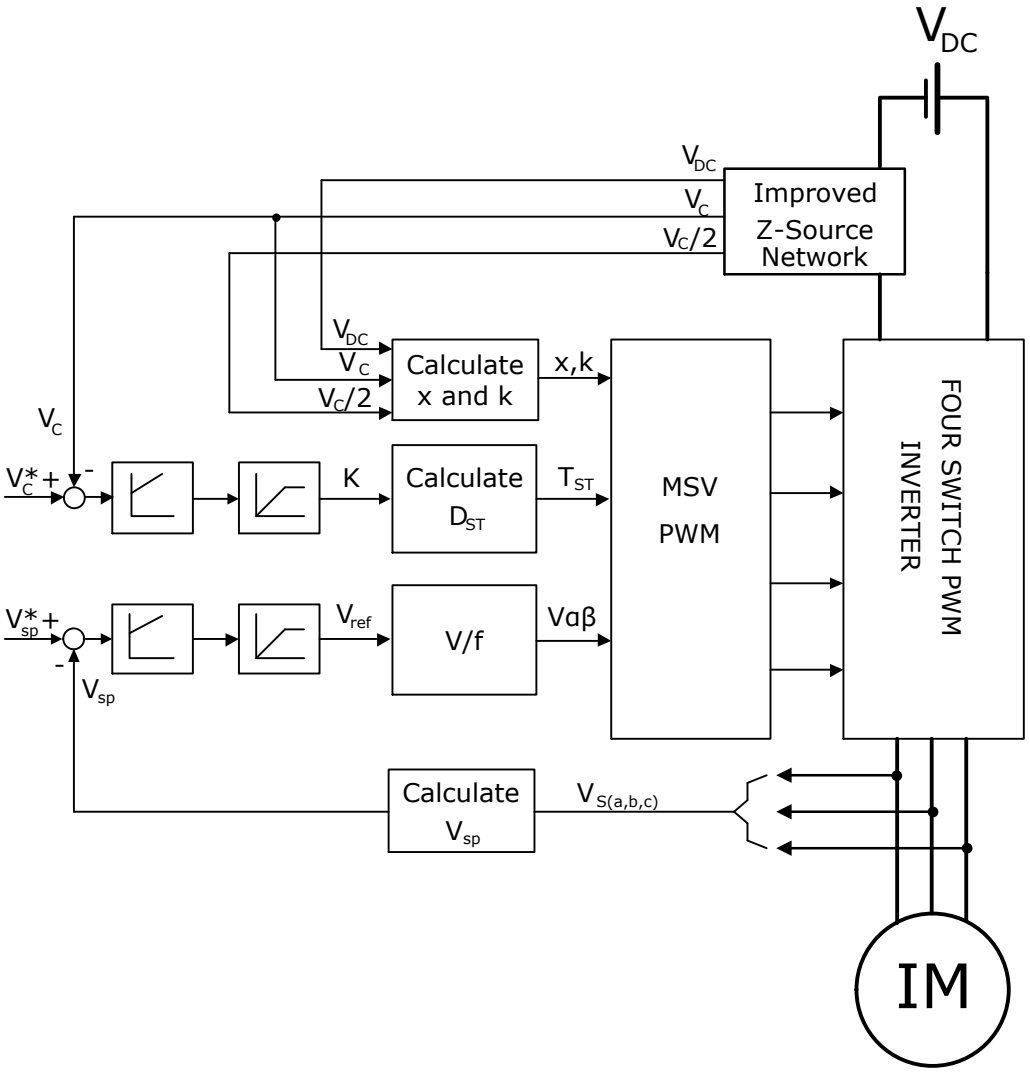

Figure 4.8 Block diagram for voltage control of improved four-switch three-phase Z-source induction motor drive

4.4.1 Control algorithm for DC boost and AC output voltage

The Z-source utilizes the shoot-through state to step up the dc link voltage by conducting both upper and lower switches of any phase legs. Thus, the Z-source inverter can boost the voltage to the desired ac output voltage, which is greater than the available dc link voltage. The capacitor voltage V_C is equivalent to the dc

link shoot- through time duty ratio. Fig. 4.3 shows the relationship between $\frac{V_C}{V_{DC}}$ and the shoot-through time duty ratio D_{ST}. As the relationship has nonlinear characteristics, the shoot-through time cannot linearly control the capacitor voltage.

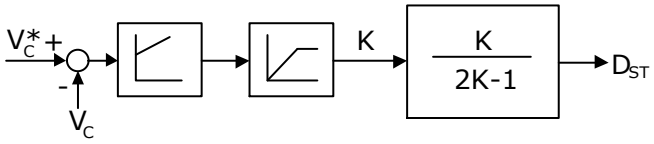

Figure 4.9 Capacitor voltage controller using linearization method

The nonlinearity may deteriorate the transient response of capacitor voltage. In order to overcome the problem, the algorithm for controlling linearly the capacitor voltage is shown in Fig. 4.9. The output of the PI controller of V_C becomes K and can be defined as

$$K = \frac{V_C}{V_{DC}} \tag{4.25}$$

where the K is greater than 0 for stepping up the capacitor voltage. Using (4.19) and (4.25), the shoot-through time D_{ST} is calculated from

$$D_{ST} = \frac{K}{2K-1} \tag{4.26}$$

The output of PI controller of VC becomes K and then the D_{ST} can be calculated from K from (4.26). As the capacitor voltage is linearly controlled by K, the good transient performance of capacitor voltage can be obtained.

4.4.2 AC output voltage control

The ac output voltage is assigned as a feedback signal at the output voltage PI controller, the phase delay between the reference ac output voltage and actual ac output voltage is generated due to the integral component in the PI controller. Instead of ac output voltage, the peak output voltage is used to control the ac output voltage, because the peak output voltage is dc value. After detecting 3-phase line voltages, the 3-phase voltages are transformed into 2-axis voltages in the stationary reference frame, V_{ds}^s and V_{qs}^s, and then the peak output voltage V_{sp} can be derived as follows

$$V_{sp} = \sqrt{\left(V_{ds}^s\right)^2 + \left(V_{qs}^s\right)^2} \tag{4.27}$$

The output of PI controller V_{sp} becomes the reference voltage for V/f speed control. Block diagram for ac output voltage control is shown in Fig. 4.10.

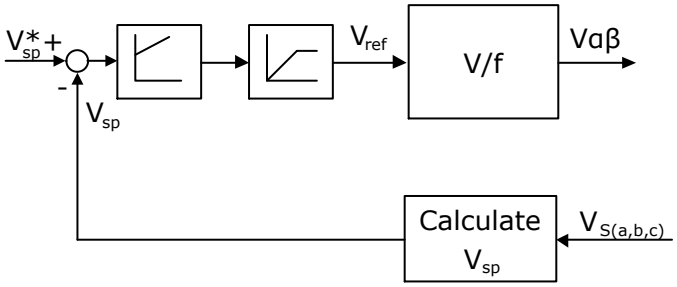

Figure 4.10 Block diagram for ac output voltage control

4.4.3 Split capacitor voltage balance compensation

During the shoot-through state the voltage seen by the load is equal with the voltage across capacitor C_2. This will discharge de C_2 capacitor and move the potential value from the fixed point referenced to the ground of the dc supply, unbalance the split capacitor which affect the inverter performance. To correct this situation the measured voltage on capacitor C_3 and measured k is introduced in vector calculation

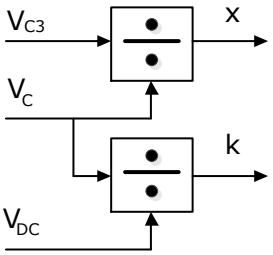

Figure 4.11 Block diagram for voltage balance compensation and boost factor

$$x = \frac{VC_3}{VC} = \frac{1}{2} \tag{4.28}$$

Substituting V_C from (4.18) and using the expression (4.28) the five voltage vectors can be derived as

$$
\begin{aligned}
\underline{V_1} &= \left(-1 - j\sqrt{3}\right) xkV_{DC} \\
\underline{V_2} &= \left(\frac{5}{6} - j\sqrt{3}\right) xkV_{DC} + \frac{2}{3}V_{DC} \\
\underline{V_3} &= \left(\frac{1}{6} + j\frac{\sqrt{3}}{6}\right) xkV_{DC} + \left(\frac{1}{3} + j\frac{\sqrt{3}}{3}\right) V_{DC} \\
\underline{V_4} &= \left(-\frac{7}{6} + j\frac{\sqrt{3}}{3}\right) xkV_{DC} + \left(-\frac{1}{3} + j\frac{\sqrt{3}}{3}\right) V_{DC} \\
\underline{V_{ST}} &= \left(\frac{1}{6} + j\frac{\sqrt{3}}{6}\right) xkV_{DC} + \left(\frac{1}{3} + j\frac{\sqrt{3}}{3}\right) V_{DC}
\end{aligned}
\tag{4.29}
$$

Finally the expressions of the v_α and v_β components of a desired voltage space phasor $\underline{v_s}$ using can be given by

$$
\begin{aligned}
V_\alpha &= \frac{V_{DC}}{3T_s}\left[\left(4xk+2\right)\left(t_2 - t_1 - 2t_4\right) + \left(xk+1\right)T_s\right] \\
V_\beta &= \frac{V_{DC}}{\sqrt{3}T_s}\left[\left(4xk+1\right)\left(-t_1 - t_2\right) + \left(xk+2\right)T_s\right]
\end{aligned}
\tag{4.30}
$$

Given (4.21) – (4.23) and (4.30) calculate the duty ratios for the four transistors and generate the four gating pulses.

Considering $t_4 = 0$ from expression of $V_{S\alpha}$ and $V_{S\beta}$ results the time for vector V_1, V_2, V_3

$$
\begin{aligned}
t_1 &= \frac{2T_s\left(V_{DC}\left(xk+1\right) - \sqrt{3}V_\beta\right)}{2\left(4xk+1\right)V_{DC}} - \frac{T_s\left(3V_\alpha - \sqrt{3}V_\beta\right)}{2\left(4xk+1\right)V_{DC}} \\
t_2 &= \frac{\sqrt{3}T_s\left(\sqrt{3}V_{\alpha} - TV_\beta\right)}{2\left(4xk+1\right)V_{DC}} \\
t_3 &= \frac{T_s\left(3xkV_{DC} + \sqrt{3}V_\beta\right)}{\left(4xk+1\right)V_{DC}} - \frac{T_s k}{2k+a}
\end{aligned}
\tag{4.31}
$$

The duty ratios D_V and D_W to generate the two complementary signals for the two phase legs of the inverter bridge and the D_{ST} for the shoot-trough signal are

$$
\begin{aligned}
&D_U = 1 - D_1 = D_{ST} + D_3 + D_2 = D_V + D_2 \\
&D_V = D_{ST} + D_3 \\
&D_{ST} = \frac{t_{ST}}{T_S} = \frac{K}{2K-1} \\
&D_U = \frac{6xkV_{DC} + 3V_{s\alpha} + \sqrt{3}V_\beta}{2(4xk+1)V_{DC}} \\
&D_V = \frac{3xkV_{DC} + \sqrt{3}V_\beta}{(4xk+1)V_{DC}}
\end{aligned}
\tag{4.32}
$$

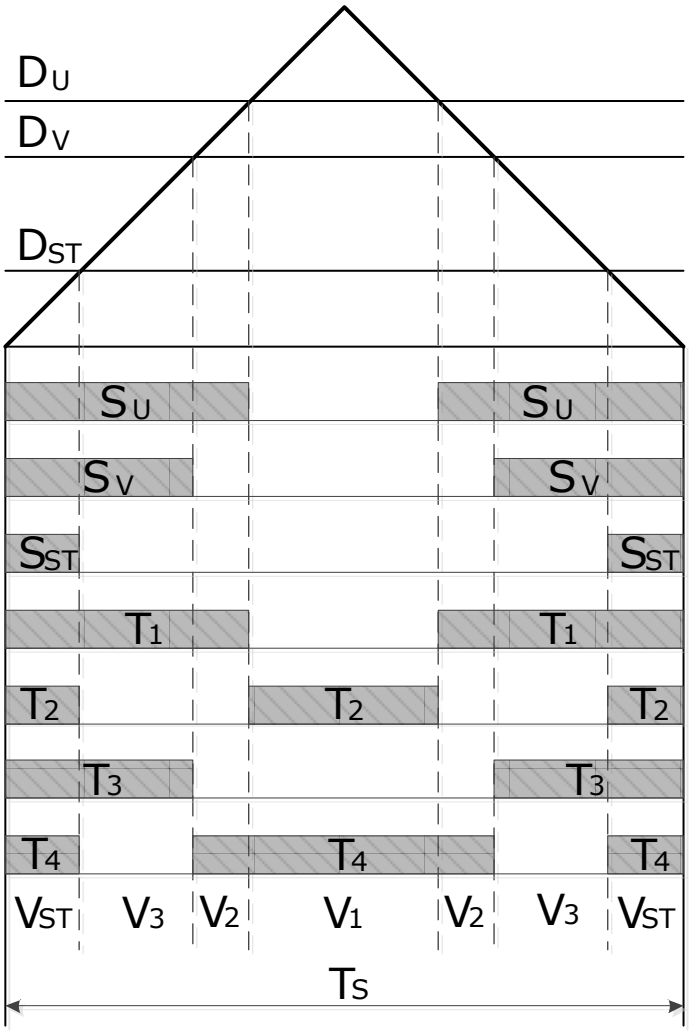

Figure 4.12 PWM signal waveform generation for T_1, T_2, T_3 and T_4

4.5 Simulation Results

The improved four switch three-phase z-source inverter with induction machine drive and its control algorithms was simulated to validate the theory. In order to verify the peak dc-link voltage control strategies, simulations are carried out using PLECS software for a 0.5 kW induction motor using parameters in Table 4.2 and for four switch three-phase Z-source inverter network in Table 4.3.

Parameter	Value
Output power	0.5kW
RMS line voltage	400 V
Input frequency	50Hz
No. of poles	4
Stator resistance, R_s	16 Ω
Rotor resistance, R_r	18.5 Ω
Stator leakage inductance, L_{ls}	0.043 Ω
Rotor leakage inductance, L_{lr}	0.043 Ω
Mutual inductance, L_m	0.585 Ω
Moment of inertia, J	0.001 kg·m^2
Rated dc input voltage	200Vdc

Table 4.2 0.5 kW induction motor parameters

Z-SOURCE NETWORK PARAMETERS

Parameter	Value
Capacitors	235μF
Inductors	6.4mH
Inductors resistance	0.9Ω

Table 4.3 Z-source network parameters

Figures 4.13 – 4.21 show the simulation results for V/f control of a 0.5 kW induction motor fed by a improved four switch three-phase z-source inverter. Figure 4.13 and Figure 4.14 expose the stator current during motor starting from zero to rated speed with full load torque is proportional to speed square, Figure 4.15 shows the motor filtered voltage during motor starting from zero to rated speed, Figure 4.16 illustrates the capacitor voltage, the split capacitor voltages and the dc input voltage. Figure 4.17 shows the Z-impedance inductor current I_{L1} and I_{L2}. Figure 4.18 and Figure 4.19 shows the instantaneous and filtered dc-link voltage V_i. Motor speed ant torque of the 0.5 kW induction machine are illustrated in Figure 4.20. Figure

4.21 shown modulation signals D_V, D_W and D_{ST} for the four-switch three-phase improved Z-source inverter.

The machine accelerates to 50 Hz with speed squared proportional load torque in 0.15, seconds peaks while the capacitor voltage is boosted at 500 V Figure 4.13-4.21; also the inductor current Figure 4.17 which is divided between the two inverter legs does not warrant oversizing of the standard inverter.

As we can see in Figure 4.18 and Figure 4.19 the dc-link voltage is not equal anymore to the average C_1 voltage as in the case of the traditional Z-source inverters. Thus for the same voltage boost a higher average input dc-link voltage can be obtained.

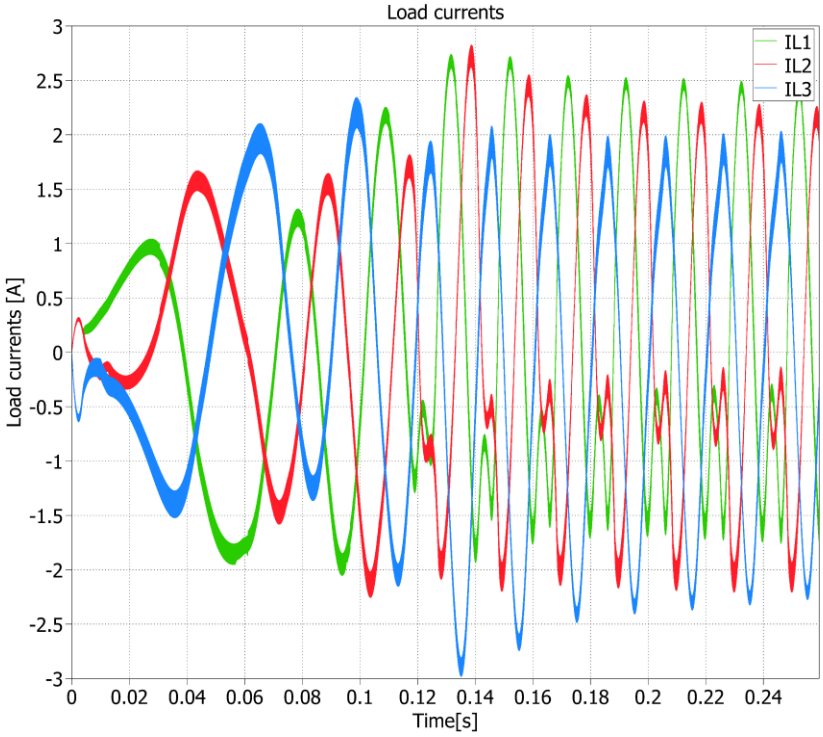

Figure 4.13 Simulated load currents at start-up

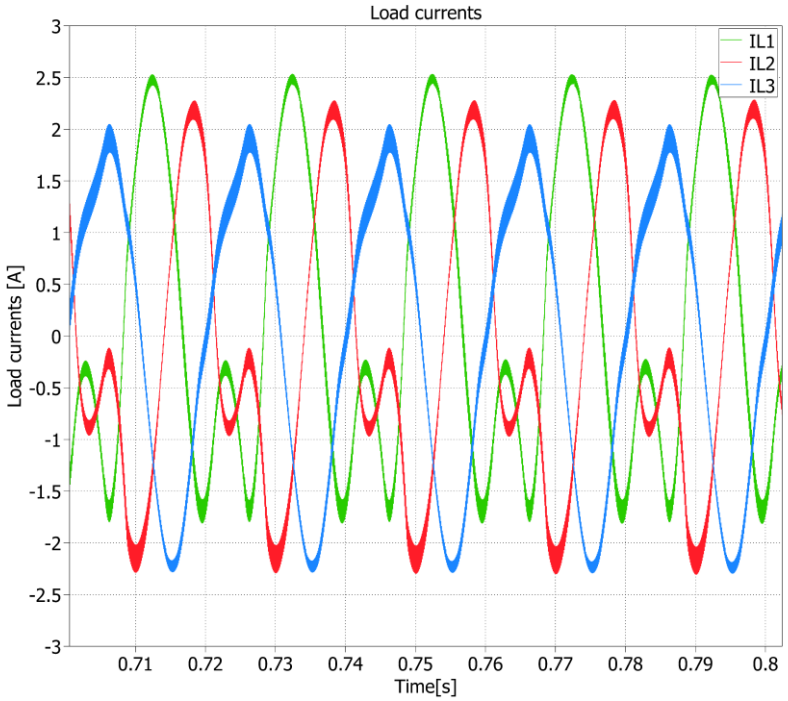

Figure 4.14 Simulated load currents (zoom)

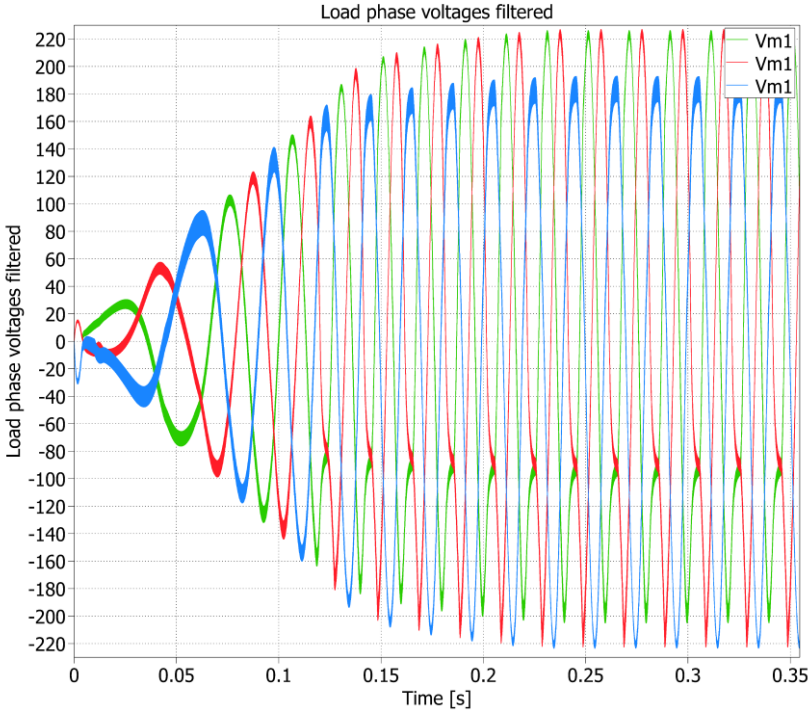

Figure 4.15 Simulated filtered phase voltages

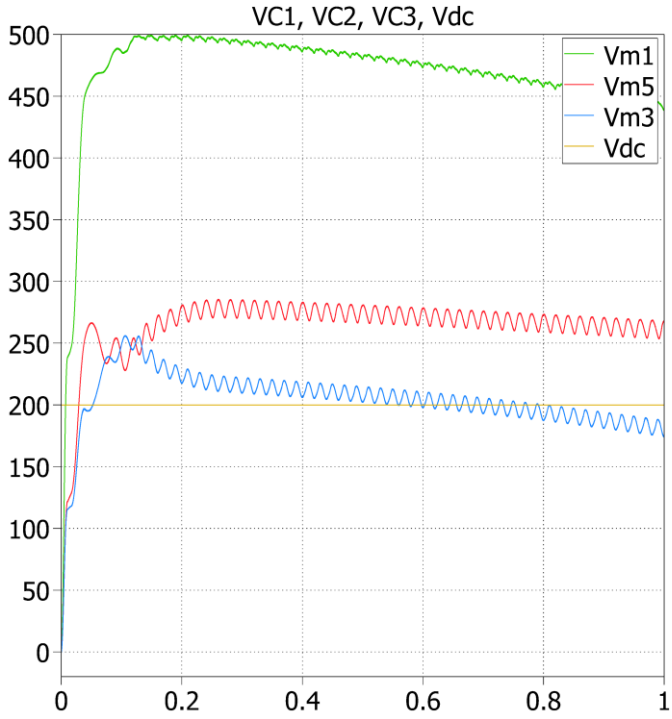

Figure 4.16 Simulated voltage waveforms across C_1, C_2, C_3 and the input dc voltage

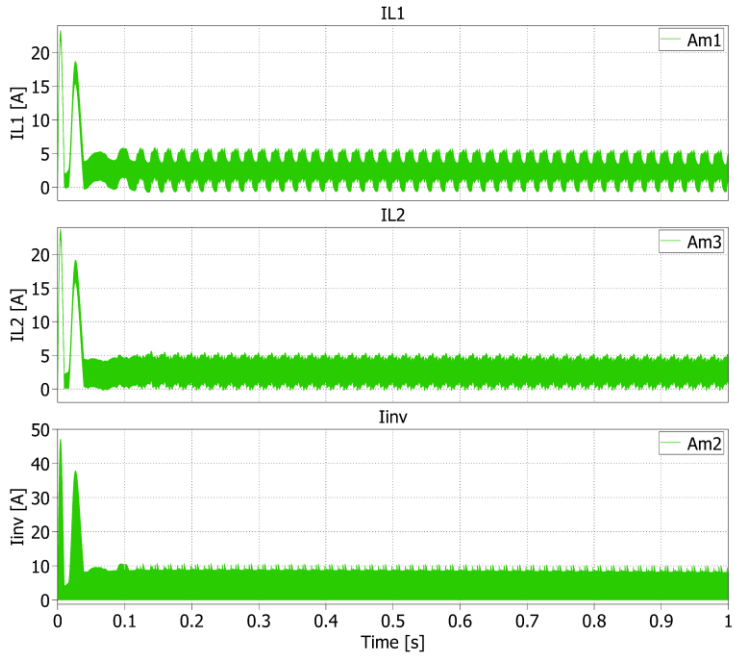

Figure 4.17 Simulated z-impedance inductor current I_{L1}, I_{L2} and inverter current

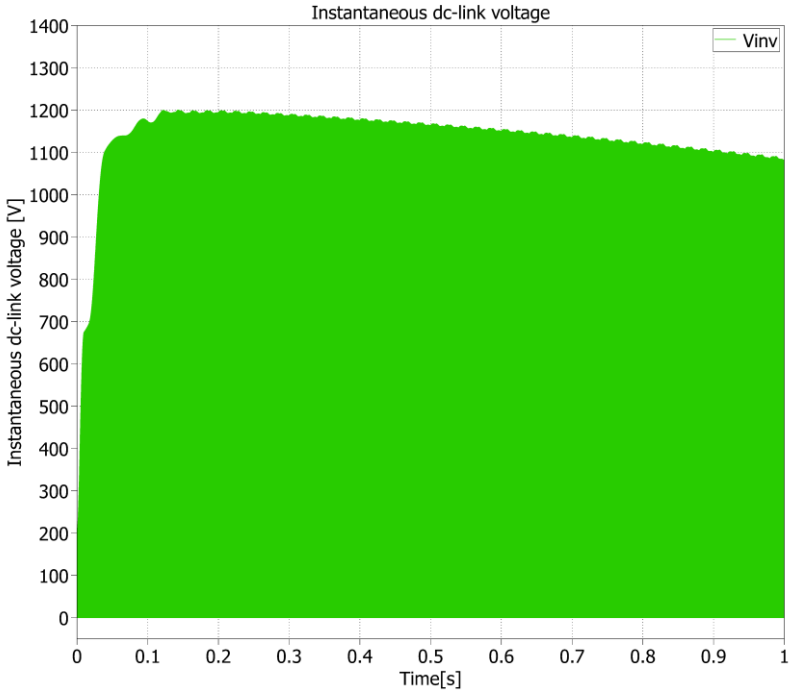

Figure 4.18 Simulated instantaneous dc-link voltage V_i

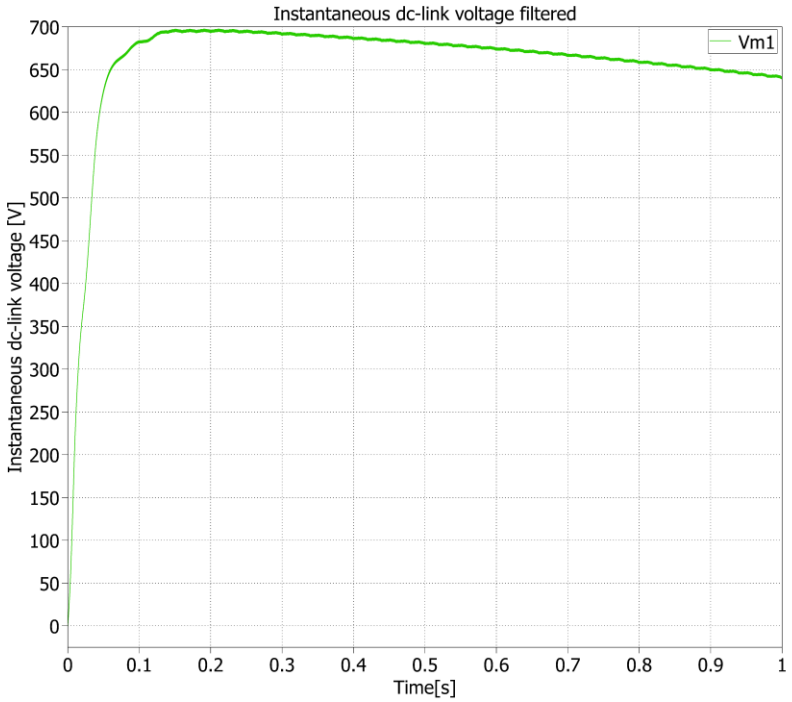

Figure 4.19 Simulated filtered dc-link voltage V_i

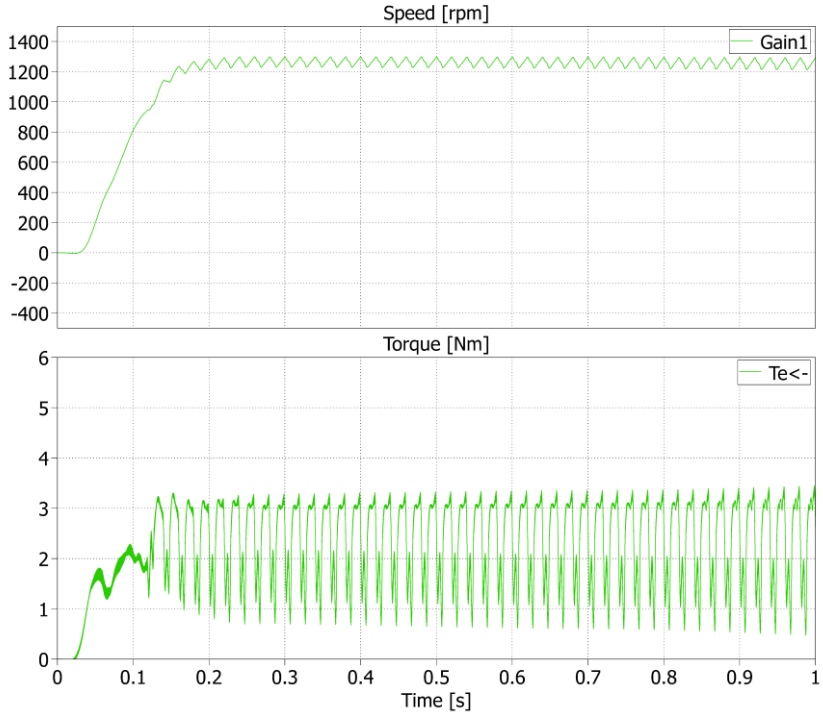

Figure 4.20 Simulated speed ant torque of the 0.5 kW induction machine

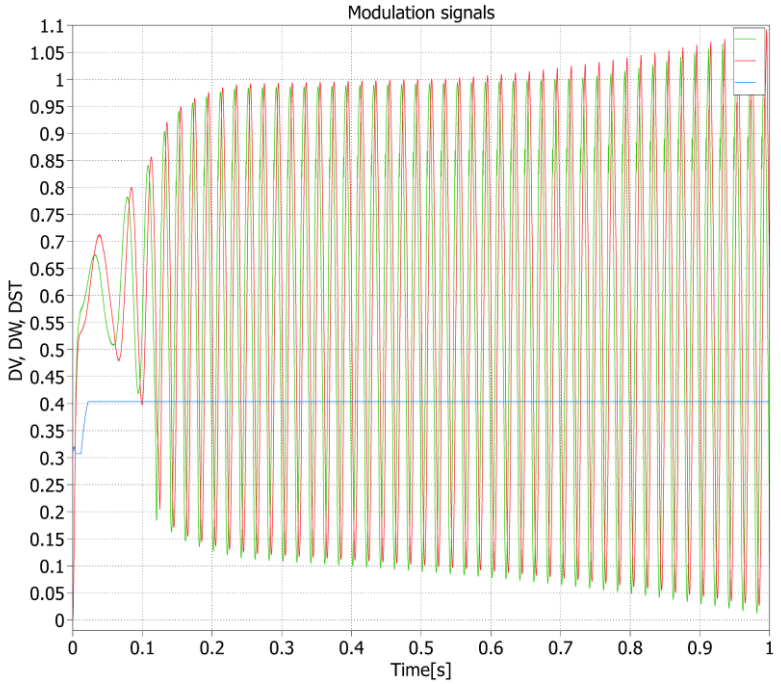

Figure 4.21 Simulated modulation signals D_v, D_W and D_{ST}

4.5.1 Experimental Results

A laboratory setup was built to validate the proposed improved four switch Z-source there-phase inverter. The control algorithm based on equations (4.28)-(4.32) was implemented on a TMS 320F28335 digital signal processor from Texas Instruments with a clock frequency of 120MHz. The experimental wave forms are shown in Figure 4.22 – 4.25.

The laboratory Z-Source data are not exactly as in simulation and a further work is needed.

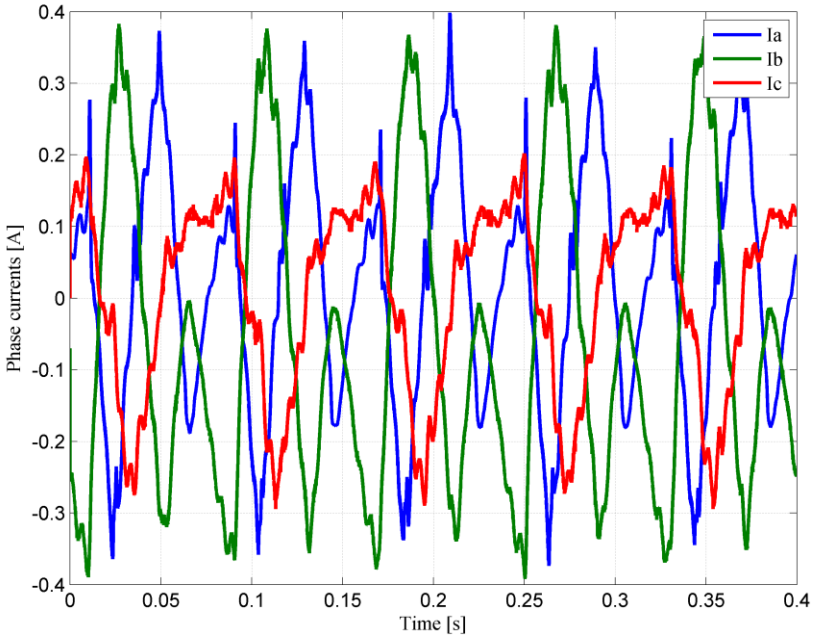

Figure 4.22 The steady state motor stator currents during 12.5Hz rated speed with full ventilator (proportional to speed square) load

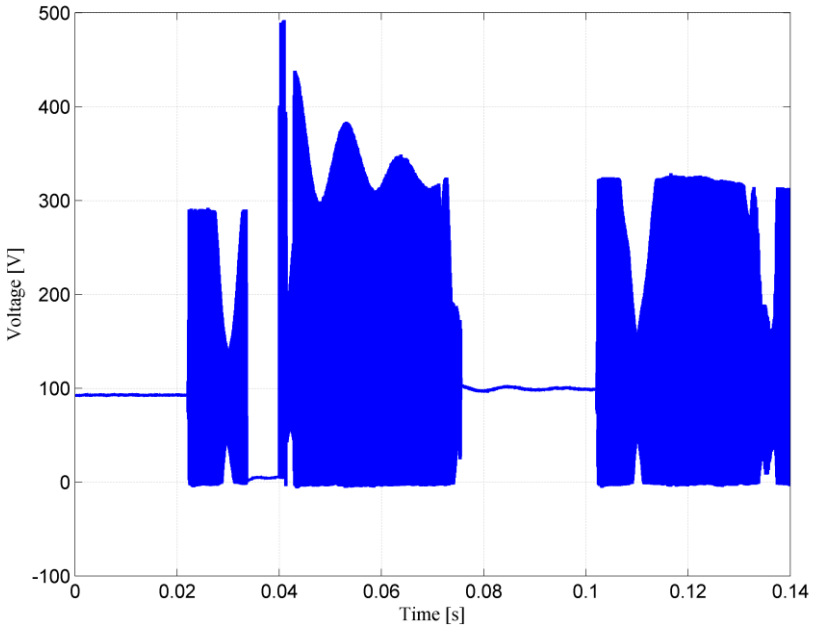

Figure 4.23 The instantaneous dc-link voltage Vi

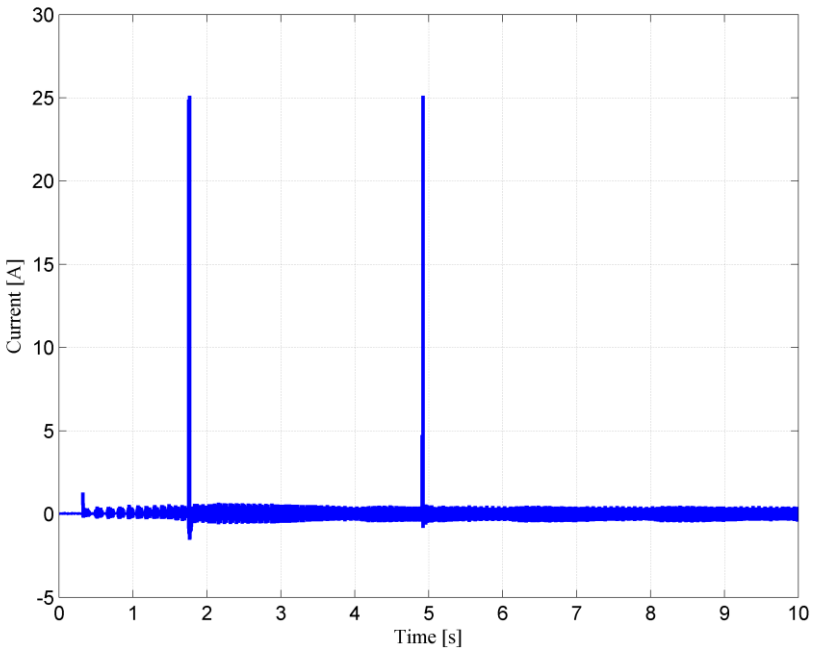

Figure 4.24 The current trough Z-source network diode.

4.6 Conclusions

This chapter presented the improved four-switch z-source three-phase inverter with induction machine with full load torque is proportional to speed square.

The algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the improved four-switch three-phase Z-source inverter feed an induction motor drive has been proposed. The proposed algorithm has been verified in simulation and the experimentally results needs further work and study.

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CHAPTER 5 EXPERIMENTAL SETUP

The experimental setup of the four switch three phase Z-source inverter for induction motor drive is presented in Figure 5.1. The hardware system contains a personal computer, a digital control system with a Digital Signal Processor (DSP), a ZSI and other hardware. Its components are:

1. The personal computer (PC) accomplishes two functions: software development for the four switch three phase Z-source inverter for induction motor drive and monitoring and data acquisition. For software development, firmware software tools (compilers, debuggers and IDE-s) have been used.
2. The eZdsp F28335 board contains the TMS320F28335 DSP from Texas Instruments. It is a floating-point, 32-bit DSP with Harvard architecture, powered at 120 MHz clock frequency, 68K bytes on-chip RAM, 512K bytes on-chip Flash memory, 256K bytes off-chip SRAM memory, on chip 12 bit Analog to Digital (A/D) converter with 16 input channels. This subsystem is responsible for the realization of the control algorithms, sampling period generation, and for PWM generation. Programs for this platform were developed in C language and in assembler. The communication between the PC and TMS is realized on the USB interface using the Code Composer IDE from Texas Instruments.
3. The eZdsp EXM contains the ZSI interface and the signal conditioning module.
4. The driver board contains four 2.5 Amp gate drive optocoupler with integrated desaturation (VCE) detection and fault status feedback HCPL-316J drivers. The driver board receives the four switching signals from the EXM module trough a fiber optics interface.
5. The Z-source Inverter is an open architecture inverter based on a BSM 15 GD 120 D2 IGBT Power Module 1200v V_{CE} and 25A I_C, 3-phase full-bridge including fast free-wheel diodes packaged with insulated metal base plate. It is operated at 10 kHz switching frequency.
6. The voltage sensors board contains three LV 25-P voltage transducers using the Hall effect.
7. The induction machine nameplate data are:
   - Producer: Electromotor
   - Type: 5MP
   - P_N=0.15kW
   - U_n=380V, Y I_n=0.53A
   - U_n=220V, Δ I_n=0.91A
   - f_N=50Hz
   - n_N=2890rpm
   - cosφ=0.67
   - Rotor: squirrel cage

This architecture is powerful and flexible and allows modular software development. In normal operation, two programs run simultaneously: one on the DSP platform and one on the PC. The DSP system operates stand-alone and runs the drive algorithm. The PC is the system's supervisor and runs the user interface.

The DSP executes the acquisitions and control algorithms which implements the SWM and controls the ZSI by sending the modulation signals to drivers.

The software package developed for the four switch three phase Z-source inverter for induction motor drive contains the ZSI drive project. It is developed in C++ language and assembler for the eZdsp F28335 platform and implements the proposed control algorithm for the real drive. The program is based on object-oriented technology. This code is developed for stand-alone, real-time execution.

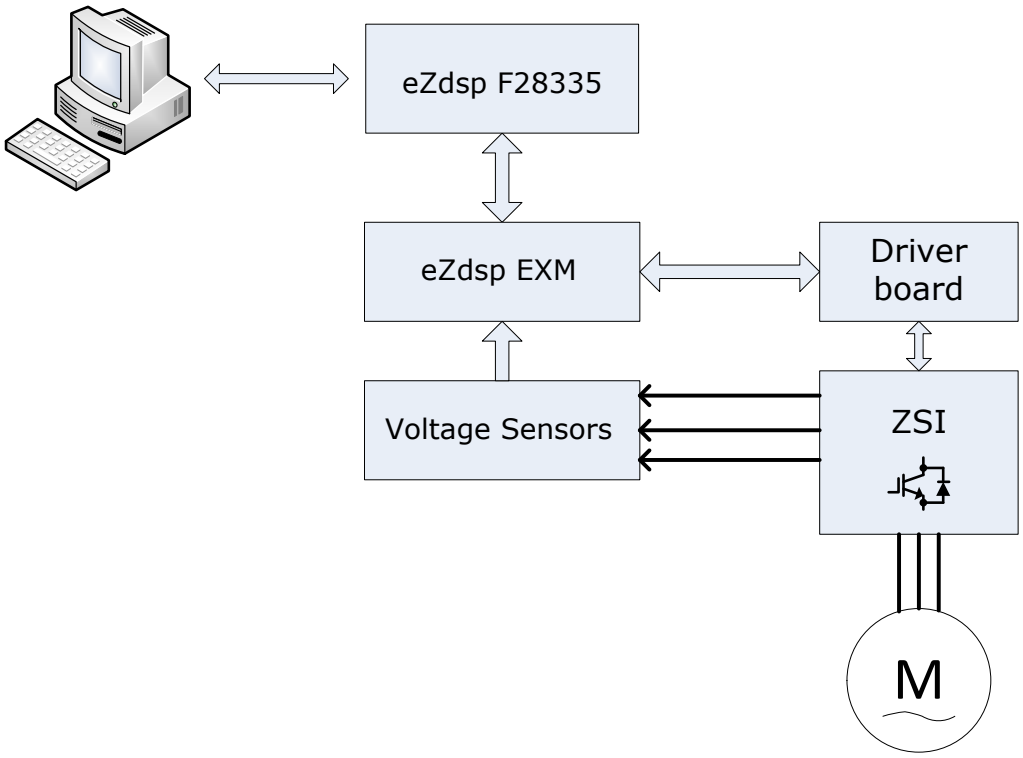

Figure 5.25 Experimental setup of the four switch three phase Z-source inverter for induction motor drive.

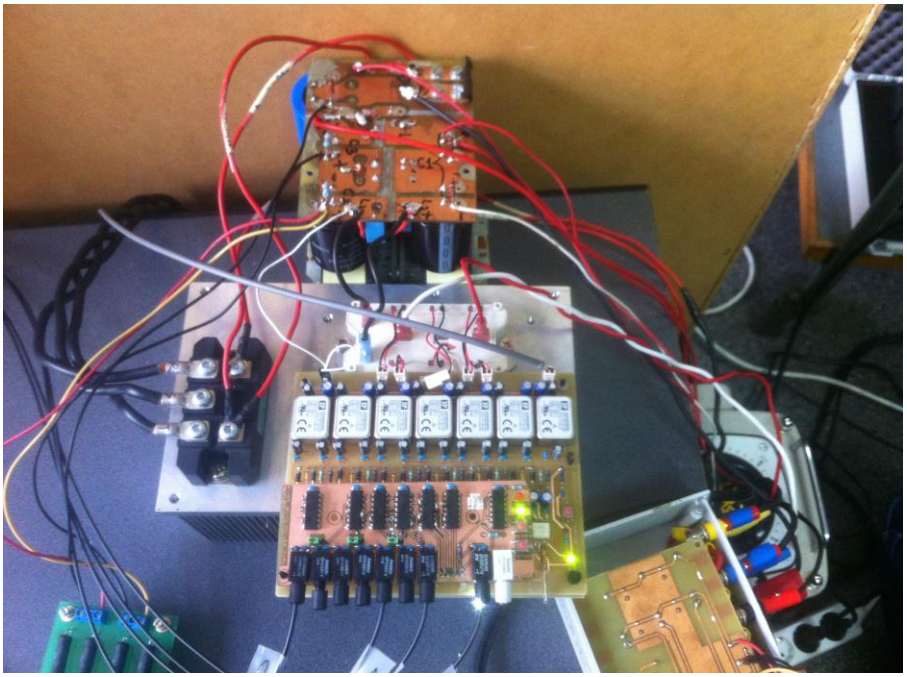

Figure 5.26 Z-source network and inverter bridge with drivers.

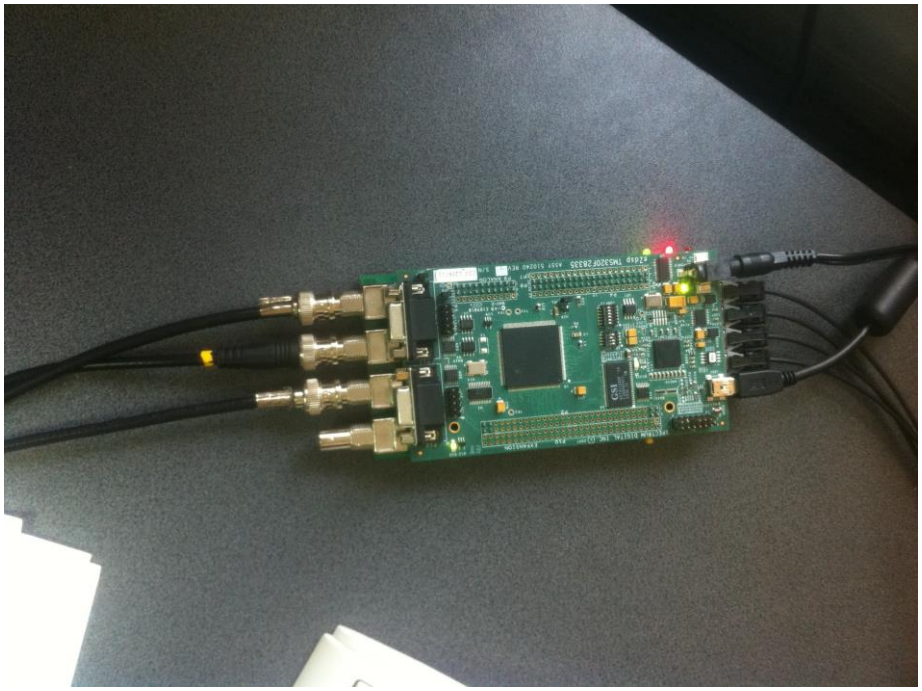

Figure 5.27 TMS 320F28335 digital signal processor from Texas Instruments

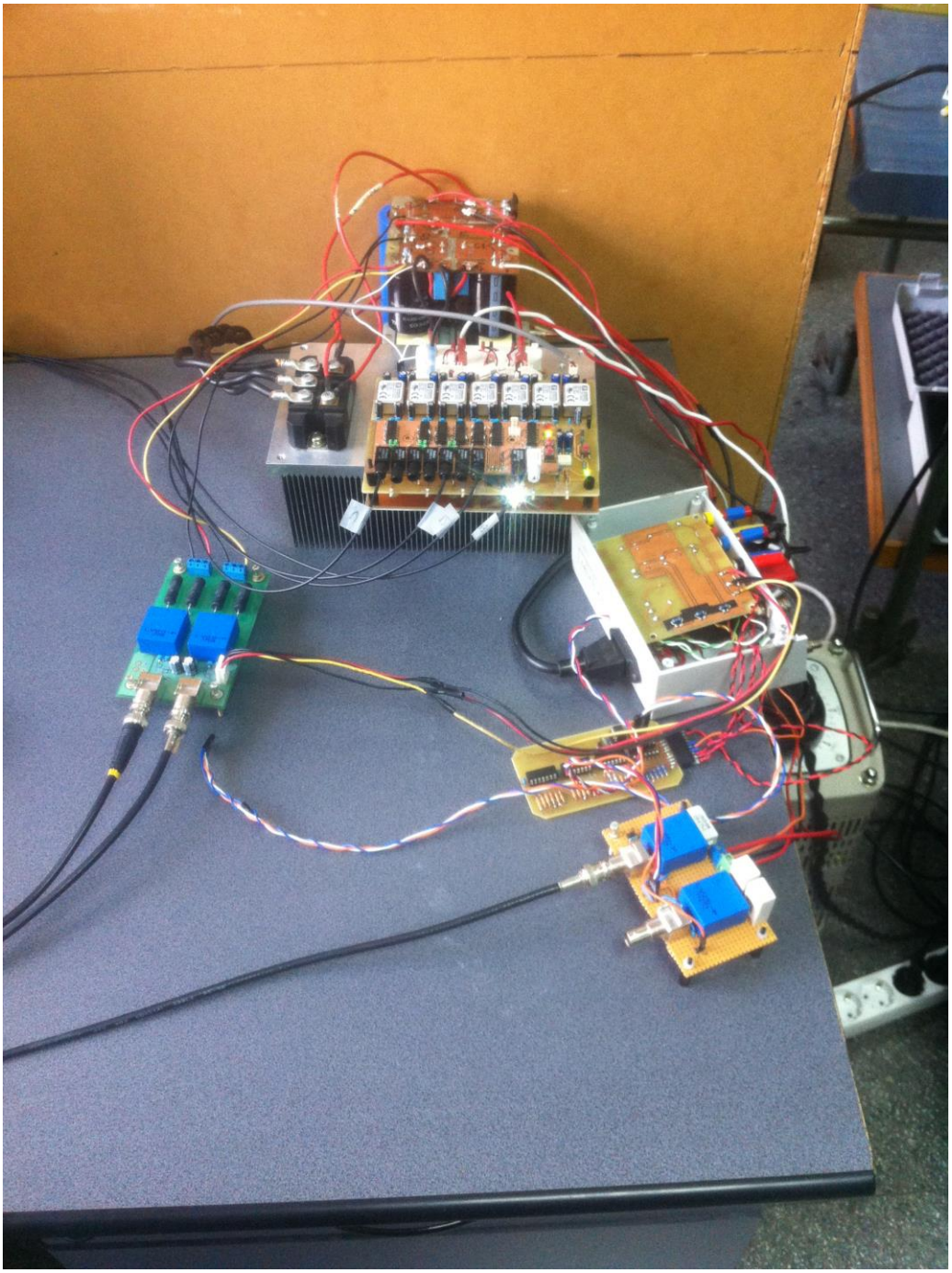

Figure 5.28 Laboratory setup for Z-source inverter experiments

Figure 5.29 Auto-transformer for charging the Z-source network, induction machine and the measurement system.

The laboratory setup were design and build from scratch in order to validate the proposed four-switch z-source three-phase inverter with induction machine and the algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive.

In Figure 5.2 we can see the Z-source network and inverter bridge with drivers used to carry out the experiments. In Figure 5.3 we have the TMS 320F28335 digital signal processor from Texas Instruments used to implement the control algorithm am generate the SVM pulses. In Figure 5.4 we have de Z-source inverter and the voltage sensors. In Figure 5.5 we have the auto-transformer for charging the Z-source network, induction machine with full ventilator (proportional to speed square) load and the measurement system.

CHAPTER 6 CONTRIBUTION AND CONCLUSIONS

The dc output voltage of the environment friendly electrical energy generation system fluctuates in a wide range and usually its voltage level is less than the input voltage desired at the input of a DC-AC converter. The voltage can be boosted with a DC-DC converter to the desired voltage level for the DC-AC stage or with a DC-AC converter including a Z-source network. The combination of the Z-source network and six-switch or a four switch three-phase inverter enhances the properties of the DC-AC stage thus providing the ability to boost the input voltage and to override the voltage sags. One way to further improve the properties of the DC-Ac stage is to reduce the number of switches.

Four-switch three-phase Z-source with split impedance network capacitors topology has some excellent advantages however it needs modification in structure of z-source network.

Based on the above listed reasoning the original contributions and conclusions of the author would be the following:

- Comprehensive study of the three-phase Z-source inverter with four respectively six switches has been carried out. The relevant formulae describing the operation of a Z-source inverter were pointed out.
- A closed loop speed control of induction motor fed by six switch Z-source inverter based on close loop Volts/Hertz control strategies and the peak dc-link voltage is controlled by a closed loop voltage controller within the period of zero vectors of space vector modulation was validate.
- The algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive were proposed.
- The algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the improved four-switch three-phase Z-source inverter feed an induction motor drive were proposed.
- Based on analytically derived equations the four-switch three-phase inverter with parallel and series Z-source network with induction motor drive was validated through digital simulation.
- One of the proposed four-switch three-phase Z-source inverter with induction motor drive was validated through experiments.
- The laboratory setup was design and build from scratch by the author in order to validate the proposed four-switch z-source three-phase inverter with induction machine and the algorithm to control the dc boost, split capacitor voltage balance and the ac output voltage of the four-switch three-phase Z-source inverter feed an induction motor drive.
- The control algorithm used in experiments was implemented on a 32-bit floating point digital signal processor TMS320F28335. The control programs were written in C++ language.

AUTHOR PAPERS RELATED TO THE THESIS

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