Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 49(63), Fascicola 1, 2004

A Log-Domain Circuit Design Method Based on F^{-1} N F Models

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Abstract: We developed in [1] a systematic modular design method for externally linear internally nonlinear (ELIN) circuits. This is a general and unitary approach for reconfiguring a linear block diagram into an equivalent ELIN block diagram described by F^{-1}, N, F nonlinear functions.

We focus in this paper on log-domain design rules and performe more circuit simulations in order to prove the applicability of this direct method and make it possible to be automatically applied.

Keywords: ELIN circuits, log-domain, nonlinear integrators, modular analog VLSI design.

I. INTRODUCTION

There are various methods for designing Externally Linear Internally Nonlinear (ELIN) circuits and Log-domain techniques are mostly used. The general and systematic method is based on the state-space formulation. This one was introduced by Frey [2] and developed by other authors. Intuitive modular methods based on log- domain integrators were given [5, 3, 4]. In this paper we focus on a simple method for designing a linear circuit with an ELIN structure. The proceeding was given in [1] and is based on the above named methods but it is more general, direct and does not need any intermediate flow graph transformation. In a block diagram described by linear differential equations or transfer functions, by substituting each linear operating block by equivalent nonlinear modules the ELIN schematic results directly. We give examples in log-domain and make also some observations and clarify some conditions to be fulfilled.

II LINEAR BLOCK DIAGRAM TRANSFORMATIONS

The direct method to transform a linear block diagram described by transfer functions or linear differential equations into an ELIN diagram can be deduced as it follows:

Consider a linear relation between two variables:

$$y_2 = \mathrm{Lin}(y_1) \tag{1}$$

If generally y_i are signals with a nonlinear dependence on x_i of the form:

$$y_i = F(x_i)\ ; \quad x_i = F^{-1}(y_i)\ ; \quad i = 1,2,... \tag{2}$$

we can express two signals x_1 and x_2 respectively by a nonlinear relationship

$$x_2 = F^{-1}\left(\mathrm{Lin}\left(F(x_1)\right)\right) = N(x_1) \tag{3}$$

Taking into account the expressions (1), (2), and (3) the block diagrams in Fig. 1 result.

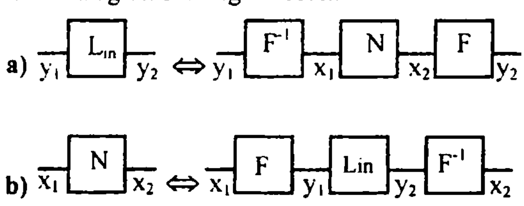

Fig 1. Linear – Nonlinear Block Transformation **a)** A linear building block consisting in nonlinear components; **b)** The behavioral model of block N.

For each F^{-1} – F pair of functions and a certain Lin dependence, nonlinear N building blocks can be derived. For a circuit consisting in linear blocks the corresponding ELIN diagram can be found as it follows:

Departing from a block diagram, one can substitute each linear building block the a corresponding nonlinear block. Adding them input and output F, F^{-1} terminal blocks respectively the ELIN form of the t. f. is obtained. The proceeding was derived in [1].

Two equivalent Lin- ELIN block diagrams are shown in figure 2.

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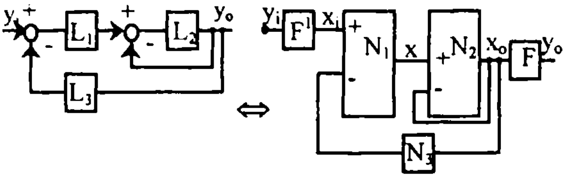


F . 2 Eq va L - ELIN b ck d agram .

The above transformations are independent of the order of the linear differential equations symbolized by **L** and the nature of signals y (currents or voltages) and also of the function **F**.
If F-F^{-1} are **exp- ln** functions, characteristic for bipolar transistors:

$$i_c = I_s \cdot e^{v_{BE}/V_T} \; ; \quad v_{BE} = V_T \cdot \ln \frac{i_c}{I_s} \qquad (4)$$

the ELIN circuits are in the log- domain. In this case it is advantageous to have currents in/out (y→i) for the linear basic blocks and voltages for the nonlinear blocks (x→v). The simplest and most frequently used **N** blocks are the nonlinear integrators.

III NONLINEAR LOG-DOMAIN INTEGRATORS

Integrators are mostly used in such schematics. Their structures were already given in literature [2], [3] but we would like to make some observations in order to simplify the setting of parameters and the direct drawing-up the schematics.

Multiple input integrator

We have to implement an **n** inputs integrating block:

$$\text{Lin:} \quad \frac{\tau di_o}{dt} = k_1 \cdot i_1 + k_2 \cdot i_2 + ... = \sum_j^n k_j \cdot i_j \qquad (5)$$

$k_1, k_2, \ldots$ are real numbers, positive or negative,
$\tau > 0$ is the time constant
i_1, i_2, are input currents of the form:

$$\text{for } i = F(v) = I\exp^{v/V_A} \; ; \; v = F^{-1}(i) = V_A \ln \frac{i}{I} . \qquad (6)$$

the nonlinear core N corresponding to such an integrator [1] is shown in figure 3, where

$$v_o = V_A \ln \frac{i_o}{I_o} \; ; \; v_j = V_A \ln \frac{i_j}{I_j} \; ; \; j = 1,2,\ldots,n \qquad (7)$$

$$i_c = \sum_{j=1}^{n} k_j I_j e^{(v_j - v_o)/V_A} \; ; \qquad (8)$$

$$I_o = \frac{CV_A}{\tau} \; ; \qquad (9)$$

$V_A = 2V_T$; 51 mV for an usual **e** cell

We consider class A exponential cells, having one directional non null currents, therefore setting the biasing currents I_j is very important for the proper operation.

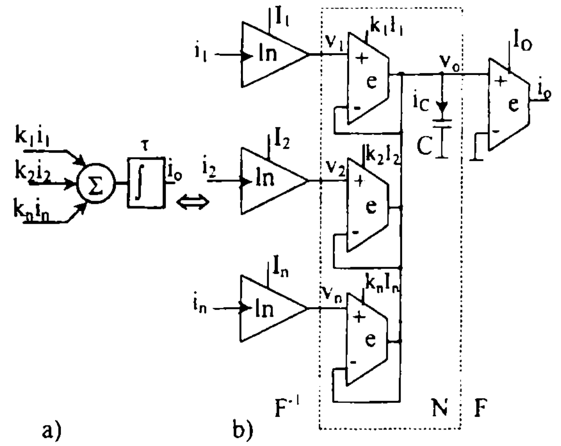


Fig 3 Multiple input integrator;
a) Symbol; b) Implementation with **e** cells.

Requirements and particular cases

- Current i_C is positive, negative or zero so that the circuit configuration should permit this current flow. Therefore equation (5) can be implemented only if it has at least two terms (n=2) and in this case $k_1 k_2 < 0$.
- If the integrator to be implemented has only **one input signal**, the second term in the right hand sum (5) will be considered a constant current without deteriorating the transfer function, that is:

$$\tau \cdot \frac{di_o}{dt} = k_1 \cdot i_1 + k_2 \cdot I_2 \; ; \quad H(s) = \frac{i_o(s)}{i_1(s)} = \frac{k_1}{\tau \cdot s} ; \qquad (10)$$

with $\quad k_1 \cdot k_2 < 0$; $i_2 = I_2$, resulting in $v_2 = 0$

The second input **ln** module of such an integrator can be cancelled and the corresponding v_2 input of the nonlinear N block will be grounded.

- Currents I_j in relations (7) and (8) can be chosen so that when all the signals are zero, circuits should have appropriate biasing currents I_j:

$$\sum_{j=1}^{n} k_j \cdot I_j = 0 \qquad (11)$$

- If the integrator has a negative feedback, one of the currents is i_o and the corresponding term in the sum (11) becomes: $k_O I_O$ ($k_O < 0$).

This case is specific for a **lossy integrator**:

$$\tau\frac{di_o}{dt}=k_1\cdot i_1-i_o \qquad (12)$$

or $$\tau\frac{di_o}{dt}+i_o=k_1\cdot i_1\ ;\quad H(s)=\frac{k_1}{\tau\cdot s+1} \qquad (13)$$

From (12) and (11) the relation between biasing currents results:

$$k_1\cdot I_1 - I_0 = 0 \qquad (14)$$

The general and the equivalent scheme respectively are given in Figure 4.

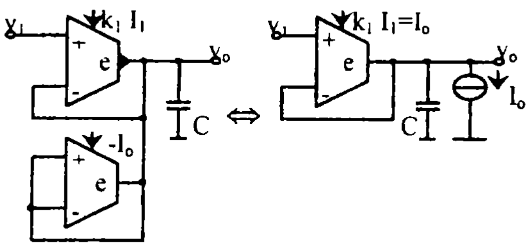


Fig 4. Nonlinear Lossy Integrator

IV. EXAMPLES

We proved the above presented method by performing various simulations. Some of them will be given in the following.

a) **Third order low pass filter** (leap frog filter).

The passive model of a LPF is given in figure 5,a and the corresponding flow graph in figure 5,b.

Substituting each linear integrator by a nonlinear one and adding input/output F^{-1}/F blocks results in the block diagram shown in Fig. 6.

Applying (11) and (9) for each integrator relations (16) result. We proved the above presented method by performing various simulations. Some of them will be given in the following

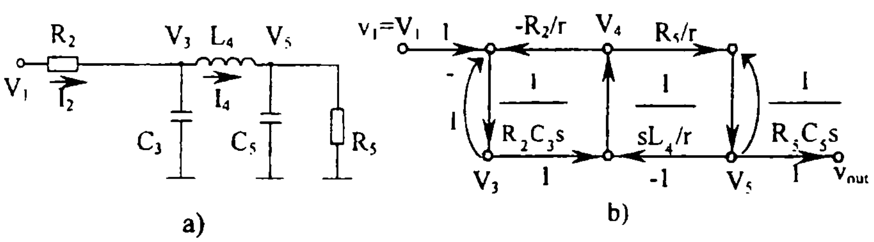


Fig 5 – Third order LPF

a) Passive prototype; b) Flow graph

$$\begin{cases} V_3=\dfrac{V_1-V_4R_2/r-V_3}{R_2C_3s} \\ V_4=\dfrac{V_3-V_5}{sL_4/r} \\ V_5=\dfrac{V_4R_5/R-V_5}{R_5C_5s} \end{cases} \qquad (15)$$

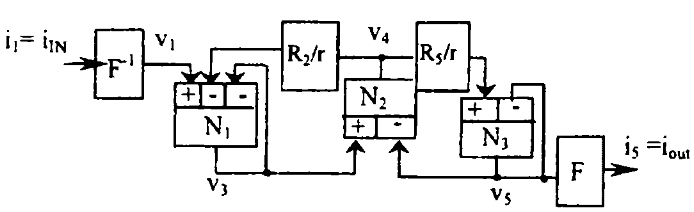


Fig 6 – $F^{-1}NF$ model of the LPF in Fig 5

$$I_3=\frac{C_3V_A}{\tau_3}=\frac{C_3V_A}{R_2C_3}$$

$$I_4=\frac{C_4V_A}{\tau_4}=\frac{C_4V_A}{L_4/r} \qquad (16)$$

$$I_5=\frac{C_5V_A}{\tau 5}=\frac{C_5V_A}{R_5C_5}$$

$$I_5=I_3\ ;\ I_5=\frac{R_5}{r}I_4\ ;\ I_1=I_3+\frac{R_2}{r}I_4$$

if $R_5=R_2=r \Rightarrow I_3=I_4=I_5\ ;\ I_1=2I_3$

The schematic in log domain is given in figure 7.

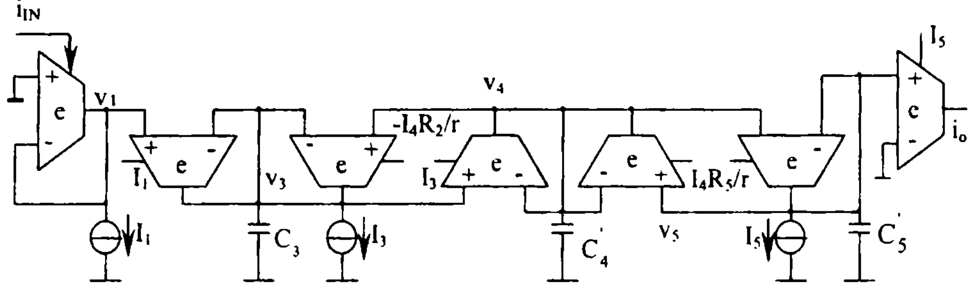


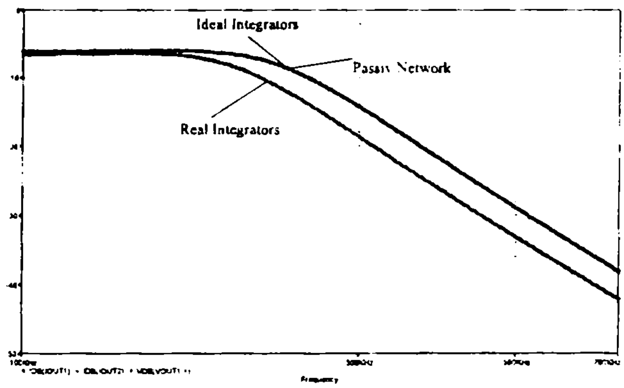
Fig 7 – LPF implemented with **e** cells

Biasing currents and requirements are directly deduced from the flow graph taking into account relations (5)(9) and (11). The passive model (Fig. 5,a) and the ELIN one (Fig. 7) have been simulated for proving the validity of the design. The simulated schematic is given in figure 8,a and the resulted frequency characteristics are given in Fig. 8,b for:

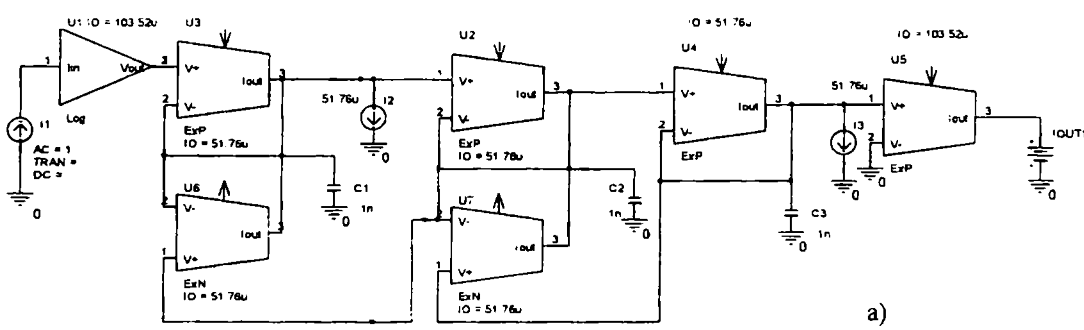
$L_4 = 1\text{mH}$ $R_5 = R_2 = r = 1\text{k}\Omega$;

$C'_3 = C'_4 = C'_5 = 1\text{nF}$; $I_3 = I_4 = I_5 = 51.76\mu\text{A}$; $I_1 = 103.52\mu\text{A}$

One can see the best results using ideal **e** cells. Unoptimized but very simple real cells introduce some errors with respect to the design data.



b)



a)

Fig 8 – a) Simulated schematic; b) Frequency characteristic

b) **Oscillator**

The transfer function of an oscillator is of the form:

$$H(s) = \frac{\omega_0}{s^2 + \omega_0^2} \qquad (14)$$

For this equation the linear block diagram is shown in figure 9. After replacing each linear integrator by a nonlinear one we get the corresponding ELIN block diagram from figure 10. The schematic is given in figure 11.

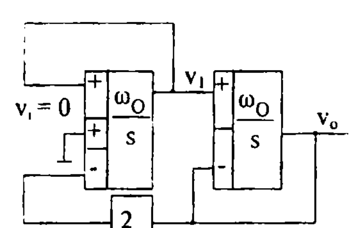


Fig. 9

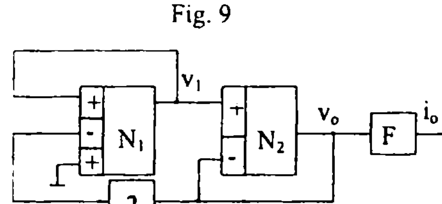


Fig. 10

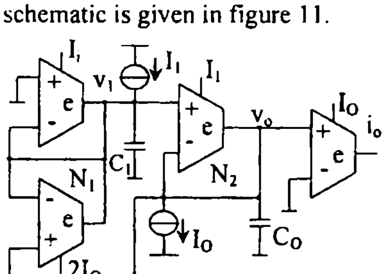


Fig. 11

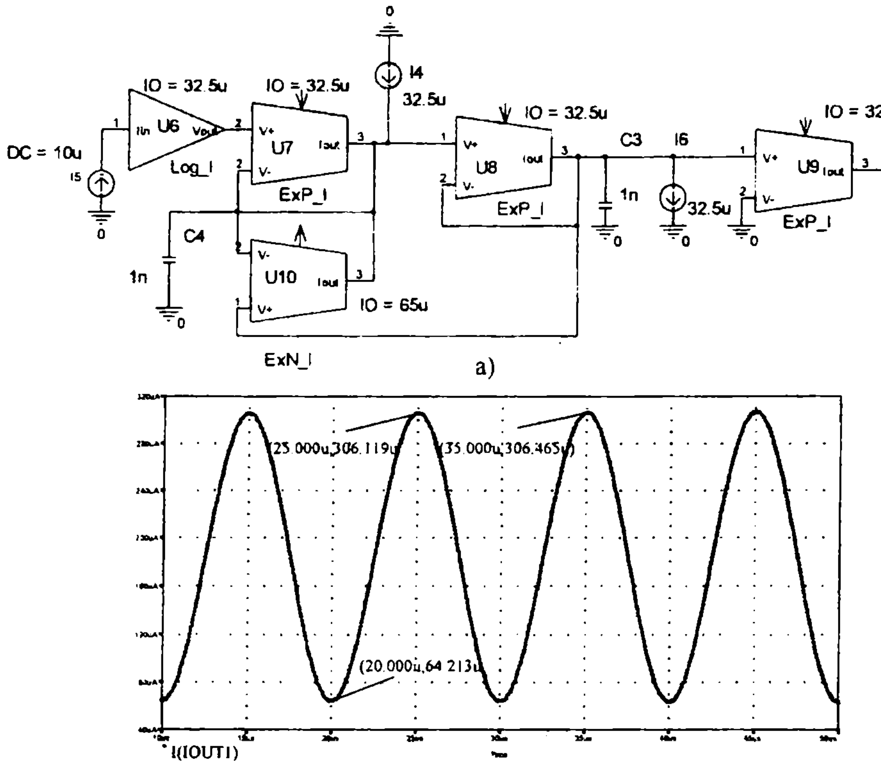
The values for the biasing currents and capacitors are obtained from the following equations :

node v_1: $I_1 = \dfrac{C_1 \cdot V_A}{\tau_1} = C_1 \cdot V_A \cdot \omega_0$; $I_1 + I_i = 2I_0$

node v_o: $I_o = \dfrac{C_o \cdot V_A}{\tau_o} = C_o \cdot V_A \cdot \omega_0$; (15)

$$I_1 = I_o \Rightarrow I_1 = I_i = I_o \ ; \ C_1 = C_n$$

The circuit from figure 12,a is designed for f_0=100KHz. The simulation results of this circuit are given in figure 12,b.



a)

b)

Fig 12. ELIN Oscillator a) schematics, b) simulation results

c) **State variable Filter**

The block diagram of a State Variable Filter is given in figure 13 and the corresponding ELIN $F^{-1}NF$ block diagram is given in figure 14.

The corresponding transfer functions and the considered parameters are:

$$\frac{i_2}{i_I} = \frac{1}{\tau_1\tau_2 s^2 + \tau_2 s + 1} \ ;$$

$$\frac{i_1}{i_I} = \frac{\tau_2 s}{\tau_1\tau_2 s^2 + \tau_2 s + 1} \ ; \qquad (16)$$

$$\frac{i_0}{i_I} = \frac{\tau_1\tau_2 s^2}{\tau_1\tau_2 s^2 + \tau_2 s + 1}$$

$\tau_1 = \tau_2 = 159\mu s$; $f_0 = 1kHz$; $C_1 = C_2 = 1nF$

$I_1 = I_2 = 325nA$; $I_I = 975nA$

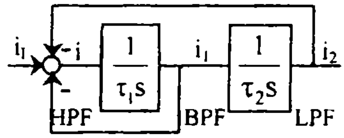


Fig 13

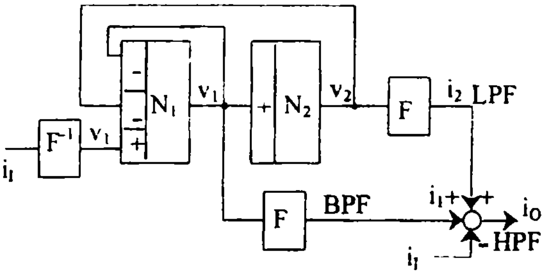


Fig 14

The schematics is given in figure 15 and in figure 16 we have the simulation results of this circuit

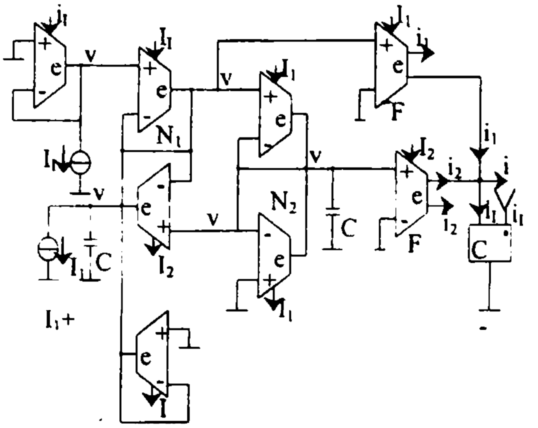


Fig. 15 State variable filter schematics

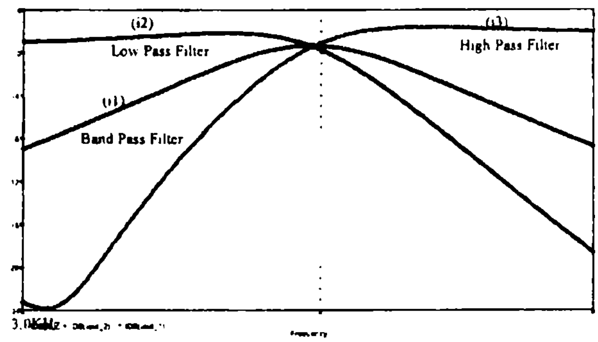


Fig. 16 Frequency characteristic of the State variable Filter

V. CONCLUSIONS

A Linear current-mode circuits can be implemented by using specific nonlinear voltage-mode blocks . A linear current-mode circuit can be directly reconfigured departing from its block diagram. The direct procedure given by authors is a general one and the reconfigured block diagram does not depend on a certain F function. Of course parameters and circuit structure depend on F. Relations between parameters and requirements for log-domain circuits have been also deduced.

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