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Designing and implementation of dual voltage, low leakage and low power bi-directional CMOS I/O circuits

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Abstract – This paper presents the designing and implementation of the dual voltage, low leakage and low power bidirectional input-output (I/O) circuits. The proposed architecture contains a pre-driver block, an output driver and an ESD (electro-static discharge) protection block. The output driver stage was designed to be supplied with 1.8V or 3.3V (dual voltage concept) and, also, for three values of the output current driving capabilities (4mA, 8mA and 12mA).

The results show that the total parasitic power consumption and leakage current are less than 160 uW/MHz and 4.10 nA, respectively.

Keywords: I/O, ESD, HBM

I. INTRODUCTION

The I/O circuits, known as pad circuits, are the interface part between the core side and package pins of the integrated circuits. The power and the leakage current consumption of the I/O circuits have the greatest influence for the overall performances of the integrated circuits that contain these I/O's. Also, as the actual internal circuits increase in speed, the faster I/O circuits are needed.

To improve circuit operating speed and performance, the device dimensions of MOSFET have been shrunk in the advanced deep-submicron integrated circuits. In order to follow the constant-field scaling requirement and to reduce power consumption, the power-supply voltages in CMOS IC's (integrated circuits) have also been scaled downwards. So, most microelectronics systems require the interfacing of semiconductor chips or subsystems with different internal power supply voltages. With the mix of power supply voltages, chip-to-chip interface I/O (input/output) circuits must be designed to avoid electrical overstress across the gate-oxide [1], to avoid hot-carrier degradation [2] on the output devices, and to prevent undesirable leakage current paths between the chips [3], [4].The I/O circuits are one of the most important circuits because of their role to interface the integrated circuit with external environment. The difficult demands over designing of these kinds of input-output circuits are fast speeds simultaneously with low leakage and low power consumption and, nevertheless, the most important demand is for ESD protection circuits the level of spike voltage applied on I/O pin which becomes greater than 2kV for HBM (Human Body Model), touching in some cases 8kV. In this paper many trade-offs such as low power consumption, low leakage currents, high speed and dual voltage capabilities for the final stage had been accomplished.

II. BIDIRECTIONAL PAD ARCHITECTURE

The architecture and the truth table of the proposed bi-directional circuits are shown in fig.1, respectively table 1. The architecture contains a pre-driver block, an output driver and an ESD (electro-static discharge) protection block.

From the truth table it can be, easily, noticed that this pad contains also the pull-up feature that was designed for low leakage integrated circuits, the typical value for the pull-up resistance is 75kohm.

The proposed architecture contains a pre-driver block, an output driver and an ESD (electro-static discharge) protection block.

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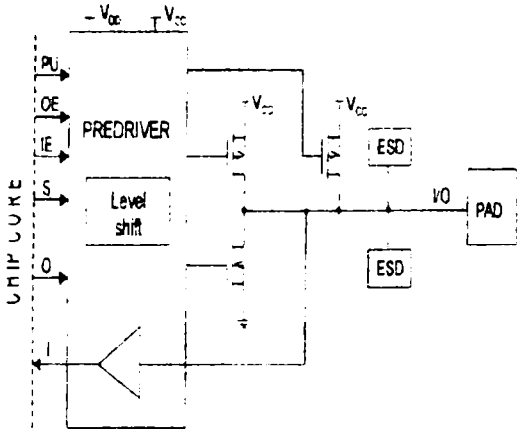

Fig 1 The architecure of the proposed bidirectional pads

Function	IEN	OE	PU	O	I	IO
Bidirectional Pad (IO=I=O)	0	1	X	0	0	0
	0	1	X	1	1	1
Input pad (IO=I)	0	0	X	X	0	0
	0	0	X	X	1	1
	0	0	1	X	1	1
High Impedance(IO=Z)	1	0	0	X	1	Z
Pull-up (IO=1)	1	0	1	X	1	1
Output pad	1	1	X	0	1	0
	1	1	X	1	1	1

Table.1 The truth table of bidirectional pads

Each block of the architecture is presented in the next sections. The most important contributions of this architecture were:
- the designing of a special predriver circuit for low power and low leakage current consumption;
- a special ESD structure to meet the trade-off between the leakage current consumption, dual voltage concept, and ESD level (HBM 2kV).

III. THE PRE-DRIVER BLOCK

The schematic of the pre-driver block it is presented in fig.2.

It can be seen that this pre-driver contains the classical structure of tri-state output pads and the stage input pad.

Actually the pre-driver is responsible for dynamic performances of pads: propagation times, power consumption, leakage current consumption, slew-rate and simultaneously switching parameters.

To design a dual voltage pad simultaneously with low leakage and low power requests is a difficult task.

The pre-driver has a huge capacitor load represented by the output transistors from the output stage (see the fourth section).

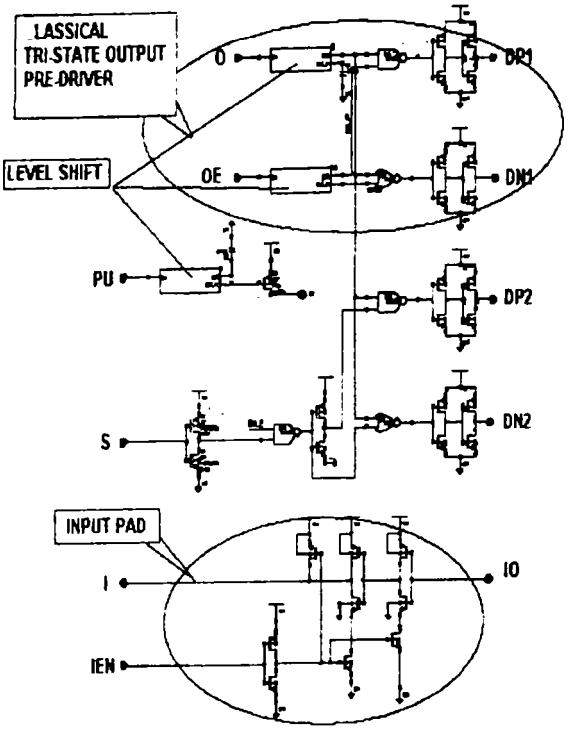

Fig.2 The complete schematic of pre-driver block

For driving huge loads it is needed large buffers and this means a large leakage current consumption and a larger short-circuit power consumption. But the main problem is that the I/O's should have a lower propagation times from core signals (O – output of core circuits, I – input of core circuits to the pad pin – IO) and in the same time low power consumption.

More than this, the demand of the maximum limits for the power consumption of the I/O circuits it is continuously decreasing touching some limits that is almost impossible to achieve.

The power consumption of the pads includes the short circuit power consumption and the leakage power consumption, the load power consumption component it is treated separately.

Beside of the classical tri-state output and input pad stages it is revealed the special low power pre-driver circuits feature, namely the logic schematic that disables half of output stage during 3.3V for VCC (supply of driver stage) and enables all output stage for 1.8V for VCC. So, the VCC can take both value of supply voltage 3.3V and 1.8V (dual voltage concept). Also the level-shift circuits that make the interface and shifting in level operation between core circuits and I/O circuits are presented in schematic of pre-driver stage.

The pull-up stage that is revealed in pre-driver schematic was designed for pull-up specification 75Kohm in typical corner.

A. *The low power and low leakage feature description*

Increasing the fan-out capabilities of the pre-driver gates especially for the buffers can reduce the

short circuit power consumption for the overall pad circuit, but the drawback of this technique it is the increasing of leakage current and, obviously, the leakage power consumption. The low power feature that was successfully achieved in these output pads combines this method with splitting the output stage for 3.3V VCC supply where half of the transistors are enough. So, when the S signal it is 0 and VCC=VDD=1.8V (fig. 3a) all output signals for driver stage (final stage) DN1, DP1, DN2, DP2 are driving all transistors from output stage. When the S it is with VCC level (this for VCC=3.3; VDD=1.8) than only DN1, DP1 are for driving, DN2, DP2 remains with "0" level (fig.3b).

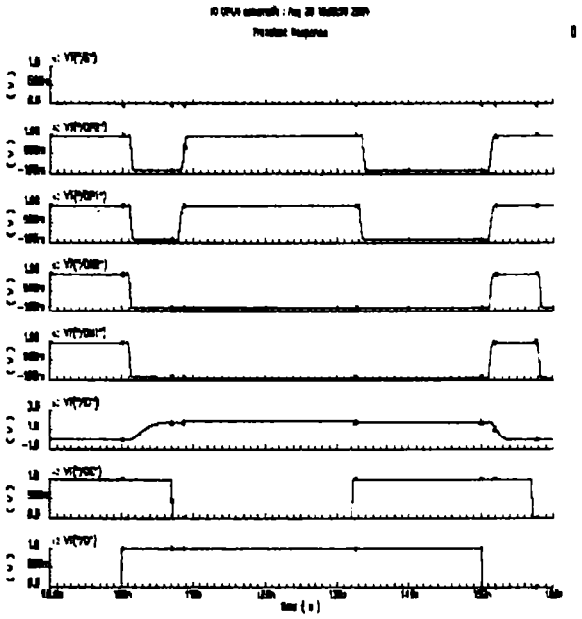

Fig.3a Wav f rm f r DN1, DP1, DN2, DP2 i_nal in case of VCC=VDD=1.8 (S= "0" logic)

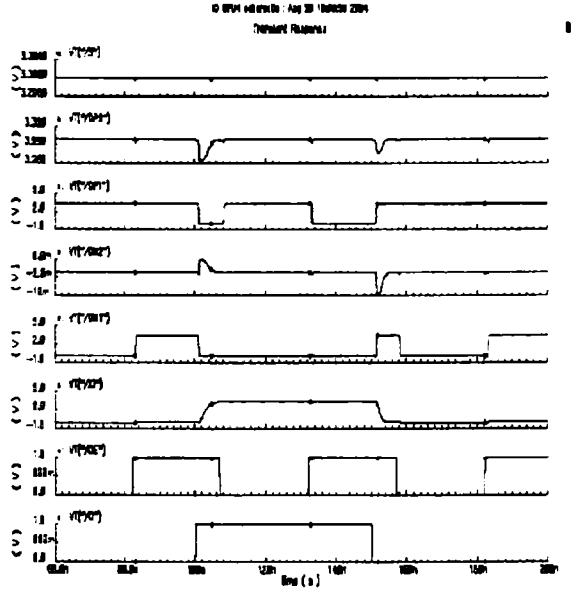

Fig.3b Waveforms for DN1, DP1, DN2, DP2 signals in case of VCC=3.3 VDD=1.8 (S= "1" logic)

B. The non-overlapping signals technique

Another technique that can be implemented for low power operation it is called non-overlapping technique. The three state pre-driver circuit it is shown in fig.4 a. Using this technique with the proposed technique improves the short circuit power consumption of the output pad but increase the leakage current over the maximum limit 7 nA which has a direct implication of the increasing leakage current for the intended chip which has almost 130 pins with this feature (bi-directional pad) (in totally are 256 pins for industrial application of the wanted integrated circuit). The complete schematic including both: non-overlapping technique and the proposed technique without low leakage current consumption stress can be implemented like in fig.4 b.

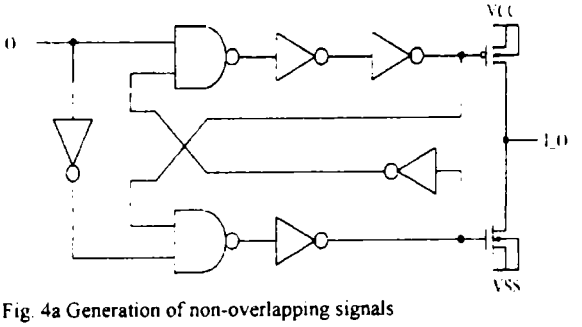

Fig. 4a Generation of non-overlapping signals

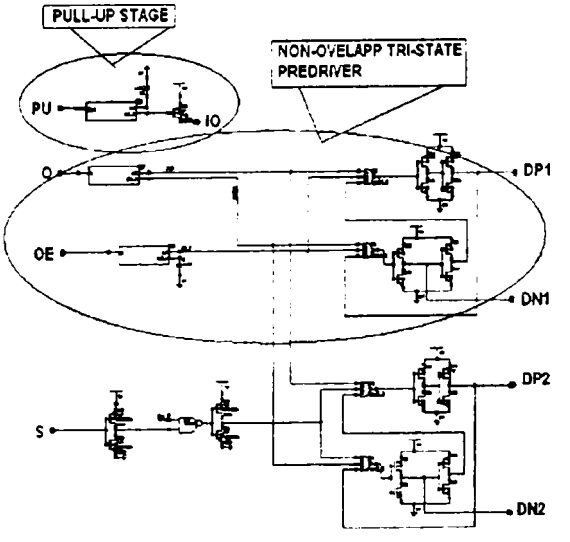

Fig.4b Non-overlapping pre-driver (only tri-state output stage) schematic

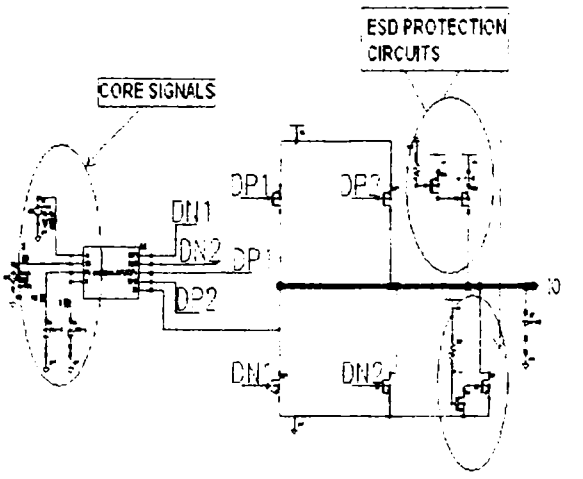

Fig 5 The schematic of the driver stage (including interconnections with pre-driver block)

IV. THE OUTPUT STAGE (THE DRIVER BLOCK)

The complete schematic of the output stage including ESD protection circuits it is shown in fig.5. Mathematical relations for sizing the output transistors are suggested in (1), (2) and (3).

$$i_{IO\_AC} = C_{Load} * \frac{dV}{dt} \quad (1)$$

$$I_{IO\_DC} = I_{OL} = I_{OH} \quad (2)$$

$$I_{TOTAL\_OUTPUT\_STAGE} = I_{IO\_DC} + i_{IO\_AC} \quad (3)$$

The configuration for the output stage it is indirectly determined by ESD considerations, these stage were designed to meet the dual voltage concept and, of course, to decrease the ESD sensitivity. So, in the final stage we have implemented only with 3.3v transistors but these, also, must drive successfully huge loads, tens of pico-farads, in low voltage operation 1.8V supply. The need of 1.8 V supply and current drive for instance 12 mA in worst case impose huge sizes for 3.3V transistors models, that why we need to design a special pre-driver to disable half of these transistors of during 3.3v voltage supply.

V. ESD PROTECTION CIRCUITS

ESD stresses on an I/O pad have four basic pin combination modes: positive-to-GND (PS-mode), negative-to-GND, positive-to-VCC (PD-mode), and negative-to-VCC (ND-mode) ESD stress conditions [5], [6]. To have high enough ESD robustness of the CMOS output stage, the CMOS output stage is generally drawn with larger device dimensions and a wider spacing from the drain contact to the poly gate, which often occupy a larger area in the I/O cell. The VCC-to-GND ESD clamp circuits across the power lines of CMOS IC's have been reported to effectively increase ESD robustness of CMOS I/O circuits [7]-[10]. The ESD protection circuit proposed for these output pads is drawn in fig 6.

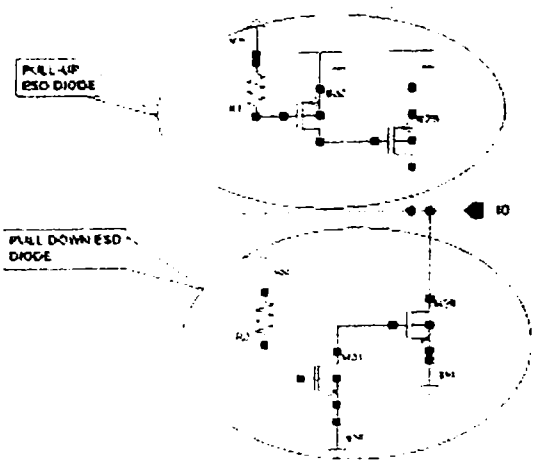

Fig 6 The proposed schematic of ESD for the output side of circuit

It can be seen from schematic two kinds of structures named soft-pull up and soft-pull down fig.6.

The test reports above ESD are shown in fig.7. The I-V characteristics are plotted with on a digital scope after a spike with 2kV amplitude HBM was applied to test these output pads.

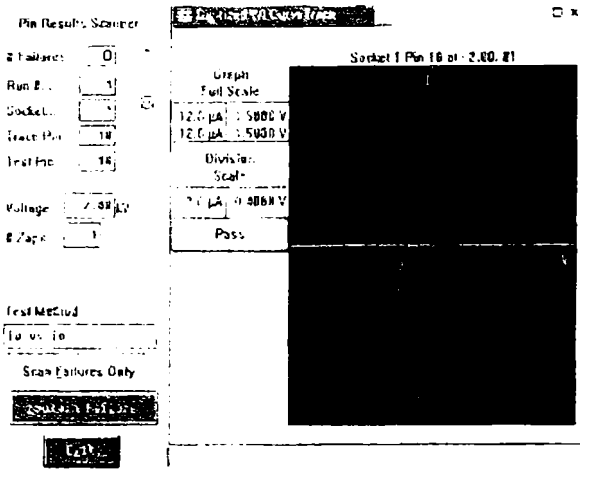

Fig 7 The ESD test report for HBM

These ESD circuits, also, have the negative influence over leakage current consumption. The layout for the output pad and the layout for the supply pads are shown in fig.8.

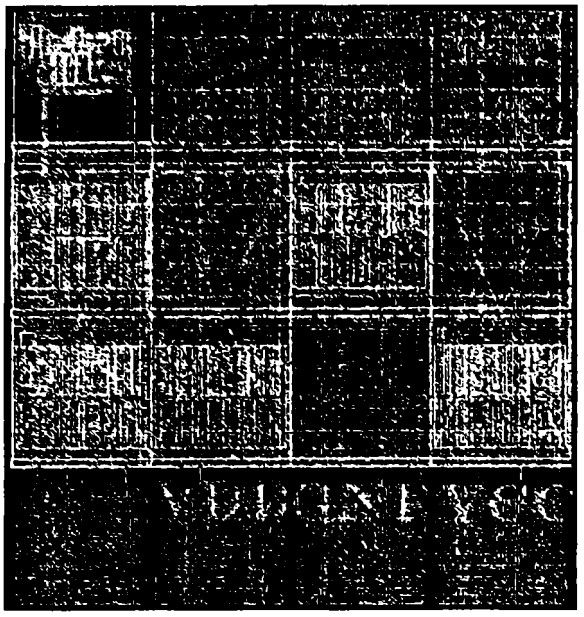

Fig 8 Layout view of an bi-directional pad with supply pads

VI. CONCLUSIONS

A new type of pre-driver was successfully designed and proved his performances in CMOS 0.18µm 1P6M (one poly-silicon six metals, single well process). The performances of these output pads impose them to be used on chips with many pads, especially for low power and low leakage applications. The output driver stage was designed to be supplied with 1.8V or 3.3V (dual voltage concept) and, also, for three values of the output current driving capabilities (4mA, 8mA and 12mA).

Bi-directional mode	*Propagation Times (Load C=40pF on IO pin, C=0.1pF on I input of core)*		Parasitic power consumption (no load at pin IO and I)	DC parameter measured at 85°C
Circuit name	**O to IO (worst case1.8)** (ns)	**IO to I (worst case 1.8)** (ns)	**Average Power Consumption (best case VCC=3.6V, VDD=1.8V, FF -55 °C)** (µW/Mhz)	**Leakage Current** (nA)
BPU4 (4mA DC LVTTL)	8	1.5	60	2,6
BPU8 (8mA DC LVTTL)	6	1.65	102	3.1
BPU12 (12mA DC LVTTL)	4	1.7	160	4.1

Table 2 Dynamic and static performances of BPUx pads

The post layout simulations were done at best accuracy level of the layout parasitic extraction for all process and temperature corners. The static (leakage current consumption) and the dynamic performances for the succesfully silicon tested bi-directional pad are presented in table2.

The results show that the total parasitic power consumption and leakage current are less than 160 uW/MHz and 4.10 nA, respectively.

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