# PC-based system for automated calibration of a digital voltmeter

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**Abstract – The paper presents a system built around a PC and the application in LabVIEW for automated calibration of a digital voltmeter against a high accuracy voltmeter. The devices communicate within the system through standard interfaces RS 232 and IEEE 488.**
**Keywords: automated calibration, standard interfaces, virtual instrument.**

## I. INTRODUCTION

Calibration of a digital voltmeter (DVM) must be done against an etalon that can be either a voltage calibrator or a high accuracy digital voltmeter. In the second case a voltage source is also needed. In both cases several voltage values have to be measured and compared with those indicated by the etalon. These operations can easily be done automatically by using an appropriate experimental setup that consists of a PC, a programmable power supply, the DVM to be calibrated and a high accuracy voltmeter.

## II. DESCRIPTION OF THE SYSTEM

The system that has been developed for the calibration of a DVM consists of a PC, a programmable power supply, the DVM to be calibrated and a high accuracy voltmeter (fig. 1).
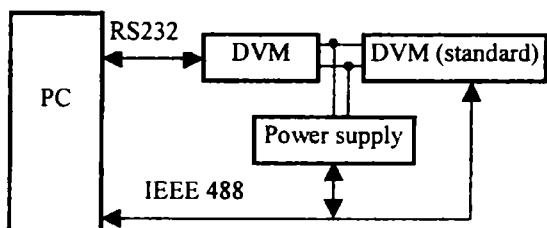


Fig.1. System schematics.

The power supply and the high accuracy voltmeter are connected to the PC via the IEEE 488 parallel interface [1]. For the DVM to be calibrated a 4 1/2 digit Voltcraft 4650 CR with built-in RS 232 serial interface was considered.

An application (virtual instrument - VI) has been developed in order to control all the devices and to accomplish the required tasks. The inputs of this VI are: the voltage range of the DVM to be calibrated, its number of digits, the formula given in its specification for calculating the maximum permissible error, the number of points (voltage values) and the number of times the measurements should be repeated at each point in order to obtain an averaged result. The tasks to be accomplished by the system are described in the following:

Step 1 – The VI calculates the first voltage value and sends it to the programmable power supply.

Step 2 – After a convenient delay the readings of the two voltmeters are sent to the PC. Step 2 is repeated the required number of times, and the readings are averaged. The averaged results are output in a table, and the error is calculated and compared to the maximum permissible error.

Steps 1 and 2 are repeated for the required number of points.

In the end, the operator sees a table with the averaged readings of the two voltmeters, the actual error and the maximum permissible error. Additionally, an array of LEDs indicates whether and at which point the error exceeds the limit.
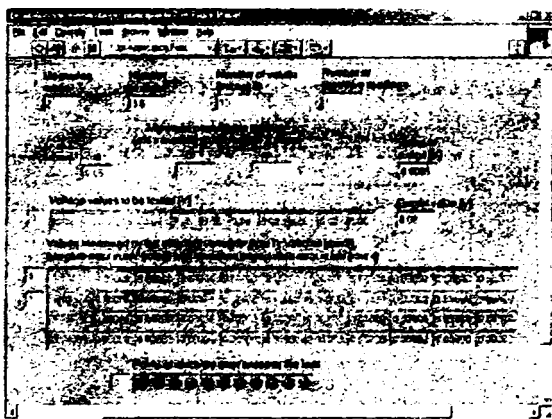
The front panel of the VI is shown in fig. 2.



Fig. 2. Front panel of the VI.

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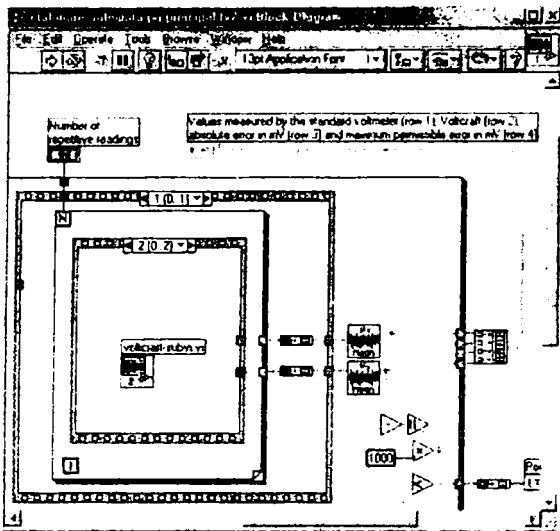A part of the block diagram is shown in fig. 3.



Fig. 3. Part of the block diagram of the main VI.

A hierarchical approach has been considered, consisting of a main VI, subVIs, subVIs of the subVIs and so on. The main VI consists of a two-frame sequence structure that implements steps 1 and 2 described above.

In step 1 a voltage value is calculated and sent to the programmable power supply by calling the hm8142.vi. This is a subVI that manages the communication with the power supply via the IEEE 488 parallel interface [1].

Step 2 consists of a three-frame sequence structure:

i.   a 3-second delay to allow the DVMs indications to settle
ii.  the value measured by the high accuracy voltmeter is input to the PC
iii. the value measured by the DVM to be calibrated is input to the PC.

Frames *ii* and *iii* are then repeated the desired number of times (for obtaining averaged measurements). The averaged results are then written into the main table of the front panel. Steps 1 and 2 are repeated for the required number of points.

In frames *ii* and *iii* two other subVIs are called: hp3455.vi and voltcraft.VI, respectively. These subVIs manage the communication between the PC and the two voltmeters, by means of parallel and serial interfaces, respectively.

In the main VI the maximum permissible error for each voltage value to be measured is also calculated and written into the main output table on the front panel. The actual error is obtained by subtracting the two measured voltage values after averaging. The actual error is also written in the main table on the front panel. If the actual error is less than the maximum permissible error, the corresponding LED on the front panel will be powered on. A non powered LED indicates the voltage value for which the maximum permissible error has been exceeded.

The block diagrams of the main VI and of the subVIs have been supplied with error handling blocks. These blocks are not necessary if the system operates properly, but if the application stops, it is very difficult to find out why. The general structure of such a block is presented in fig. 4.
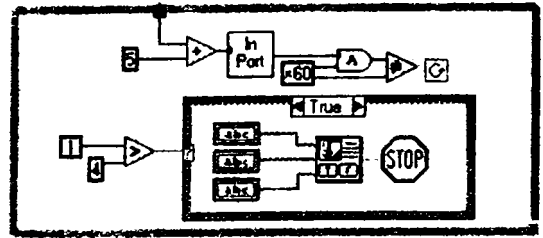


Fig. 4. Error handling block.

## III. EXPERIMENTAL RESULTS

Fig. 5 presents the front panel of the main VI after running the application.
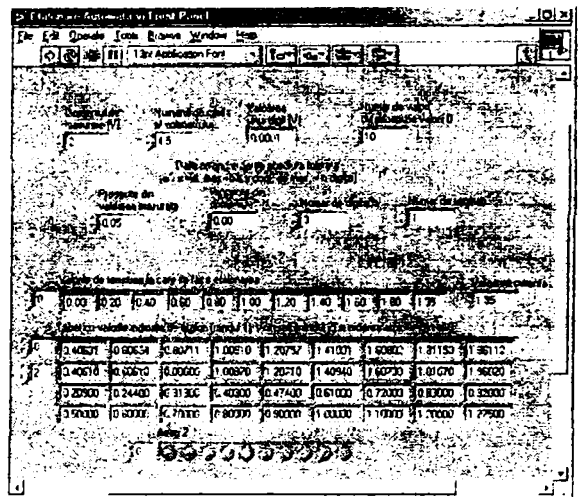


Fig. 5. Front panel of the main VI
after running the application.

A printed report can be easily generated.

## IV. CONCLUSION

The VI presented in this paper eases very much the job of the human operator. It also gives way to implementing an e-learning application, namely conducting the experiment from a remote location [3].

## REFERENCES

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