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Low power current mode analog architecture for fuzzy logic systems

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Abstract – The present paper proposes a highly programmable current mode architecture for a low power implementation of a fuzzy logic system. The solution eliminates the aggregation of the individual contributions of the fuzzy rules to the final result and avoids the division operation in the defuzzification block.

Keywords: Electronic Circuits, Fuzzy Logic Sytems

I. INTRODUCTION

In this paper it is proposed a low power current mode analog architecture for fuzzy logic systems. The general architecture of a fuzzy logic system is presented in Fig.1 [1]. The main blocks of the system are:

- the fuzzyfication module, converts the crisp actual value of the input fuzzy variable into a membership degree of a fuzzy set, which is defined over the universe of discourse of the concerned input variable.
- the rule base; its content encodes the fuzzy algorithm of the system.
- the inference engine computes the overall output fuzzy set based on the individual contribution of each rule. The outputs of the fuzzyfication modules are matched to each rule premise by means of the logical connectives (usually min or product operator) and a firing degree is established for each rule. Then, the firing degree is used to determine a "clipped" fuzzy set for the output fuzzy variable; this represents the individual contribution of the fuzzy rule. Finally, the individual contributions are aggregated and the overall fuzzy set is computed.
- the defuzzification module converts the overall fuzzy set into a single crisp value.

In Section II, a parallel architecture suitable for analog low power implementation is introduced. Subsequently, a circuit called basic cell is presented (section III). In the next two sections is shown how this circuit can be used to built a highly programmable fuzzyfication circuit (section IV) and a multiple inputs multiplier cell (section V). Section VI is dedicated to Hspice simulation results of the introduced circuits and the fuzzy logic system. In the last section, some conclusions are drawn.

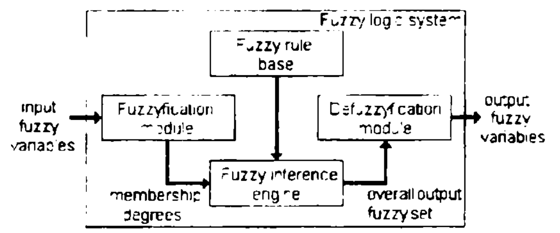

Fig. 1. The general structure of a fuzzy logic system

II. THE PROPOSED ARCHITECTURE

In this work, we have considered a particular structure of the fuzzy logic system:

- the input fuzzy sets are normalized and generate a fuzzy partition over the universe of discourse where are defined (e.g. the adiacent fuzzy sets have a 50% overlap).
- the antecedents are connected into premise only by AND logical connectives; the AND connective is defined by the product operator.
- the rule base of the fuzzy logic system is complete.
- it is used the Larsen implication (the implication function is defined by the product operator).
- all the consequences of the fuzzy logic system are represented as crisp values.

These specifications pave the way for a simple hardware architecture of the fuzzy logic system, that eliminates the aggregation of the individual contributions of the fuzzy rules to the final result and avoids the division operation in the defuzzyfication block [2]. Also, an actual value of an input fuzzy variable activates at most two adiacent input fuzzy sets. Thus, for each input fuzzy variable there are at most two alpha values, (e.g. membership degrees of the input fuzzy sets) denoted α_L and α_R (α_R=1-α_L) that has nonzero values (see Fig.2).

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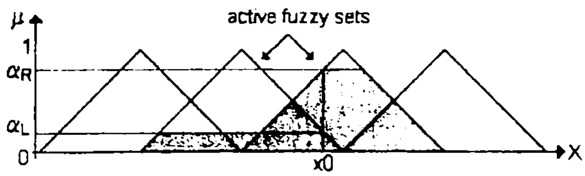

Fig.2. The alpha values of a fuzzy partition.

Moreover, for N fuzzy inputs, it can be stated that there are at most 2^N active fuzzy rules that contribute to the output of the fuzzy logic system [3]. Consequently, if it is considered only two input fuzzy variables, X and Y respectively, the output of the fuzzy logic system U can be computed as:

$$u = \frac{\beta_1 \cdot C_1 + \beta_2 \cdot C_2 + \beta_3 \cdot C_3 + \beta_4 \cdot C_4}{\beta_1 + \beta_2 + \beta_3 + \beta_4} \qquad (1)$$

where β values are the firing degrees of the active fuzzy rules and C values are the crisp consequents of these rules. However, the firing degrees of the active fuzzy rules can be replaced function of the alpha values of the input variables and the output expression becomes:

$$u = \frac{\alpha_{XL}\alpha_{YL}C_1 + \alpha_{XL}\alpha_{YR}C_2 + \alpha_{XR}\alpha_{YL}C_3 + \alpha_{XR}\alpha_{YR}C_4}{\alpha_{XL}\alpha_{YL} + \alpha_{XL}\alpha_{YR} + \alpha_{XR}\alpha_{YL} + \alpha_{XR}\alpha_{YR}}$$

If the α_R values are replaced with $1-\alpha_L$ values, it can be seen that the denominator of the above expression is always equal 1, thus, the division operation can be eliminated in the output variable expresion:

$$\begin{aligned} u &= \alpha_{XL} \cdot \alpha_{YL} \cdot C_1 + \alpha_{XL} \cdot \alpha_{YR} \cdot C_2 + \\ &+ \alpha_{XR} \cdot \alpha_{YL} \cdot C_3 + \alpha_{XR} \cdot \alpha_{YR} \cdot C_4 \end{aligned} \qquad (2)$$

The same reasoning can be employed if the number of the input variables is greater than two. The relation (2) gives the opportunity to develop a fuzzy logic system architecture as is depicted in the Fig.3.

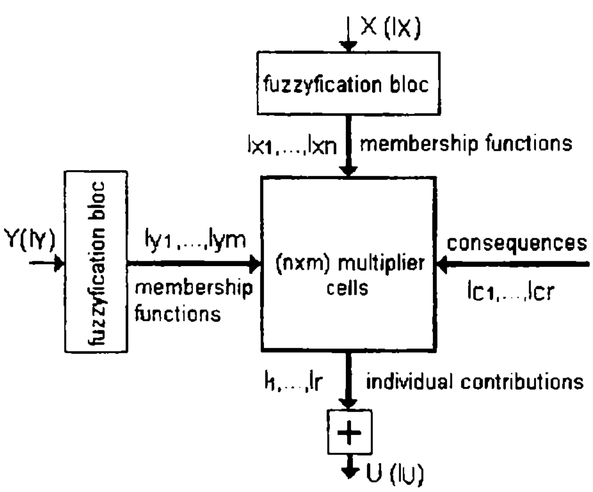

Fig.3. The proposed architecture of the fuzzy logic system.

The input fuzzy variables are represented by means of the electrical currents I_X and I_Y respectively. The fuzzyfication blocks are similar and are used to genera e he alp' a va'u b d t hi- functions of the input fuzzy sets. The alpha values and the consequences of the fuzzy rules are represented as the electrical currents: I_{xi}, i=1,...,n, I_{yj}, j=1,...,m, and I_{ck}, k= ...,r respect ve y r=nxm . The terms nvo ved in the relation (2) are generated by a matix of nxm three inputs multiplier cells, as electrical currents I_k, k=1,...,r. These currents represent the individual contributions of the fuzzy rules. Finally, as the proposed solution is based on a current mode technique, the addition block is implemented as a simple connection point (circuit node), by means of Current Kirkhoff Law.

III. THE BASIC CELL

In our solution, the fuzzyfication circuits and the multiplier cells are implemented on the base of the same circuit, that can be seen as a basic cell. The basic cell is depicted in the Fig.4. It has a translinear loop which involves MOS transistors operating in the weak inversion region [4]. If all transistors are saturated, each of them exhibits an exponential dependence between theirs currents and the gate-source voltage:

$$I_D \cong I_0 \cdot exp\left(\frac{\kappa \cdot V_{GS}}{V_T}\right) \qquad (3)$$

where I_0 is a current that depends on the W/L aspect ratio, κ is the body effect coefficient of the transistor, with tipical values between 0.7 and 1 and V_T is the thermal voltage. Then, if I_3 and I_4 are positive currents, it can be stated that:

$$\frac{I_2}{I_1} = \frac{I_4}{I_3} \qquad (4)$$

The transistor M_5 is used to keep the transistors of the translinear loop in the saturated region, when a set of basic cells are stacked to built a fuzzyfication circuit or a multiplier cell.

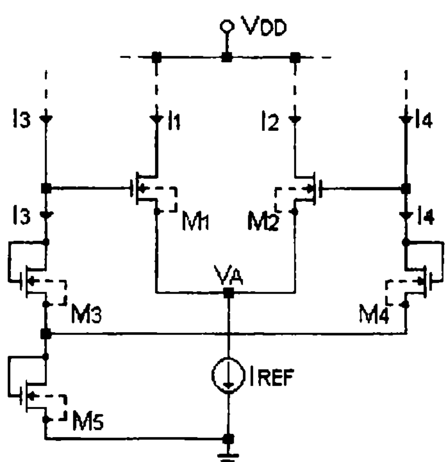

Fig.4. The basic cell.

IV. THE FUZZYFICATION CIRCUIT

The basic cell is a versatile circuit. By stacking a set of basic cells, it can be implemented a fuzzyfication block. If a fuzzyfication circuit is to be implemented, I_3 and I_4 currents must be replaced by I_R-I_X and I_X-I_L respectively, where I_X is the actual value of the input fuzzy variable and I_L and I_R ($I_L<I_R$) are used to alter the shape of the membership functions. The operation of the basic cell with the replaced currents is analysed in [5]. If $I_X \in [I_L, I_R]$ all the translinear loop transistors are ON; if $I_X<I_L$, M_2 and M_4 are OFF and M_1 and M_3 are ON, otherwise the states of the translinear loop transistors are reversed. Then, the output currents I_1 and I_2 of the basic cell can be expressed as:

$$I_1 = \begin{cases} I_{REF} & I_X \le I_L \\ -m\cdot(I_X - I_R) & I_L < I_X < I_R \\ 0 & I_R \le I_X \end{cases}$$

$$I_2 = \begin{cases} 0 & I_X \le I_L \\ m\cdot(I_X - I_L) & I_L < I_X < I_R \\ I_{REF} & I_R \le I_X \end{cases} \tag{5}$$

$$m = \frac{I_{REF}}{I_R - I_L}$$

The parameter m represents the slope of these currents and it can be adjusted by means of the I_L and I_R values, if one of these currents together with I_{REF} are fixed. The height of the output currents is controlled by the I_{REF} value. Thus, the basic cell has the capability to generate various shaped output currents. This ability can be used to built a highly programmable fuzzyfication circuit.

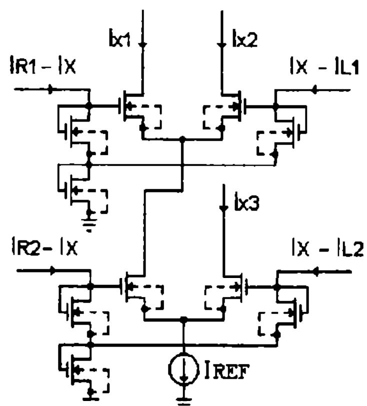

Fig.5. The fuzzyfication circuit.

In the Fig.5 is presented a fuzzyfication circuit that generates three membership functions. More membership functions can be generated by stacking another basic cells in a similar manner as the one shown in Fig.5. Various shaped membership functions can be obtained by adjusting the parameters $I_{L1,2}$ and $I_{R1,2}$. As a general rule, for a proper operation of the fuzzyfication ciruit, $I_{Rk}<I_{Lk+1}$ must be fulfilled. If $I_{Rk}=I_{Lk+1}$, triangular membership functions are generated, otherwise trapezoidal membership functions are generated (when $I_{Rk}<I_{Lk+1}$). If $I_{Rk}-I_{Lk}=I_{Rk+1}-I_{Lk+1}$ symmetric membership functions are generated, otherwise asymmetric membership functions are generated (when $I_{Rk}-I_{Lk} \neq I_{Rk+1}-I_{Lk+1}$). Based on the operation of the basic cell, the membership functions expressed by means of the currents I_{X1} and I_{Xn} (I_{Xn} is I_{X3} in Fig.5) have a Z shape and a S shape respectively. Another important feature of this circuit is the generated membership functions always form a fuzzy partition over the universe of discourse. This was one of the requirements of the proposed architecture.

V. THE MULTIPLIER CELL

This cell outputs the individual contribution of a fuzzy rule as a result of the multiplication between the firing degree and the consequent of the considered rule. Moreover, the firing degree is computed as the multiplication between the alpfa values located in the premise of the rule. Thus, at this level is implemented the implication function and the AND logical connective, that connects the antecedents of the premise. A three inputs multiplier cell can be obtained by stacking two basic cells and replacing the currents I_3 and I_4 as it is shown in the Fig.6. I_{xi} and I_{yj} stand on the alpha values, generated for the actual values of the inputs X and Y respectively and I_{ck} represents the consequence of a fuzzy rule. The current I_{REF} is the supply current value used in the fuzzyfication circuit. If I_{xi} and $I_{REF}-I_{xi}$ are positive currents, from relation (5) it can be stated that:

$$I_D = \frac{I_{ck}\cdot I_{xi}}{I_{REF}} \tag{6}$$

Also, on the base of the same relation, the output current $I_{\beta K}$ of the multiplier cell can be expressed as:

$$I_{\beta K} = \frac{I_D \cdot I_{yj}}{I_{REF}} = I_{xi}\cdot I_{yj}\cdot I_{ck} \tag{7}$$

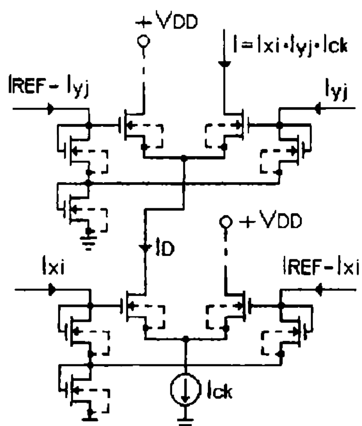

Fig.6. The three inputs multiplier cell.

VI. SIMULATION RESULTS

Finally, we have extended the fuzzyfication circuits to generate five membership functions and we have developed an architecture for a complete fuzzy rule base, expressed as in the Table.1.

Table 1. The fuzzy rule base; (the consequences are: PB=45nA, PS=35nA, Z=25nA, NS=15nA, NB=5nA).

Y \ X	NB	NS	Z	PS	PB
NB	PB	PS	Z	NS	NB
NS	PB	PS	Z	NS	NB
Z	PB	PS	Z	NS	NB
PS	PB	PS	Z	NS	NB
PB	PB	PS	Z	NS	NB

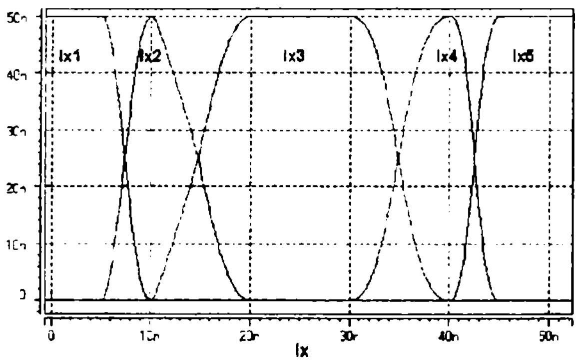

Fig.7. The Hspice simulation of the fuzzyfication circuit. $I_X \in [0nA, 50nA]$; $I_{REF}=50nA$; $I_{L1}=5nA$, $I_{R1}=10nA$, $I_{L2}=10nA$, $I_{R2}=20nA$, $I_{L3}=30nA$, $I_{R3}=40nA$, $I_{L4}=40nA$, $I_{R4}=50nA$, $I_{REF}=50nA$.

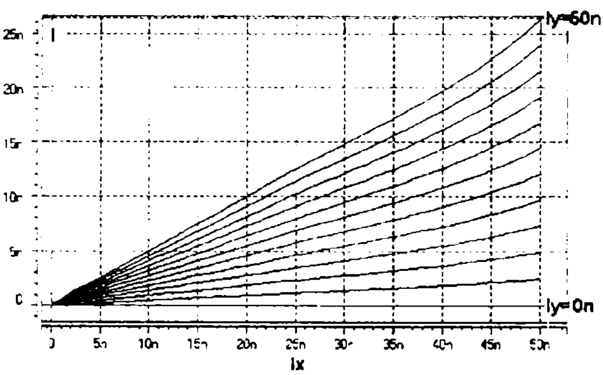

Fig.8. The Hspice simulation of the multiplication cell: $I_X=[0nA \div 50nA]$, $I_Y=[0nA \div 50nA]$, $I_C=25nA$.

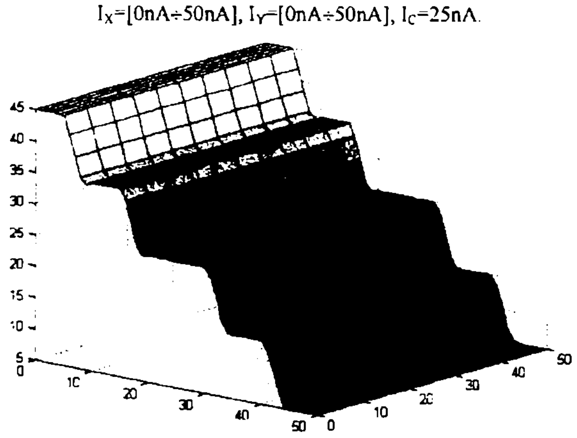

Fig.9. The control surface of the proposed fuzzy logic system (the input fuzzy sets have symmetric, triangular shapes: $I_{REF}=50nA$, $I_{L1}=2nA$, $I_{R1}=17nA$, $I_{L2}=17nA$, $I_{R2}=32nA$, $I_{L3}=32nA$, $I_{R3}=47nA$, $I_{L4}=47nA$, $I_{R4}=62nA$.

We have tested the fuzzyfication circuit, the multiplier cell and the fuzzy logic system by various Hspice [6] simulations. The circuits were simulated in AMI 0.5u technology. The simulation results were confirmed the functionality of the proposed architecture, as it can be seen from Fig.7, Fig.8 and Fig.9 respectively.

VII. CONCLUSIONS

This work has proposed a current mode parallel architecture of a fuzzy logic system. It involves MOS transistors operating in the weak inversion region. This feature allows low power solutions for the system integration. Also, the architecture is highly programmable that makes it suitable for neuro-fuzzy system implementations.

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