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DC-DC Converter in Which the Duty Factor is Controlled by the Capacitor Voltage

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Abstract – The d.c.-d.c. converters, which assure the conversion from d.c.-d.c., have both at the input and at the output, different values for the voltages and the continuous currents. In most cases, the output voltages must remain constant when the input voltage and the load resistance change within certain limits. The paper analyses the variation of the output voltage when the input voltage presents relatively small variations in time and suggests a PWM command solution for the minimization of these variations.

Keywords: converter dc-dc, PWM control, Pspice.

I. INTRODUCTION

Because of their high performances, the d.c.-d.c. converters they have been widely used in many fields. In order to achieve these performances, there were two major objectives, which imposed themselves in time namely: the creation of converters in which the conversion efficiency is closer to the ideal one and the reduction of the mechanical dimension. When we study the functioning of the d.c. converters in dynamic regime, we are interested especially in their behavior, when the duty factor (D) varies. Usually, when the power supply V_{IN} varies the duty factor varies too, from one period to another.

In addition to [1-3], we shall analyze the behavior of the step-down and step-up converters in continuous conduction mode (CCM), which contain real circuit elements. The inductor will have a series resistance R_L and the capacity a resistance R_C. The power supply V_{IN} presents periodical variations in time ($\pm\Delta V_{IN}$) for constant commutation frequency and a fixed load resistance.

II. FUNDAMENTAL CONVERTERS TOPOLOGIES

Fig.1. shows the topology of the step-down converter containing real circuit elements.

These continuous current converters have the function of realizing constant voltages at the output even if the input voltages changes. In the case of the step-down converter, the output voltage is constant and smaller that the input voltage.

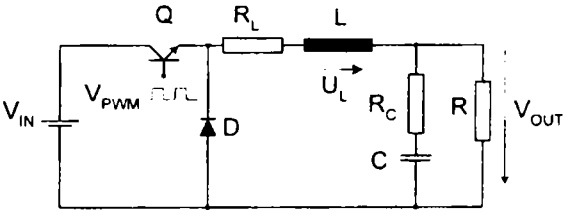

Fig.1 Step-down power stage whit parasitic included

During a period of functioning T , the circuit present two equivalent circuits. When the transistor Q is in conduction, the diode D is turned off and the current through the inductance grows; implicitly, the energy accumulated in the inductance grow, as well as, the capacitor voltage. The load resistance will have the voltage V_{OUT}.

As the inductance function as a current source, when the transistor Q is turned off, the diode D turned on assuring a current through the load; thus, the energy accumulated in the induction drop, determining a reduction of the current.

It is important to mention that, irrespective of the equivalent circuit, the current will permanently flow through the load, that is the converter will function in continuous conduction mode (CCM). The output capacitor C together with L form a low-pass LC filter which has the role of reducing the ΔV_{OUT} perturbations of the output voltage. In order to maintain constant the output voltage even if the power supply varies, we have to modify the duty factor and to keep the commutation frequency constant.

By applying the method of the averaged model for the study of the dynamic regime [4], every converter can be mathematical described with the following equations:

$$X = -A^{-1}bV_{IN};\quad Y = c^T x = -c^T A^{-1} b V_{IN} \qquad (1)$$

- *statically d.c. model*

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$$\dot{x} = A\hat{x} + b\hat{v}_{IN} + [(A_1 - A_2)X + (b_1 - b_2)V_{IN}]\hat{d}$$
$$\hat{y} = c^T\hat{x} + (c_1^T - c_2^T)X\hat{d} \quad (2)$$

- *dynamically d.c. model (small signal)*, where :

$$A = DA_1 + D'A_2$$
$$b = Db_1 + D'b_2$$
$$c^T = Dc_1^T + D'c_2^T \quad (3)$$
$$D(t) = D + \hat{d};\ D' = 1 - D$$
$$v_{IN} = V_{IN} + \hat{v}_{IN};\ \hat{d} = D_1; D_2$$

X- state-space vector; A_1, A_2 switched model matrices; b_1, b_2 control vectors; D duty ratio; d perturbation duty ratio; y the output.

Taking into account the equivalent circuit of the converter and the equations (1), (2) and (3) static and dynamic regime of the buck converter is described by the following equations:

$$X = -A^{-1}bV_{IN} =$$
$$-\begin{bmatrix} -\dfrac{RR_L + R_LR_C + RR_C}{L(R+R_C)} & -\dfrac{R}{L(R+R_C)} \\ \dfrac{R}{C(R+R_C)} & -\dfrac{1}{C(R+R_C)} \end{bmatrix}^{-1}\begin{bmatrix} \dfrac{D}{L} \\ 0 \end{bmatrix}V_{IN} \quad (4)$$

$$V_{OUT} = c^TX = -c^TA^{-1}bV_{IN} =$$
$$= -\begin{bmatrix} R//R_C & \dfrac{R}{R+R_C} \end{bmatrix}\cdot$$
$$\begin{bmatrix} -\dfrac{RR_L + R_LR_C + RR_C}{L(R+R_C)} & -\dfrac{R}{L(R+R_C)} \\ \dfrac{R}{C(R+R_C)} & -\dfrac{1}{C(R+R_C)} \end{bmatrix}^{-1}\begin{bmatrix} \dfrac{D}{L} \\ 0 \end{bmatrix}V_{IN}$$

- averaged model of the stationary regime.

$$\hat{x} = \frac{d}{dt}\begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} = \begin{bmatrix} -\dfrac{RR_L + R_LR_C + RR_C}{L(R+R_C)} & -\dfrac{R}{L(R+R_C)} \\ \dfrac{R}{C(R+R_C)} & -\dfrac{1}{C(R+R_C)} \end{bmatrix}\begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix}$$
$$\pm\begin{bmatrix} \dfrac{D}{L} \\ 0 \end{bmatrix}\Delta V_{IN} \pm \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}V_{IN}\hat{d}$$
$$\hat{y} = v_{OUT} = c^Tx = \begin{bmatrix} R//R_C & \dfrac{R}{R+R_C} \end{bmatrix}\begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} \quad (5)$$

- averaged model of the dynamic regime.

Fig. 2. presents the topology of the step-up converter with real circuit elements. As it's name shows it, the step-up converter increases the voltage, the value of the average output voltage being greater that the power supply. When the transistor Q is in conduction, the input voltage supplies energy to the inductance L. The diode is reversal polarized and, thus turned off, and the capacitor C is discharged to the load R, assuring at the output the constants voltages V_{OUT}. When the transistor is blocked the diode D enters in conduction and the voltage accumulated on the inductance adds to the power supply and is transferred to the capacitor and to the load.

By applying the method of the averaged model of step-up converter is:

- averaged model of the stationary regime.

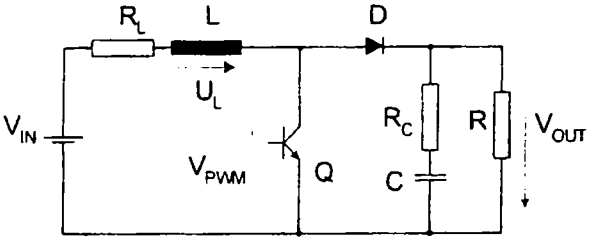

Fig.2. Step-up power stage whit parasitic included

$$X = -A^{-1}bV_{IN} =$$
$$-\begin{bmatrix} -\dfrac{R_L + (1-D)R//R_C}{L} & -\dfrac{(1-D)R}{L(R+R_C)} \\ \dfrac{(1-D)R}{C(R+R_C)} & -\dfrac{1}{C(R+R_C)} \end{bmatrix}^{-1}\begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}V_{IN};$$
(6)
$$V_{OUT} = c^TX = -\begin{bmatrix} (1-D)(R_C//R) & \dfrac{R}{R//R_C} \end{bmatrix}\cdot$$
$$\begin{bmatrix} -\dfrac{R_L + (1-D)R//R_C}{L} & -\dfrac{(1-D)R}{L(R+R_C)} \\ \dfrac{(1-D)R}{C(R+R_C)} & -\dfrac{1}{C(R+R_C)} \end{bmatrix}^{-1}\begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}V_{IN};$$

- averaged model of the dynamic regime.

$$\frac{d\hat{x}}{dt} = \begin{bmatrix} \dfrac{d\hat{i}}{dt} \\ \dfrac{d\hat{v}}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_L + (1-D)R//R_C}{L} & -\dfrac{(1-D)R}{L(R+R_C)} \\ \dfrac{(1-D)R}{C(R+R_C)} & -\dfrac{1}{C(R+R_C)} \end{bmatrix}\begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} +$$
$$\pm\begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}\Delta V_{IN} \pm \begin{bmatrix} \dfrac{(1-D)R^2 + RR_C}{L(R+R_C)} \\ -\dfrac{R}{L(R+R_C)} \end{bmatrix}\cdot$$
$$\cdot\frac{V_{IN}\hat{d}}{(1-D)^2R + R_L + D(1-D)R//R_C} \quad (7)$$

$$\hat{y} = v_{OUT} = \left[(1-D)R \,//\, R_C \quad \frac{R}{R = R_C} \right] \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} \pm$$

$$\pm \frac{V_{L..} R \,//\, R_C \cdot \hat{d}}{(1-D)^2 R + R_l + D(1-D)R \,//\, R_C} \qquad (8)$$

III. COMMAND STRATEGIES

The controller in Fig. 3. consists of an error amplifier, PWM modulator, constant frequency saw-tooth ramp (V_{Ctr}), reference voltage (V_{ref}) and voltage divider (R_{r1},R_{r2}). The divider is used to scale down the sensed output voltage V_{OUT} so that it can be compared to reference voltage V_{ref}, at the input of the error amplifier. The voltage at the output of the error amplifier, which is proportional to the error (difference) between the scaled output voltage and reference voltage, is then compared to generate a signal with desirable duty cycle to drive the switch.
The output volta_e is adjusted so that, if the output voltage tends to increase, the output voltage of the error amplifier drop, as well as the duty factor D. In these conditions, the conduction duration of the driver PWM transistor, well remain constant at the chosen value, which is obtained through the feedback. The frequency of the saw-tooth generator V_{Ctr} is constant and has linear and constant positive slope.

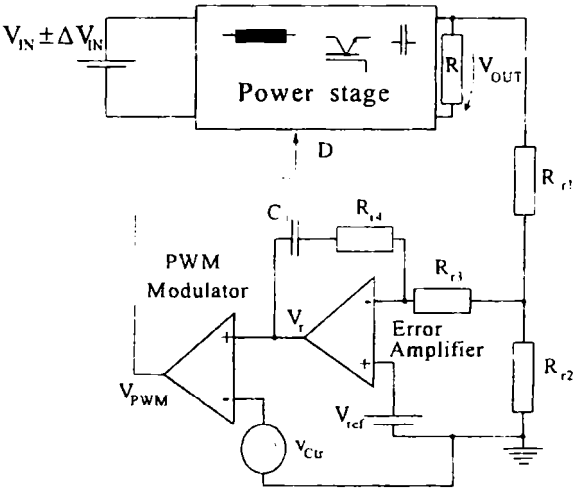

Fig.3 Conventional block output-voltage-feedback control scheme

Compensation resistant (R_{r3}, R_{r4}) and capacitate C_r of the error amplifier are used to provide a proper gain, bandwidth, and frequency compensation of the loop so that the loop is stable for all operating conditions.
Fig. 4. presents the main waveforms determined by the functioning of the circuit in Fig. 3. the supply voltage V_{IN}, the output voltage V_{OUT}, the voltage V_r at the output of the error amplifier, the saw-tooth signal V_{Ctr} and command signal at the output of the modulator PWM. Suppose that, at the moment t_1, the supply voltage increases by ΔV_{IN}, for a short time. In these conditions we can notice in the Fig. 4. that, the sudden increase of the supply voltage, disturbs heavily the output voltage V_{OUT}, with ΔV_{OUT}

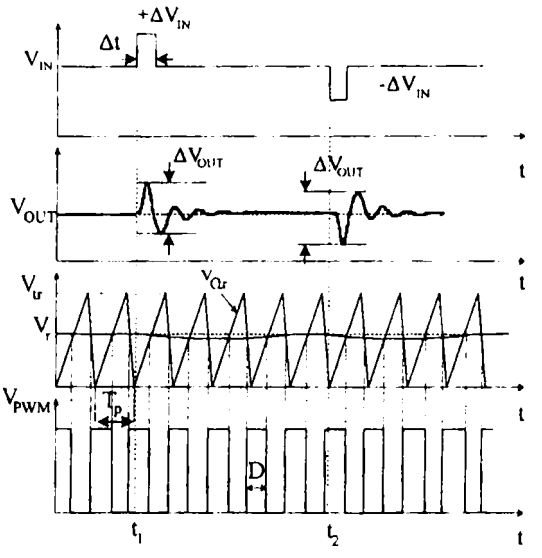

Fig.4 Waveforms during occurs ΔV_{IN} perturbation

Because of the short-term variations of the power supply, the system consisting of: the output voltage, feedback and command signal has a slow response.
The phenomenon can be easily explained following .he ...efo.m.. The ....on of .he .ol..ge .IN determines a slight modification of the voltage at the output of the error amplifier V_r, which leads to an insignificant modification of the duty factor D.

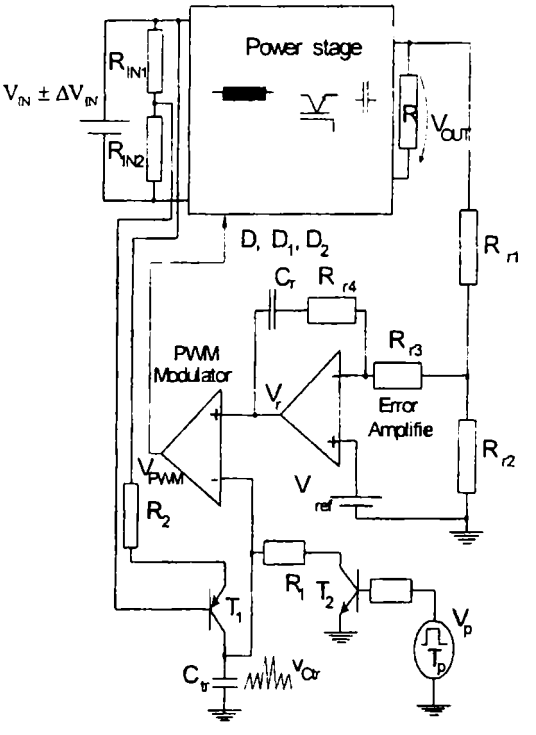

Fig.5. Proposed block output-voltage-feedback control scheme

Consequently, there will be oscillations in the waveform of the output voltage with great short time perturbations (ΔV_{OUT}), which disappear in time towards the output voltage, which is constant.

In Fig.5. presents the proposed circuit for the correction of the over voltages which appear in the output voltage. The proposed circuit is similar to the one in Fig. 3., but in this case the saw-tooth signal is taken aver from the capacitor C_{tr}. The capacitor is charged from the input voltage divider, the resistor R_2 and the transistor T_1.

The discharge of the capacitor is made through the resistor R_1 and the transistor T_2. The switching (T_p) frequency of the converter, whose period is constant is fixed by the pulsate voltage source(V_p) used to command the transistor T_2. The functioning of the circuit can be easily explained by analyzing the waveforms presented in Fig. 6. The positive step voltage, which appears in the power supply at the moment t_1, is quickly identified on the resistive divider R_{IN1}, R_{IN2} too, determining a positive slope in the charging of the capacitor C.

From the waveforms of the capacitor voltage, we can ~~notic~~ that, the positive slope appears only when we ave over voltage (of the power supply), the period of the saw-tooth command signal of the capacitor C_{tr}, remaining constant for all the functioning duration.

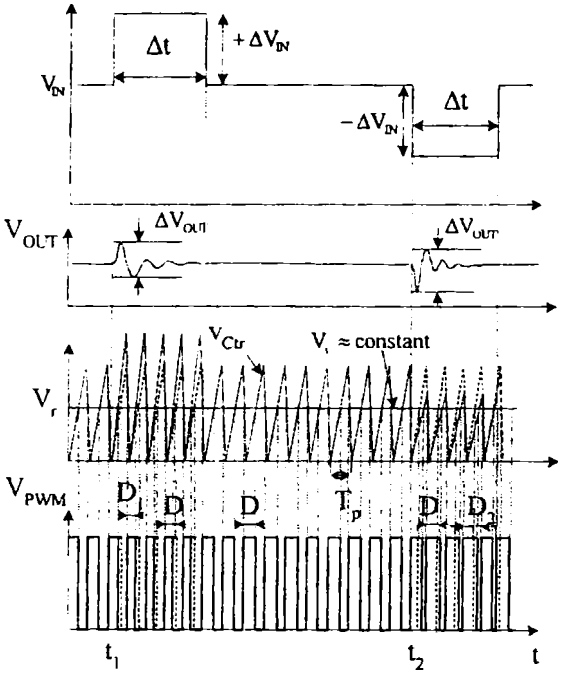

Fig.6 Waveforms during occurs $\pm\Delta V_{IN}$ perturbation for proposed circuit

The output voltage of the error amplifier V_r, remains approximately constant, by comparison with the Vc_{tr} voltage, a command signal V_{PWM} will appear. Where the duty factor D, doesn't remain constant of the entire period of functioning. The feedback of the system is prompt in this case, because, when the output voltage tends to increase, the positive slope of the voltage used to charge the capacitor C will determine a smaller duty factor D, which becomes D'; thus , the conduction duration of the transistor (which is implemented into the switch) will diminish, realizing an adjustment of the output voltages.

IV. SIMULATION RESULTS

The step-down (buck) converter proposed for the simulation, has an inductance L = 330uH, C = 330uF, R_L = 0,25 ohm, R_C = 0,1 ohm, a load resistance R = 4 ohm, a power supply V_{IN} = 15V, ΔV_{IN} = ±5V and V_{OUT} =7.5 V. The switching frequency is constant at the f_p = 10kHz value. Fig. 7. shows $V_{IN} \pm \Delta V_{IN}$ and V_{OUT} obtained by simulations using the command method presented in Fig.3

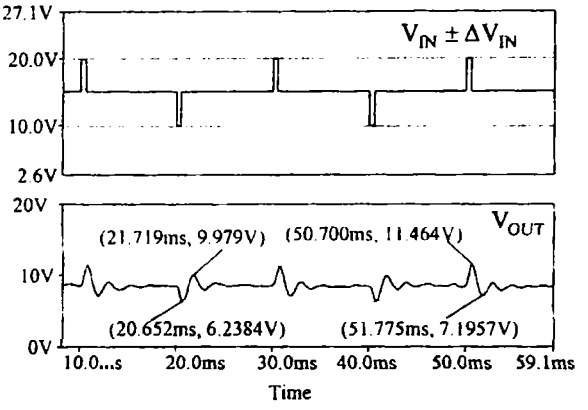

Fig.7. Simulated waveforms output voltage and of the power supply for a conventional command

Fig. 8. Simulated waveforms for the voltages: V_{Ctr}, V_r and V_{PWM} using the command method presented in Fig.3

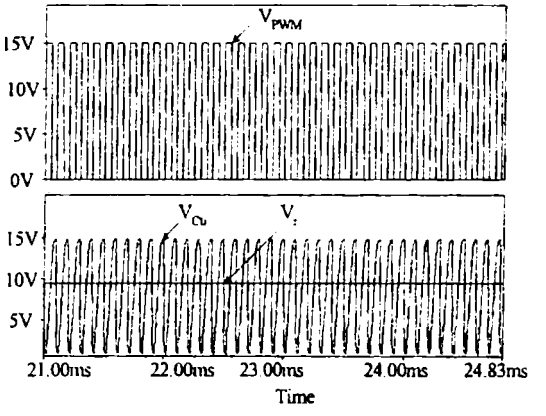

Fig.8. Simulated waveforms for V_{PWM}, and V_{Cu} , V_r for a conventional command

Fig. 9 shows the waveforms of the output voltage and of the power supply for the same step-down converter, but this case, the command strategy is realized as in the proposed circuit presented in the

Fig. 5. Fig. 10 presents the waveforms for the

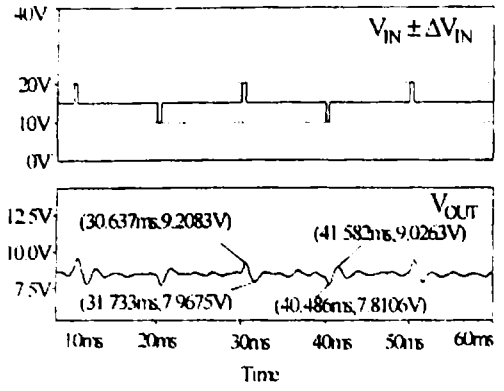

Fig 9 Simulated waveforms output voltage and of the power supply for a proposed

voltages: V_{Ctr}, V_r and V_{PWM} obtained by simulations.

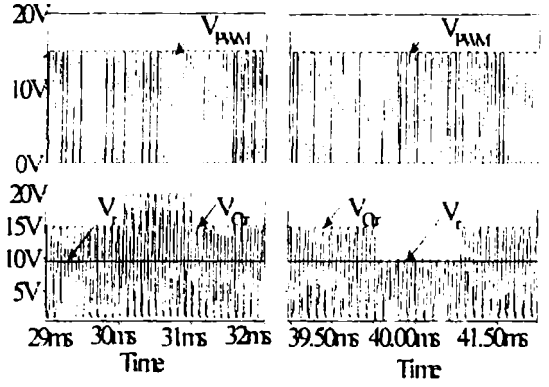

Fig 10 Simulated waveforms for V_{PWM} and V_{Ctr}, V_r for a proposed command

The step-up converter proposed for the simulation, has an inductance L = 280uH, C = 500uF, R_L = 0,2 ohm, R_C = 0,1 ohm, a load resistance R = 4 ohm, a power supply V_{IN} = 15V, which is periodically disturbed at each 20ms with a voltage ΔV_{IN} = ±5V, V_{OUT} = 27V. The switching frequency is constant at the f_p = 10kHz value.

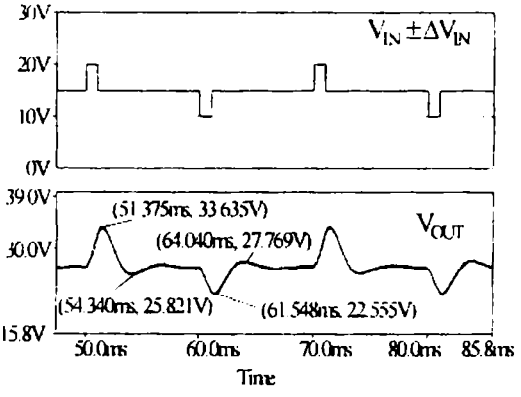

Fig 11 Simulated waveforms output voltage and of the power supply for a conventional command

Fig. 11 presents the waveforms of the output voltage and of the power supply, using the command method presented in Fig. 3

Fig. 12 shows the waveforms of the output voltage and of the power supply for the same step-up converter, but this case, the command strategy is realized as in the proposed circuit presented in the Fig. 7.

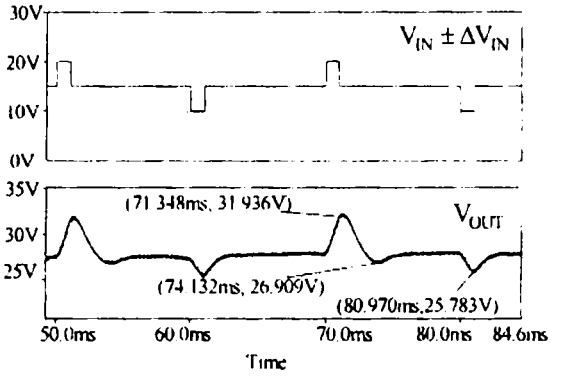

Fig 12 Simulated waveforms output voltage and of the power supply for a proposed command

CONCLUSIONS

By analyzing the waveforms of the output voltages of the buck converter, obtained by these two PWM strategies, we can notice that in the first situation $\Delta V_{OUT} \approx 4$ V and in the second one when we apply the correction of the duty factor D, $\Delta V_{OUT} \approx 1$ V. Also, in the case of the step-up converter, using the same command strategies as for the buck converter, we will obtain an improvement correction of the output voltage in the case of negative perturbations of the power supply . Analyzing the values of the ΔV_{OUT} variations we can say that the short-term perturbations of the power supply determine important changes in output voltages, which can be easily adjust without using input filters for the correction of the power supply.

REFERENCES

[1] J. Yungtack and M. M. Jovanovic, A new input-voltage feedforward harmonic-injection technique with nonlinear gain control for single-switch, three-phase, DCM boost rectifiers IEEE Transaction on Power Electronics vol. 28, pp. 268-277, march 2000

[2] I. Calderone, I. Pinola and V. Varioli, Optimal feed-forward compensation for PWM DC/DC converters with "linear" and "quadratic" conversion ratio IEEE Transaction on Power Electronics vol. 7, pp. 349-355, Apr. 1992.

[3] B. Arbetter and D. Maksimovic, Feed-forward pulse-width modulators for switching power converters, in Proc. IEEE Power Electron. Spec. Conf. (PESC) Record, 1995, pp. 601-607

[4] R. D. Middlebrook and Slobodan Cuk, A general unified approach to modeling switching-converter power stages. IEEE Power Electron. Spec. Conf. (PESC) Rec., pp. 18-34, 1976.