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Digital Video Broadcasting Terrestrial Modulator Implemented on Motorola MSC8101 DSP

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Abstract – This paper presents implementation aspects of a DVB-T modulator on MSC8101 Motorola DSP. It gives a general description of the DVB-T system, but it also identifies all the main processes applied to the data stream: starting with transport multiplex adaptation and energy dispersal, outer coding and outer interleaving, inner coding and inner interleaving, mapping and signal modulation, OFDM transmission.
Keywords: DVB-T modulator.

I. INTRODUCTION

Digital Video Broadcasting (DVB) is a term that is generally used to describe digital television and data broadcasting services that comply with the DVB "standard". The potential advantages of digital television broadcasting over conventional analogue broadcasting are numerous and well known. For the broadcaster, digital technology offers significantly improved operational flexibility, providing the means for completely new services that go beyond the scope of conventional television programs. Important benefits concern the broadcasting infrastructure, with better integration with the digital studios and playout centers and, thanks to digital compression, more efficient use of the broadcast spectrum. The viewer become an active participant in the broadcasting process, having generally improved video and audio quality, improved program and service choice, better navigational aids to facilitate the choice between the various services on offer and greater control over content delivery.

In fact, there is no single DVB standard, but rather a collection of standards, technical recommendations and guidelines (DVB-S and DVB-C for satellite and cable). The established MPEG-2 standard was adopted in DVB for the source coding of audio and video information and for multiplexing a number of source data streams and ancillary information into a single data stream suitable for transmission. DVB-T standard defines a system performing the adaptation of the baseband TV signals from the output of the MPEG-2 transport multiplexer to the terrestrial channel characteristics. Actually, DVB technology allows the broadcasting of "data containers", in which all kinds of digital data can be transmitted: compressed image, sound or data. Comparing to other data broadcasting systems, a key difference in DVB is that the different data elements within the container can carry independent timing information. This allows audio information to be synchronized with video information in the receiver, even if the video and audio information does not arrive at the receiver at exactly the same time.

The DVB standard also provides flexibility. For example, a 38 Mbit/s data container could hold eight standard definition television (SDTV) programs, four enhanced definition television programs (EDTV) or one high definition television (HDTV) program or 550 ISDN channels, all with associated multi-channel audio and ancillary data services.

This paper presents implementation aspects of a DVB-T modulator on MSC8101 Motorola DSP. It gives a general description of the DVB-T system, but it also identifies all the main processes applied to the data stream: starting with transport multiplex adaptation and energy dispersal, outer coding and outer interleaving, inner coding and inner interleaving, mapping and signal modulation, OFDM transmission.

Tests were performed both using Matlab and CodeWarrior C interface for MSC8101 processor in conformity with ETSI EN 300 744 standard (Digital Video Broadcasting framing structure, channel coding and modulation for digital terrestrial television).

II. DVB-T MODULATOR SYSTEM

The DVB-T system addresses the terrestrial broadcasting of MPEG-2 coded TV signals. Therefore an appropriate adaptation of the digital coded transport stream to the different terrestrial channel characteristics is necessary. These requirements result in a flexible transmission system that uses a multi-carrier modulation, the so called Orthogonal Frequency Division Multiplex (OFDM) technique, combined with a powerful concatenated error correction coding (Coded Orthogonal Frequency Division Multiplex, COFDM).

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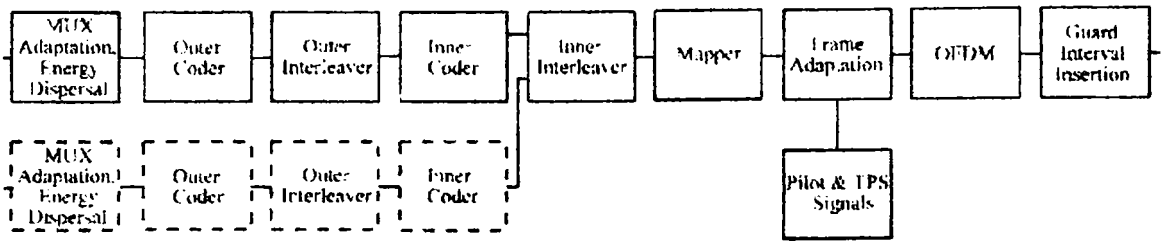


Fig. 1. Transmitter block diagram

In the modulator system (Fig. 1), the following processes shall be applied to the data stream: transport multiplex adaptation and randomization for energy dispersal, outer coding (Reed-Solomon code), outer interleaving (convolutional interleaving), inner coding (punctured convolutional code), inner interleaving, mapping and modulation, Orthogonal Frequency Division Multiplexing (OFDM) transmission.

Since the system is designed for digital terrestrial television services to operate within the existing VHF and UHF (Very and Ultra-High Frequency) spectrum allocation for analogue transmissions, it is required that the system provides sufficient protection against high levels of Co-Cannel Interference emanating from existing PAL/SECAM/NTSC services.

It is also a requirement that the system allows the maximum spectrum efficiency when used within the VHF and UHF bands; this can be achieved by using Single Frequency Networks (SFN) operation.

In fact, two modes of operation are defined in the OFDM technique with two options in the number of carriers: a "2K mode" and an "8K mode". The "2K mode" is suitable for single transmitter operation and for small SFN networks with limited transmitter distances. The "8K mode" can be used both for single transmitter operation and for small and large SFN networks.

As far as bandwidth requirements are concerned, the preferred channel spacing is 8 MHz, but if desired, 7 MHz or 6 MHz spacing is also possible by scaling down all system parameters.

The error correction can be separated in two blocks: the outer coding and outer interleaving that are common to the Satellite and Cable Baseline Specifications (DVB-S and DVB-C) and the inner coding is common to Satellite Baseline Specifications. The use of inner interleaving is specific to the DVB-T system.

To accommodate different transmission rates, in addition to five code rates, three types of non-differential modulation schemes can be selected: QPSK, 16-QAM and 64-QAM. The 16-QAM and 64-QAM can also be used in combination with uniform or non-uniform mapping rules and thus input data streams can be separated in a low and a high priority data stream with different error protection for hierarchical transmission purposes. These two bitstreams are mapped into the signal constellation by the Mapper and Modulator. This feature allows the simultaneous broadcasting of different programmes with different error protection and coverage areas.

III. IMPLEMENTATION ASPECTS

A. *Motorola MSC8101 DSP Performances*

The family of the MSC8101 processor implements a new model of instructions' execution called VLES (Variable Length Execution Set), which allows in general the usage of more parallels addressing and computing units, during the same cycle.

The next lines present the most important features of the present processor as following:

- up to 10 MIPS (Million Instructions Per Second) for every Mhz frequency;
- 4 ALU (Arithmetic Logic Unit) which include dedicated circuits for addition, multiplication and bit operating units;
- in every ALU there a presented MAC (Multiply and ACcumulate) and shifter units.

Concerning the registers, the MSC8101 processor presents next features:

- 16 registers of 40 bits length used for integers and fractional operations;
- 16 register for addressing of 32 bits length, from which 8 bits can be used for generating base addresses in buffers;
- 4 offset registers for addressing and 4 registers for circular addressing.

Some other features of this DSP are about the presence of the orthogonal instruction set coded on 16 bits; the possibility of executing up to 6 instructions in one cycle. Another important feature of the MSC8101 is that it has a CMOS logic which allows reduced power consumption.

B. *Transmitter blocks implementation*

DSP implementation consists on processing each MPEG-2 transport packet of 188 bytes. Outer coding is formed by a RS encoder (204,188) followed by a 12 stages interleaver. Inner coding is a convolutional code of rate ½. The output from convolutional encoder can be optionally punctured. Accordingly, the overall convolutional code rate is 1/2, 2/3, 3/4, 5/6 or 7/8. Interleaving is performed here both bit-wise and symbol-wise. Former is done depending on the symbol rate (bits/symbol), based on typical permutation operators. The symbol-wise interleaver maps the bit words onto the active subcarriers. Every carrier is modulated by a modulation symbol. QPSK, 16-QAM and 64-QAM are used as modulation methods, e.g. 2, 4 or 6 bits per modulation symbol.

The bits are assigned to the particular points in the phase space according to the so called Gray-code mapping. The advantage of this mapping is the fact that closest constellation points differ only in one bit.
Each frame is formed by 68 OFDM symbols. Four frames constitute one super-frame. Each symbol is formed by 6817 samples in 8K mode and 1705 subcarriers in 2K mode. The symbol is formed by applying an IFFT operator to the 8K/2K samples resulted as the data samples, intercalated with pilot samples and zero subcarriers. A computational efficient radix 4 IFFT algorithm was implemented to be used both in 2K or 8K modes in order to achieve time requirements for a real-time processing.

The *transport multiplex adaptation and randomization block* consists of a shift register of 16 cells that randomizes input data and derandomizes received data. Randomization is done for the 187 bytes within each transport packet. The sync byte from the beginning of each packet is not randomized. The scrambling operation consists in a logical XOR function between input data and a scrambled sequence. We used for performing the data processing two buffer of 1504 bytes length. Since the scrambling is not applied to the sync byte, we modified the content of the scrambled sequence for bytes having the index 0, 188, 2*188 and so on with 0x00.

Each transport packet of 188 bytes enters a *Reed-Solomon encoder* (204,188) in order to become an error protected packet. The Reed-Solomon code allows to correct up to 8 random erroneous bytes in a received word of 204 bytes. An alternative RS (255,239) may be approached, by adding 51 zeros at the beginning of the information word, discarded after RS coding procedure. The software implementation is about computing of 16 parity bytes and appending them to the end of one bloc data of 188 bytes length. In order to perform this operation which is based on the input bloc data of 188 bytes we used according to the standard an a-logarithmic table and a table which describes the coding polynomial.

The *outer interleaving* represents the next data processing bloc in the entire chain of the data computing. Due to the working way of this interleaver, for a software implementation we simulate its functionality basing only on the circular addressing capabilities of the DSP.
The next module of the data processing chain is about the *inner coding*. This bloc works together with a puncturing which describes the way of how the output data from a base inner convolutional code of rate 1/2 are passing for obtaining other coding rates. The system allows punctured rates of 2/3, 3/4, 5/6 or 7/8 in addition to the mother code of rate 1/2.
The algorithm used for implementing the base inner coding is based on a logical XOR performed between the content of different delay registers. Due to the fact that this block can work with different rate we take

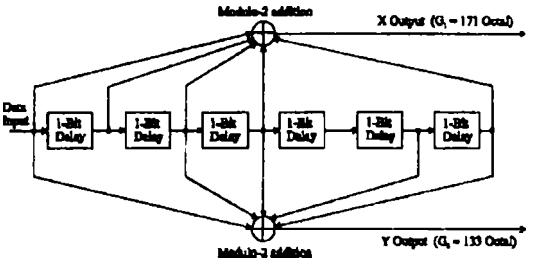


Fig. 2. Convolutional encoder

into account for the output buffer the maximum length which is about 1632 elements. This number of bits is obtained from the next relation:

$$Number_{bits} = 204_{bytes} \cdot 8_{bits/octet} \cdot \frac{1}{rate} \qquad (1)$$

where rate is ½.

Inner interleaving is performed here bit-wise followed by symbol interleaving. Former is done depending on the symbol rate (bits/symbol), based on typical permutation operators. The symbol interleaver maps the bit words onto the active subcarriers.
First interleaving, which is performed at the bit level, requires several interleaving schemes. We used for the data storage up to 6 tables. Also we have to keep in mind that, according to the standard, the input data is split in 2, 4 or 6 pieces (as the modulation is QPSK, 16-QAM, or 64-QAM) and after that on each sub-stream it was applied the interleaving algorithm.
Next block is also about the interleaving which is performed at the symbol level. Regarding the implementation in C we used for this two output buffers each one having different length, according to the modulator operation in 2K symbols or 8K symbols. One symbol here is represented by data pairs obtained at the output of the bit interleaver. The new indexes of the symbols are obtained by using an permutation table which contain an pseudo-aleator sequence.

The *symbol mapping* represents the next module and is about assigning to each symbol a complex number, based on the signal constellation corresponding to the QPSK, 16-QAM and respectively 64-QAM. Fig. 3 presents for instance the signal constellation for the QPSK modulation scheme.

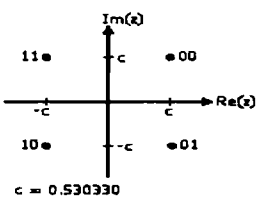


Fig. 3. Signal Constellation for QPSK Modulation

Concerning the implementation, one thing must be underlined here. In the theory the value of c is 1, but

here this value was considerate lower than 1. This is about the fact that the medium energy for 4 signals is:

$$E\{c \times c^*\} = \frac{|1+j|^2 + |1-j|^2 + |-1+j|^2 + |-1-j|^2}{4} = \frac{8}{4} = 2 \quad (2)$$

Due to the fact that the standard states to have a medium energy of 1 and due to the limitations concerning the number representation the value of c is c=0.530330. In a similar way it was processed for the others signal constellations.

Some information for the control of the transmission as continual pilots, scattered pilots and TPS pilots must be inserted in the data streams before the Inverse ast ourier rans orm (IFFT). he implementation of the IFFT that was performed is based on the M-t-r-l- benchm-rk- lg-rithm. This is a-o-t of two algorithms one of them, radix 2, used for input vector length of $N=2^M$ and the other on, radix 4, used for vector lengths of $N=4^M$.

Each frame is formed by 68 OFDM symbols. Four frames constitute one super-frame. Each symbol is formed by 6817 samples in 8K mode and 1705 subcarriers in 2K mode. The symbol is formed by applying a IFFT operator to the 8K/2K samples resulted as the data samples, intercalated with pilot samples and zero subcarriers. After IFFT, we pad a cyclic prefix (1/4, 1/16, 1/32, 1/64).

IV. PERFORMANCES

Regarding the performance of the implemented modulator it must be underlined first of all that there was needed to be processed a great amount of data. That is way the cycles burned for performing all the operation contained in the transmission chain have big values for both operating mode of 2K or 8K.

With all of these, it may be said that this modulator work in real time, meaning that it was possible to obtain a number of cycles close to the limit but lower that this. Next figure presents these results together with the cycle burned for each group of functions.

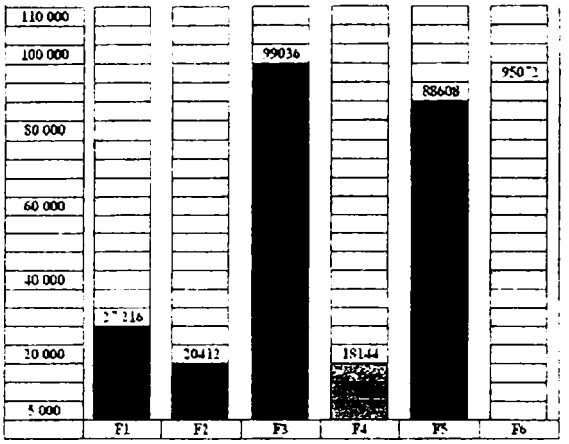
In fig. 3 we denoted with F1...F6 next 6 group of functions:

F1 – Iner Coding Function;
F2 – 1st Interleaving and Convolutional Encode
F3 – Bit Interleaving Function
F4 - Symbol Interleaving Function
F5 – Symbol Mapping Function
F6 – Inverse Fast Fourier Transformer Function

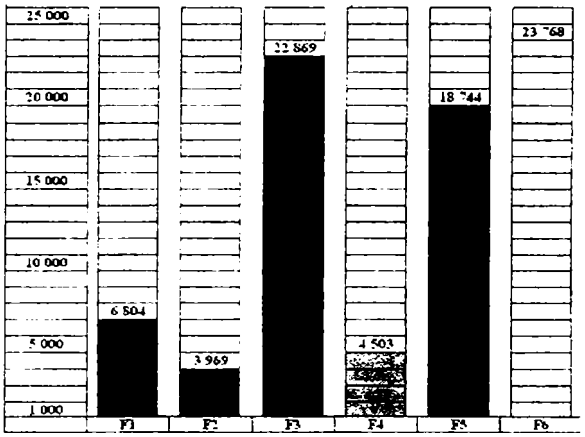
V. CONCLUSIONS

The implementation of the DVB-T modulator represent a complex work due to the fact that on the one hand there are a lot of operation that must be performed and on the other hand due to the great amount of data that have to be processed.

Taking into account that an implementation intends to have a code which is running in a real time, the work becomes more difficult.



2K: execution time ≈ 80 700 cycles out of 79 200



8K: execution time ≈ 348 500 cycles out of 384 000

Fig. 3. Cycles burned for the modulator 2K mode (right) and 8K mode (left)

The target of the cycles count were achieved on the one hand thanks to the MSC8101 capabilities and on the other hand thanks to the optimization technique used in C such as: loop merging, split computation and so on. Even if the implemented solution for the DVB-T modulator, work in real time, due to the fact that we are at the time limit the future development of this work will consists in developing the big cycles burning module in assembling language.

VI. ACKNOWLEDGMENT

Implementations of algorithms presented above were performed using development software and DSP boards donated by Freescale Semiconductor Romania to our University.

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