Compensated CMOS delay cells over process, voltage and temperature variations

Cristian Ionaşcu[1], Dănuţ Burdia[2], Bogdan Dimitriu[3]

Abstract — One of the challenges in digital systems is the distribution of the generated on-chip clock with a small uncertainty. In this paper a high performance compensated delay cell concept it is presented. It is based on a current reference, which is almost insensitive to PVT (process, voltage and temperature) variations. Using this current reference the delay value of the compensated delay cell it is nearly constant over temperature range (-55C to 125C) and voltage range (1.62V to 1.98V). Post layout simulation results shows a ratio for the value of the delay between best case corner and worst case corner smaller than 1.5.
Keywords:

I. INTRODUCTION

Static CMOS inverters are traditionally used for clock buffering due to their simplicity and drive capability with low power consumption. However, CMOS inverters have poor supply-induced delay sensitivity of approximately 1% - delay / 1% - VDD. With long chains, this poor supply-noise rejection of the inverter could result in significant jitter [1]-[7].

The functionality of this device is quite simple and can be easily understood with the aid of the simple switching model of the MOS transistor. This "switching model" consider the transistor as a switch with an infinite off-resistance (for $|V_{GS}| < |V_{TH}|$) and a finite on-resistance (for $|V_{GS}| > |V_{TH}|$). The dynamic response of the inverter is dominated mainly by the output capacitance of the gate, C_L, which is compose of the drain diffusion capacitance of the NMOS and PMOS transistors, the capacitance of connecting wires, and the load capacitance (the input capacitance of the fan-out gates). In order to explain the inverter dynamic behavior we will make use for the transistor switching model. The gate response time is determined by the time needed the capacitor to charge through the resistor Rp or Rn. In fact we have a RC network and the propagation delay of such a network is proportional to it's time constant RC_L. Hence, to have a fast inverter we should keep the output capacitance small or to decrease the on-resistance of the transistors. The second conditions is achieve by increasing the W/L ratio of the device. The on-resistance of the NMOS and PMOS transistor is not constant, but is a nonlinear function of the voltage across the transistor.

A method to compute the propagation delay of the inverter is to integrate the capacitor (dis)charge current.

$$t_p = \int_{v_1}^{v_2} \frac{C_L(v)}{i(v)} dt \qquad (1)$$

with i the (dis)charging current, v the voltage over the capacitor, and v_1 si v_2 the initial and final voltage. The voltage dependencies of the on resistance and the load capacitor are addressed by replacing both by a constant linear element with a value averaged over the interval of interest. An expression for the average on-resistance of the MOS transistor is

$$R_{eq} = \frac{2}{V_{DD}} \int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1 + \lambda V)} dV =$$

$$= \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{7}{9}\lambda V_{DD}\right) \qquad (2)$$

with $I_{DSAT} = k\frac{W}{L}\left((V_{DD} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right)$ (3)

Now, we make appeal to RC network response to a voltage step input that is proportional to the time-

constant of the network, formed by puling-down resistor and the charge capacitor. Hence,

$$t_{pHL} = \ln(2)R_{eqn}C_L = 0.69R_{eqn}C_l \quad (4)$$

Similarly, we can obtain the propagation delay for the low to high transition

$$t_{pLH} = \ln(2)R_{eqp}C_L = 0.69R_{eqp}C_l \quad (5)$$

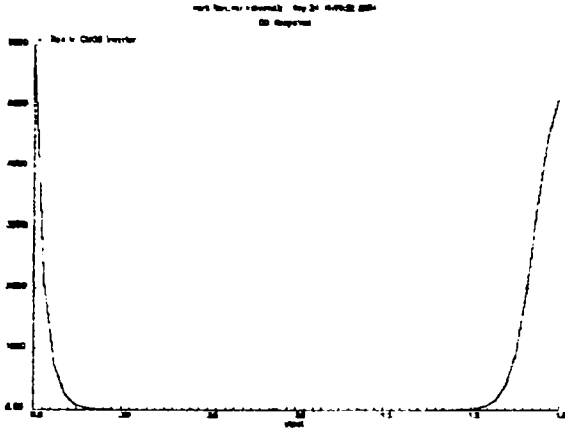## II PROPAGATION DELAY BASED ON THE DESIGNING PERSPECTIVE

Fig. 1 Ron for CMOS inverter

For $V_{DD} \gg V_{TH} + V_{DSAT}/2$ the resistance becomes virtually independent of the supply voltage. This is confirmed by the Fig.1 which plots the simulated equivalent resistance as a function of the $\text{-u}^{-1}\text{--}$ lt g V_{DD}. Only minor improvemen in a resistance due to the channel – length modulation can be observed when raising the supply voltage. Once the supply voltage approaches V_T, a dramatic increase in resistance can be observed.

In order to see the variation of the delay with R_{eq} and C_L we should obtain an explicit expression of the delay with these parameters. In this equation we will consider that the channel–length modulation parameter λ is negligible.

$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSAT_n}} = 0.52\frac{C_L V_{DD}}{(W/L)_n k_n' V_{DSAT}(V_{DD}-V_{THn}-V_{DSAT}/2)} \quad (6)$$

In the majority of designs, the supply voltage is chosen high enough so that $V_{DD} \gg V_{THn} + V_{DSATn}/2$. In this conditions, the delay became virtually independent of the supply voltage.

$$t_{pHL} \approx 0.52\frac{C_L}{(W/L)_n k_n' V_{DSATn}} \quad (7)$$

The load capacitance of the inverter is formed by two components – the intrinsic capacitance (C_{int}) and the extrinsic capacitance (C_{ext}). The intrinsic capacitance is the sum of all diffusion capacitances of the NMOS and PMOS transistors and the gate-drain

overlap capacitances (Miller capacitances). The C_{ext} is the given by the fanout and wiring capacitance.

$$t_p = 0.69R_{eq}(C_{int} + C_{ext}) = 0.69\ R_{eq}C_{int}(1+C_{ext}/C_{int}) \quad (8)$$

The equation above is true for a minimum sized inverter. Taking into account the sizing factor S for a gate formed with transistors S time larger than the minimum sized gate we obtain

$$t_p = 0.69(R_{ref}/S)(SC_{iref})(1 + C_{ext}/(SC_{iref})) =$$
$$= 0.69R_{ref}C_{iref}(1+\frac{C_{ext}}{SC_{iref}}) = t_{p0}(1+\frac{C_{ext}}{C_{iref}}) \quad (9)$$

C_{int} – diffusion and Miller capacitances are both proportional with the with of the transistor ($C_{int} = SC_{iref}$) : R_{eq} - the resistance of the gate relates to the reference gate as $R_{eq} = R_{ref}/S$, [8], [9].

The conclusion that we can draw is that the intrinsic delay of the inverter t_{p0} is independent of the sizing of the gate and is purely determined by technology parmeters and inverter layout.

III THE COMPENSATED DELAY CELL OVER PVT

A. The classical delay cell based on RC network

In the following section will be discussed an uncompensated delay cell based on a RC topology (Fig.2).
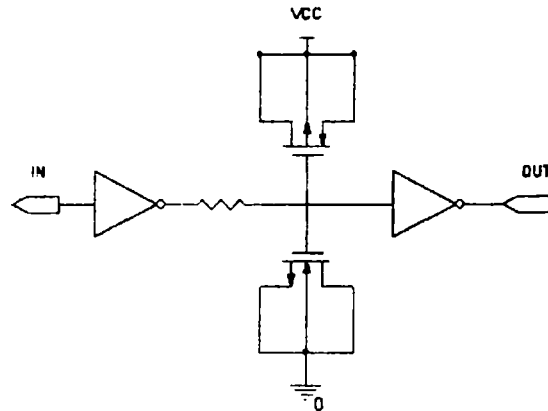

Fig. 2 The RC delay cell schematic

The criteria of estimating the variation of propagation was the best case – worst case report delays and that means that the variation best case with respect to worst case is wished in most of the applications:

$$\frac{t_{pWC}}{t_{pBC}} = 1.5 \quad (10)$$

This delay cell was built in CMOS 0.18μm single N-well salicide process. The resitor is poly without salicide in p implant, bassically it is the most precise

resis'or in 'his 'echono'ogy. The capaci'or wa bui''
based on NMOS and PMOS transitors. The results are
shown in Table 1 using post layout simulation results
with best accuracy – rcc exctracts (resistor and cross
coupled capacitors).

The variation of the propagation delay value is
around 1.7 (the ratio between best case corner and
worst case corner). This result is explained mainly by
the variation of the resistor value and also it is due to
the technology parameters (variation of gate threshold
level with process and temperature, variation of
charging and discharging transient curents for the
MOS capacitors).

This kind of delay cells is used for the
applications were the performances of delay over
PVT are not having much influence over the global
performances of application.

Corner			R (Ω)	C_{load} (Ff)	
				5	
P	V (V)	T (°C)		t↑ (ps)	t↓ (ps)
1.5ns + Poly delay cell					
TT	1.8	25	typ	1832	1907
FF	1.98	-55	low	1595	1543
SS	1.62	125	high	2543	2618
SF	1.98	125	high	1789	2302
FS	1.98	125	high	2055	2020
SF	1.62	125	high	1918	2321
FS	1.62	125	high	2157	2069
SF	1.98	-55	low	1533	1618
FS	1.98	-55	low	1671	1501
‾‾	.	-55	ow	1	1 39
FS	1.62	-55	low	1813	1562
Wc/Bc(t↑)				1.6	-
Wc/Bc(t↓)				-	1.7

Table.1 Post layout results for the RC delay cell

Type	R (Ω)		
	Low (T=-55°C)	typ (T=25°C)	high (T=125°C)
P+poly	5010	6320	7890

Table 2

B. Compensated delay cell line over PVT using a bandgap current

The proposed idea in this paper represents a
better solution for delay propagation over PVT. This
solution has a simple concept but it is difficult to
implement.

The basic idea is to use a nearly constant current
over process voltage and temperature which supplies
a chain of invertes. The global schematic for 1.6ns
delay cell is shown in Fig.3.

According to the schematic there are two
transistors (M1 and M2) that plays the role of the
current sources which must be matched with the same
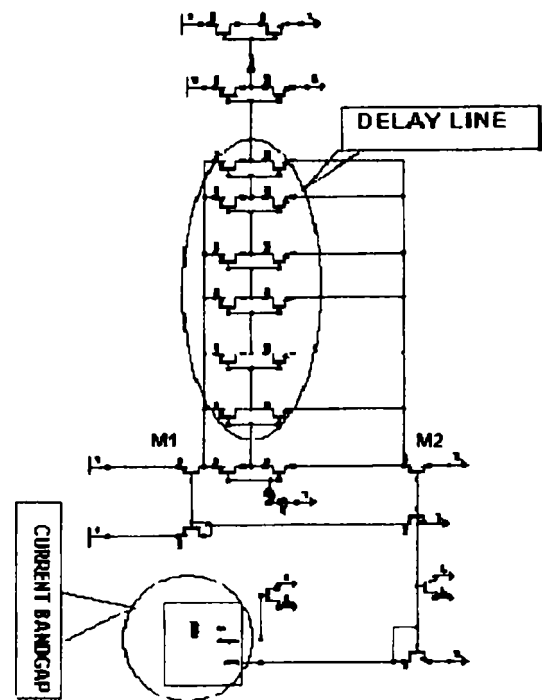value of current that is coming from current bandgap
block.

Fig 3 Compensated delay cell network schematic

As we want to keep the inverter characteristic as
symetric as possible (same tp_{HL} ans tp_{LH}), those two
degenerating transistors (current sources) are used
(one PMOS on the V_{DD} power supply to control the
Tplh, and one NMOS to the ground path in order to
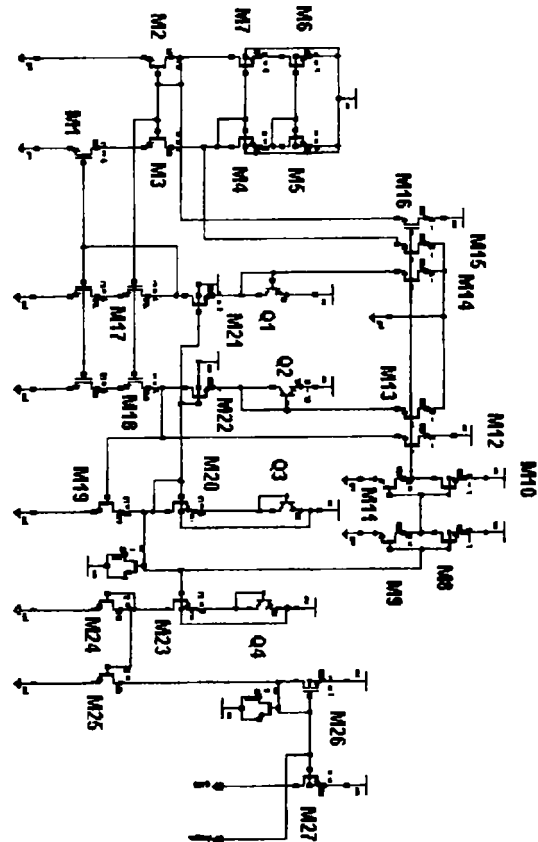control the tp_{HL} delay).

Fig4. The schematic of the current bandgap

The bandgap biasing circuit itself (Fig.4) consists of three feedback loops. The first and second loop are positive feedback loops with appropriately small gains, while the third loop is a negative feedback loops with significantly large gain. The first feedback loop consists of transistors M1-M7, which are responsible for generating the wide-swing, cascode biasing for transistors M17 and M18. The second loop (M8-M16) is the start-up circuit. It ensures the biasing cell does not remain in the start-up state where no DC current flows throughout the entire bandgap circuit. The third loop consists of transistors M19, M20 and Q3, and is the negative feedback loop that is responsible for generating the bandgap current. This negative feedback loop has a significantly large gain that is found at the drain of M18, which is the only high impedance node in the circuit.

Post layout simulation results show a low variation of generated current from bandgap. Actually, for extreme corners which are FF (fast PMOS fast NMOS) -55°C VCC+10% = 3.6V and SS (slow PMOS slow NMOS) 125°C, VCC - 10% = 2.97V the variation of current is less than 4%. But the main drawback is the variation of current in the other corners like FS (fast PMOS and slow NMOS) and SF, which is revealed in the Table 3 in the delay value results.
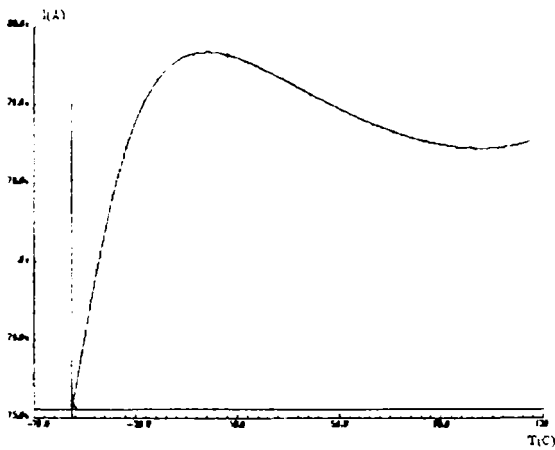

Fig.5 Output current of the bandgap used in delay cell corner FF (fast NMOS fast PMOS) -55°C VCC=3.6

Corner			C_load (fF)	
			5	
P	V_DD (V)	T (°C)	t↗ (ns)	t↓ (ns)
1.6ns delay cell				
TT	1.8	25	1.5234	1.40518
FF	1.98	-55	1.35	1.60231
SS	1.62	125	1.68315	1.67341
SF	1.98	125	1.36463	1.33606
FS	1.98	125	1.3991	1.717872
SF	1.62	125	1.3757	1.40848
FS	1.62	125	1.52.64	1.60654
SF	1.98	-55	1.48624	1.6123

FS	1.98	-55	1.61004	1.870848
SF	1.62	-55	1.75631	1.83399
FS	1.62	-55	1.82941	1.71872
Wc/Bc(t↗)			1.309	
Wc/Bc(t↓)				1.399

Table 3 Post layout simulation results for the proposed delay cell

Table 3 shows the results for the proposed compensated delay cell with a variation of delay value over PVT lower than 40%. The variation of the propagation delay is explained by the variation of current in the SF and FS and also the variation of threshold of the inverters used in the delay chain.
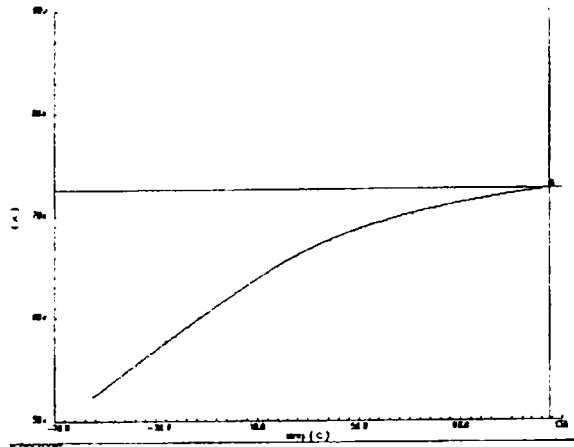

Fig. 6 Output current of the bandgap used in delay cell corner: FF (fast NMOS fast PMOS) 125°C VCC=2.97V

V CONCLUSIONS

In this paper was presented a simple delay cell method with good results. This solution can be used successfully in applications where is required a lower clock skews generation, like balanced clock trees, adaptive PLL's, or for a better synchronizations of the digital blocks.
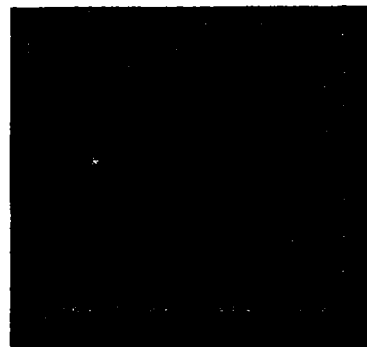

Fig.7 Layout view of RC delay cell

REFERENCES

[1] Mozhgan Mansuri, Chih-Kong Member, "Low-Power Adaptive Bandwidth PLL and Clock Buffer With Supply-Noise

Compensation", *IEEE Journal of Solid State circuits, Vol. 38, No. 11, November 2003.*

[2] S. Sidiropoulos *et al.*, "Adaptive bandwidth DLLs and PLLs using regulated supply CMOS buffers," in *IEEE Symp. VLSI Circuits Dig. Tech.Papers*, June 2000, pp. 124–127.

[3] J. M. Ingino, "A 4 GHz 40 dB PSRR PLL for an SOC application," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2001, pp.392-393.

[4] V. R. von Kaenel *et al.*, "A high-speed, low-power clock generator for a microprocessor application," *IEEE J. Solid-State Circuits*, vol. 33, pp.1634–1639, Nov. 1998.

[5] Mozhgan Mansuri, Chih-Kong Member, "A 320 MHz CMOS PLL for microprocessor clock generation," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1715–1722, Nov. 1996.

[6] I. A. Young, "A PLL clock generator with 5–110 MHz lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1599–1607, Nov. 1992.

[7] J. Maneatis, "Low-jitter process independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, pp.1723–1732, Nov. 1996.

[8] W.Dally and J.Polton, "Digital Systems Engineering", Cambridge University Press, 1998.

[9] N.Hedenstierna and K.Jeppson, " CMOS Speed and Buffer Optimization", *IEEE Transactions on CAD, Vol CAD-6,No.2, pp 270-281*