New Reducing Complexity Techniques for Computational Circuits Using Bulk-Driven Subthreshold-Operated and FGMOS Devices

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Abstract – Four computational circuits realized for MOS technology, implementing multiplier/divider, exponential, squaring functions and Euclidean distance will be presented. The multiplier/divider circuit is designed using bulk-driven subthreshold- operated MOS transistors in order to reduce the circuit complexity and to respond, also, to the low-power requirements. The circuit output current is independent on process parameters. A new method for reducing the approximation error caused by a limited expansion in Taylor series of the exponential function will be presented, having the advantage of obtaining a very good frequency response as a result of the operation in saturation of MOS transistors. The MOS implementation of the squaring function based on a new principle using the arithmetic mean of the input potentials, as well as an original realization of the Euclidean distance function independent on technological parameters will be further described.

Keywords: approximation error, limited Taylor series expansion, bulk-driven subthreshold-operated MOS transistors, FGMOS devices

I. INTRODUCTION

Computational circuits are important building blocks for telecommunication applications, medical equipments, hearing devices or disk drives. Because of the rapid development of CMOS VLSI technology, many analog signal-processing functions can be achieved by employing the square-law model of MOS transistors working in saturation. Based on this principle, several basic building blocks, such as multipliers, dividers, squarers, exponential, logarithmic or Euclidean distance circuits have been developed.

In order to respond to the low-power requirements of the newest CMOS designs, the subthreshold operation of the MOS transistor is an interesting choice. Based on the logarithmical law of a MOS transistor in weak inversion, the implementation of a CMOS current-mode multiplier/divider becomes very simple (even with respect to the bipolar version). The result will be a smaller silicon area consumption than that obtained

in [1] – [3], making the circuit compatible with low-power VLSI designs.

The exponential law is available only for the weak inversion operation of the MOS transistor. The great disadvantage of the computational circuits using subthreshold-operated MOS devices [4], [5] is the poor frequency response caused by the much smaller drain currents. As a result, for circuits realized in CMOS technology that require a good frequency behavior, only MOS transistors working in strong inversion (usually in saturation) are usable. The new idea for obtaining the exponential law using the square characteristic of the MOS transistor in saturation is the approximation of the exponential function with its $n-th$ order expansion (the polynomial series). The approximation error will be proportional to the number of terms neglected in the expansion.

The squaring function could be easily obtained in CMOS technology using the quadratic characteristic of the MOS transistor working in saturation. The proposed circuit for computing this function presents the important advantage (with respect to the classical implementations [6], [7]) of a smaller value of the minimal supply voltage, obtained by using a new principle based on the arithmetic mean of the input potentials.

The complexity of the original Euclidean distance circuit presented in the end of the paper has been strongly decreased with respect to other similar circuits by replacing classical MOS devices by FGMOST (Floating Gate MOS Transistors), the Euclidean function being, in addition, independent on technological parameters.

II. THEORETICAL ANALYSIS

A. *Current multiplier/divider using bulk-driven MOS transistors*

The proposed current multiplier/divider using bulk-driven subthreshold-operated MOS transistors is presented in Fig. 1. The double drive of the MOS devices (on gate and on bulk) allows the reduction of

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the computational circuit complexity. Unfortunately, the possibility of implementation in silicon is limited to CMOS technologies with independent wells. Considering a weak inversion operation of all the transistors from Fig. 1, the relations among the currents from Fig. 1 could be written as:

$$\frac{I_1}{I_2} = \frac{I_{Y_1}}{I_{X_1}}\left(\frac{I_{Y_2}}{I_{X_2}}\right)^{\frac{1}{n-1}} \tag{1}$$

A generalization of relation (1) for different values of current sources I_0 (I_{Z_1}, I_{W_1} and I_{Z_2}, I_{W_2}, respectively) allow obtaining a more complex relation between the circuit currents:

$$\frac{I_1}{I_2} = \frac{I_{Y_1}}{I_{X_1}}\frac{I_{Z_1}}{I_{W_1}}\left(\frac{I_{Y_2}}{I_{X_2}}\frac{I_{Z_2}}{I_{W_2}}\right)^{\frac{1}{n-1}} \tag{2}$$
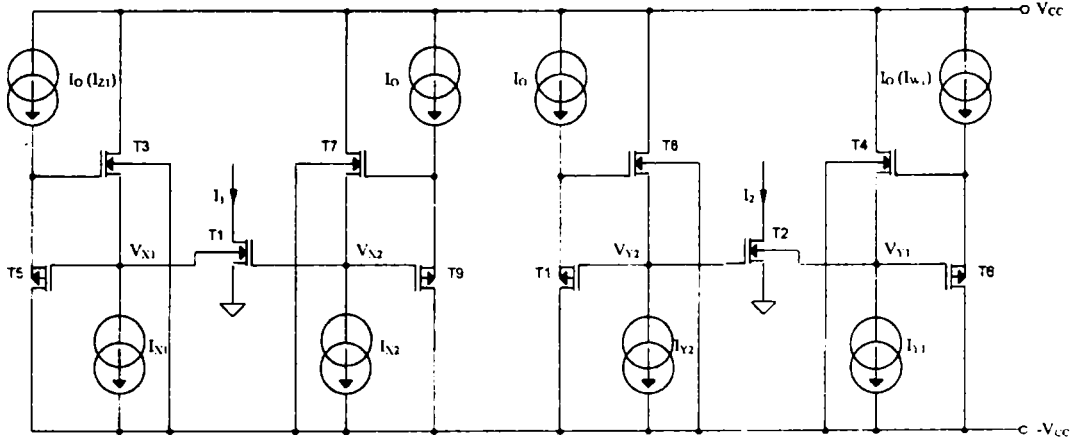

Fig. 1. Current multiplier/divider using bulk-driven MOS transistors

B. The pseudo-exponential function circuit with third-order approximation

The new idea for implementing the exponential function for applications that require a good frequency response is to approximate $\exp(x)$ by its limited polynomial series and to use exclusively the quadratic characteristic of the MOS device working in saturation:

$$I_0 \exp\left(\frac{I_{in}}{I_0}\right) \cong I_0\left[1 + \frac{I_{in}}{I_0} + \frac{1}{2}\left(\frac{I_{in}}{I_0}\right)^2 + \frac{1}{6}\left(\frac{I_{in}}{I_0}\right)^3\right] \tag{3}$$

The first step is the implementation of the function x^2, where $x = I_{in}/I_0$, presented in Fig. 2.

$$I_{out1} = \frac{K}{2}(V - V_T)^2 = I_0 + \frac{I_{in}}{2} + \frac{I_{in}^2}{16I_0} \tag{4}$$

So, subtracting I_0 and $I_{in}/2$ from expression (4), it is possible to obtain a quadratic dependence of the output current I_{out1} on the input current I_{in}.

In order to obtain the third-order term from the approximate expansion of the exponential function, the new idea is to use a similar circuit, presented in Fig. 3.
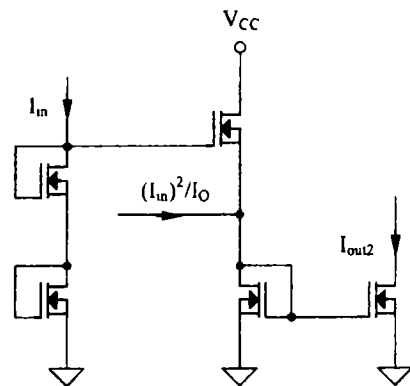
Fig. 3. The circuit for implementation the x^3 function
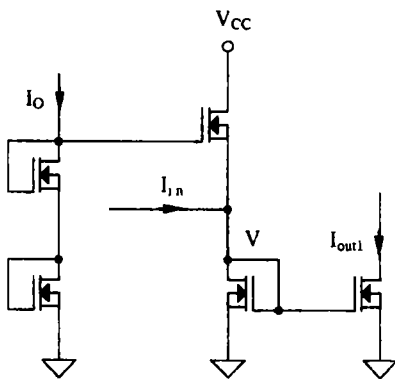

Fig. 2. The circuit for implementation the x^2 function

Considering that all transistors from Fig. 2 are working in saturation, it results that:

Similarly, the expression of the output current from Fig. 3 will be:

$$I_{out2} = I_{in} + \frac{I_{in}^2}{2I_0} + \frac{I_{in}^3}{16I_0^2} \tag{5}$$

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In conclusion, the third-order approximation of the exponential function using the two previous circuits is:

$$I_0 \exp\left(\frac{I_{in}}{I_0}\right) \cong I_0 + \frac{40}{3}\left(I_0 - I_{out_1}\right) + 5I_{in} + \frac{8}{3}I_{out_2} \quad (6)$$

The approximation error of the expansion (6) is, practically, very close to the fourth-order neglected term, $\varepsilon_4 = I_{in}^4 / 24I_0^4$.

The implementation of the approximate expansion (6) for the exponential function is presented in Fig. 4.

C. *CMOS voltage squarer based on the arithmetic mean of the input potentials*

The proposed circuit for computing the squaring function (Fig. 5) presents the important advantage (with respect to the classical implementations [6], [7]) of a smaller value of the minimal supply voltage, obtained by using a new principle based on the arithmetic mean of the input potentials.

Fig. 4. The implementation of exponential function with third-order approximation

Fig. 5. CMOS squarer using arithmetic mean of the input potentials

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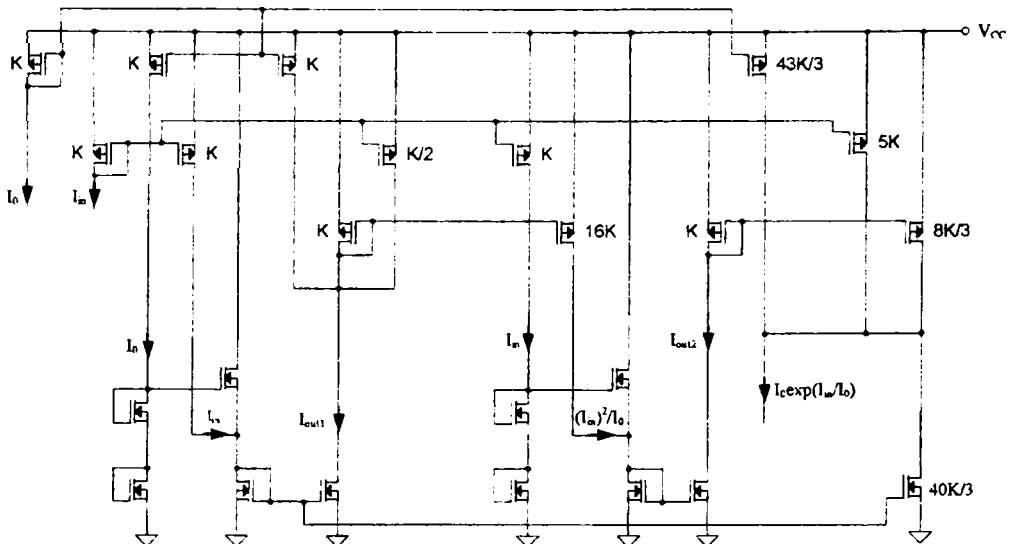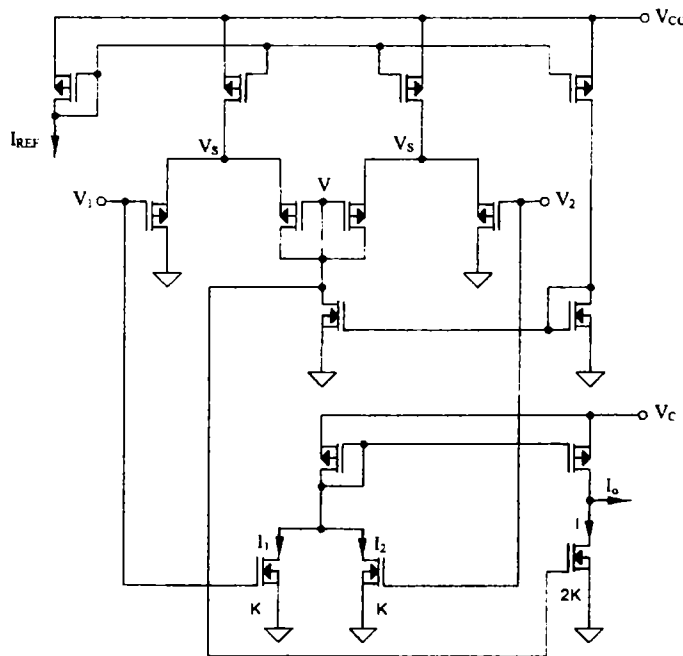Because the potential V from Fig. 5 is equal to the arithmetic mean of the input potentials, it results that the circuit computes the square of the differential input voltage:

$$I_O = \frac{K}{4}(V_a - V_b)^2 \qquad (7)$$

D. *The Euclidean distance circuit*

The structure of a current-mode CMOS Euclidean distance circuit with n inputs, consisting in n current squarer circuits and a square-root circuit is presented in Fig. 6. The square and square-root functions are obtained by using the same core, based on classical MOS transistors and on a FGMOS transistor (used for reducing the circuit complexity).

The Euclidean distance between two n-dimensional vectors $V_a = (V_{a1}, V_{a2}, ..., V_{an})$ and $V_b = (V_{b1}, V_{b2}, ..., V_{bn})$ is defined as:

$$\|V_a - V_b\| = \sqrt{\sum_{k=1}^{n}(V_{ak} - V_{bk})^2} \qquad (8)$$

being a direct measure of similarity between the vectors V_a and V_b. An equivalent function based on current-mode operation could be written as

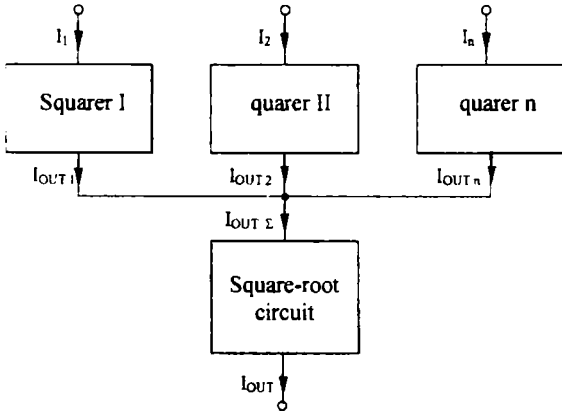$$I_{OUT} = \sqrt{\sum_{k=1}^{n} I_k^2} \; .$$

Fig. 6. The structure of a CMOS Euclidean distance circuit

Principle of operation of the CMOS squarer

The implementation of a CMOS voltage squarer using a FGMOS transistor for reducing the circuit complexity is presented in Fig. 7.

The FGMOS transistor is a MOS transistor whose gate is floating. The first silicon layer over the channel represents the floating-gate and the second polysilicon layer, located over the floating-gate implements the multiple input gates. This floating-gate is capacitive coupled to the multiple input gates.

The drain current of a FGMOS transistor with n-input gates working in the saturation region is given by the following equation:

$$I_D = \frac{K}{2}\left[\sum_{i=1}^{n} k_i(V_i - V_S) - V_T\right]^2 \qquad (9)$$

where $K = \mu_n C_{ox}(W/L)$ is the transconductance parameter of the transistor, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, W/L is the transistor aspect ratio, $k_i, i = 1, ..., n$ are the capacitive coupling ratios, V_i is the i-th input voltage, V_S is the source voltage and V_T is the threshold voltage of the transistor. Equation (9) shows that the FGMOS transistor drain current in saturation is proportional to the square of the weighted sum of the input signals, where the weight of each input signal is determined by the capacitive coupling ratio of the input. Considering that all MOS transistors from Fig. 7 are working in saturation and $k_1 = k_2 = 1/2$, the output current expression is:

$$I_{OUT_1} = \frac{I_1^2}{4I_O} \qquad (10)$$

The more important advantage of the original implementation of the current squarer proposed in Fig. 7 is the absolutely (in a first-order analysis) independence of the circuit output current on technological parameters (K, V_T).

Principle of operation of the square-root circuit

There are many possibilities of implementation a s uare-root circuit usin the uadratic characteristic of the MOS transistor in saturation. The main goals of this class of circuits are the silicon occupied area, the i d d f th t t / a e o technological parameters (that is independence on temperature) and a small sensitivity to the second-order effects (bulk or short channel effects and mobility degradation).

The new proposed implementation (Fig. 8) of the square-root circuit is based on a structure similar to the circuit used in the previous paragraph for ob a n ng he squar ng nc n.

The expression of the output current for the entire Euclidean distance circuit will be:

$$I_{OUT} = \sqrt{4I_O I_{OUT_\Sigma}} = \sqrt{\sum_{k=1}^{n} I_k^2} \qquad (11)$$

The main advantage of the square-root circuit (independence of the output current on the technological parameters) is still valuable for the Euclidean distance circuit, whose block diagram is presented in Fig. 6.

Fig. 7. CMOS squarer using a FGMOS transistor

Fig. 8. Square-root circuit using a FGMOS transistor

III. CONCLUSIONS

There were presented four computational circuits realized for CMOS technology, implementing multiplier/divider, exponential, squaring and Euclidean distance functions. The current multiplier/divider circuit was designed using bulk-driven MOS transistors in order to reduce the circuit complexity. The proposed circuit responds, also, to the low-power requirements due to the subthreshold operation of MOS transistors, the circuit output current being independent on the process parameters. The proposed exponential circuit, based on a limited expansion in Taylor series of the exponential function, presents an important reducing of the approximation error, taking into account the third-order term from the previous mentioned expansion. The circuit frequency response is very good as a result of the operation in saturation of the MOS transistors. The proposed circuit for computing the squaring function presents the important advantage (with respect to the classical implementations) of a smaller value of the minimal supply voltage, obtained by using a new principle based on the arithmetic mean of the input potentials. The complexity of the original Euclidean distance circuits presented in this paper has been strongly decreased by replacing classical MOS devices by FGMOST (Floating Gate MOS Transistors), the Euclidean function being, in addition, independent on technological parameters.

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