Buletinul Ştiinţific al Universităţii "Politehnica" din Timişoara

Seria ELECTRONICĂ şi TELECOMUNICAŢII
TRANSACTIONS on ELECTRONICS and COMMUNICATIONS

Tom 49(63), Fascicola 1, 2004

The Switching Characteristics of the MOSFET Driver Used in the PWM Control of a DC Motor - A Small Handbook for Engineers

Pompilian Tofilescu, Gheorghe Grama [1]

Abstract – The present paper presents few issues regarding the PWM (pulse width modulation) control of a DC motor using a power MOSFET driver. There are shown the algorithms and the calculations used to determine the switching times and switching power dissipation of the MOSFET. The calculations are based on the device datasheet specifications and are verified by lab tests and measurements.
The paper is based on the authors' experience in the automotive electronics design and analysis field and wants to be a useful tool for the design engineers, which will be involved in the DC motor control design.

Keywords: DC motor, PWM control, power MOSFET, switching characteristics.

I. INTRODUCTION

PWM method is one of the most used methods in the DC motors control because is accurate and relatively simple. The reason is that almost all microcontrollers provided by various suppliers for a wide field of application have one or more PMW outputs and the characteristics of PWM signal (duty cycle, frequency) can be easy modified by software.
A common application of this type of control in automotive electronics field is the control of fuel pump motor. The schematic draft is presented in the figure below:

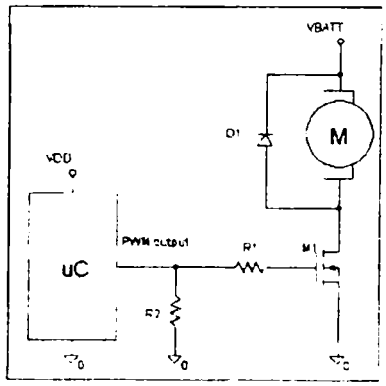

Fig. 1 PWM Control Schematic

Where:
- D1 is the freewheeling diode
- R1 (usually from few decades to few hundreds ohms) is used to control the switching time of the MOSFET (M1)
- R2 is the pull down resistor and keeps the gate of M1 low when the microcontroller output is in high impedance state.

The average current through the motor coil is proportional with the duty cycle of the PWM signal.
The issues that appear in this type of control are:
- the variation of the output pulse width due by the switching times of the MOSFET driver
- the switching times variations induced by component tolerances
- power dissipation during MOSFET switching could be significant and overstresses the device.

II. THEORETICAL BRIEF

This section will explain the behavior of the MOSFET during switching. To drive a MOSFET on or off a certain amount of electrical charge is necessary to be pumped to or sunk from the gate. A typical test circuit to study this behavior is shown in the figure above:

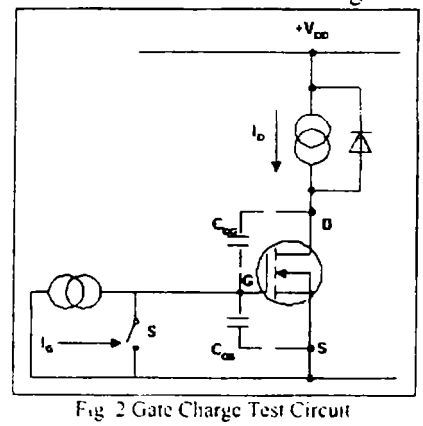

Fig. 2 Gate Charge Test Circuit

The basic gate charge waveforms and from the test circuit above are:

[1] The INstitute for the Analysis of Systems SA Craiova,
1 Tehnicii Street, 200440, Craiova, Dolj, Romania, www.inas.ro
Phone: +40 251 438 789
Fax: +40 251 438 906
tpompilian@inas.ro, ggrama@inas.ro

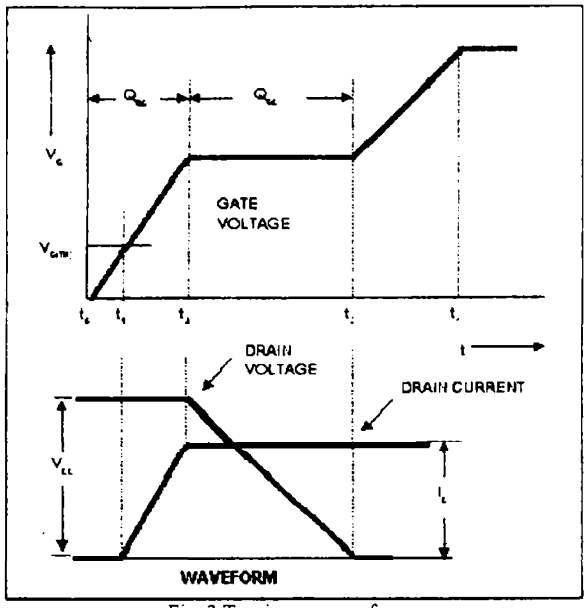

Fig. 3 Turning on waveforms

Before time t_0, the switch S is closed; the device under test (DUT) supports the full circuit voltage, V_{DD}, and the gate voltage and drain current are zero. S is opene at t me t_0; t e gate-to-source capac tance starts to charge, and the gate-to-source voltage increases. No current flows in the drain until the gate reaches the threshold voltage. During period t_1 to t_2, the gate-to-source capacitance continues to charge, the gate voltage continues to rise and the drain current rises proportionally. So long as the actual drain current is still building up towards the available drain current, I_D, the freewheeling rectifier stays in conduction, the voltage across it remains low, and the voltage across the DUT continues to be virtually the full circuit voltage, V_{DD}. At time t_2, the drain current reaches I_D, and the freewheeling rectifier shuts off; the potential of the drain now is no longer tied to the supply voltage, V_{DD}. The drain current now stays constant at the value I_D enforced by the circuit, while the drain voltage starts to fall. Since the gate voltage is inextricably related to the drain current by the intrinsic transfer characteristic of the DUT (so long as operation remains in the "active" region), the gate voltage now stays constant because the "enforced" drain current is constant. We note this value of gate voltage with VGS(pl). No charge is consumed by the gate-to-source capacitance, because the gate voltage remains constant. The drain voltage excursion during the period t_2 to t_3 is relatively large, and hence the total drive charge is typically higher for the "Miller" capacitance C_{DG} than for the gate-to-source capacitance G_{CS}. At t_3 the drain voltage falls to a value equal to I_D x $R_{DS(ON)}$, and the DUT now comes out of the "active" region of operation.

The gate voltage is now no longer constrained by the transfer characteristic of the device to relate to the drain current, and is free to increase. This it does, until time t_4, when the gate voltage becomes equal to the voltage "behind" the gate circuit current source. The time scale on the graphs of the gate-to-source voltage is directly proportional to the charge delivered by the drive circuit, because the current remains constant throughout the whole sequence. Thus the length of the period t_0 to t_1 represents the charge Q_{GS} consumed by the gate-to-source capacitance, while the length of the period t_2 to t_3 represents the charge Q_{GD} consumed by the "Miller" capacitance. The total charge at time t_3 is the charge required to switch the given voltage V_{DD} and current I_D. The additional g ft m , that will be noted Qg_res (residual gate charge), do not represent "switching" charge. It is simply the excess charge which will be delivered by the drive circuit because the amplitude of the applied gate drive voltage o lly will high th the required to accomplish switching.

Similar considerations apply to the turn-off interval.

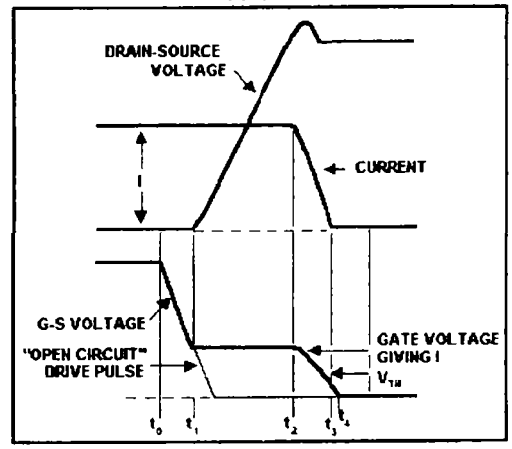

Fig. 4 Turn off waveforms

Figure 4 shows theoretical waveforms for the MOSFET during the turn-off interval. At t_0 the gate drive starts to fall until, at t_1, the gate voltage reaches a level that just sustains the drain current and the device enters the linear mode of operation. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constant drain current. Once again, the lower the impedance of the driver circuit, the greater the charging current into the drain-gate capacitance, and the faster will be the rise time of the drain voltage. At t_3 the rise of drain voltage is complete, and the gate voltage and drain current start to fall at a rate determined by the gate-source circuit impedance.

III. APPLICATION

The waveforms shown in the paragraph above are idealized, theoretical curves. In reality the currents and voltages rise or fall follow exponential, not linear functions. In the theoretical example we assumed also a constant current source used to charge the MOSFET gate. In reality the drive circuit can be more complicated than the circuit shown in the first section and do not provide a constant current to the gate. So

the switching times could not be easy calculated as a ratio between the charge and a constant current value. Let's consider the circuit below.

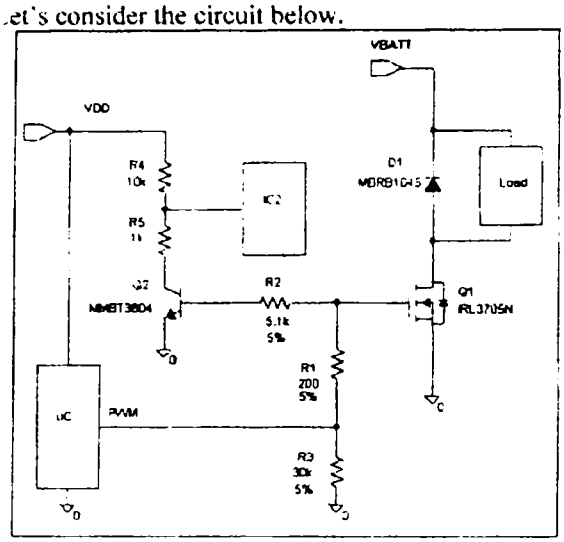

Fig. 5 PWM control circuit

Where:

- uC is a Texas Instruments microcontroller
- IRL3705N is a HEXFET power MOSFET from International Rectifier
- MBRB1045 is a Schottky power diode from ON Semiconductor
- MMBT3804 is a small signal general purpose bipolar transistor from ON Semiconductor and is used to provide a switching monitor signal to IC2
- Load is the DC motor coil

We approach separately the turn on and the turn off cases.

3.1 Specifications

Supply voltages are:

- VBATT = 14V
- VDD = 5V

The circuit load is a DC motor with 14V/12A nominal values. The specifications for PWM micro input are 10% to 90% duty cycle and 9600Hz frequency.

We use the following model for the microcontroller output pin:

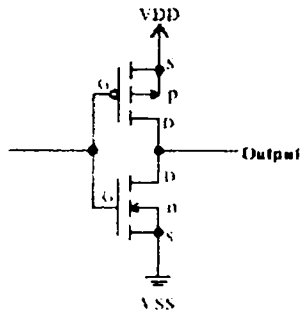

Fig. 6 Microcontroller output pin model

We note Rdson_high and Rdson_low the "on" resistance of the two transistors figured above, that will model the logic states "0" and "1" of the output. The values of Rdson_high and Rdson_low are picked up from the device datasheet:

- Rdson_high = 200Ω
- Rdson_low = 135Ω

Other parameters of interest are:

- Q2 parameters:
- VBE saturation; value picked up from device datasheet VBE = 0.65V
- IB_Q2 when Q2 is saturated. This value can be calculated from the circuit that drives Q1 modeled as below, when microcontroller output is logic "1".

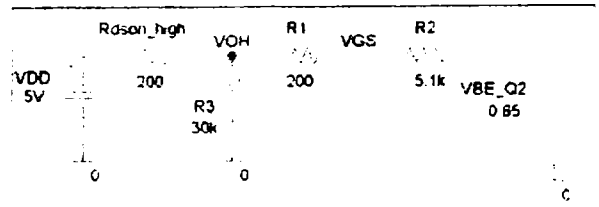

Fig. 7 Electrical model of Q1 drive circuit

From Millman theoreme:

$$VOH = \frac{\frac{VDD}{Rdson\_high} + \frac{VBE\_Q2}{R1+R2}}{\frac{1}{Rdson\_high} + \frac{1}{R3} + \frac{1}{R1+R2}} \quad (1)$$

and

$$IB\_Q2 = \frac{VOH - VBE\_Q2}{R1+R2} \quad (2)$$

The same circuit can be used to calculate Q1 gate to source voltage when micro output is logic "1".

$$VGS\_high = \frac{R1 \cdot VBE\_Q2 + R2 \cdot VOH}{R1+R2} = 4.654V \quad (3)$$

- Q1 parameters:
- VGS(pl) – as in section above is the value of Q1 gate voltage when the drain current achieves the maximum available, enforced by the circuit.

This value is picked up from the transfer characteristics of the device:

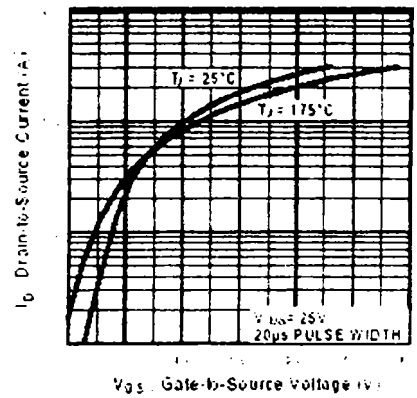

Fig. 8 IRL3705N Transfer Characteristics

- Qgs – gate to source charge.
- Qgd – gate to drain charge
- Qg_res – gate charge consumed to rise gate to source voltage from VGS(pl) to VGS_high.

The significances of these three parameters were presented in the section II.
The values of Qgs, Qgd and Qg should be evaluated using device datasheet, gate charge vs. gate to source voltage diagram:

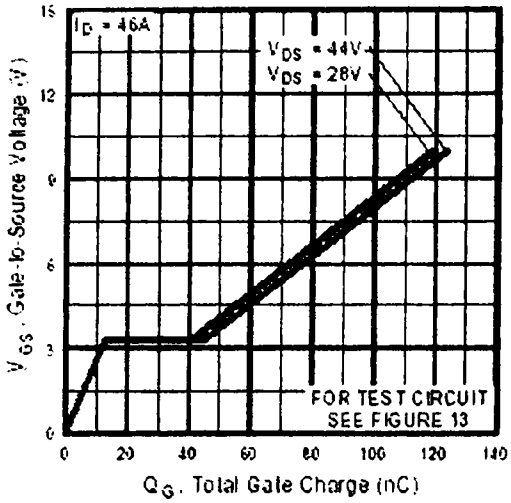

Fig. 9 - IRL3705N – Qg vs. VGS Characteristic

The diagram above should be adjusted for our operation point: VGS(pl)=2.75V, VGS_high=4.654V and VBATT = 14V and we obtain;

- Qgs = 24nC
- Qgd = 10nC
- Qg_res = 25.834nC

3.2 Turn-on switching characteristics

The turn-on delay time td(on) is the time interval between the moment when the gate to source voltage (VGS) start to increase and the moment when drain to source voltage (VDS) starts to decrease.
The rise time of the microcontroller output voltage is much lower than the FET switching time therefore we can neglect it. The switching time of Q2 (MMBT3904) is also much lower than FET switching time therefore we can assume that Q2 goes into saturation almost instantaneously.
The Q1 gate charging current is not a constant current during the FET state transition.
The IG_ch waveform looks like in the figure below:

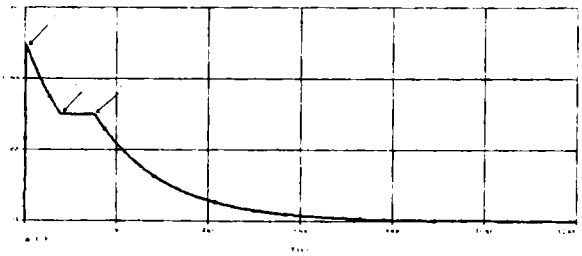

Fig. 10 Gate charging current

In the turning-on moment (t0) the gate to source voltage of Q1 is low and the micro output voltage goes up. IG_ch rises very fast to the peak value that can be defined as:

$$IG\_ch(t0) = \frac{VDD}{Rdson\_high + R1} \quad (4)$$

From t0 to t1 IG_ch falls during the charging of the gate to source capacitance. In the t1 moment Cgs is charged, the gate charge is Qgs and VDS starts to fall. The interval t1 – t0 is turn-on delay time of FET driver. The t1 moment corresponds to the VGS(pl).
At the t1 moment the gate charging current is calculated as the ratio between the difference VDD – VGS(pl) and the sum R1 + Rdson_high like in the following equation:

$$IG\_ch(t1) = \frac{VDD - VGS(pl)}{R1 + Rdson\_high} \quad (5)$$

IG_ch(t1) is actually the charging current of Miller capacitance and is required to achieve Qds.
We calculate Q2 base current as:

$$IB\_Q2 = \frac{VGS(pl) - VBE\_Q2}{R2} \quad (6)$$

Because from t0 to t1 the IG_ch waveform is almost linear, we assume that the gate charging current required by Qgs is the average current on t1-t0 time interval minus Q1 base current:

$$IG\_ch = \frac{IG\_ch(t0) + IG\_ch(t1)}{2} - IB\_Q2 \quad (7)$$

So,

$$td(on) = \frac{Qgs}{IG\_ch} \quad (8)$$

Fall time tf is defined as the ratio between gate to drain (Miller) charge and the gate charging current calculated above at the t1 moment:
To calculate tf we use the diagram shown in paragraph above.

$$tf = \frac{Qgd}{IG\_ch(t1)} \quad (9)$$

For the power dissipation estimation we need also the current drain time characteristics.
We note the time interval between the moment when the VGS starts to increase and the moment when the drain current starts to increase with td_ID_rise and we will calculate it using fig.3.
Mathematically td_ID_rise is equal with the ratio between the gate to source charge corresponding to the VGS threshold and the gate charging current.

$$td\_ID\_rise = \frac{Qsg(VGS(th))}{IG\_ch(t1,t2)} \quad (10)$$

Where Qgs(VGS(th)) can be estimated from the diagram presented in fig. 10 and IG_ch is the gate charging current calculated as the average between the gate charging current at t1 and gate charging current at t2 minus the Q1 base current:

$$IG\_ch(t1.t2) = \frac{IG\_ch(t1) - IG\_ch(t2)}{2} - \frac{VGS(pl) - VBE\_Q2}{R2} \quad (11)$$

The current drain rise time is:

$$tr\_ID = td(on) - td\_ID\_rise \quad (12)$$

3.2 Turn-off switching characteristics

The turn-off delay time is the time interval between the moment when the gate to source voltage (VGS) start to decrease and the moment when drain to source voltage (VDS) starts to increase. We will calculate it using fig. 4.

The rise time of the microcontroller output voltage is 25ns much less than the FET switching time therefore we can neglect it. The switching time of Q2 (MMBT3904) is also much less than FET switching time therefore we can assume that Q2 cuts off almost instantaneously. The gate discharging current waveform is similar with the charging current waveform. In the turning-off moment (t0) the gate to source voltage of Q1 is high and the micro output voltage goes down. At t0 IG_disch has the peak value and starts to decrease following the decreasing of the VGS until t1 moment when VGS reaches the VGS(pl) value. The time interval t1 – t0 is the turn off delay time of the FET driver.

The peak value of discharging current:

$$IG\_disch(t0) = \frac{VGS\_high}{Rdson\_low + R1} \quad (13)$$

The discharging current at t1:

$$IG\_disch(t1) = \frac{VGS(pl)}{R1 + Rdson\_low} \quad (14)$$

We assume that the gate discharging current required to calculate td(off) is the average current on t1-t0 time interval:

$$IG\_disch\_avg = \frac{IG\_disch(t0) + IG\_disch(t1)}{2} \quad (15)$$

And

$$td(on) = \frac{Qg}{IG\_disch\_avg} \quad (16)$$

To calculate drain to source voltage rise time tr we use the same fig. 4. Mathematically tr time is defined as the ratio between gate to drain (Miller) charge and the gate discharging current calculated at t1 moment:

$$tr = \frac{Qgd}{IG\_disch(t1)} \quad (17)$$

For power calculations too we need to find the MOSFET current drain fall time.

From fig. 4. that is the time interval between the t2 to t3. Mathematically drain current fall time is the ratio between the gate to source charge (from t2 to t3) and the gate discharging current. IG_disch23 - the average between the gate discharge current at the t2 moment and the gate discharge current at the t3 moment.

$$IG\_disch(t2) = \frac{VGS(pl)}{R1 + Rdson\_low} \quad (18)$$

$$IG\_disch(t3) = \frac{VGS(pl) - VGS(th)}{R1 + Rdson\_low} \quad (19)$$

$$IG\_disch23 = \frac{IG\_disch(t3) + IG\_disch(t2)}{2} \quad (20)$$

$$tf\_ID = \frac{Qgs - Qgs(th)}{IG\_disch23} \quad (21)$$

3.3 Numerical results, waveforms and measurements

Using the equations from sections above we can put the results of the switching characteristic analysis for the presented example in tabular form as below.

All calculations are done using Mathcad11.

Table 1. Parameters

Parameter	Value	Remarks
VBATT	14V	Circuit specification
VDD	5V	Circuit specification
VBE_Q1	0.65V	Datasheet specification
ID	10.8A	For 90% duty cycle. 1.16Ω equivalent load resistance, neglecting Rds(on) of Q1
Rdson_high	200Ω	Datasheet specification
Rdson_low	135Ω	Datasheet specification
Qgd	24C	Evaluated from fig. 10
Qgs	10C	Evaluated from fig. 10
Qg	25.83C	Evaluated from fig. 10
Qgs(th)	5.455C	Evaluated from fig. 10
R1	200Ω	Circuit specification
R2	5100Ω	Circuit specification
R3	30k	Circuit specification
VGS(th)	1.5V	Datasheet specification
VGS_high	4.654V	Calculated, eq. (3)
VGS(pl)	2.75V	Evaluated from fig. 9

Table 2. Results

Parameter	Value	Remarks
td(on)	1.156μs	drain voltage "on" delay time
tf	4.604μs	drain voltage fall time
tr_ID	0.351μs	drain current rise time
td(off)	2.338μs	drain voltage "off" delay time
tr	2.924μs	drain voltage rise time
tf_ID	0.761μs	drain current fall time

Using these values we can build drain current and drain voltage waveforms during one period of the micro output signal, assuming 10% duty cycle:
Figure below shows a zoom in the interest area

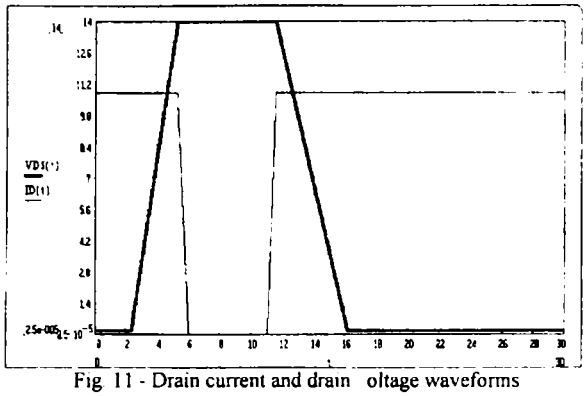

Fig. 11 - Drain current and drain voltage waveforms

From the graph above can be easy deduced the power dissipation waveform.

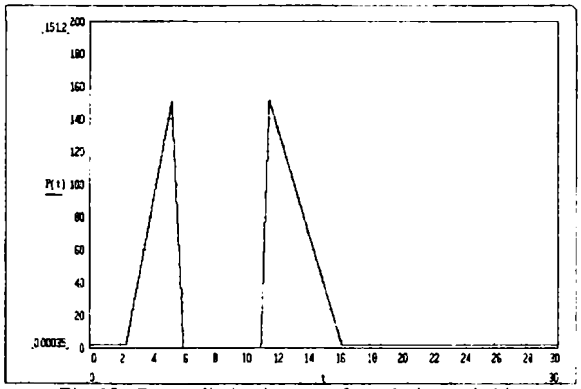

Fig. 12 - Power dissipation waveform during switching

Numerically,

- Pmax = 151.2W – maximum peak power
- Pon = 1.633W – "on" state power dissipation
- Poff = 0.35mW - "off" state power dissipation
- Pavg = 7.745W – average power on a period

Another important issue related by the PMW control type is the variation of the output pulse width induced by components' tolerances and other parameters' variations. For the present example, we can achieve a maximum variation of output pulse width by:

$\Delta t- = 8.229us$

$\Delta t+ = 6.817us$

The values are calculated based on the equations presented in the section above, taking into account the variations specified in the design specs or in the components' datasheet. To determine the sense of each parameter influence we used the first derivative of the input-output functions.

Is easy to see that for a certain value of duty cycle – let's say 10% - those variations are significant, almost 100% of output pulse width.

The theoretical analysis was verified by lab measurements and the real results are very close to theoretical results.

The oscilloscope traces obtained from lab measurements on the circuit are shown below:

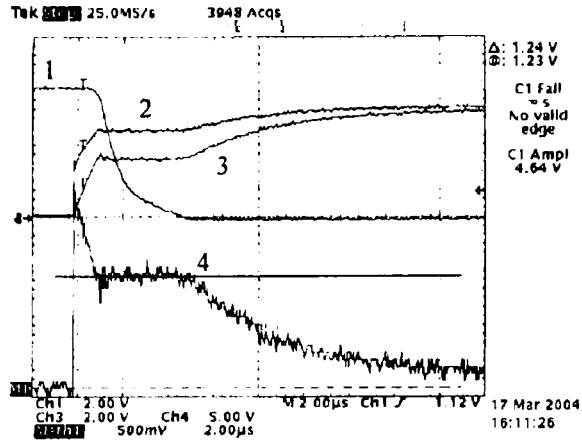

Fig. 13 - Scope traces

Where

- 1 – Q1 drain voltage waveform
- 2 – micro output waveform
- 3 – Q1 gate to source voltage waveform
- 4 – micro output current waveform

IV. CONCLUSIONS

Present paper wants to be a useful tool for the engineers involved in the designs those use MOSFETs to drive inductive loads or imply the PWM control of DC motors.

The analyses presented above would help the design engineers to understand the behavior of a MOSFET during switching and the influence of the drive circuit. It could help they to choose the right values of the circuit parameters and refine the design to make the circuit working properly.

REFERENCES

[1] Paul Horowitz, Winfield Hill, *The Art of Electronics. Second Edition*, Cambridge University Press, 1989.

[2] International Rectifier, *Application Note AN-944*, "Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs", http://www.irf.com/technical-info/appnotes.htm

[3] International Rectifier, *Application Note AN-937*, "Gate Drive Characteristics and Requirements for HEXFET® Power MOSFETs", http://www.irf.com/technical-info/appnotes.htm.

[4] International Rectifier, IRL3705 HEXFET® Power MOSFET Datasheet, PD - 9.1370C.

[5] ON Semiconductor, Small Signal Device Data, Bipolar Transistors, JFETs and Diodes, DL126/D, Rev. 7, 2001, pp. 572.

[6] ON Semiconductor, Rectifier Device Data, DL151/D, Rev. 4, 2003, pp. 170.

[7] Mathsoft Engineering & Education, Inc., Mathcad11, User's Guide, 2002.