HYBRID DC-DC CONVERTERS FOR AUTOMOTIVE AND RENEWABLE ENERGIES SYSTEMS

Teză destinată obţinerii
titlului ştiinţific de doctor inginer
la
Universitatea Politehnica Timişoara
în Domeniul INGINERIE ELECTRICĂ
de către

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Ziua susţinerii tezei: 14.03.2014

Acknowledgements

I wish to express my endless gratitude to my supervisor Professor Nicolae Muntean, for giving me the chance to be part of his research team, for his competent guidance, support and patience, without which this work would have not been possible.

I am grateful to Professor Frede Blaabjerg, for his support during the three months PhD internship at the Institute of Energy Technology, Aalborg University, Denmark.

I wish to thank the referents, Professor Mircea Rădulescu and Professor Iulian Birou, from Technical University of Cluj-Napoca and Professor Alexandru Hedeş, from Politehnica University Timisoara, for their pertinent comments and relevant suggestions.

I am also thankful for their support, to my friends and all my colleagues from the Electrical Engineering Department.

Finally, I will always be thankful to my family for the unfailing support and encouragement throughout all my years of study.

Timişoara, March 2014   Ovidiu Roman PELAN

Abstract,
        The wide spread applications of power electronics in global industrialization are challenging the future electrical infrastructure and contributes to non-carbon based electricity production. The power electronic converters can be considered the heart of the renewable energy systems and are responsible for the power generation, transmission/distribution and end-user application.
        The work presents a research in the field of the DC-DC converters. After a literature research three Hybrid Buck DC-DC converters were studied, simulated, designed, built and integrated in real applications (switched-inductor HBDC-L, switched-capacitor HBDC-C and switched-capacitor/inductor HBDC-C/L).
        A full analysis and design prototyping of the three Hybrid Buck DC-DC converters is presented in this work.
        The main current and voltage, simulation and experimental waveforms are presented, discussed and compared.
        A comparative study of a HBDC-L, a HBDC-C and a HBDC-C/L, in CCM and BCM, with the classical Buck (BDC) and between the hybrid converters is made. A relative price (given in percent), of all the converters, is presented.
        Laboratory models and full-scale industrial prototypes were built.
        Two industrial applications for automotive and renewable energy systems are presented. A general description of each experimental setup operating principles is made in order to give a complete image of the presented industrial solutions.
        Both applications are sustained by experimental results in order to validate the theoretical considerations.

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OBJECTIVES

The main objectives of the thesis are:

- To present an overview of the main DC-DC converters configurations;
- To describe analytically, through digital simulations and experiments two Hybrid Buck DC-DC converters presented in the literature as configurations;
- To propose and also to completely describe a new Hybrid Buck DC-DC converter based on mixing the above structures;
- To build and test small power, configurable laboratory prototypes, in order to validate the theoretical results;
- To present and discuss a comparative evaluation of the Hybrid Buck DC-DC converters;
- To design, integrate and test two industrial prototypes into adequate applications (renewable energy and automotive systems);
- To present experimental results for the proposed applications.

OUTLINE

The thesis is organized in 7 chapters:

- Chapter 1 presents a general overview of the main DC-DC converters topologies and applications in the renewable energy and automotive areas. The classical Buck DC-DC converter (BDC), used as reference configuration in the following chapters is then analyzed.
- In Chapter 2 the Hybrid Buck Switched-Inductor DC-DC converter (HBDC-L) is presented. A full analysis and design procedure was made. Equations for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor current are presented and discussed. A laboratory prototype of the HBDC-L was built to validate the theoretical considerations. Main current and voltage waveforms, simulation and experimental results are presented, discussed and compared.
- In Chapter 3 the Hybrid Buck Switched-Capacitor DC-DC converter (HBDC-C) is presented. A full analysis and design procedure is made. Analytical expressions for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor current are presented and discussed. The experimental results are obtained through a laboratory model, and are compared with the theoretical considerations. Main current and voltage, simulation and experimental waveforms are presented and discussed.
- In Chapter 4 the Hybrid Buck Switched-Capacitor/ Switched-Inductor DC-DC converter (HBDC-C/L) is proposed, as a combination between the HBDC-L and HBDC-C converters. Again, full analytical description and design procedure are made. Equations for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor current are presented and discussed. A laboratory model was built to validate the theoretical considerations, in order to compare and discuss current and voltage waveforms.
- In Chapter 5 a comparative study of a classical BDC, HBDC-C, HBDC-L and HBDC-C/L, in continuous current mode (CCM) and at the boundary (BCM) between CCM and discontinuous current mode (DCM), was made. The differences between the studied converters are presented and discussed in order to highlight the advantages and disadvantages in different situations.
- In Chapter 6, HBDC-L and HBDC-C are integrated in two real renewable energy and automotive industrial applications. The experimental setups are described, including some details regarding the equipment used in the experimental platform and experimental results are presented to validate the applications study.
- In Chapter 7, the overall conclusions, the main contributions and some future work are presented.

NOMENCLATURE

Abbreviations

BAT	Battery bank
BCM	Boundary conduction mode
C_1, C_2	Capacitors
CCM	Continuous current mode
CHG	Solar Charge Controller
C_{out}	Output capacitor
DB	Diodes bridge rectifier
DC	Direct current
DCM	Discontinuous current mode
GW	Gigawatts
HBDC	Hybrid Buck DC-DC converters
HBDC-C	Hybrid Buck Switched-Capacitor DC-DC converter
HBDC-C/L	Hybrid Buck Switched-Capacitor/Switched-Inductor DC-DC converter
HBDC-L	Hybrid Buck Switched-Inductor DC-DC converter
Inv	Inverter
MER	Multiple element resonant power
PMSG	Permanent magnet synchronous generator
PRC	Parallel resonant converters
PV	Photovoltaic
RCP	Rapid control prototyping
RMS	Root mean square
RTI	Real-time interface
SC	Supercapacitor
SR	Synchronous rectifier
SRC	Series resonant converters
T	Transistor
ZCS	Zero-current-switching
ZVS	Zero-voltage-switching

Symbols

C	Capacitor's capacity	F
D	Duty-cycle	-
D1, D2	Diodes	-
f_{min}	Minimum switching frequency	Hz
f_s	Switching frequency	Hz
I_{Cout}	Current through output capacitor	A
$I_{Cout,ripple}$	Output capacitor current ripple	A
I_D	Average forward current of one diode	A

I_{in}	Input current	A
$\hat{I}_{in}$	Peak input current	A
$I_{in,max}$	Maximum input current	A
$I_{in,min}$	Minimum input current	A
I_L	Inductor current	A
$I_{L,lim}$	Average value of the "limit" currents through the input and output inductances	A
$I_{L,lim,max}$	Maximum average inductor current in BCM	A
$I_{L,max}$	Maximum average inductor current	A
$I_{Lin,lim,max}$	Maximum average input inductor current in BCM	A
$I_{Lin,max}$	Maximum value of the current through the input inductor	A
$I_{Lin,min}$	Minimum value of the current through the input inductor	A
$\hat{I}_{Lout}$	Output peak inductor current	A
$I_{Lout,lim,max}$	Maximum average output inductor current in BCM	A
$I_{Lout,max}$	Maximum value of the current through the output inductor	A
$I_{Lout,min}$	Minimum value of the current through the output inductor	A
I_{out}	Average output current	A
$I_{out,max}$	Maximum output current	A
$I_{out,min}$	Minimum output current	A
I_T	Average value of the current through T during T_s	A
$\hat{I}_T$	Peak transistor current	A
$I_{T,max}$	Maximum transistor current	A
$I_{T,rms}$	Transistor RMS current	A
I_{Ton}	Average value of the current through T during t_{on}	A
L	Inductance	H
L_{in}	Input inductor	H
L_{out}	Output inductor	H
$P_{in,max}$	Maximum input power	W
$P_{out,max}$	Maximum output power	W
R	Resistance	Ω
T_s	Switching period	s
t_{on}, t_{off}	Switching periods	s
V_C	Voltage drop across the input capacitor	V
$V_{D,max}$	Maximum reverse voltage across a diode	V
V_{D1}	Reverse voltage of one diode	V
V_{in}	Input voltage	V
V_L	Voltage across the inductor	V
V_{Lin}	Voltage drop across the input inductor	V
V_{Lout}	Voltage drop across the output inductor	V
V_{out}	Output voltage	V
V_T	Voltage drop over the transistor	V
$V_{T,max}$	Maximum transistor voltage	V

Greek Symbols

η	Efficiency	%
Δi_L	Current variation	A
ΔV_{out}	Voltage ripple of the output capacitor	V

ΔI_{Lin}	Inductor current ripple	A
ΔV_C	Voltage ripple through capacitor	V
ΔV_{Cout}	Voltage ripple through output capacitor	V

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1. DC-DC CONVERTERS – A GENERAL OVERVIEW

1.1. Introduction

Energy technology is an interdisciplinary engineering science so important not only for global industrialization and general energy system but also in energy saving, renewable energy systems and automotive industry [1.1].

There are two types of energy sources: nonrenewable and renewable. Nowadays nonrenewable energy sources are petroleum, coal, natural gas and nuclear power. It can be said that the world is facing an energy crisis. Expert's opinions are divided regarding the exact moment when our nonrenewable energy sources will be gone (decades minimum, a few hundred years maximum). Mainstream renewable energy sources are wind power, hydropower, solar energy, biomass, biofuel and geothermal. A strong commitment regarding the renewable energies development can protect our environment by reducing emissions that contribute to global warming, increase economic development and preserve natural resources for future generations.

Figure 1.1 presents the global energy consumption in our days [1.1].
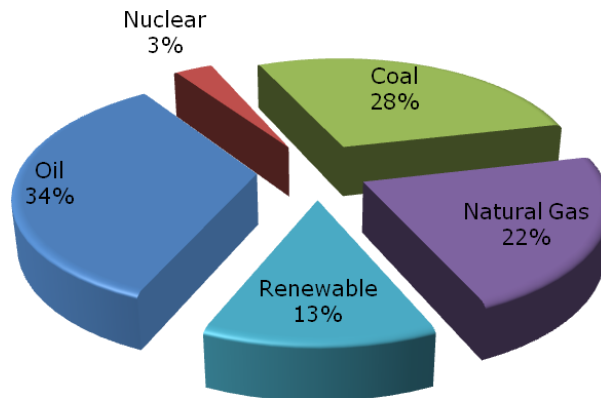
Fig.1.1. Global energy consumption.

Almost 84 % of total energy in the world is generated by fossil fuels (oil, coal, natural gas) the rest is provided by the renewable sources and nuclear power. Unfortunately, the use of fossil fuel generates pollutant gases (SO_2, CO, NO_X, HC and CO_2) which affect the environment. The United Nations (UN) Intergovernmental Panel on Climate Change (IPPC) said, with 90 % certainty, that the burning of fossil fuel causes the climate change problem [1.1].

The wide spread applications of power electronics in global industrialization are challenging the future electrical infrastructure and contributes to non-carbon based electricity production [1.2].

Total renewable power capacity worldwide exceeded 1,470 gigawatts [GW] in 2012, up about 8.5 % from 2011. Hydropower rose to an estimated 990 [GW], while other renewable grew 21.5 % to exceed 480 [GW]. Globally, wind power accounted for about 39 % of renewable power capacity added in 2012, followed by hydropower and solar PV, each accounting for approximately 26 % (Table 1.1). Solar PV capacity reached the 100 [GW] milestone to pass bio-power and become the third largest renewable technology in terms of capacity (but not generation), after hydro and wind [1.3].

TABLE 1.1. Global renewable energy capacity and biofuel production, 2012.

	Added during 2012	Existing at end-2012
Power Generation	(GW)	
Bio Power	+ 9	83
Geothermal power	+ 0.3	11.7
Hydropower	+ 30	990
Ocean power	∼ 0	0.5
Solar PV	+ 29	100
Concentrating solar thermal power CSP	+ 1	2.5
Wind power	+ 45	283
Hot Water/Heating	(GW_{th})	
Modern bio-heat	+ 3	293
Geothermal heating	+ 8	66
Solar collectors for water heating	+ 32	255
Transport Fuels	(billion liters/year)	
Biodiesel production	+ 0.1	22.5
Ethanol production	- 1.1	83.1

The increasing use of renewable energy systems imposes two big challenges [1.4]:
-   the first challenge would be a smooth transition of the electrical power production from the fossil-based and conventional energy sources to renewable energy sources;
-   the second challenge is related to the use of power electronics in power generation, the power transmission/distribution and the end-user application.

Considering the evolution of the power electronics technology in the last decades, who brought improvements for power electronic converters and renewable energy generation [1.4]-[1.9] together with intelligent control strategies, makes renewable energy systems more efficient and controllable in order to achieve a better and flexible integration with the power grid. The power electronic converters can be considered the heart of the renewable energy systems and are responsible for the power generation (Fig. 1.2).
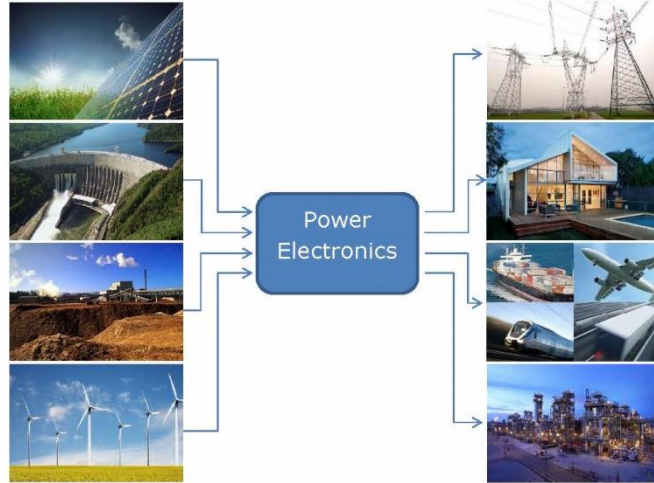
Fig.1.2. Power electronics as interface between renewable energy sources and consumers.

In the last decade the very dynamic automotive industry went through important changes and several radical paradigm shifts, in order to remain competitive under the market pressure. The commercial introduction of hybrid and electrical vehicles has also introduced under the hood a more complex electrical system which employs several busses of different voltages and of larger power than in regular cars. In such conventional cars the traditional 12 [V] bus must supply large currents due to a substantial increase of consumers. Recently, automakers have investigated the use of localized busses with larger voltages, such as 48 [V], for large consumers. In all situations, the interconnection between busses requires DC-DC converters with high power density and efficiency [1.10].

Dual voltage (42/14 [V]) automotive power systems have the possibility to convert the energy from 42 [V] to 14 [V] batteries/busses. When the power flow is unidirectional a Buck DC-DC converter structure is used [1.11].

Fig. 1.3 shows the typical topology of a dual power system with a DC-DC converter between the two power busses.
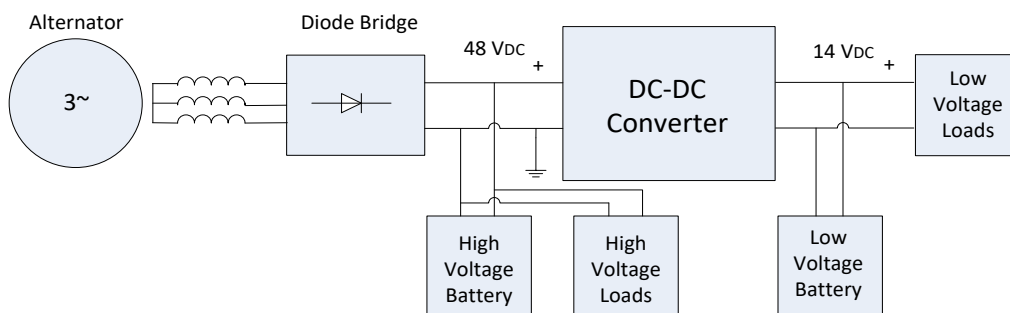
Fig.1.3. Dual voltage automotive power system.

In many renewable energy conversion systems, and especially in automotive applications, DC-DC converters, in conventional or dedicated structures, play an important role. Voltage conversion ratio, high efficiency, quality of the control algorithms, etc. are important goals treated in this research field.

A large number of converter topologies with higher voltage conversion ratios obtained from classical DC-DC converters by adding additional components have been presented in the literature [1.12-1.18]. Reference [1.12] presents several modified Ćuk converter topologies which incorporate additional capacitors or inductors. Each new passive component raises the input-to-output voltage conversion ratio but requires at least one additional diode and a transistor, which increases the complexity of the circuit and the cost.

Several configurations of quadratic converters obtained by applying a systematic synthesis procedure are presented in [1.13]. They can be used in applications where extremely large range of voltage conversion ratios are necessary and have the advantage of using only one additional transistor over two buck converters in cascade.

New topologies with increased voltage conversion ratio can be obtained by inserting capacitor-switching or inductor-switching cells into the simple step-up and step-down converters [1.14, 1.15].

New step-down converter topologies have been obtained by inserting simple circuits such as inductor-switching and capacitor-switching blocks in the structure of the classical DC-DC converters [1.14].

New step-up converter configurations obtained by inserting a step-up C-switching block in Ćuk, Zeta and Sepic converters are presented in [1.15].

Using a coupled-inductor cell, formed by a coupled inductor and a diode, in the structure of buck, boost, buck-boost, Ćuk, Sepic and Zeta converters, higher step-up and step-down conversion ratios were obtained in [1.16] and [1.17]. Paper [1.18] shows how step-up and step-down hybrid converter topologies with high voltage conversion ratios can be obtained from a DC-DC converter by inserting a capacitor-switching or an inductor-switching block in their structure. In the comparison with the conventional and quadratic DC-DC converters, presented in [1.18], it is shown that in the hybrid topologies, the energy stored in the magnetic field of the inductors is somehow higher than in the classical converters and much lower than in quadratic converters. A unified method can be used for developing hybrid converter topologies (HBDC), with advantages regarding the magnetic components, compared with the quadratic converters [1.18].

A comparative analysis of the conventional Buck DC-DC converter (BDC) and Hybrid Buck Switched-Inductor DC-DC converters (HBDC-L) in continuous conduction mode and boundary conduction mode, taking into account the average and RMS values of the input, output and inductors currents, and the maximum voltage and current stresses of the transistor was presented in [1.18]. The Hybrid Buck Switched-Capacitor DC-DC converter (HBDC-C) is obtained by inserting a capacitor-switching cell at the input of the BDC, [1.18] and [1.20]. Some comparison aspects between HBDC-C and BDC, regarding equations for average, RMS and peak transistor current, transistor voltage stress, peak and average values of input and output inductor currents in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are also treated in [1.20].

Other topologies which have, as hybrid converters, a higher voltage conversion ratio are quadratic converters, which can be used in several applications [1.21–1.24].

A high step-down conversion ratio can be obtained for BDC if the output filter inductor is replaced by a tapped-inductor (two coupled inductors). The duty cycle is extended by increasing the turn ratio of the tapped-inductor. Other advantages of this topology are the reduced voltage stress of the bottom switch for a synchronous converter and the improved efficiency [1.25]. Coupled inductors can be also used with good results in interleaved step-down converters [1.26].

By rearranging the components of the converter presented in [1.25] and adding one diode a wide-input-wide-output DC-DC topology can be obtained, which can be used for high step-up and step-down conversion ratios with high efficiency [1.27].

By replacing the simple inductor with a coupled inductor in a DC-DC converter or by coupling the two inductors in a hybrid L-switched cell converter, new high conversion ratio topologies can be obtained [1.25 – 1.29].

There is an increased interest in the utilization of the high voltage conversion ratio topologies (including the hybrid converters) in a wide range of industry applications [1.30 - 1.33].

For renewable energy applications a bidirectional DC-DC converter with high step-up/step-down voltage gain, presented in [1.30], was used to charge a 24 [V] battery from a 200 [V] DC-bus or to support the DC-bus using the battery stored energy.

An improvement in step-down conversion ratio and efficiency can be obtained for the interleaved buck converter for a different arrangement of components [1.31]. Only an additional capacitor is needed in comparison with the classical topology.

New configurations are proposed also for multi-input DC-DC converters with high step-up/down voltage conversion ratio [1.32, 1.33].

Some comparisons between conventional DC-DC converters and hybrid ones were presented in the literature [1.19, 1.20, 1.34], but the real place of the hybrid topologies in industry is not yet fully settled.

Buck, Boost and Buck-Boost combined with an L-switching or C-switching cell are named diode-assisted DC-DC converters in [1.34]. A short comparison is presented in the paper which shows that the modified converters are promising in some applications.

1.2. DC-DC converters topologies

Conversion technique is a big research area in the field of power electronics with applications in industry, research and development even in daily life. The conversion technique equipment can be classified in:

-   AC/AC transformers;
-   AC/DC rectifiers;
-   DC/DC converters;
-   DC/AC inverters.

Fig. 1.4 presents a classification of the DC-DC converters made in [1.35]. The DC-DC converters are divided in six generations for understanding the converter evolution and development [1.35]:

1. First generation (classical/traditional) converters;

2. Second generation (multiple quadrant) converters;
3. Third generation (switched component SI/SC) converters;
4. Fourth generation (soft switching: ZCS/ZVS/ZT) converters;
5. Fifth generation (synchronous rectifier SR) converters;
6. Sixth generation (multiple element resonant power MER) converters.

All topologies are sorted in three groups:

- Voltage-lift converters;
- Super-lift converters;
- Ultra-lift converters.

The voltage-lift converters can convert the input voltage into a higher voltage with high power efficiency, density and a simple structure. Voltage-lift technique is a method widely applied in electronic circuit design and his output voltage increased in arithmetic progression.

In super-lift technique the output voltage transfer gain can be very high, super-lift technique is more powerful than voltage-lift technique, and increases in arithmetical progression.

Ultra-lift technique combines the characteristics of Voltage-lift and Super-lift techniques to create the very high voltage transfer gain converter.

1.2.1. First generation converters

The first generation converters perform in a single quadrant mode, in low power range (<100 [W]) and is divided in five categories.

Fundamental Converters are Buck, Boost and Buck-Boost converters. The main problems of these converters are the very large output voltage ripple and the linkage between input and output.

Transformer-type Converters are a large group of converters like forward, push-pull, fly-back, half-bridge, bridge and Zeta converter. These converters have high transfer voltage gain (their gain depends usually on the transformer's turn ratio N) and high isolation between input and output.

Developed Converters are derived from fundamental converters they additionally have a low-pas filter. In this category are positive output (P/O) Luo-converter, negative output (N/O) Luo-converter, double output (D/O) Luo-converter, Cùk converter, Sepic and tapped inductor converters. With this type of converters a random output voltage, higher or lower than the input voltage, can be obtained and low output voltage ripple (lower than 2%).

Voltage Lift Converters divided in:
- Self-Lift Converters – derived from developed converters as Luo, Cùk and Sepic.
- Positive Output Luo-Converters – they work in the first quadrant with large voltage amplification.
- Negative Output Luo-Converters – they work in the third quadrant with large voltage amplification and perform positive to negative DC-DC voltage increasing conversion with cheap technology (simple structure), high efficiency and high power density.
- Modified Positive Output Luo-Converters.

DC-DC Converters

1 G
Classical Converters

Fundamental Circuits
- Buck Converter
- Boost Converter
- Buck-Boost Converter

Developed
- Positive Output Luo-Converter
- Negative Output Luo-Converter
- Double Output Luo-Converter
- Cùk Converter
- SEPIC
- Tapped-Inductor Converters

Transformer
- Forward Converter
- Fly-Back Converter
- Push-Pull Converter
- Half-Bridge Converter
- Bridge Converter
- ZETA Converter

Voltage-Lift
- 7 Self-Lift Converters
- Positive Output Luo-Converter
- Negative Output Luo-Converter
- Modified P/O Luo-Converter
- Double Output Luo-Converter

Super-Lift
- Positive Output Cascade Boost Converter
- Negative Output Cascade Boost Converter
- Positive Output Super-Lift Luo-Converter
- Negative Output Super-Lift Luo-Converter

2 G
Multi-Quadrant Converters

- Transformer-type Converter
- Developed → Multi Quadrant Luo-Converter

3 G
Switched-Component Converters

Switched-Capacitor Converter
- Two Quadrants Converter
- Four Quadrants SC Luo-Converters
- Multi-Lift
  - P/O Multi-Lift Push-Pull Luo-Converter
  - N/O Multi-Lift Push-Pull Luo-Converter

Switched-Inductor Converter
- Transformer-type Converter
- Four Quadrants SI Luo-Converters

4 G
Soft-Switching Converters

- ZCS-QRC----Four Quadrants Zero-Current Switching Luo-Converter
- ZVS-QRC----Four Quadrants Voltage-Current Switching Luo-Converter
- ZTC---- Four Quadrants Zero-Transition Luo-Converter

5 G
Synchronous Rectifier Converters

- Flat Transformer Synchronous Rectifier Converter
- Synchronous Rectifier Converter with Active Clamp Circuit
- Double Current Synchronous Rectifier Converter
- ZCS Synchronous Rectifier Converter
- ZVS Synchronous Rectifier Converter

6 G
Multi-Elements Resonant Power Converters

- 2-Elements
- 3-Elements - ∏ - CLL Current Sources on Resonant Inverter
- 4-Elements
  - Double Gamma-CL Current Source Resonant Inverter
  - Reverse Double Gamma-CL Resonant Inverter Power Converter

Fig.1.4. DC-DC converter family.

- Double Output Luo-Converters – perform from positive to positive and negative DC-DC voltage increasing conversion with cheap technology (simple structure), high efficiency and high power density.

Super Lift Converters – the typical circuits are sorted in four series: positive output super-lift Luo-converters, negative output super-lift Luo-converters, positive output cascade boost converters and negative output cascade boost converters.

1.2.2. Second generation converters

These converters are called multiple quadrant converters and perform two and four-quadrant operation with medium output power.

There are two categories of second generation converters: derived from first generation of converters and constructed with transformers. The transformer-type multi-quadrant converters can change the direction of the current using transformer polarity and diode rectifier. These converters are derived from the forward, half-bridge and bridge converters.

1.2.3. Third generation converters

Are called switched component converters and are built using capacitors and inductors (so called switch-capacitor, switch-inductor). These converters can perform in two or four-quadrant operation with high output voltage range, power density and high efficiency.

1.2.4. Fourth generation converters

Fourth generation converters are called soft-switching converters. The main categories are: zero-current-switching (ZCS), zero-voltage-switching (ZVS) and zero-transition (ZT) converters. These converters can perform in single quadrant operation but also in two and four-quadrant operation with high output power (thousands of W).

1.2.5. Fifth generation converters

These converters are called synchronous rectifier (SR) DC-DC converters and were required by the development of computing technology. The fundamental topology is derived from the forward converter.

1.2.6. Sixth generation converters

Sixth generation converters are called multiple energy storage elements resonant converters (MER). In the literature many topologies are series and parallel resonant converters (SRC, PRC) with two, three of four energy storage elements.

1.3. Classical Buck DC-DC converter (BDC)

The BDC is presented in detail (analysis and operating modes) in this chapter [1.35–1.37]. The justification for this subchapter is related by the fact that

all the hybrid DC-DC converters that will be described in the next chapters are derived from the BDC [1.18].

A basic DC-DC converter uses a pair of switches, usually one of the switches is controlled (transistor) and the other uncontrolled (diode) is used to ensure the power flow. The converter also uses a capacitor and an inductor to store and transfer energy from input to output and also to smooth or filter voltage and current.

The DC-DC converters can operate in two distinct modes: Continuous Current Mode (CCM) and Discontinuous Current Mode (DCM).

Figure 1.5 presents the BDC configuration and the t_{on}/t_{off} states.

a)

b)

c)
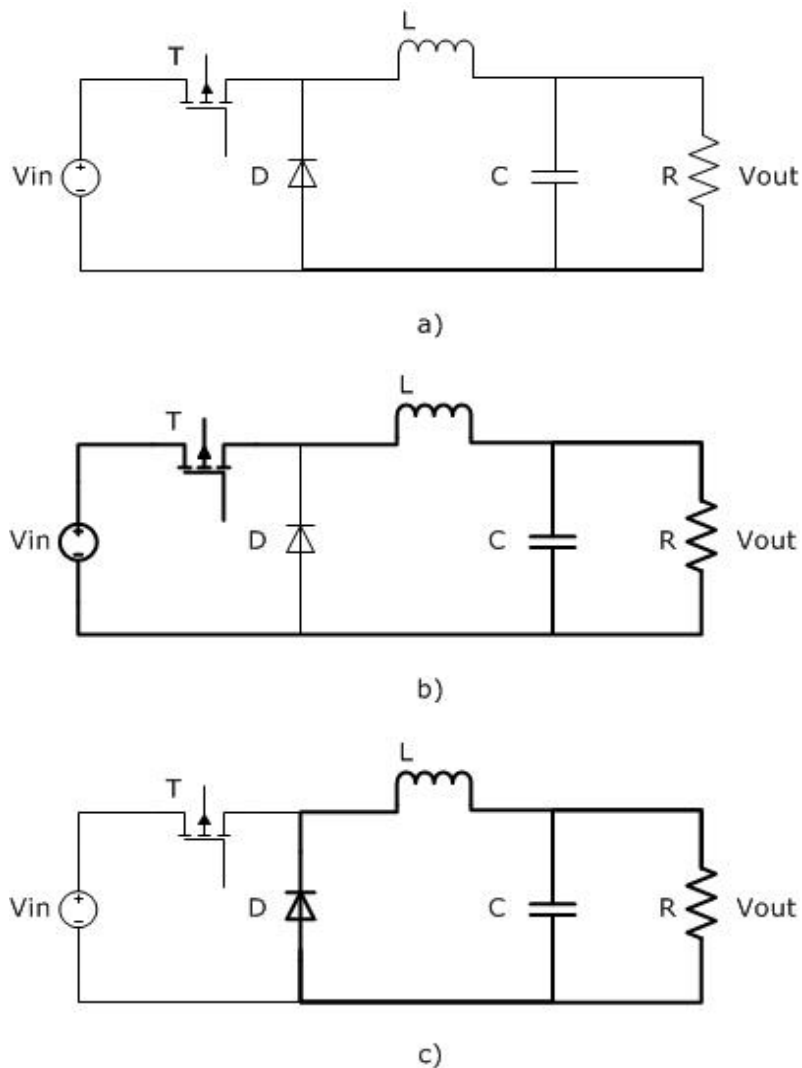
Fig.1.5. BDC:
a) Converter diagram; b) t_{on} switching topology; c) t_{off} switching topology.

When the controlled switch is on during a time interval, $D \cdot T_s$, the switch conducts the current through the inductor and the diode (uncontrolled switch) is reverse biased; a positive voltage across the inductor results.

$$v_L = V_{in} - V_{out} \tag{1.1}$$

When the switch is turned off, the current through the inductor continues to flow (because of the energy stored in the inductor) through the diode this time during a time interval, $(1-D) \, T_s$, until the switch is turned on again.

$$v_L = -V_{out} \tag{1.2}$$

The above two paragraphs are describing the operation mode of the BDC during one switching period, T_s.

1.3.1. BDC in continuous current mode (CCM)

Figure 1.6 presents the BDC waveforms for the voltage across the output inductor, current through the inductor, current through the output capacitor and output voltage in CCM.

If the input voltage V_{in} and the output voltage V_{out} are considered constant (C sufficiently large to assume that the output voltage ripple is zero) during one switching period, the following equations can be written:

$$\int_{0}^{T} v_L = \int_{0}^{t_{on}} v_L + \int_{0}^{t_{off}} v_L = 0 \tag{1.3}$$

$$(V_{in} - V_{out}) \cdot D \cdot T_s + (-V_{out}) \cdot (1-D) \cdot T_s = 0 \tag{1.4}$$

The relation between V_{out} and V_{in} given in (1.5) is obtained from (1.3) and (1.4).

$$V_{out} = D \cdot V_{in} \tag{1.5}$$

The duty cycle, D, as a function of output to input voltage ratio is:

$$D = \frac{t_{on}}{T_s} = \frac{V_{out}}{V_{in}} \tag{1.6}$$

Considering the BDC efficiency ($P_{in} = \eta \cdot P_{out}$) the following equation can be written:

$$V_{in} \cdot I_{in} = \eta \cdot V_{out} \cdot I_{out} \tag{1.7}$$

Considering $\eta = 1$:

$$\frac{I_{out}}{I_{in}} = \frac{V_{in}}{V_{out}} = D \tag{1.8}$$
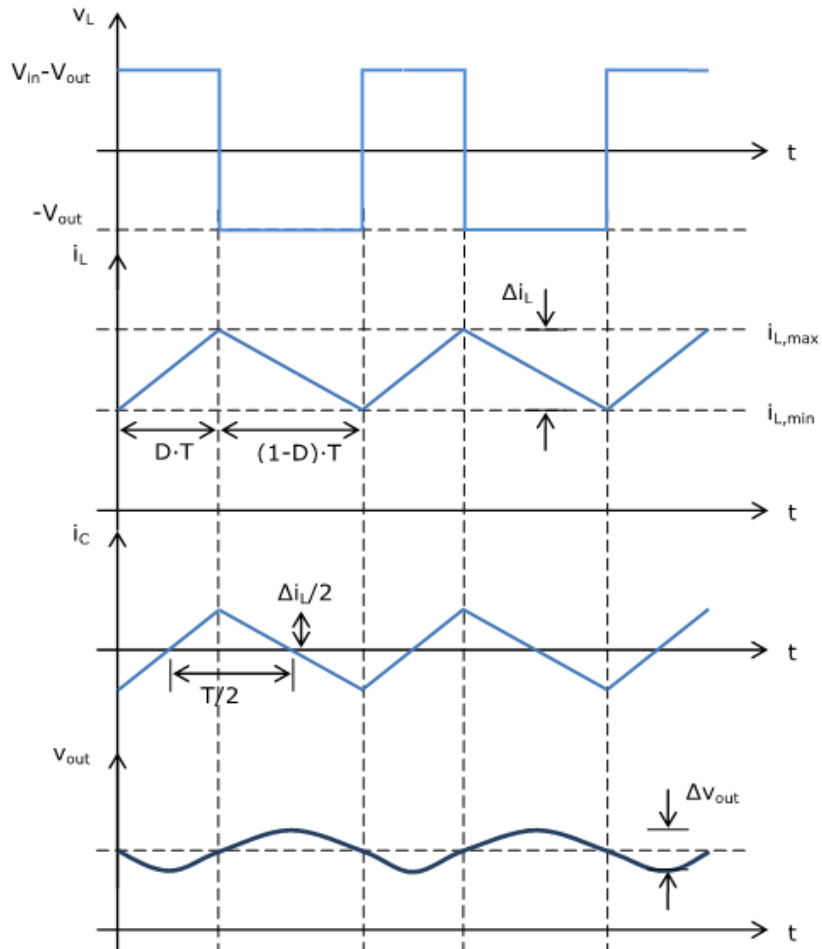
Fig.1.6. BDC waveforms.

For BDC the average value of the inductor current is equal with the output current.

$$I_L = I_{out} \tag{1.9}$$

The current variation of the output inductor is given by the following expression:

$$\Delta i_L = \frac{1}{L} \cdot \int_0^{D \cdot T_s} v_L \cdot dt \tag{1.10}$$

The maximum and minimum values of the inductor current are given by equations (1.11) and (1.12):

$$I_{L,max} = I_L + \frac{\Delta i_L}{2} \tag{1.11}$$

$$I_{L,min} = I_L - \frac{\Delta i_L}{2} \tag{1.12}$$

The average value of the output current which is equal with the current through the output inductor can be calculated with:

$$I_L = I_{out} = \frac{V_{out}}{R} \tag{1.13}$$

The voltage ripple of the output capacitor:

$$\Delta v_C = \Delta v_{out} = \frac{1}{C} \cdot \int i_C \cdot dt = \frac{1}{C} \cdot \frac{1}{2} \cdot \frac{T_s}{2} \cdot \frac{\Delta i_L}{2} \tag{1.14}$$

therefore:

$$\Delta v_{out} = \frac{1}{C} \cdot \int i_C \cdot dt = \cdot \frac{\Delta i_L}{8 \cdot f_s \cdot C} \tag{1.15}$$

The average current through the transistor during t_{on} switching time is equal with the average current through the output inductor.

$$I_{T_{on}} = I_{L_{on}} = I_{out} \tag{1.16}$$

The average value of the current through transistor during the entire switching period can be calculated from $I_{T,on}$ using equation (1.17):

$$I_T = I_{T_{on}} \cdot D = I_{out} \cdot D \tag{1.17}$$

The average current through the diode during t_{off} switching time is equal with the average current through the output inductor in the same time interval and equal with zero during t_{on} switching time.

All the above presented equations are true when the BDC is operating in CCM.

The Boundary Current Mode (BCM), by definition, is an operating mode at the limit between CCM and DCM when the current through the inductor goes to zero at the end of the t_{off} switching time.

In BCM the average current through the output inductor is:

$$I_L = I_{out} = \frac{\Delta i_L}{2} \tag{1.18}$$

The minimum inductor current in this case is equal with zero and the maximum inductor current is equal with Δi_L.

Fig. 1.7 presents the waveforms of the voltage drop across the output inductor and the current through the output inductor in BCM.
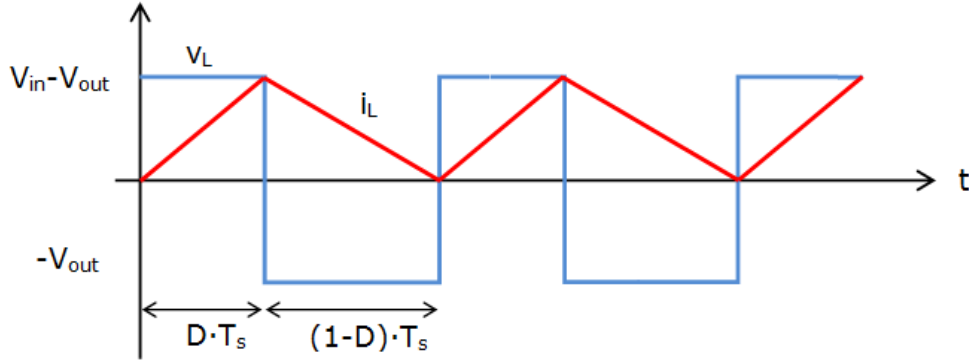
Fig.1.7. BDC waveforms for BCM.

From (1.13) and (1.19) the minimum output current expression (1.20) can be calculated:

$$\Delta i_L = \frac{1}{L} \cdot (V_{in} - V_{out}) \cdot D \cdot T_s = \frac{1}{L} \cdot V_{out} \cdot (1 - D) \cdot T_s \qquad (1.19)$$

$$I_{out,min} = I_L = \frac{1}{2 \cdot L} \cdot V_{out} \cdot (1 - D) \cdot T_s \qquad (1.20)$$

In BCM, using (1.13) and (1.20), the expressions of f_s, R and L can be obtained. The minimum inductor current (1.22) for CCM can be obtained if the switching frequency and the load are established.

$$\frac{V_{out}}{R} = \frac{1}{2 \cdot L} \cdot V_{out} \cdot (1 - D) \cdot T_s \qquad (1.21)$$

$$L_{min} = \frac{(1 - D) \cdot R}{2 \cdot f_s} \qquad (1.22)$$

If the values of the inductance L and resistance R are established, the minimum switching frequency for CCM is given by:

$$f_{s\,min} = \frac{(1 - D) \cdot R}{2 \cdot L} \qquad (1.23)$$

If the values of the switching frequency f_s and inductance L are established, the minimum output load R for CCM can be calculated:

$$R_{min} = \frac{2 \cdot f_s \cdot L}{(1 - D)} \qquad (1.24)$$

1.3.2. BDC in discontinuous current mode (DCM)

The Discontinuous Current Mode (DCM), by definition, is an operating mode of the BDC in which the current through the inductor goes to zero in a smaller time interval that the t_{off} switching time.

Fig. 1.8 presents the waveforms of the voltage drop across the output inductor and the current through the output inductor in DCM.

The most common applications for this type of converter require keeping the output voltage constant. DCM will be treated using Fig. 1.8 as a visual support.

Using (1.8) and (1.20) the maximum average inductor current can be expressed:

$$\lim_{D \to 0}(I_{L,lim}) = I_{L,lim,max} = \frac{1}{2 \cdot L} \cdot V_{out} \cdot T_s \qquad (1.25)$$

The relation between the average inductor current (1.20) and maximum average inductor current (1.25) can be expressed using (1.26):

$$I_{L,lim} = I_{L,lim,max} \cdot (1-D) \qquad (1.26)$$

The expression of the voltage conversion ratio is:

$$\frac{V_{out}}{V_{in}} = \frac{D}{D + \Delta_1} \qquad (1.27)$$
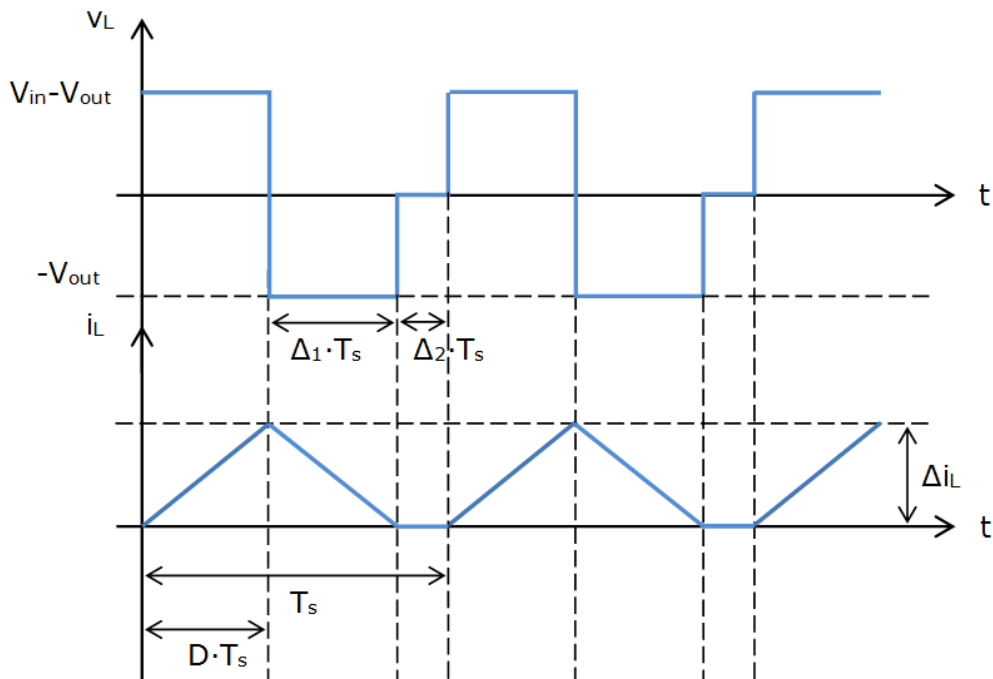
Fig.1.8. BDC waveforms for DCM.

The maximum average inductor current equation:

$$I_{L,max} = \frac{\Delta_1}{L} \cdot V_{out} \cdot T_S \qquad (1.28)$$

The average output current can be expressed as:

$$I_{out} = I_{L,max} \cdot \frac{D + \Delta_1}{2} = I_{out,lim,max} \cdot \Delta_1 \cdot (D + \Delta_1) \qquad (1.29)$$

Using (1.27) and (1.29) the expression of the duty cycle can be determined:

$$D = \frac{V_{out}}{V_{in}} \cdot \sqrt{\frac{\dfrac{I_{out}}{I_{L,lim,max}}}{1 - \dfrac{V_{out}}{V_{in}}}} \qquad (1.30)$$

1.4. Hybrid DC-DC converters

Hybrid structures, using switched-capacitors and/or switched-inductors, have been reported as an alternative to high frequency transformer converters.

A new approach is proposed in [1.18]: simple circuits, formed by either two capacitors and two or three diodes, or two inductors and two or three diodes are defined. These simple circuits or switching blocks are inserted in the structure of classical Buck, Boost, Buck-Boost, Cửk, Sepic and Zeta converters in order to obtain high step-up and step-down voltage conversion ratios.

The voltage conversion ratio expression shows that the hybrid converters are able to reduce/increase the output voltage more than the original converter.

The superiority of these hybrid converters is based on less energy in the magnetic field, leading to saves in the size and cost of the inductors, and less current stress in the switching elements, leading to smaller conduction losses [1.18]. These hybrid converters have the same number of elements as the quadratic converters and their performances (DC gain, current and voltage stress for the transistors and diodes, current through inductors) are compared to those of quadratic converters in [1.18].

1.4.1. Switched-capacitors/switched-inductor step-down/step-up structures

Fig. 1.9 presents three switching cells formed by either two capacitors C_1, C_2, $C_1 = C_2$, and three diodes D_1, D_2, D_{12} (Fig. 1.9.a) or two inductors L_1, L_2, $L_1 = L_2$ and two diodes D_1, D_2 (Fig. 1.9.b and c).

These switching cells can provide a step-down of the input voltage and will be denoted with Down 1, Down 2 and Down 3.

For the switching block Down 1 (Fig. 1.9.a) in t_{on} switching topology capacitors C_1 and C_2 are discharged in parallel and in t_{off} switching topology the capacitors are charged in series ($V_{C1} = V_{C2} = V_C$). For Down 2 and 3 circuits, in t_{on}

switching topology the inductors (L_1 and L_2) are charged in series and discharged in parallel in t_{off} switching topology.

Fig. 1.10 presents three switching cells formed by either two capacitors C_1, C_2, $C_1=C_2$, and two diodes D_1, D_2 (Fig. 1.10.a and b) or two inductors L_1, L_2, $L_1=L_2$ and three diodes D_1, D_2, D_{12} (Fig. 1.10.c).
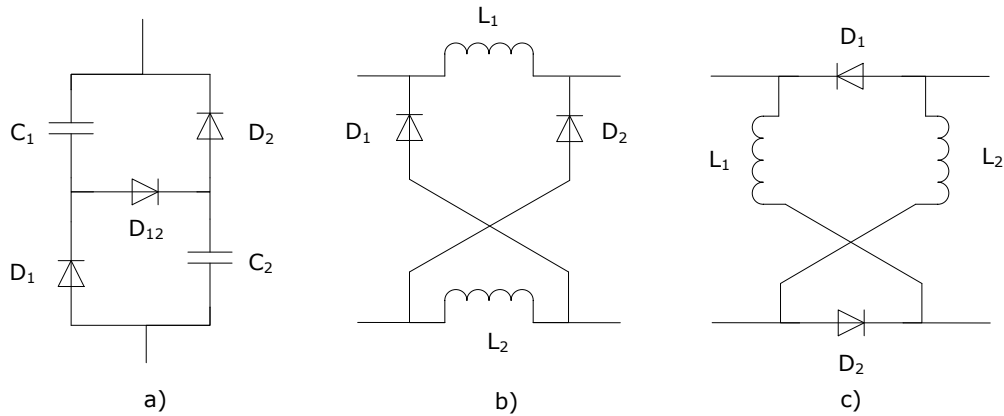
Fig.1.9. Step-down switching cells:
a) Down 1; b) Down 2; c) Down 3.
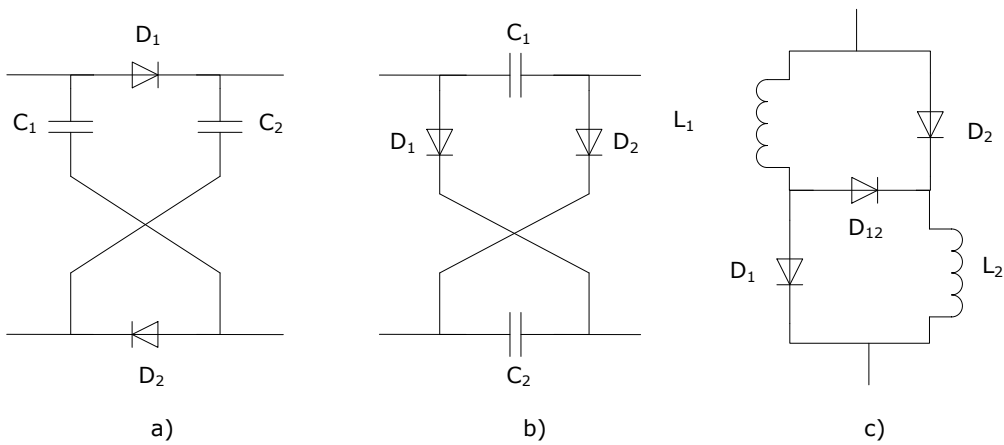
Fig.1.10. Step-up switching cells:
a) Up 1; b) Up 2; c) Up 3.

These switching cells can provide a step-up of the input voltage and will be denoted with Up 1, Up 2 and Up 3.

During t_{off} switching topology, for Up 1 and Up 2 (Fig. 1.10.a and b), C_1 and C_2 are charged in parallel ($V_{C1}=V_{C2}$) and discharged in series during t_{on} switching topology. For Up 3 (Fig. 1.10.c), during t_{on} switching topology, inductors L_1 and L_2

are charged in parallel and during t_{off} switching topology the inductors are discharged in series.

1.4.2. New hybrid transformerless DC-DC converters

The presented switching cells are inserted in the structure of the classical Buck, Boost, Buck-Boost, Cửk, Sepic and Zeta converters according to Table 1.2.

TABLE 1.2. Possible implementation of Hybrid DC-DC converters using C/L switching cells.

C/L circuit Converter	Down 1	Down 2	Down 3	Up 1	Up 2	Up 3
Buck	●	●				
Boost				●		●
Buck-Boost	●			●		●
Cửk	●	●			●	●
Sepic	●		●			●
Zeta		●			●	●

Hybrid Buck converters are obtained by inserting Down 1 and Down 2 switching cells in the structure of the BDC. Two hybrid step-down DC-DC converters are obtained and presented in Fig. 1.11 and Fig. 1.12.

The Hybrid Buck converter presented in Fig. 1.11 is obtained by inserting an inductor (in order to reduce the input current ripple), L_{in}, and the Down 1 switching cell at the input of the BDC.
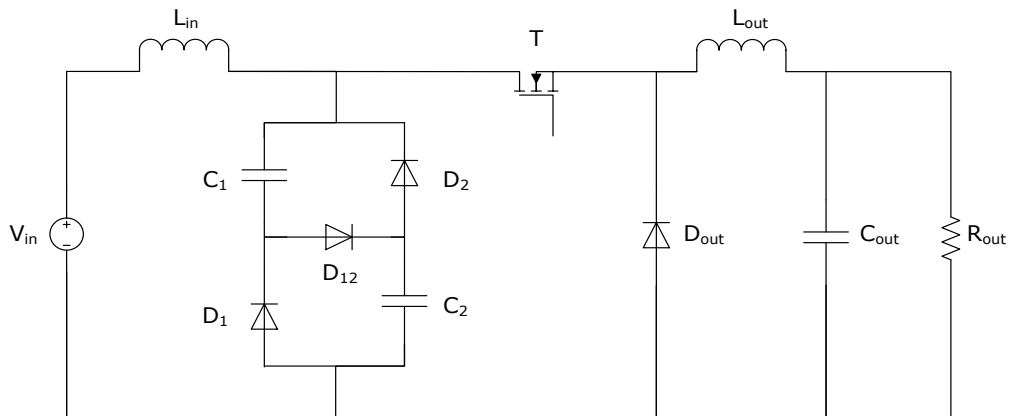
Fig.1.11. Hybrid Buck DC-DC converter with switching block Down 1.

The Hybrid Buck converter presented in Fig. 1.12 is obtained by replacing the output inductor and the output diode of the BDC with the Down 2 switching cell.

The voltage conversion ratio is the same for both hybrid converters:

$$\frac{V_{out}}{V_{in}} = \frac{D}{2-D} \tag{1.31}$$

The output voltage is reduced (2-D) times more than in the case of the BDC.
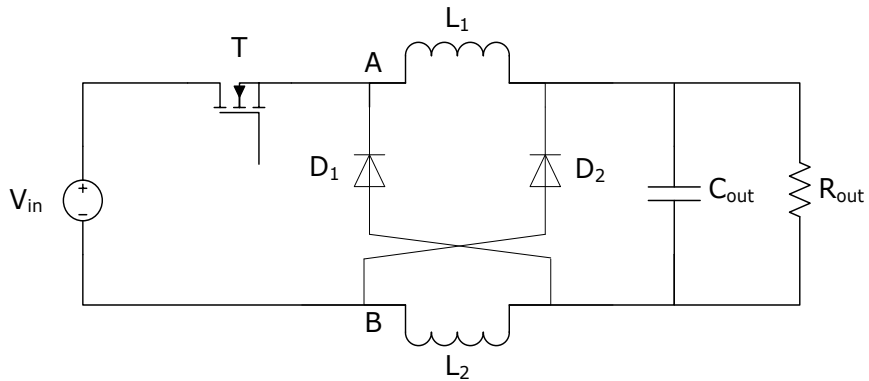
Fig.1.12. Hybrid Buck DC-DC converter with switching block Down 2.

Hybrid Boost converters are obtained by inserting Up 1 and Up 3 switching cells in the structure of the classical Boost converter. Two hybrid step-up DC-DC converters are obtained and presented in Fig. 1.13 and Fig. 1.14.

The Hybrid Boost converter presented in Fig. 1.13 is obtained by replacing the diode of the classical Boost converter with the Up 1 switching cell and inserting an inductor (in order to reduce the output current ripple), L_{out}, after Up 1 switching circuit.
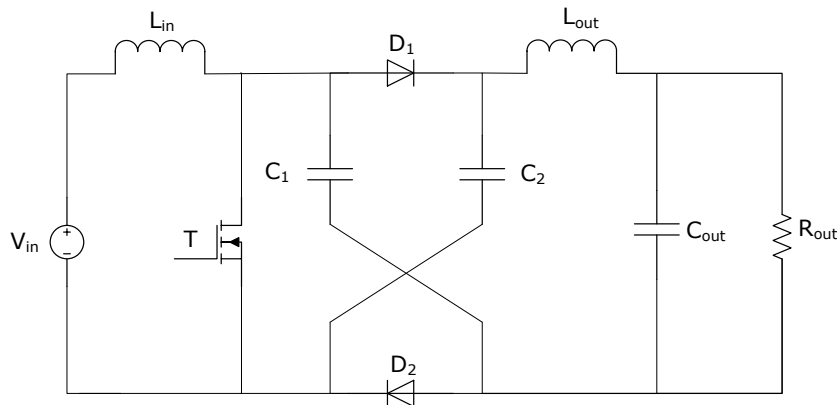
Fig.1.13. Hybrid Boost DC-DC converter with switching block Up 1.

The voltage conversion ratio for the hybrid Boost DC-DC converter with switching cell Up 1:

$$\frac{V_{out}}{V_{in}} = \frac{1 + D}{1 - D}$$

(1.32)

The output voltage is boosted (1+D) times more than in the case of the classical Boost converter.

The Hybrid Boost converter presented in Fig. 1.14 is obtained by replacing the input inductor, L_{in}, of the classical Boost converter with the Up 3 switching block.
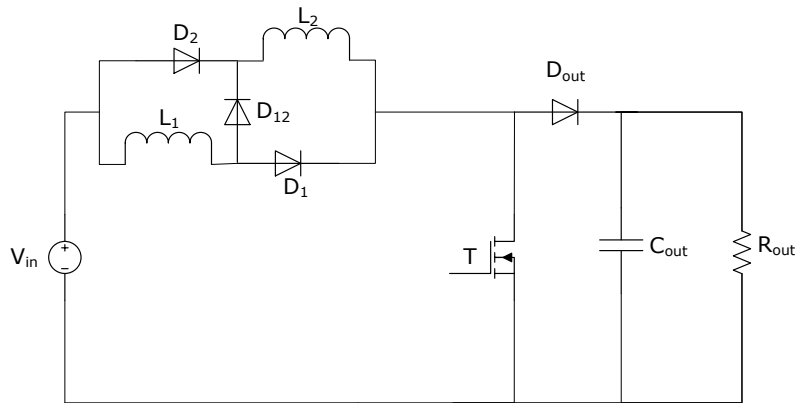
Fig.1.14. Hybrid Boost DC-DC converter with switching block Up 3.

Hybrid Buck-Boost converters are obtained, as shown in Table 1.2, by inserting Down 1, Up 1 and Up 3 switching cells in the structure of the classical Buck-Boost converter. Three hybrid DC-DC converters are obtained (two step-up and one step-down hybrid DC-DC converters) and presented in Fig. 1.15 - Fig. 1.17.

The Hybrid Buck-Boost DC-DC converter presented in Fig. 1.15 is obtained by inserting an inductor (in order to reduce the input current ripple), L_{in}, and the Down 1 switching cell at the input of the classical Buck-Boost converter.
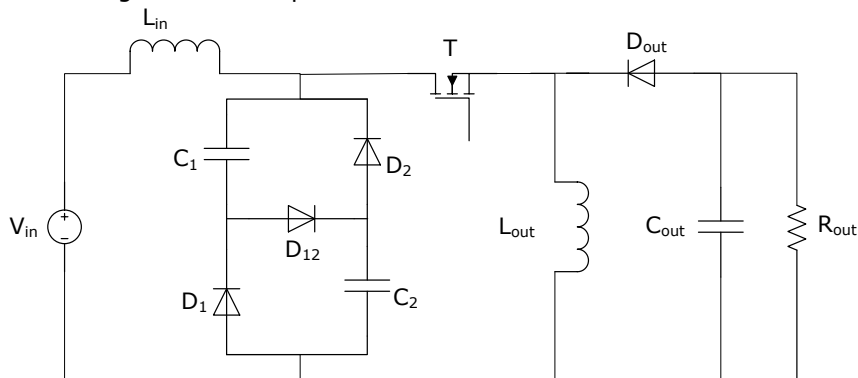
Fig.1.15. Hybrid Buck-Boost DC-DC converter with switching block Down 1.

The voltage conversion ratio for Hybrid Buck-Boost DC-DC converter with Down 1 switching block:

$$\frac{V_{out}}{V_{in}} = \frac{D}{(1-D)\cdot(2-D)} \tag{1.33}$$

The output voltage is reduced (2-D) times more than in the case of the classical Buck-Boost converter.

The Hybrid Buck-Boost DC-DC converter presented in Fig. 1.16 is obtained by replacing the diode of the classical Buck-Boost converter with the Up 1 switching cell and by inserting an inductor, L_{out}, in order to reduce the output current ripple.
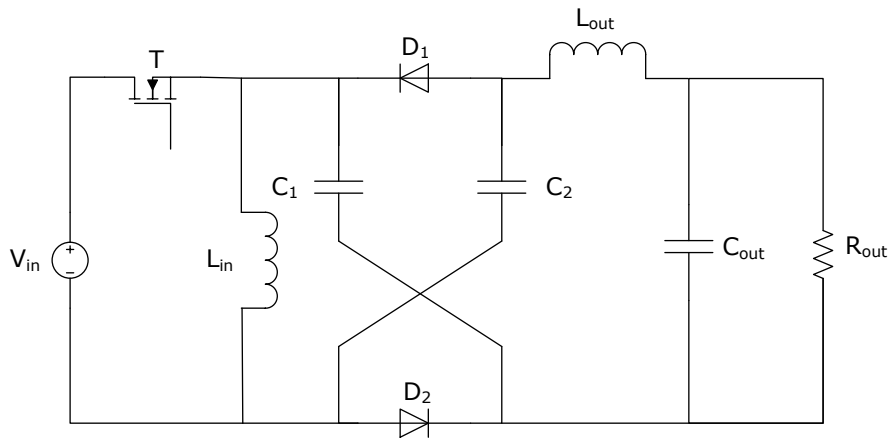
Fig.1.16. Hybrid Buck-Boost DC-DC converter with switching block Up 1.

The Hybrid Buck-Boost DC-DC converter presented in Fig. 1.17 is obtained by replacing the inductor of the classical Buck-Boost converter with the Up 3 switching cell.
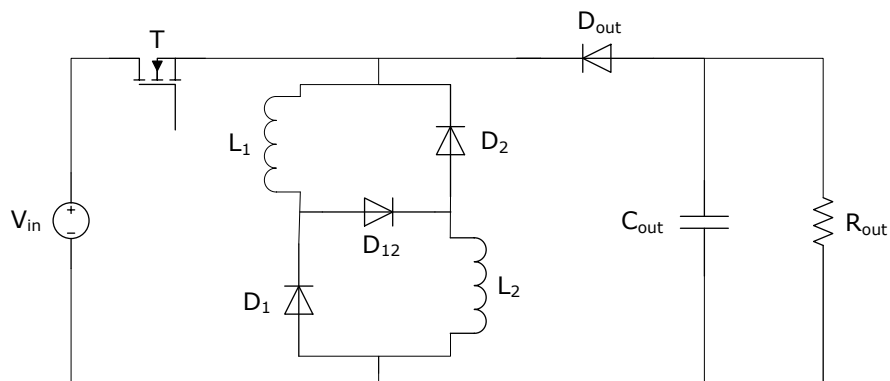
Fig.1.17. Hybrid Buck-Boost DC-DC converter with switching block Up 3.

The voltage conversion ratio is the same for Hybrid Buck-Boost DC-DC converter with switching block Up 1 and Up 3:

$$\frac{V_{out}}{V_{in}} = \frac{2 \cdot D}{(1-D)} \tag{1.34}$$

For both converters, presented in Fig. 1.16 and Fig. 1.17, the double of the voltage conversion ratio of the classical Buck-Boost converter is achieved.

Hybrid Cúk converters are obtained, as shown in Table 1.2, by inserting either the step-down switching blocks Down 1 and Down 2, or step-up switching cells Up 2 and Up 3 in the structure of the classical Cúk converter.

Four hybrid DC-DC converters are obtained (two step-up and two step-down hybrid DC-DC converters) and presented in Fig. 1.18 - Fig. 1.21.

The Hybrid Cúk DC-DC converter presented in Fig. 1.18 is obtained by replacing the capacitor of the classical Cúk converter with the Down 1 switching cell.
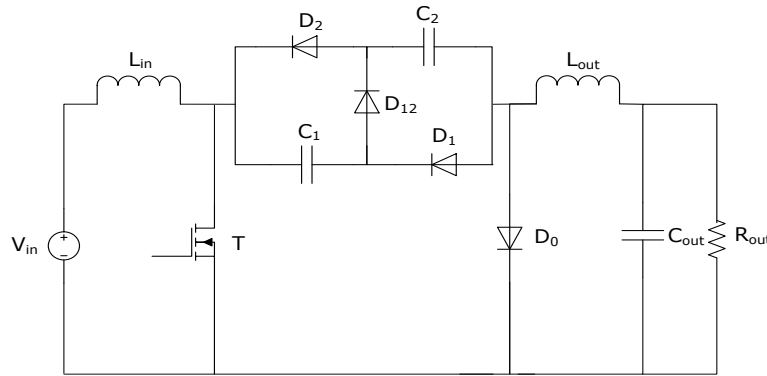
Fig.1.18. Hybrid Cúk DC-DC converter with switching block Down 1.

The Hybrid Cúk DC-DC converter presented in Fig. 1.19 is obtained by replacing the diode of the classical Cúk converter with the Down 2 switching cell.
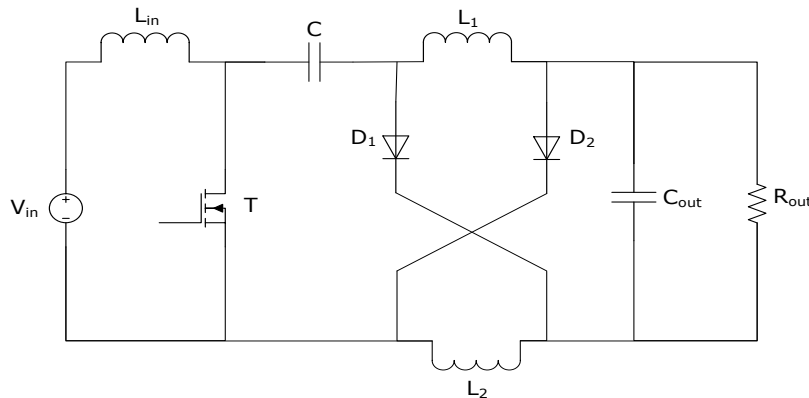
Fig.1.19. Hybrid Cúk DC-DC converter with switching block Down 2.

For the Hybrid Củk DC-DC converter presented in Fig. 1.18 and Fig. 1.19, the voltage-second balance equations on the inductors lead to:

$$\frac{V_{out}}{V_{in}} = \frac{D}{2 \cdot (1-D)}$$ (1.35)

resulting a step-down voltage ratio two times smaller than in the case of classical Củk converter.

The Hybrid Củk DC-DC converter presented in Fig. 1.20 is obtained by replacing the capacitor of the classical Củk converter with the Up 2 switching cell.

The Hybrid Củk DC-DC converter presented in Fig. 1.21 is obtained by replacing the capacitor of the classical Củk converter with the Up 3 switching cell.

The voltage-second balance equations on the inductors in Fig. 1.20 lead to:

$$\frac{V_{out}}{V_{in}} = \frac{1+D}{(1-D)}$$ (1.36)
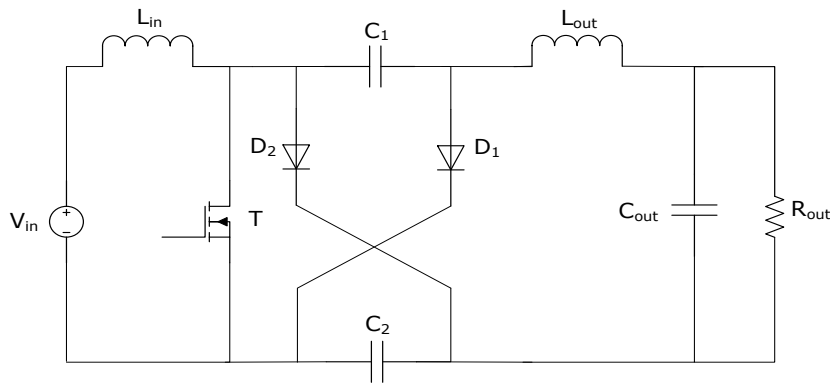
Fig.1.20. Hybrid Củk DC-DC converter in step-up mode with switching block Up 2.
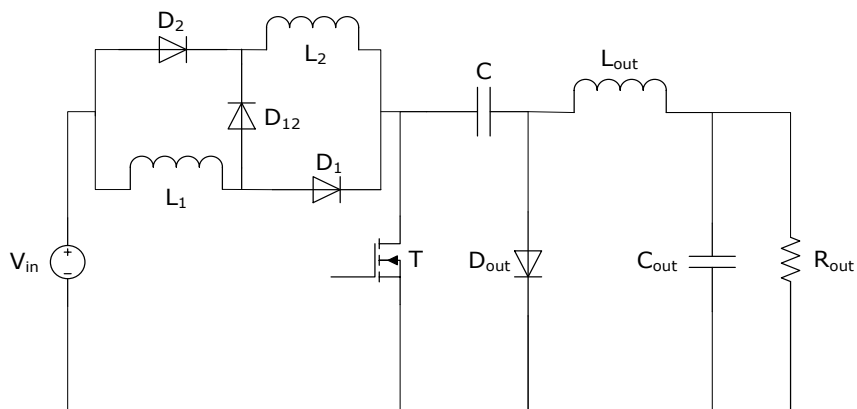
Fig.1.21. Hybrid Củk DC-DC converter in step-up mode with switching block Up 3.

The voltage-second balance equations on the inductors in Fig. 1.21 lead to:

$$\frac{V_{out}}{V_{in}} = \frac{D \cdot (1+D)}{(1-D)} \qquad (1.37)$$

resulting a step-up (1+D) times more than in the case of classical Cùk converter.

Hybrid Sepic converters are obtained, as shown in Table 1.2, by inserting either the step-down switching blocks Down 1 and Down 3, or step-up switching cell Up 3 in the structure of the classical Sepic converter.

The Hybrid Sepic DC-DC converter presented in Fig. 1.22 is obtained by replacing the capacitor of the classical Sepic converter with the Down 1 switching cell.
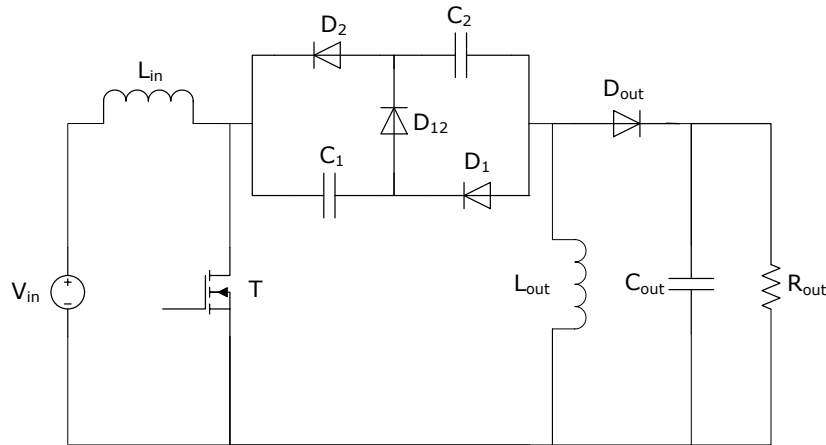
Fig.1.22. Hybrid Sepic DC-DC converter in step-down mode using switching block Down 1.

The voltage conversion ratio for this hybrid converter is:

$$\frac{V_{out}}{V_{in}} = \frac{D}{(1-D) \cdot (2-D)} \qquad (1.38)$$

The output voltage is reduced (2-D) times more than in the case of the classical Sepic converter.

The Hybrid Sepic DC-DC converter presented in Fig. 1.23 is obtained by replacing the output inductor and diode of the classical Sepic converter with the Down 3 switching cell.

The voltage conversion ratio for this hybrid converter is:

$$\frac{V_{out}}{V_{in}} = \frac{D}{2 \cdot (1-D)} \qquad (1.39)$$

The output voltage is reduced two times more than in the case of the classical Sepic converter.

The Hybrid Sepic DC-DC converter presented in Fig. 1.24 is obtained by replacing the input inductor of the classical Sepic converter with the Up 3 switching cell.

The voltage conversion ratio for this hybrid converter is:

$$\frac{V_{out}}{V_{in}} = \frac{D \cdot (1+D)}{(1-D)} \qquad (1.40)$$

The output voltage is (1+D) times more than in the case of the classical Sepic converter.
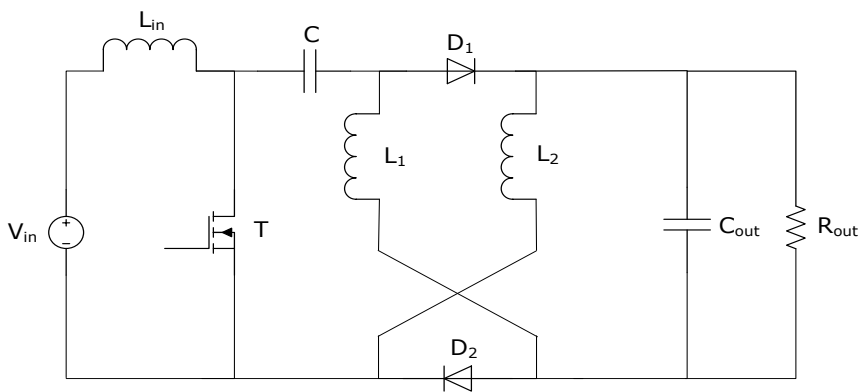
Fig.1.23. Hybrid Sepic DC-DC converter in step-down mode using switching block Down 3.
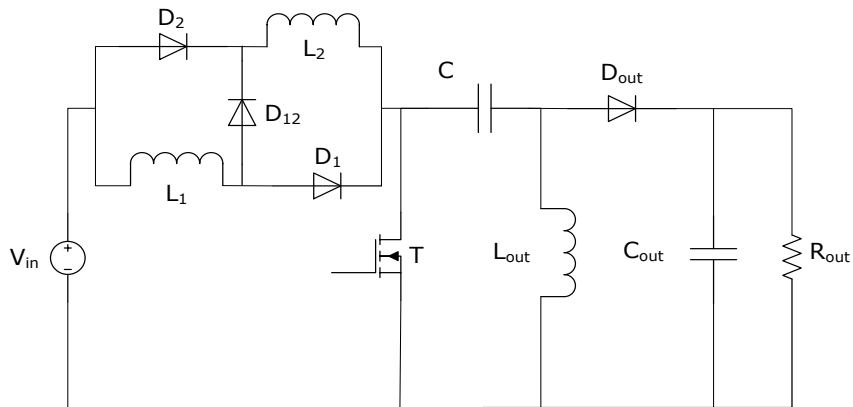
Fig.1.24. Hybrid Sepic DC-DC converter in step-up mode using switching block Up 3.

Hybrid Zeta converters are obtained by inserting either the step-down switching block Down 2, or step-up switching cells Up 2 and Up 3 in the structure of the classical Zeta converter.

The Hybrid Zeta DC-DC converter presented in Fig. 1.25 is obtained by replacing the output diode and inductor of the classical Zeta converter with the Down 2 switching cell.

The voltage conversion ratio for this hybrid converter is:

$$\frac{V_{out}}{V_{in}} = \frac{D}{2 \cdot (1-D)} \tag{1.41}$$
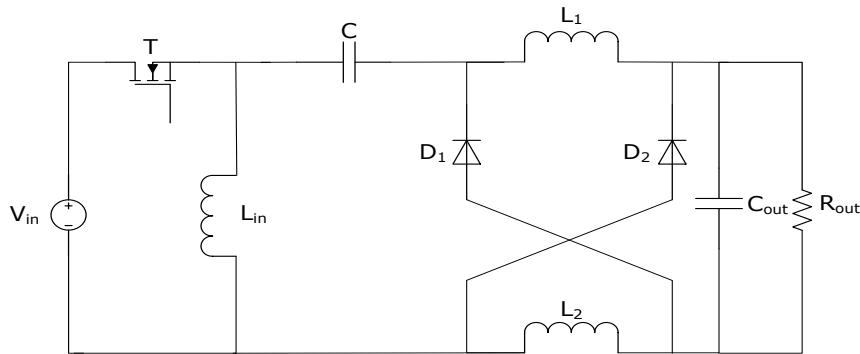
Fig.1.25. Hybrid Zeta DC-DC converter in step-down mode using switching block Down 2.

which shows a two times reduction of the output voltage compared with the classical Zeta converter.

The Hybrid Zeta DC-DC converter presented in Fig. 1.26 is obtained by replacing the middle capacitor and the output diode of the classical Zeta converter with the Up 2 switching cell.

The voltage conversion ratio is the same for this hybrid converter:

$$\frac{V_{out}}{V_{in}} = \frac{D}{2 \cdot (1-D)} \tag{1.42}$$
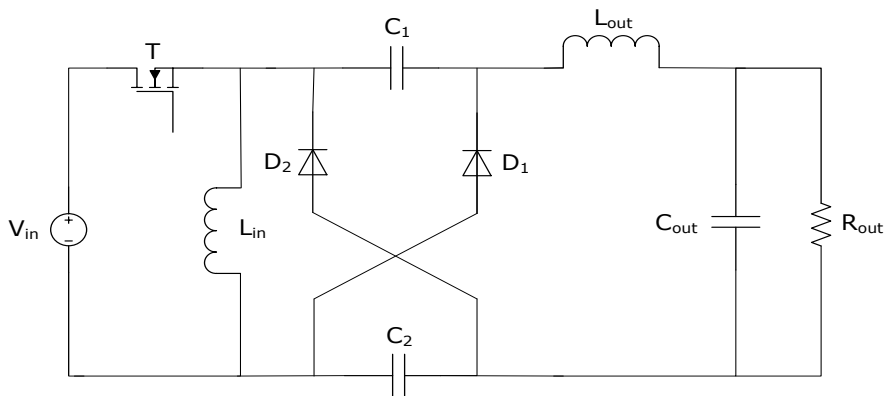
Fig.1.26. Hybrid Zeta DC-DC converter in step-up mode using switching block Up 2.

The Hybrid Zeta DC-DC converter presented in Fig. 1.27 is obtained by replacing the input inductor of the classical Zeta converter with the Up 3 switching cell.

The voltage conversion ratio for this hybrid converter is:

$$\frac{V_{out}}{V_{in}} = \frac{D \cdot (1+D)}{(1-D)} \tag{1.43}$$

In this case the output voltage is (1+D) times larger than that provided by the classical Zeta converter.
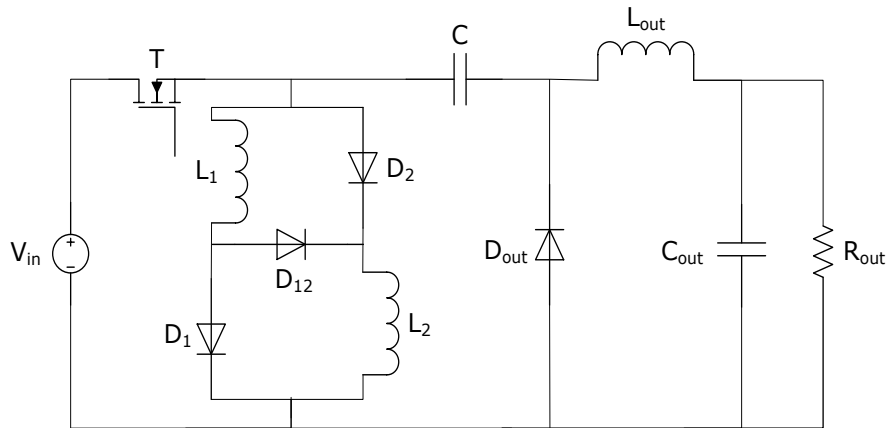
Fig.1.27. Hybrid Zeta DC-DC converter in step-up mode using switching block Up 3.

1.5. Conclusion

This chapter is designed to fit the thesis topic in the DC-DC converters family and industry related applications.

A general overview of the main DC-DC converters topologies and applications in the renewable energy and automotive areas was made.

BDC, used as the reference converter in this work, was analyzed.

A way to create new transformerless DC-DC converters, starting from classical DC-DC converter structures, using switched-capacitor or switched-inductor cells was presented. These converters can obtain a high ratio of the input (output)/output (input) voltages.

Two of the presented transformerless Buck DC-DC converters, derived from the BDC converter, and a new proposed topology, combining the first two structures, will make the subject of this work.

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2. HYBRID BUCK SWITCHED-INDUCTOR DC-DC CONVERTER (HBDC-L)

2.1. Introduction

Considering the evolution of the power electronics technology in the last decades, who brought improvements for power electronic converters [2.1-2.6] together with intelligent control strategies, makes renewable energy systems more efficient and controllable in order to achieve a better and flexible integration with the power grid [2.7-2.9]. PWM-based DC-DC converters combining the switched-inductor structures and switched-capacitor function providing a very large output voltage with different output DC levels are presented in [2.8-2.10]. DC-DC converters using switched-inductor structures are presented in [2.11-2.32].

As in the Chapter 1 has been presented, HBDC-L is a step-down converter obtained from the classical structure of the BDC by inserting a simple circuit (L-switching cell) in his structure [2.29].

This simple circuit or switching block (presented in Fig. 2.1.a) is formed by two identical inductors (L_1 and L_2) and two diodes (D_1 and D_2). The switching topologies of the L-switching cell are presented in Fig. 2.1.b and c:
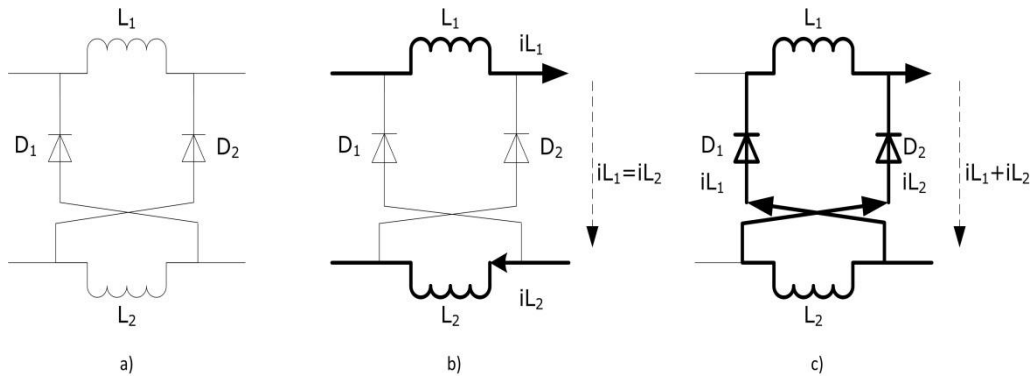
Fig.2.1. L-switching cell:
a) Circuit topology; b) t_{on} switching topology; c) t_{off} switching topology.

During t_{on} switching time the inductors (L_1 and L_2) are charged in series from the input voltage as can be seen in Fig. 2.1.b; in the t_{off} switching time the inductors are discharged in parallel. In the t_{off} switching time the output of the L-switching cell is equal with the sum of the currents through the inductors; in the other case the currents through inductors are equal as can be seen in Fig. 2.1.b [2.29].

In Fig. 2.2.a, it can be seen how the structure of the HBDC-L was obtained by replacing the output inductor of the BDC with the L-switching cell.

In the same manner, in Fig. 2.2.b and c, the switching topologies of the HBDC-L are presented. During t_{on} (=$D·T_s$) switching time the output current (i_{out}) is equal with the current through each inductor of the L-switching cell and the inductors are charged in series; during the t_{off} (=1-$D·T_s$) switching topology the output current is equal with the sum of the current through each inductor belonging to the L-switching cell and the inductors are discharged in parallel.
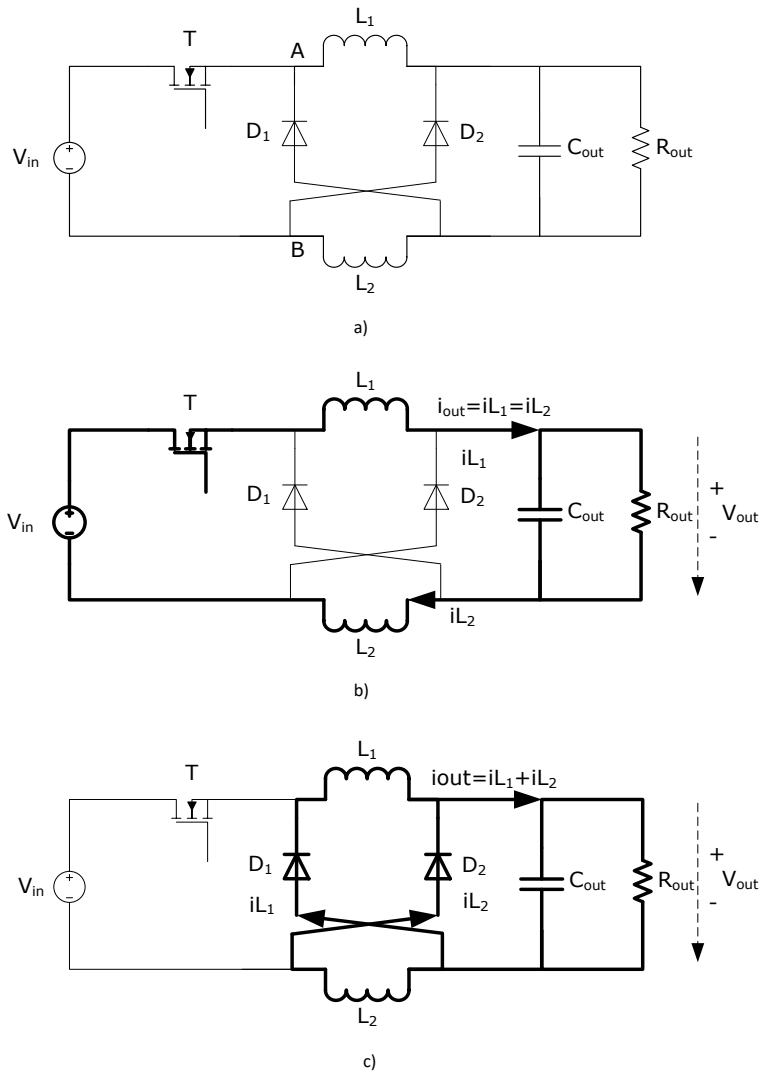
Fig.2.2. HBDC-L:
a) Converter diagram; b) t_{on} switching topology; c) t_{off} switching topology.

In the literature HBDC-L is presented only as circuit configuration and defined analytically with the input to output voltages ratio [2.28].

A complete analysis, design procedure, circuit simulations, and experimental results are the main contribution of this chapter.

2.2. HBDC-L analysis and design

If the input voltage V_{in} and the output voltage V_{out} are considered constant (C_{out} sufficiently large to assume that the output voltage ripple is zero), neglecting all power losses, and $L_1=L_2=L$, the following equations can be written:

$$V_{in} - V_{out} = 2 \cdot L \cdot \frac{di_L}{dt} \qquad (2.1)$$

during t_{on},

$$-L \cdot \frac{di_L}{dt} = V_{out} \qquad (2.2)$$

during t_{off}.

The current through inductors rises and the energy taken from the input source is accumulated in L_1 and L_2. Depending on the values of V_{in} and V_{out}, the converter operates in one of the two modes: continuous current mode (CCM) or discontinuous current mode (DCM).

Only CCM is treated in this chapter.

The waveforms of the HBDC-L current through the inductor and transistor in CCM are presented in Fig. 2.3.

In CCM the inductor current is always positive. When the active switch, T, is closed the inductor current rises from $i_{L,min}$ to $i_{L,max}$. When it is open the currents through both inductors are added to obtain the current which supplies the load. The inductor current decreases from $i_{L,max}$ to $i_{L,min}$.

Equation (2.3) can be written when the transistor is open.

$$-L_1 \cdot \frac{di_{L1}}{dt} = -L_2 \cdot \frac{di_{L2}}{dt} = V_{out} \qquad (2.3)$$

If the inductors are not equal, the slope of current i_{L1} is different from the slope of current i_{L2} and the waveforms of the two currents are also different.

If the inductors have the same value only one equation can be written:

$$-L \cdot \frac{di_L}{dt} = V_{out} \qquad (2.4)$$

The duty cycle, $D=t_{on}/T_s$, can be obtained from equations (2.3) and (2.4). If we consider that the current through inductors rises and decreases linearly, we can replace di_L/dt in equation (2.1) with:

$$\frac{\Delta i_L}{t_{on}} = \frac{I_{L,max} - I_{L,min}}{t_{on}} \qquad (2.5)$$
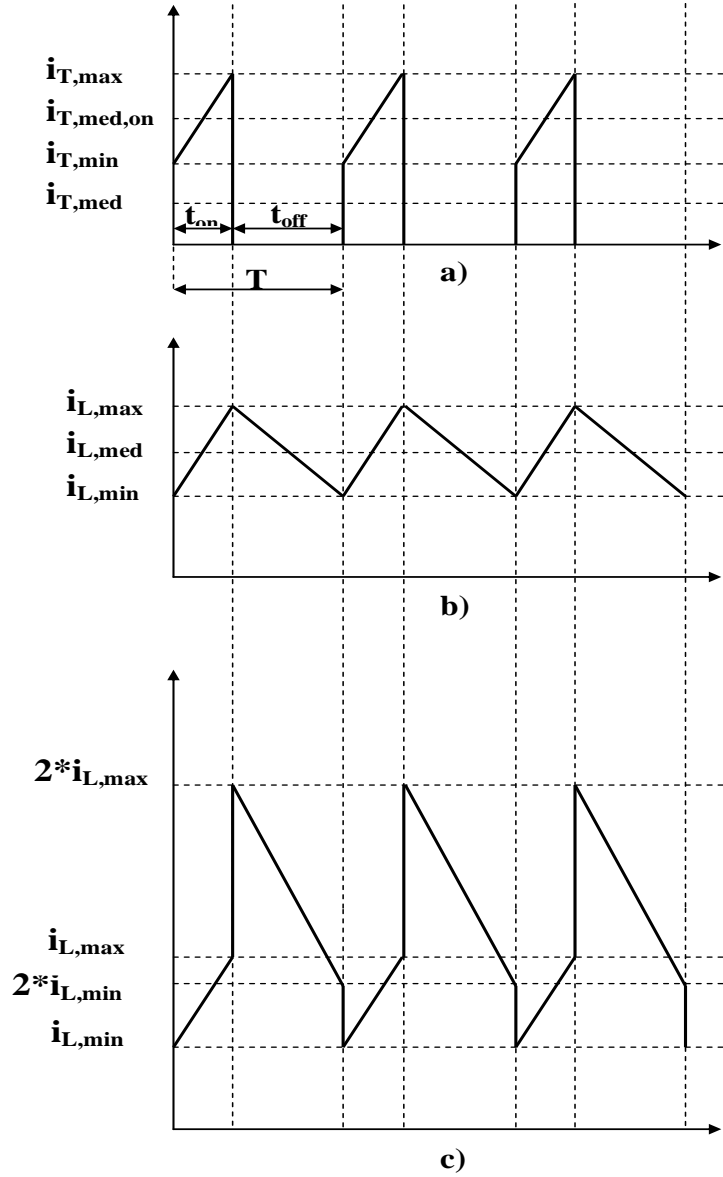
Fig.2.3. HBDC-L waveforms for CCM:
a) transistor current; b) inductor current; c) output current.

In equation (2.2) di_L/dt can be replaced with:

$$-\frac{\Delta i_L}{t_{off}} = -\frac{\Delta i_L}{T_s - t_{on}} \qquad (2.6)$$

The following system is obtained:

$$\begin{cases} V_{in} - V_{out} = 2 \cdot L \cdot \dfrac{\Delta i_L}{t_{on}} \\[3mm] V_{out} = L \cdot \dfrac{\Delta i_L}{T_s - t_{on}} \end{cases} \tag{2.7}$$

The current ripple for the inductor must be the same for T opened and T closed.

$$\frac{V_{in} - V_{out}}{2 \cdot L} \cdot t_{on} = \frac{V_{out} \cdot (T_s - t_{on})}{L} \tag{2.8}$$

or:

$$(V_{in} - V_{out}) \cdot t_{on} = 2 \cdot V_{out} \cdot t_{off} \tag{2.9}$$

For given values of V_{in} and V_{out}, the duty cycle is determined using the following expression:

$$D = \frac{t_{on}}{T_s} = \frac{2 \cdot V_{out}}{V_{in} + V_{out}} \tag{2.10}$$

Using equation (2.10) the expression of the duty cycle as a function of the input and output voltages is obtained:

$$\frac{V_{out}}{V_{in}} = \frac{D}{2 - D} \tag{2.11}$$

The switching period of the transistor is:

$$T_s = \frac{1}{f_s} \tag{2.12}$$

Considering the converter efficiency (η), the maximum input power ($P_{in,max}$) is determined using the following equation:

$$P_{in,max} = \frac{P_{out,max}}{\eta} \tag{2.13}$$

The maximum value of the input currents according to the values of the input voltage are:

$$I_{in,max} = \frac{P_{in,max}}{V_{in,min}} \tag{2.14}$$

$$I_{in,min} = \frac{P_{in,max}}{V_{in,max}} \tag{2.15}$$

The maximum values of the output current according to the values of the output voltage are:

$$I_{out,max} = \frac{P_{out,max}}{V_{out,min}} \tag{2.16}$$

$$I_{out,min} = \frac{P_{out,max}}{V_{out,max}} \tag{2.17}$$

Converter components dimensioning:

➢ Transistor (T):

The average value of the current through T during t_{on} is equal to the average value of the current through the output inductors during t_{on}:

$$I_{T_{on}} = I_{L_{1,on}} = I_{L_{2,on}} = I_{out} \tag{2.18}$$

The average value of the current through transistor during the entire switching period T_s can be calculated from $I_{T,on}$ using equation (2.19):

$$I_T = I_{T_{on}} \cdot D = I_{out} \cdot D \tag{2.19}$$

Considering:

$$V_{in} \cdot I_{in} = \frac{V_{out} \cdot I_{out}}{\eta} \tag{2.20}$$

$$I_{out} = \frac{V_{in}}{V_{out}} \cdot I_{in} \cdot \eta \tag{2.21}$$

and from equation (2.11):

$$I_{out} = \frac{(2-D)}{D} \cdot I_{in} \cdot \eta \tag{2.22}$$

$$I_{T_{on}} = \frac{I_T}{D} = \frac{(2-D)}{D} \cdot I_{in} \tag{2.23}$$

The average value of the current through transistor is given by equation (2.24):

$$I_T = (2-D) \cdot I_{in} \tag{2.24}$$

The maximum transistor current $I_{T,max}$ is equal to $I_{L,max}$.

$$I_{T,max} = I_{L,max} \tag{2.25}$$

The maximum transistor voltage can be obtained applying Kirchhoff Law II when T is open. The voltage at the input of the L-switching cell in Fig. 2.2.a between point A and B is:

$$V_{AB} = -V_{out} \tag{2.26}$$

$$V_T = -V_{in} - V_{AB} = V_{in} + V_{out} \tag{2.27}$$

The maximum transistor voltage $V_{T,max}$ is obtained for $V_{in,max}$ and $V_{out,max}$.

➢   The output inductors (L_1, L_2):

The value of the average output current is equal to the average value of the current through the output inductors, L_1 and L_2:

$$I_{out} = I_{T_{on}} = I_{L_{1,on}} = I_{L_{2,on}} = I_{L_{on}} \tag{2.28}$$

$$I_{out} = \frac{P_{out,max}}{V_{out}} \tag{2.29}$$

In the t_{on} switching topology the voltage drop across the output inductor has the following expression:

$$V_L = \frac{V_{in} - V_{out}}{2} \tag{2.30}$$

We impose an inductor current ripple equal to X_1 % (X_1-constant, chosen value) of the maximum output current:

$$\Delta I_L = X_1\% \cdot I_{out,max} = X_1\% \cdot \frac{P_{out,max}}{V_{out,max}} \tag{2.31}$$

The maximum and minimum values of the current through the output inductors are calculated using:

$$I_{L_{max}} = I_L + \frac{\Delta I_L}{2} \tag{2.32}$$

$$I_{L_{min}} = I_L - \frac{\Delta I_L}{2} \tag{2.33}$$

Knowing that:

$$V_L = L \cdot \frac{\Delta I_L}{\Delta t} \tag{2.34}$$

the value of the input inductance is:

$$L = \frac{V_L}{\Delta I_L} \cdot \Delta t \tag{2.35}$$

$$L = \frac{V_{in} \cdot (1 - D)}{\Delta I_L \cdot (2 - D)} \cdot \Delta t \tag{2.36}$$

where: $\Delta t = t_{on}$.

➢   The output diodes (D_1, D_2):

Each of the two diodes D_1 and D_2 must be able to conduct a maximum forward current equal to the maximum inductor current.

To obtain the average forward current of one diode, I_D, we have to note that the currents through D_1 and D_2 are equal to the currents through L_1 and L_2 when the switching device T is closed and they are zero when T is open. Because the average diode current for t_{off} time interval, $I_{D,off}$, is equal to I_L, I_D can be written as:

$$I_D = \frac{i_{D,off} \cdot t_{off}}{T_S} = \frac{I_L \cdot (T_S - D \cdot T_S)}{T_S} = I_L \cdot (1 - D) \tag{2.37}$$

The reverse voltage across one diode when T is closed is given by equation (2.38).

$$V_{D_1} = L \cdot \frac{di_L}{dt} + V_{out} = \frac{V_{in} - V_{out}}{2} + V_{out} = \frac{V_{in} + V_{out}}{2} \tag{2.38}$$

From equation (2.38) it is clear that the maximum reverse voltage across one diode is obtained if both the input and output voltage have the maximum value.

➢   The output capacitor (C_{out}):

We impose a voltage ripple through capacitor of X_2 % (X_2-constant, chosen value) from the maximum output voltage:

$$\Delta V_{C_{out}} = X_2\% \cdot V_{out,max} \tag{2.39}$$

Knowing that:

$$\Delta V_{out} = \frac{\Delta Q}{C} \tag{2.40}$$

$$\Delta Q = \frac{\frac{\Delta I_L \cdot T_S}{2}}{2} \tag{2.41}$$

$$\Delta V_{out} = \frac{\Delta Q}{C} = \frac{1}{C} \cdot \frac{1}{2} \cdot \frac{T_s}{2} \cdot \frac{\Delta I_L}{2} \tag{2.42}$$

results:

$$C_{out} = \frac{T_s}{8} \cdot \frac{\Delta I_L}{\Delta V_{C_{out}}} \tag{2.43}$$

The current through the output capacitor is equal with the alternative component of the current through the output inductor switching cell.

$$i_{C_{out}} = i_L - I_L = i_L - I_{out} \tag{2.44}$$

2.3. HBDC-L digital simulation and experimental results

In this section, digital simulations and experimental results of HBDC-L converter will be presented. Realistic models were used to compare the simulation waveforms with experimental results obtained from HBDC-L laboratory prototype.

The values used for the HBDC-L components (in simulations and experimental setup) are:

$L_1 = 28$ [μH]
$L_2 = 28$ [μH]
$C_{out} = 3960$ [μF]
$f_s = 100$ [kHz].

The simulations were made using PSim, in open-loop.

The simulated and experimental results were obtained for: $V_{in} = 40$ [V], $D = 0.586$, and $R_{out} = 10.5$ [Ω].

The converter was operating at boundary between CCM and DCM.

Fig. 2.4 presents the PSim simulation model of the HBDC-L.
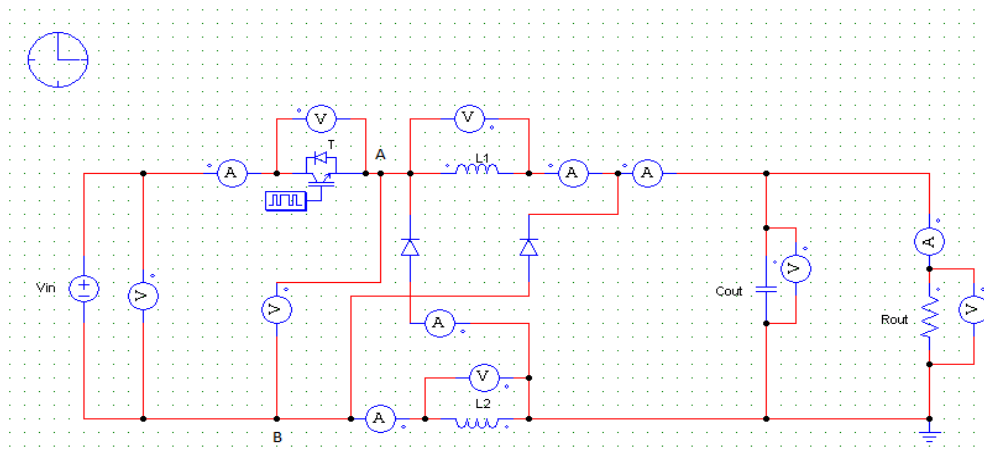
Fig.2.4. HBDC-L PSim model for open-loop simulation.

Fig. 2.5 presents the HBDC-L laboratory prototype. It was realized using interconnectable blocks designed for easy implementation. The MOSFET block with his driver, the L–switching block and the input and output filters blocks were connected in order to obtain the converter configuration.

Table 2.1 presents the calculated values of peak and average transistor and I_{sum} currents (where I_{sum} is the current at the output of the switched inductor cell) - Figs. 2.6, 2.7, 2.10, 2.11, in comparison with the same data obtained through numerical integration in PSim and from the HBDC-L laboratory prototype.

Figs. 2.9 and 2.10 present the voltage at the input of the switching-inductor cell (V_{AB} in Fig. 2.4) which is equal to the converter's input voltage when the transistor is saturated and the inverted output voltage when the transistor is closed, respectively.

TABLE 2.1. HBDC-L converter transistor and L-switched cell currents.

Current	Calculated	PSim	Experimental
$\hat{I}_T$	2.23 [A]	2.23 [A]	2.56 [A]
I_T	0.67 [A]	0.68[A]	0.85 [A]
$\hat{I}_{sum}$	4.58 [A]	4.41[A]	4.36 [A]
I_{sum}	1.62 [A]	1.57 [A]	1.63 [A]
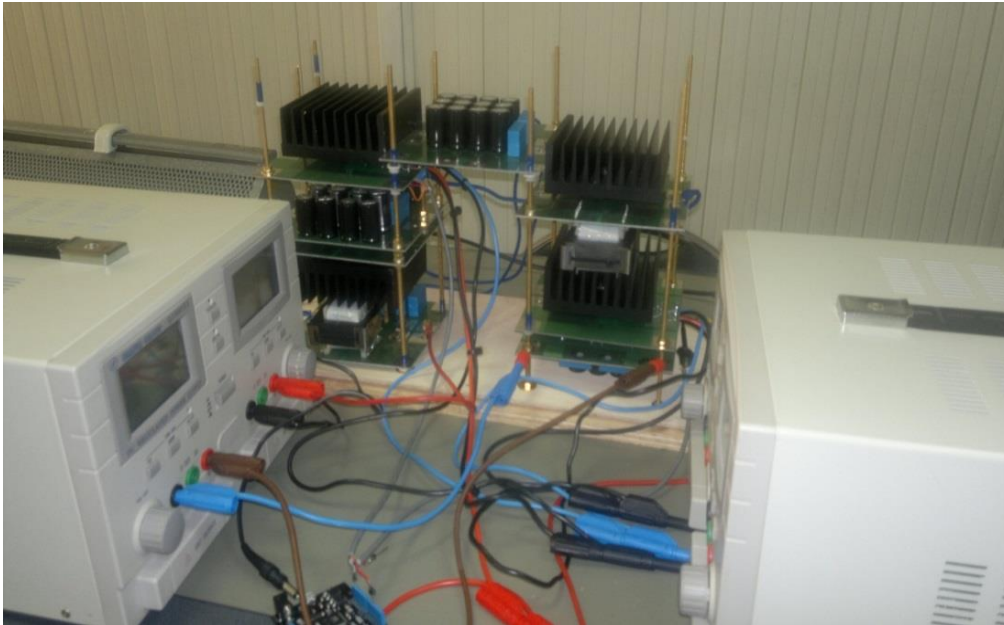
Fig.2.5. HBDC-L laboratory prototype implemented using specific blocks.
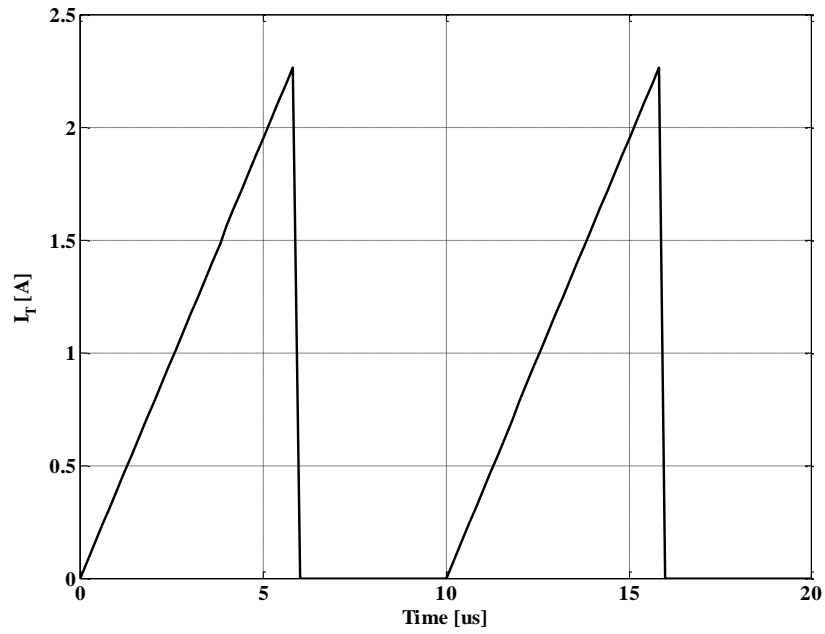
Fig.2.6. HBDC-L simulated waveform of the transistor curent.
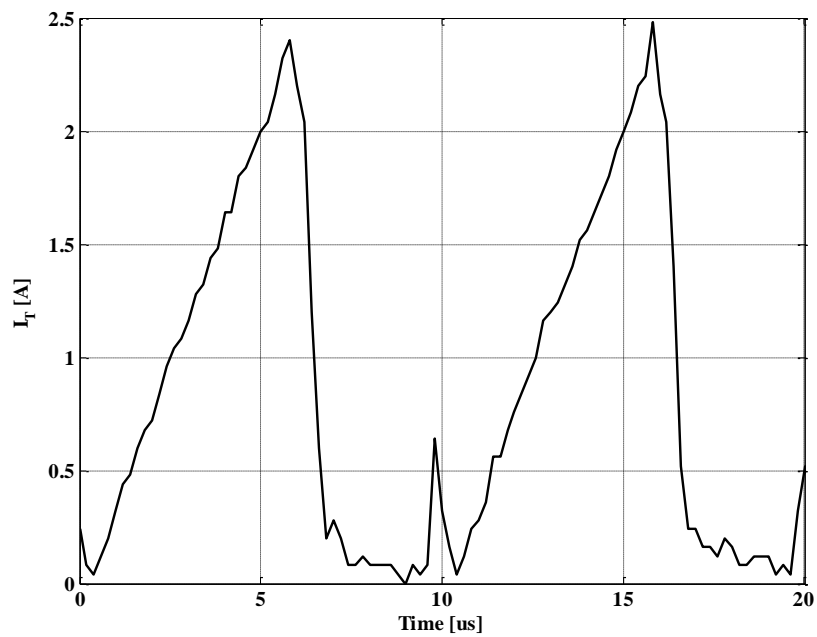
Fig.2.7. HBDC-L experimental waveform of the transistor curent.
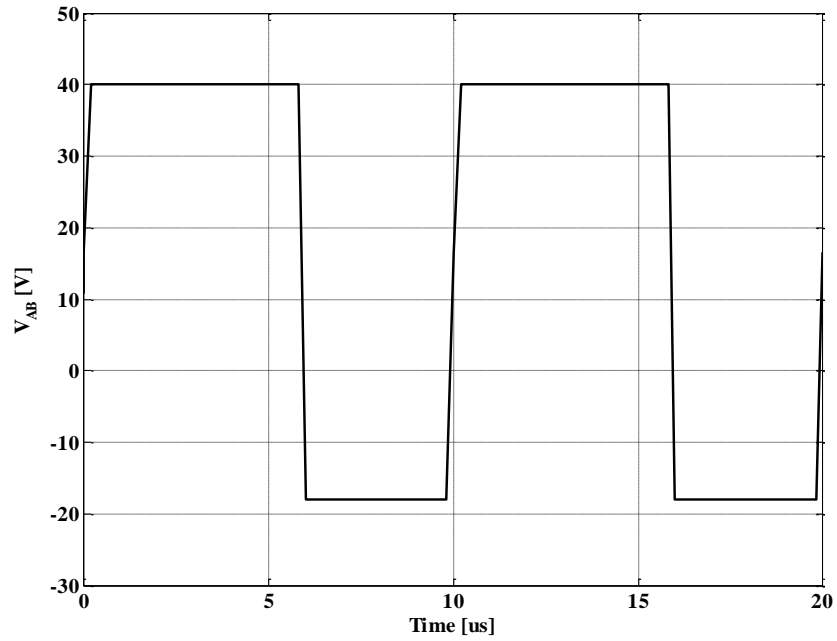
Fig.2.8. HBDC-L simulated waveform of the input voltage of the switched-inductor cell.
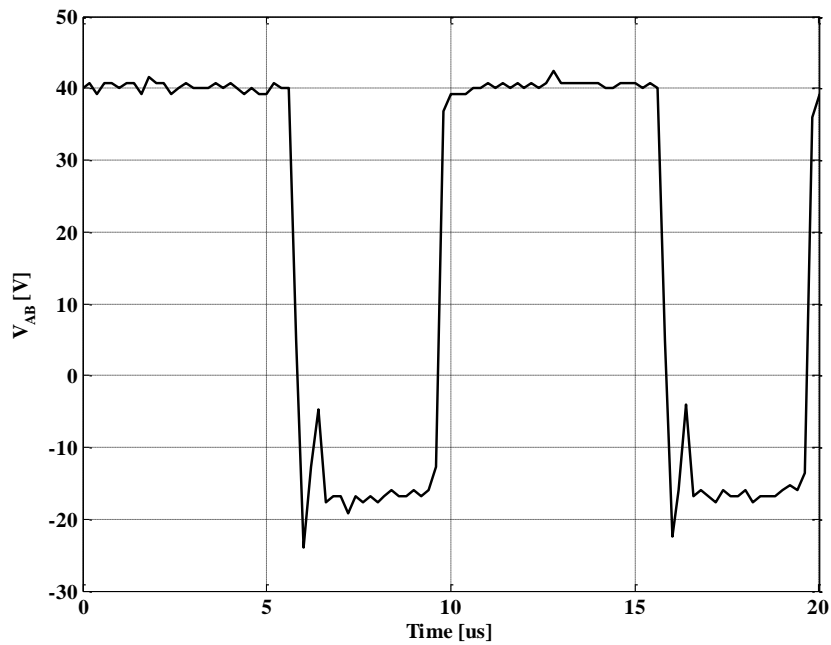
Fig.2.9. HBDC-L experimental waveform of the input voltage of the switched-inductor cell.
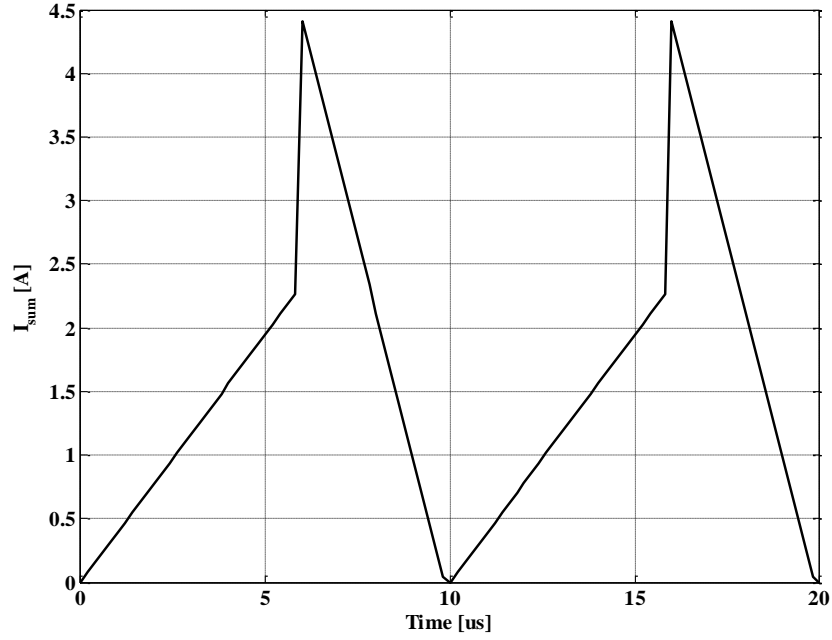
Fig.2.10. HBDC-L simulated waveform of the switched inductor cell output current (I_{sum}).
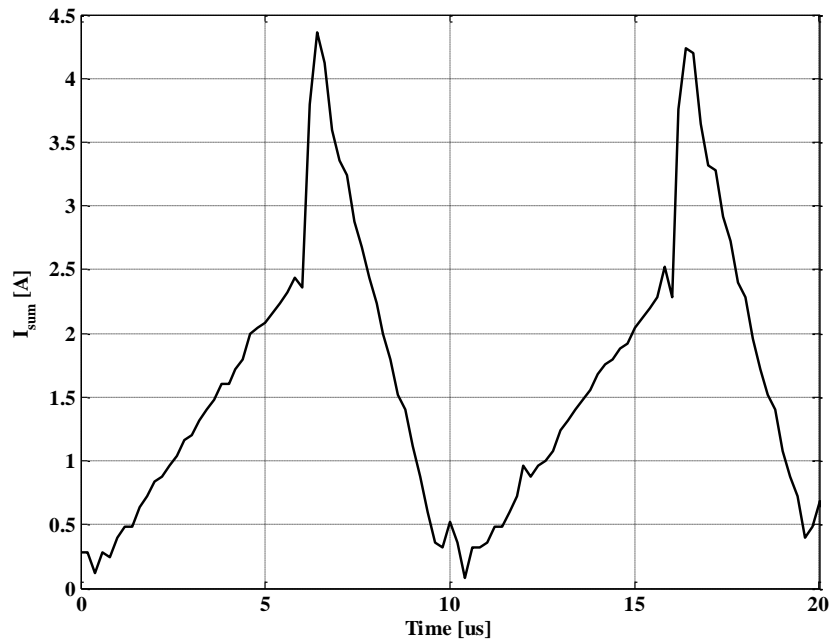
Fig.2.11. HBDC-L experimental waveform of the switched inductor cell output current (I_{sum}).

2.4. Conclusion

In this chapter HBDC-L was analyzed and studied in detail.

For a higher step-down voltage conversion ratio, the inductor and the output diode of the BDC are replaced with a switched inductor cell formed by two inductors and two diodes. The output voltage of the HBDC-L is reduced (2-D) times than the output voltage of the BDC.

A full analysis and design of HBDC-L was made.

Equations for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor current are presented.

The main current and voltage, simulation and experimental waveforms were presented and compared.

A HBDC-L laboratory model was built using modules for commutation elements, L-switching cell and filters. For the comparison between the experimental and the simulation waveforms, obtained with PSim simulation program, a simulation model with realistic electronic components was used.

All the simulation waveforms of HBDC-L are in good agreement with the experiments, confirming the theoretical study.

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3. HYBRID BUCK SWITCHED-CAPACITOR DC-DC CONVERTER (HBDC-C)

3.1. Introduction

A large variety of step-up and step-down, switched-capacitor based DC-DC converters, are presented in the literature considering the wide spread applications of power electronics in renewable energy and automotive systems [3.1-3.22].

HBDC-C is a step-down converter obtained from the classical BDC by inserting a simple circuit (C-switching cell) in his structure [3.18, 3.19].

This switching block (presented in Fig. 3.1.a) is formed by two identical capacitors (C_1 and C_2) and three diodes (D_1, D_2 and D_{12}). The switching topologies of the C-switching cell are presented in Fig. 3.1.b) and c):

During t_{on} switching time the capacitors (C_1 and C_2) are discharged in parallel; in the t_{off} switching time the capacitors are charged in series ($V_{C1}=V_{C2}=V_C$) from the input voltage. By inserting the C-switching cell shown in Fig. 3.1.a) in the structure of a BDC and adding an input inductor, L_{in}, in order to diminish the input current ripple, the HBDC-C shown in Fig. 3.2.a) is obtained. His switching topologies, t_{on} ($=D \cdot T_s$) and t_{off} ($=(1-D) \cdot T_s$) are shown in Fig. 3.2.b) and c).
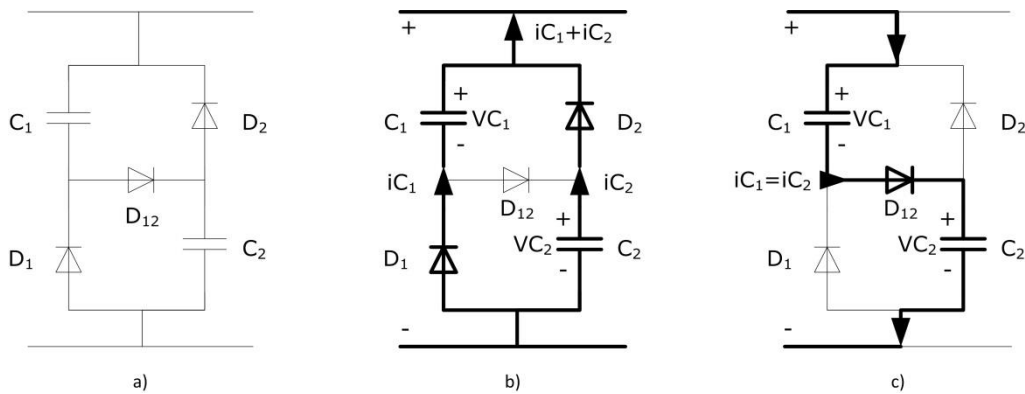
Fig.3.1. C-switching cell:
a) Circuit topology; b) t_{on} switching topology; c) t_{off} switching topology.

The input inductor (L_{in}) of the HBDC-C is added to reduce the ripple of the input current.

In the same manner in Fig. 3.2.b) and c) the switching topologies of the HBDC-C are presented.

It can be seen that during t_{on} switching time the capacitors C_1 and C_2 are discharged in parallel and with the input current i_{in} (which is the same with the current through the input inductor L_{in}) results the current through the active switch

T; during the t_{off} switching topology the capacitors C_1 and C_2 are charged in parallel from the input voltage.
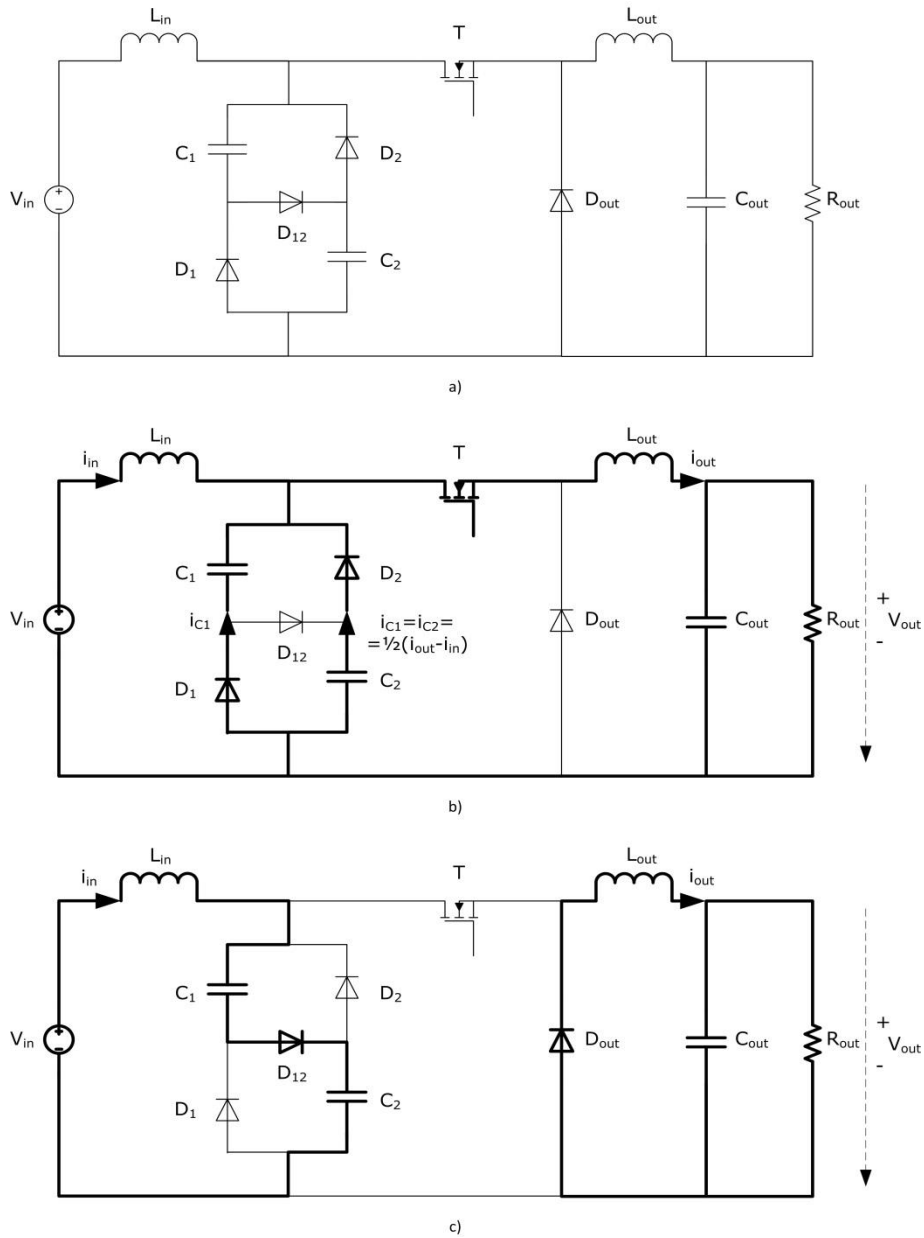
Fig.3.2. HBDC-C:
a) Converter diagram; b) t_{on} switching topology; c) t_{off} switching topology.

3.2. HBDC-C analysis and design

If the input voltage V_{in} and the output voltage V_{out} are considered constant (C_{out} sufficiently large to assume that the output voltage ripple is zero) during one switching period, the voltage-second balances on L_{in} and L_{out} can be written as:

$$\left[(1-D)\cdot(V_{in}-2\cdot V_C)+D\cdot(V_{in}-V_C)\right]=0 \tag{3.1}$$

$$\left[(1-D)\cdot(-V_{out})+D\cdot(V_C-V_{out})\right]=0 \tag{3.2}$$

The relation between V_{out} and V_{in} given in (3.3) is obtained from (3.1) and (3.2).

$$V_{out}=\frac{D}{2-D}\cdot V_{in} \tag{3.3}$$

Where:
- V_{in} – is the input voltage;
- V_{out} – is the output voltage;
- V_C – is the voltage drop across the capacitors C_1 and C_2;
- D – is the duty cycle.

From the input to output voltage conversion ratio equation (3.3) can be seen that the output voltage is reduced by (2-D) times more than in the case of the BDC.

Depending on the values of V_{in} and V_{out}, the converter operates in one of the two modes: continuous current mode (CCM) or discontinuous current mode (DCM). Only CCM is treated in this chapter.

For the input inductor L_{in} we can write the following equation:

$$\frac{1}{T_s}\left[(T_s-t_{on})\cdot(V_{in}-2\cdot V_C)+t_{on}\cdot(V_{in}-V_C)\right]=0 \tag{3.4}$$

$$\left[(1-D)\cdot(V_{in}-2\cdot V_C)+D\cdot(V_{in}-V_C)\right]=0 \tag{3.5}$$

From equation (3.5) results that the voltage drop across the input capacitor is equal with the ratio of the input voltage and (2-D):

$$V_C=\frac{V_{in}}{2-D} \tag{3.6}$$

For the output inductor L_{out} we can write the following equation:

$$\frac{1}{T_s}\left[(T_s-t_{on})\cdot(-V_{out})+t_{on}\cdot(V_C-V_{out})\right]=0 \tag{3.7}$$

$$\left[(1-D)\cdot(-V_{out})+D\cdot(V_C-V_{out})\right]=0 \tag{3.8}$$

From equation (3.9) results that the voltage drop across the input capacitor is equal with the ratio of the output voltage and duty factor (D):

$$D \cdot V_C = V_{out} \tag{3.9}$$

From equations (3.6) and (3.9) we obtain the expression of the output to input voltage ratio as a function of duty cycle:

$$D \cdot \frac{V_{in}}{2-D} = V_{out} \tag{3.10}$$

$$V_{out} = \frac{D}{2-D} \cdot V_{in} \tag{3.11}$$

From equation (3.11) and for given values of V_{in} and V_{out} we obtain the expression of the duty cycle:

$$D \cdot V_{in} = (2-D) \cdot V_{out} \tag{3.12}$$

$$D \cdot (V_{in} + V_{out}) = 2 \cdot V_{out} \tag{3.13}$$

$$D = \frac{2 \cdot V_{out}}{V_{out} + V_{in}} \tag{3.14}$$

The switching period of the transistor:

$$T_S = \frac{1}{f_S} \tag{3.15}$$

Considering the converter efficiency the maximum input power is determined using the following equation:

$$P_{in,max} = \frac{P_{out,max}}{\eta} \tag{3.16}$$

The maximum and minimum values of the input current according to the values of the input voltage are:

$$I_{in,max} = \frac{P_{in,max}}{V_{in,min}} \tag{3.17}$$

$$I_{in,min} = \frac{P_{in,max}}{V_{in,max}} \tag{3.18}$$

The maximum and minimum values of the output current according to the values of the output voltage are:

$$I_{out,max} = \frac{P_{out,max}}{V_{out,min}}$$ (3.19)

$$I_{out,min} = \frac{P_{out,max}}{V_{out,max}}$$ (3.20)

Converter components dimensioning:

➢ The input inductor (L_{in}):

In this case the value of the input current is equal to the average value of the current through the input inductor, L_{in}:

$$I_{in} = I_{L_{in}}$$ (3.21)

The input current is calculated using the following equation, considering the maximum input power and the input voltage:

$$I_{in} = \frac{P_{in,max}}{V_{in}}$$ (3.22)

In the t_{off} switching topology the voltage drop across the input inductor has the following expression:

$$V_{L_{in}} = V_{in} - V_C = V_{in} - \frac{V_{in}}{(2-D)} = V_{in} \cdot \frac{(1-D)}{(2-D)}$$ (3.23)

We impose an inductor current ripple equal to X_1 % (X_1-constant, choosen value) of the maximum input current:

$$\Delta I_{L_{in}} = X_1\% \cdot I_{in,max} = X_1\% \cdot \frac{P_{in,max}}{V_{in,max}}$$ (3.24)

The maximum and minimum values of the current through the input inductor are calculated using:

$$I_{L_{in},max} = I_{L_{in}} + \frac{\Delta I_{L_{in}}}{2}$$ (3.25)

$$I_{L_{in},min} = I_{L_{in}} - \frac{\Delta I_{L_{in}}}{2}$$ (3.26)

Knowing that:

$$V_{L_{in}} = L \cdot \frac{\Delta I_{L_{in}}}{\Delta t} \tag{3.27}$$

results the value of the input inductance:

$$L_{in} = \frac{V_{L_{in}}}{\Delta I_{L_{in}}} \cdot \Delta t \tag{3.28}$$

$$L_{in} = \frac{V_{in} \cdot (1-D)}{\Delta I_{L_{in}} \cdot (2-D)} \cdot \Delta t \tag{3.29}$$

where: $\Delta t = t_{on}$.

> The output inductor (L_{out}):

The value of the output current is equal to the average value of the current through the output inductor, L_{out}:

$$I_{out} = I_{L_{out}} \tag{3.30}$$

The output current is calculated using the following equation, considering the maximum output power and the output voltage:

$$I_{out} = \frac{P_{out,max}}{V_{out}} \tag{3.31}$$

In the switching topology t_{on} the voltage drop across the output inductor has the following expression:

$$V_{L_{out}} = V_C - V_{out} = \frac{V_{in}}{(2-D)} - V_{out} = V_{in} \cdot \frac{(1-D)}{(2-D)} \tag{3.32}$$

We impose for this inductor a current ripple of X_2 % (X_2-constant, chosen value) of the maximum output current:

$$\Delta I_{L_{out}} = X_2\% \cdot I_{out,max} = X_2\% \cdot \frac{P_{out,max}}{V_{out,max}} \tag{3.33}$$

The maximum and minimum values of the current through the output inductor are calculated using:

$$I_{L_{out,max}} = I_{L_{out}} + \frac{\Delta I_{L_{out}}}{2} \tag{3.34}$$

$$I_{L_{out,min}} = I_{L_{out}} - \frac{\Delta I_{L_{out}}}{2} \tag{3.35}$$

Knowing that:

$$V_{L_{out}} = L \cdot \frac{\Delta I_{L_{out}}}{\Delta t} \tag{3.36}$$

results the value of the input inductance:

$$L_{out} = \frac{V_{L_{out}}}{\Delta I_{L_{out}}} \cdot \Delta t \tag{3.37}$$

$$L_{out} = \frac{V_{in} \cdot (1 - D)}{\Delta I_{L_{out}} \cdot (2 - D)} \cdot \Delta t \tag{3.38}$$

where: $\Delta t = t_{on}$.

> The transistor (T):

The average value of the current through T during t_{on} is equal to the average value of the current through the output inductor during t_{on}:

$$I_{T_{on}} = I_{L_{out,on}} = I_{out} \tag{3.39}$$

The average value of the current through transistor during the entire switching period T_s can be calculated from $I_{T,on}$ using equation (3.40):

$$I_T = i_{T_{on}} \cdot D = I_{out} \cdot D \tag{3.40}$$

Considering:

$$V_{in} \cdot I_{in} = \frac{V_{out} \cdot I_{out}}{\eta} \tag{3.41}$$

$$I_{out} = \frac{V_{in}}{V_{out}} \cdot I_{in} \cdot \eta \tag{3.42}$$

and from equation (3.10):

$$\frac{V_{in}}{V_{out}} = \frac{(2 - D)}{D} \tag{3.43}$$

$$I_{out} = \frac{(2 - D)}{D} \cdot I_{in} \cdot \eta \tag{3.44}$$

$$I_{T_{on}} = \frac{I_T}{D} = \frac{(2-D)}{D} \cdot I_{in} \qquad (3.45)$$

The average value of the current through transistor is given by equation (3.46):

$$I_T = (2-D) \cdot I_{in} \qquad (3.46)$$

The voltage drop over the transistor is:

$$V_T = 2 \cdot V_C = 2 \cdot \frac{V_{in}}{2-D} \qquad (3.45)$$

➢ Capacitors (C_1, C_2, C_{out}):

➢ $C_1 = C_2 = C$

In the switching topology t_{off} ($V_{C1} = V_{C2} = V_C$) C_1, C_2 are charged in series from the input voltage, and in switching topology t_{on} they are discharged in parallel.

The voltage drop over the capacitors (V_C) is presented in equation (3.6).

We impose a voltage ripple through capacitor of X_3 % (X_3-constant, chosen value) from the maximum input voltage:

$$\Delta V_C = X_3\% \cdot V_{in, max} \qquad (3.46)$$

Knowing that:

$$i_C = C \cdot \frac{\Delta V_C}{\Delta t} \qquad (3.47)$$

and in switching topology t_{on},

$$i_C = \frac{1}{2}(I_{out} - I_{in}) \qquad (3.48)$$

results the capacitor's capacity:

$$C = i_C \cdot \frac{\Delta t}{\Delta V_C} \qquad (3.49)$$

➢ C_{out}

We impose a voltage ripple through capacitor of X_4 % (X_4-constant, chosen value) from the maximum output voltage:

$$\Delta V_{C_{out}} = X_4\% \cdot V_{out, max} \qquad (3.50)$$

Knowing that:

$$\Delta V_{out} = \frac{\Delta Q}{C} \qquad (3.51)$$

$$\Delta Q = \frac{\frac{\Delta I_{L_{out}} \cdot T_s}{2}}{2} \tag{3.52}$$

$$\Delta V_{out} = \frac{\Delta Q}{C} = \frac{1}{C} \cdot \frac{1}{2} \cdot \frac{T_s}{2} \cdot \frac{\Delta I_{L_{out}}}{2} \tag{3.53}$$

results:

$$C_{out} = \frac{T_s}{8} \cdot \frac{\Delta I_{L_{out}}}{\Delta V_{C_{out}}} \tag{3.54}$$

The current through the output capacitor is equal with the alternative component of the current through the output inductor L_{out}.

$$i_{C_{out}} = i_{L_{out}} - I_{L_{out}} = i_{L_{out}} - I_{out} \tag{3.55}$$

➢ Diodes (D_1, D_2, D_{12}, D_{out}):

➢ D_1, D_2

During t_{on} switching topology the current through diodes D_1 and D_2 is equal with the current through capacitors C_1, C_2. The current through diodes D_{12} and D_{out} during t_{on} switching topology is equal with zero.

The current through diodes i_D (D_1, D_2) is expressed with the following equation:

$$i_D = \frac{1}{2} \cdot \left(i_{L_{out},min} + \left(\frac{\Delta I_{L_{out}}}{t_{on}} \right) - i_{L_{in},min} + \left(\frac{\Delta I_{L_{in}}}{t_{on}} \right) \right) \tag{3.56}$$

➢ D_{12}

During t_{off} switching topology the current through diodes D_1 and D_2 is equal with zero. The current through diode D_{12} during t_{off} switching topology is equal with the current through C_1 and L_{in}. The current through diode D_{12} is expressed with the following equation:

$$i_{D_{12}} = \left(i_{L_{in},max} - \left(\frac{\Delta I_{L_{in}}}{t_{off}} \right) \right) \tag{3.57}$$

➢ D_{out}

The current through the output diode D_{out} during t_{off} switching topology is equal with the current through L_{out}. The current through diode D_{out} is expressed with the following equation:

$$i_{D_{out}} = \left(i_{L_{out},max} - \left(\frac{\Delta I_{L_{out}}}{t_{off}} \right) \right) \tag{3.58}$$

3.3. HBDC-C digital simulation and experimental results

In this section, digital simulations and experimental results of HBDC-C will be presented. Realistic models were used to compare the simulation waveforms with the acquired waveforms obtained from HBDC-C prototype, built for this purpose.

The values used for the HBDC-C components (in simulations and experimental setup) are:

L_{in}=28 [μH]
L_{out}=28 [μH]
C_1=C_2=2640 [μF]
C_{out} =3960 [μF].
f_s=100 [kHz].

The simulations were made using PSim simulation program, in open-loop. The experimental measurements were taken using a HBDC-C laboratory model (Fig. 2.6) using this time a C-switching cell module.

The simulated and experimental results were obtained for: V_{in}=42 [V], R_{out}=2.37 [Ω], D=0.5. The converter was operating near BCM (regarding the input current) as can be seen from Figs. 3.4 and 3.5.

Fig. 3.3 presents the PSim simulation model of the HBDC-C.
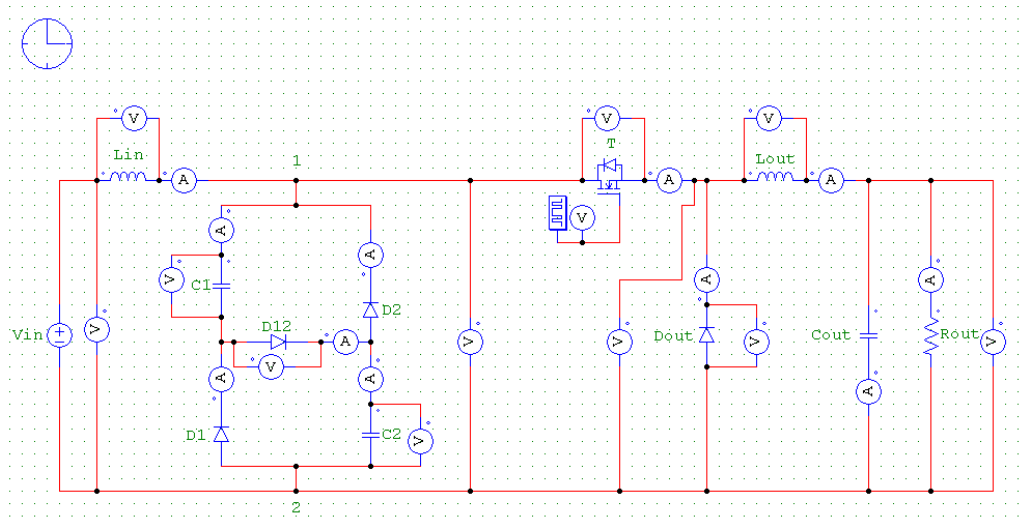
Fig.3.3. HBDC-C PSim model for open-loop simulation.

The simulated waveforms presented in Fig. 3.4-3.11 in comparison with the measured waveforms, were obtained using more realistic simulation models for the HBDC-C components.

Figures 3.4-3.5 show the current through the input inductor (L_{in}), Figs. 3.6-3.7 presents the voltage across the C-switching block, Figs. 3.8-3.19 show the current through the output inductor (L_{out}), Figs. 3.10-3.11 presents the HBDC-C's transistor drain voltage.
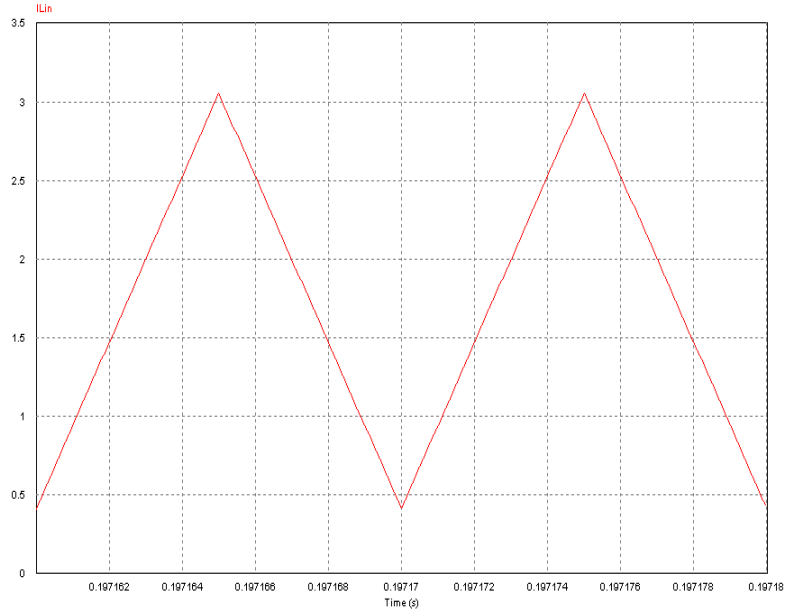
Fig.3.4. HBDC-C: simulated waveform of the current through the input inductor L_{in}.
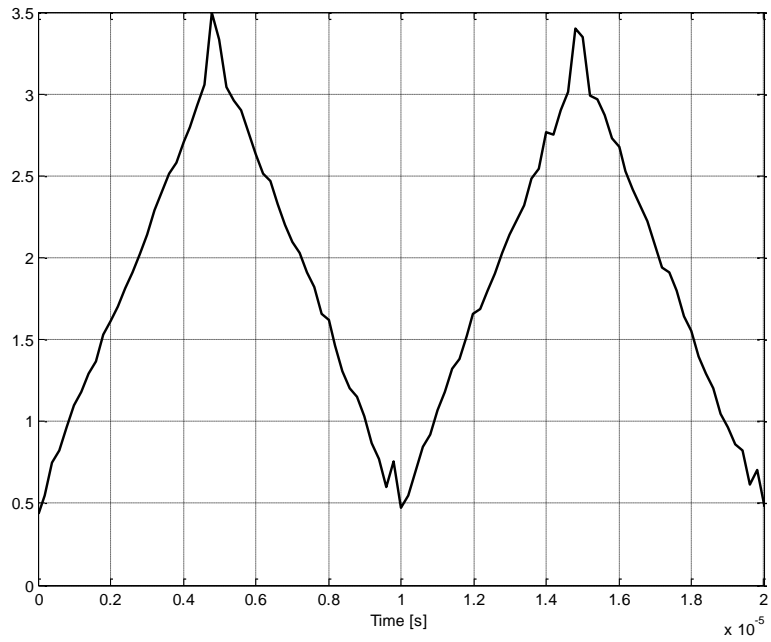
Fig.3.5. HBDC-C: experimental waveform of the current through the input inductor L_{in}.
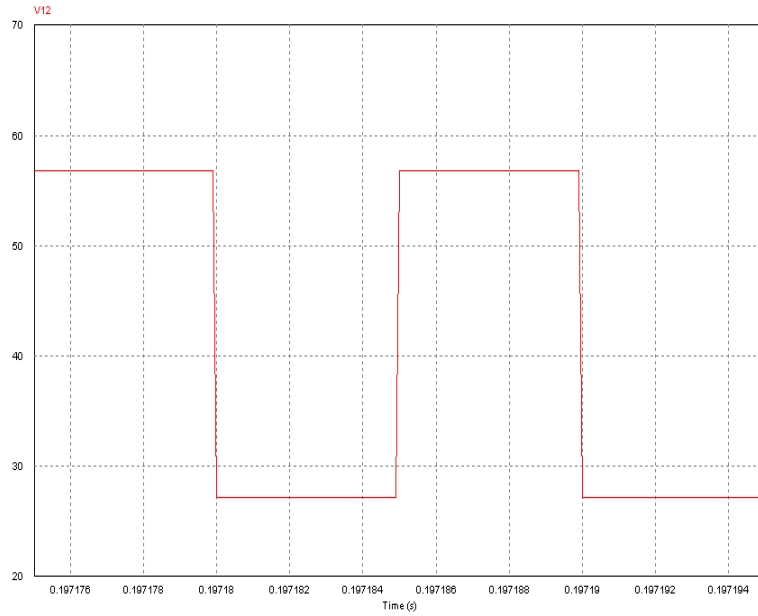
Fig.3.6. HBDC-C: simulated waveform of the voltage across the C-switching cell.
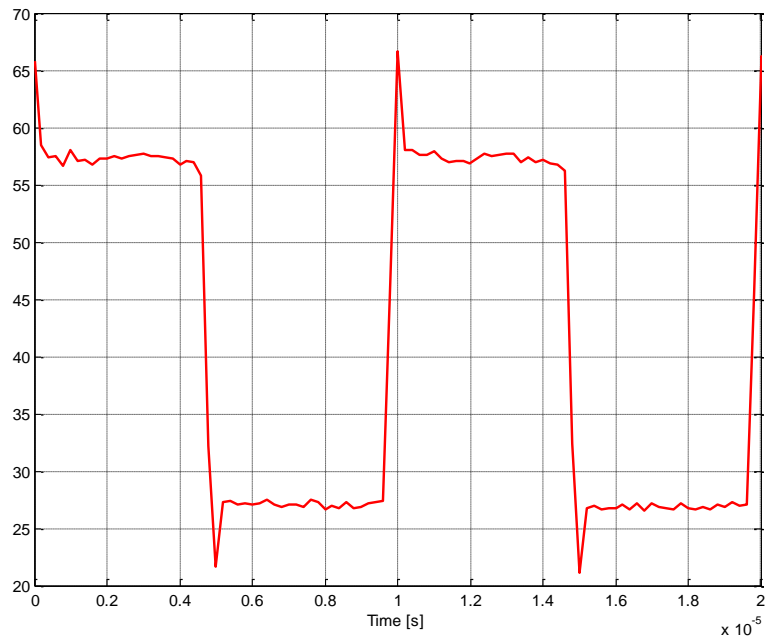
Fig.3.7. HBDC-C: experimental waveform of the voltage across the C-switching cell.
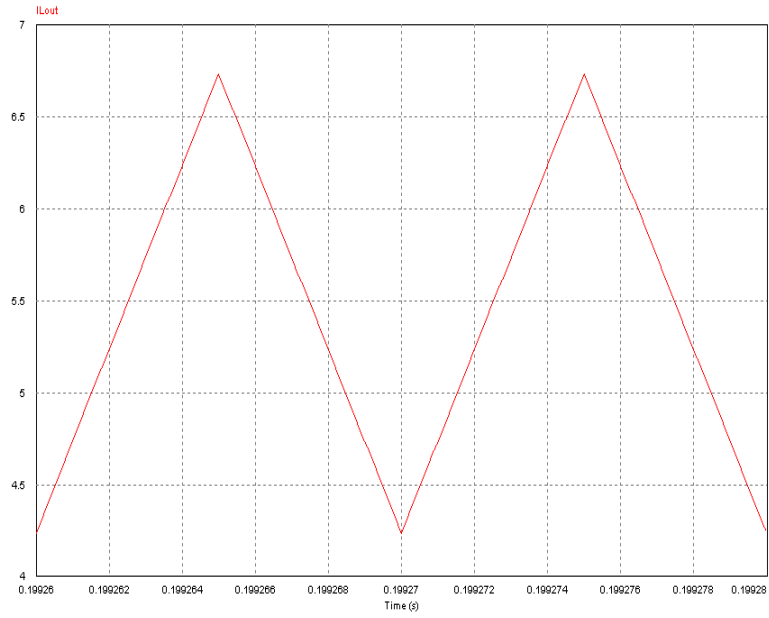
Fig.3.8. HBDC-C: simulated waveform of the current through the output inductor L_{out}.
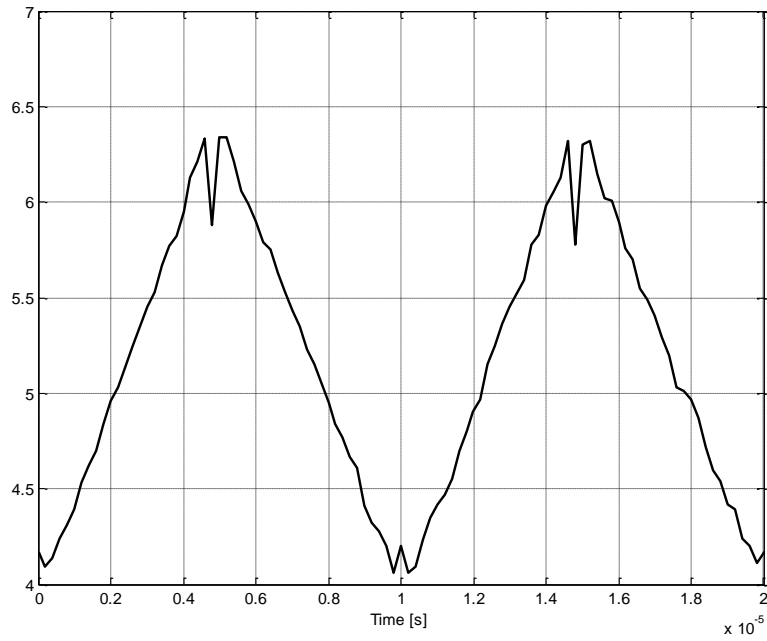
Fig.3.9. HBDC-C: experimental waveform of the current through the output inductor L_{out}.
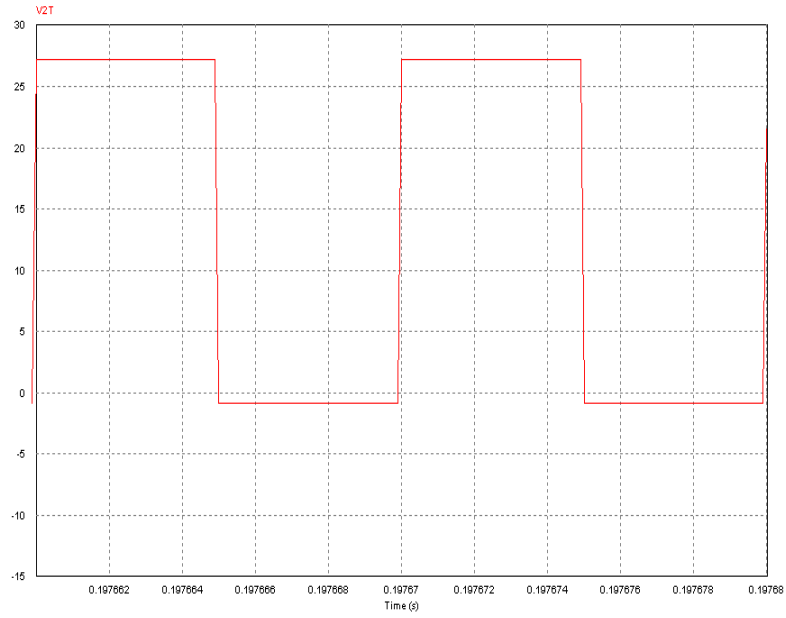
Fig.3.10. HBDC-C: simulated waveform of the transistor's drain voltage.
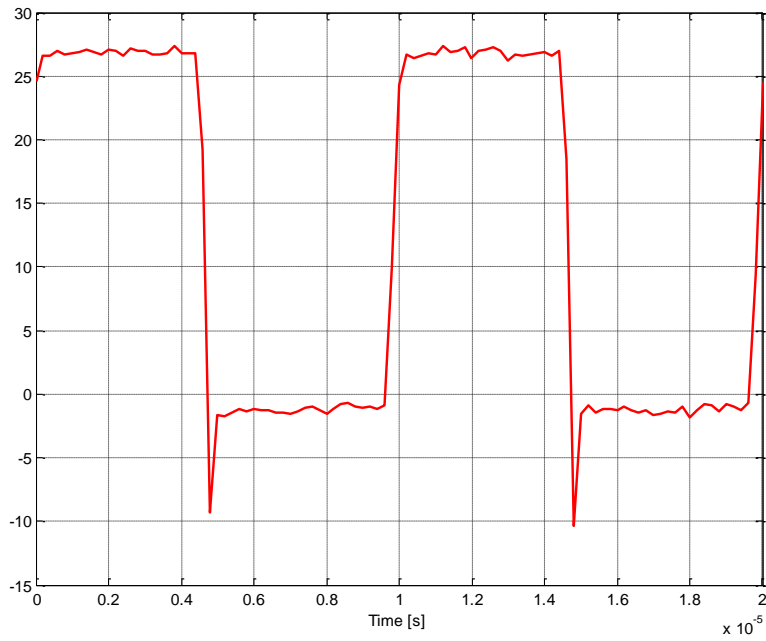
Fig.3.11. HBDC-C: experimental waveform of the transistor's drain voltage.

3.4. Conclusion

Starting from the BDC configuration and adding a C-switching cell needed for a higher step-down voltage conversion ratio, HBDC-C was obtained, analyzed and studied in detail. The output voltage of the HBDC-C is reduced (2-D) times than the output voltage of the BDC. Continuous current mode (CCM) and boundary current mode (BCM), of the HBDC-C were studied.

A full analysis and design procedure of the HBDC-C was made.

Equations for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor currents are presented and discussed.

Main current and voltage, simulation and experimental waveforms were presented and compared.

A laboratory model of the HBDC-C was built, using a configurable modular structure. For the comparison between the experimental and the simulation waveforms, obtained with PSim, a model with realistic electronic components was used.

All the simulation waveforms of HBDC-C are in good agreement with the experimental waveforms confirming the theoretical study.

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4. HYBRID BUCK SWITCHED-CAPACITOR/SWITCHED-INDUCTOR DC-DC CONVERTER (HBDC-C/L)

4.1. Introduction

In this chapter a new hybrid DC-DC converter structure is proposed and presented, as a contribution in the field of higher step-up/step-down conversion ratio DC-DC converters presented in literature [4.1-4.10].

Switching converters for DC-DC conversion can transfer energy with different DC voltage levels with little loss [4.11-4.14].

The HBDC-C/L is a step-down converter obtained from the classical structure of the BDC by inserting a simple circuit (C-switching cell) at the input and an L-switching cell at the output, or by mixing together the HBDC-C and the HBDC-L converters [4.7-4.10].

These simple circuits (Fig. 4.1) or switching blocks (C and L) were presented in detail in chapters 2 and 3 (in Fig. 2.1 and Fig. 3.1), and the converter diagram is illustrated in Fig. 4.2.
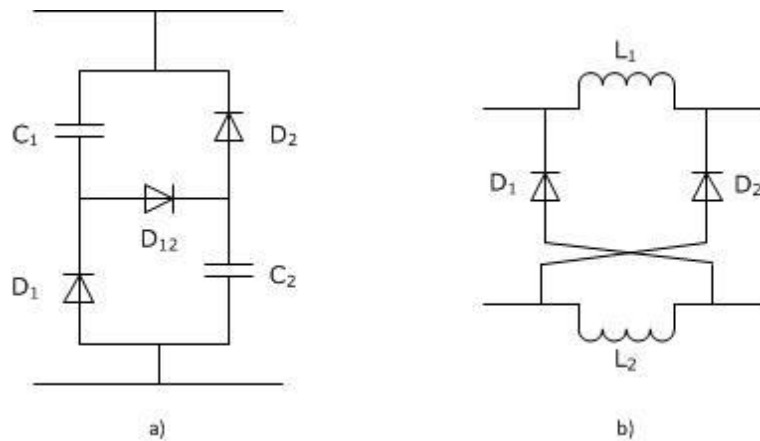
Fig.4.1. Switching cells:
a) C-switching cell; b) L-switching cell.

During t_{on} switching time the capacitors (C_1 and C_2) are discharged in parallel as can be seen in Fig. 4.3.b); in the t_{off} switching time the capacitors are charged in series ($V_{C1}=V_{C2}=V_C$) from the input voltage. The input inductor (L_{in}) of the HBDC-C/L is added to reduce the ripple of the input current.

His switching topologies, t_{on} (=$D \cdot T_s$) and t_{off} (=$(1-D) \cdot T_s$) are shown in Fig. 4.3.b and c.

It can be seen that during t_{on} switching time the output current (i_{out}) is equal with the current through each inductor of the L-switching cell and the inductors are charged in series; during the t_{off} switching time the output current is equal with the sum of the current through each inductor belonging to the L-switching cell and the inductors are discharged in parallel.
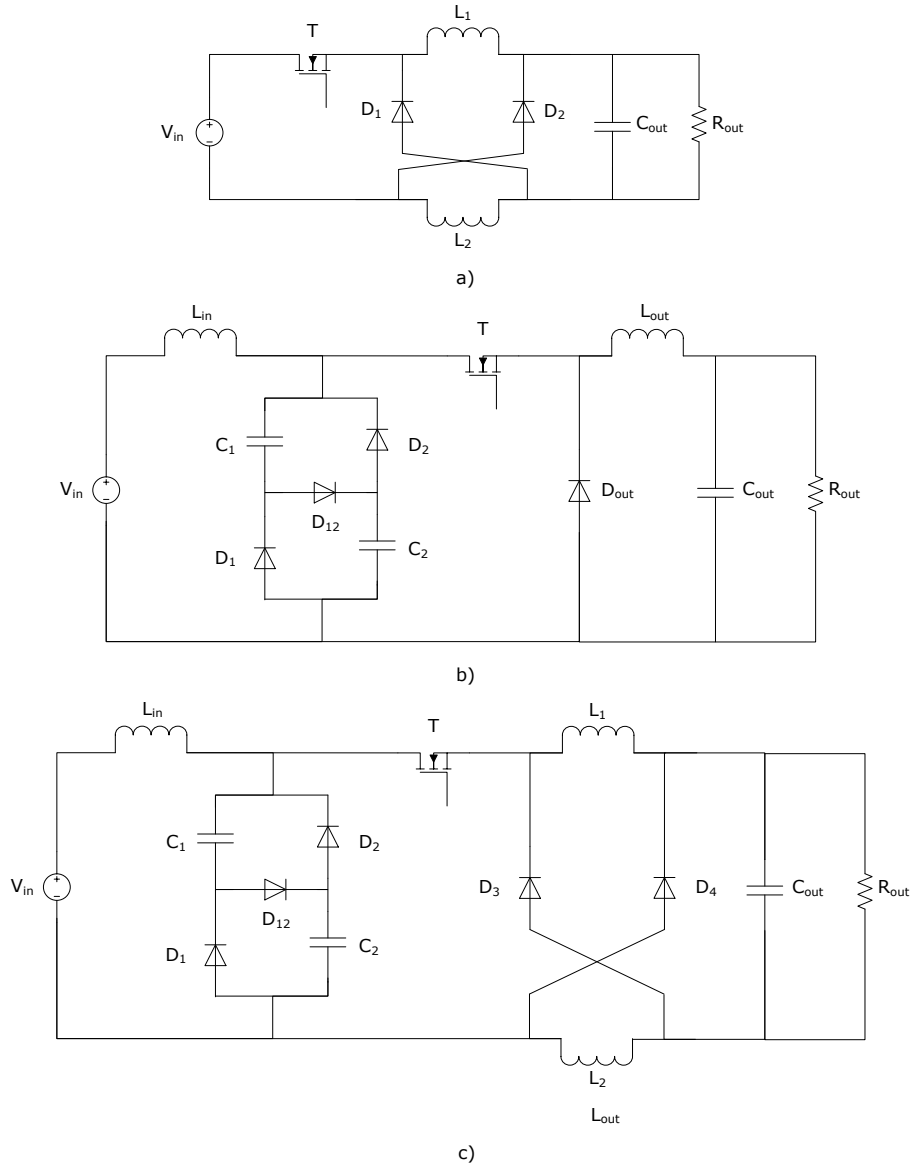
Fig.4.2. Hybrid Buck DC-DC converters:
a) HBDC-L; b) HBDC-C; c) HBDC-C/L as a combination of HBDC-L and HBDC-C.
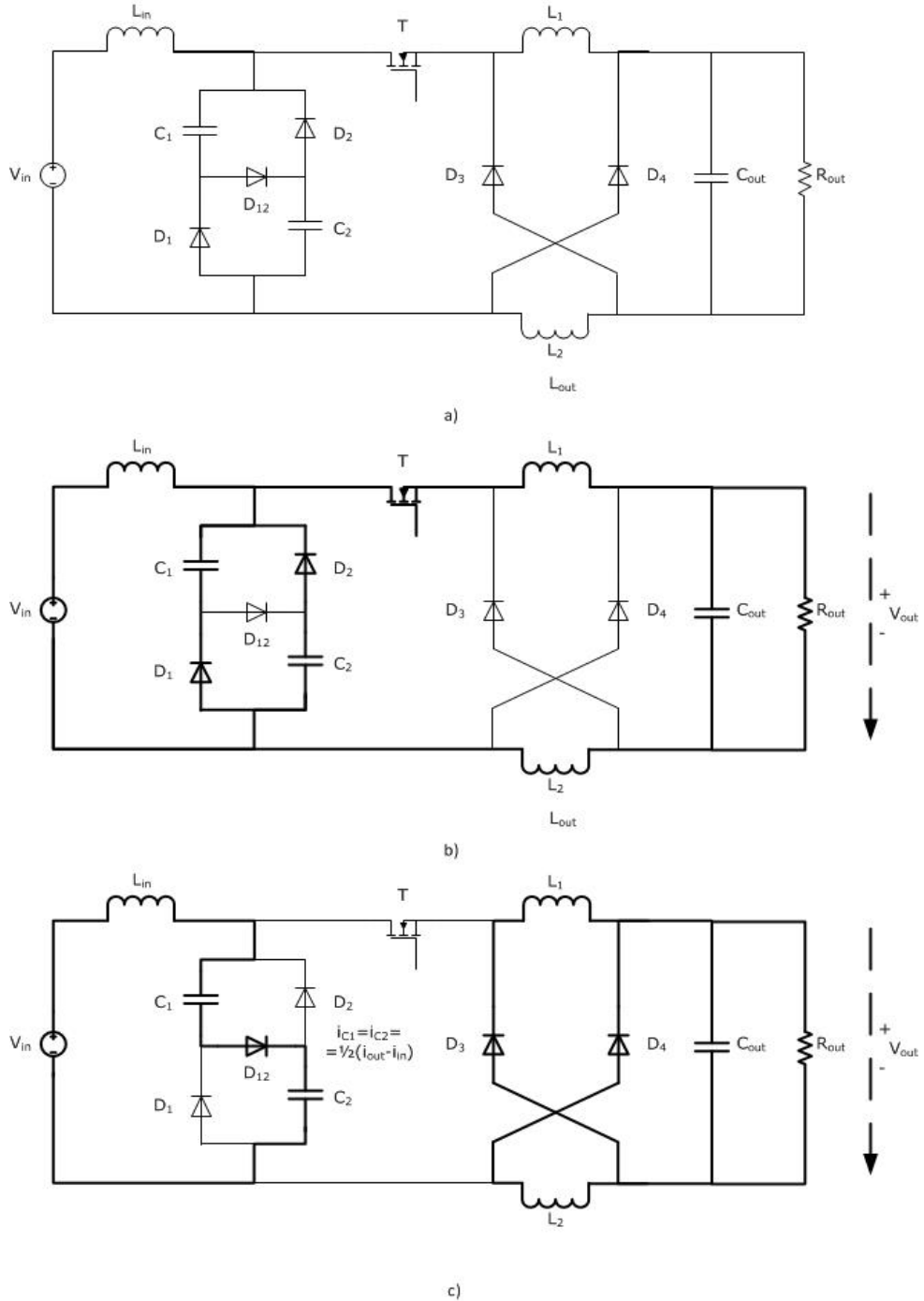
Fig.4.3. HBDC-C/L:
a) Converter diagram; b) t_{on} switching topology; c) t_{off} switching topology.

4.2. HBDC-C/L analysis and design

If the input voltage V_{in} and the output voltage V_{out} are considered constant (C_{out} sufficiently large to assume that the output voltage ripple is zero) during one switching period, the voltage-second balances on L_{in}, L_1 and L_2 can be written as:

$$\left[(1 - D) \cdot (V_{in} - 2 \cdot V_C) + D \cdot (V_{in} - V_C) \right] = 0 \tag{4.1}$$

$$\left[(1 - D) \cdot (-V_{out}) + D \cdot \left(V_C - V_{L_1} - V_{out} \right) \right] = 0 \tag{4.2}$$

$$\left[(1 - D) \cdot (-V_{out}) + D \cdot \left(V_C - V_{L_2} - V_{out} \right) \right] = 0 \tag{4.3}$$

The relation between V_{out} and V_{in} given in (4.4) is obtained from (4.1), (4.2) and (4.3).

$$V_{out} = \frac{D}{(2 - D)^2} \cdot V_{in} \tag{4.4}$$

From the input to output voltage conversion ratio equation (4.4) can be seen that the output voltage is reduced by (2-D) times more than in the case of the HBDC-C and HBDC-L converters and by (2-D)^2 times more than in the case of the BDC.

Depending on the values of V_{in} and V_{out}, the converter operates in one of the two modes: continuous current mode (CCM) or discontinuous current mode (DCM). Only CCM is treated in this chapter.

For the input inductor L_{in} we can write the following equation:

$$\frac{1}{T_s} \left[(T_s - t_{on}) \cdot (V_{in} - 2 \cdot V_C) + t_{on} \cdot (V_{in} - V_C) \right] = 0 \tag{4.5}$$

$$\left[(1 - D) \cdot (V_{in} - 2 \cdot V_C) + D \cdot (V_{in} - V_C) \right] = 0 \tag{4.6}$$

From equation (4.6) results that the voltage drop across the input capacitor is equal with the ratio of the input voltage and (2-D):

$$V_C = \frac{V_{in}}{2 - D} \tag{4.7}$$

During t_{on}, if the inductors L_1 and L_2 are considered equal ($L_1 = L_2 = L$), the next equations can be written:

$$L_1 \cdot \frac{di_{L_1}}{dt} = V_C - V_{out} - L_2 \cdot \frac{di_{L_2}}{dt} \tag{4.8}$$

$$L_1 \cdot \frac{di_{L_1}}{dt} = L_2 \cdot \frac{di_{L_2}}{dt} = L \cdot \frac{di_L}{dt} \tag{4.9}$$

$$L\frac{di_L}{dt} = \frac{V_C - V_{out}}{2} \tag{4.10}$$

For the output inductors L_1 and L_2 we can write the following equations:

$$\frac{1}{T_s}\left[(T_s - t_{on}) \cdot (-V_{out}) + t_{on} \cdot (V_C - V_L - V_{out})\right] = 0 \tag{4.11}$$

$$\left[(1-D) \cdot (-V_{out}) + D \cdot \left(\frac{V_C - V_{out}}{2}\right)\right] = 0 \tag{4.12}$$

From equation (4.12) results that the voltage drop across the input capacitor (as a function of the output voltage) is equal with:

$$V_C = \frac{2-D}{D} \cdot V_{out} \tag{4.13}$$

From equation (4.6) and (4.13) we obtain the expression of the output to input voltage conversion ratio as a function of duty cycle:

$$\frac{V_{out}}{V_{in}} = \frac{D}{(2-D)^2} \tag{4.14}$$

If the output inductors (L_1 and L_2) are equal, the slope of the current i_{L1} is the same as the slope of the current i_{L2} and we can write the following equations during t_{off} switching time interval:

$$-L_1 \cdot \frac{di_{L_1}}{dt} = -L_2 \cdot \frac{di_{L_2}}{dt} = V_{out} \tag{4.15}$$

$$-L \cdot \frac{di_L}{dt} = V_{out} \tag{4.16}$$

If we consider that the current through inductors rises and decreases linearly, we can replace di_L/dt in equation (4.10) with:

$$\frac{di_L}{dt} = \frac{\Delta i_L}{t_{on}} = \frac{I_{L,max} - I_{L,min}}{t_{on}} \tag{4.17}$$

In equation (4.16) di_L/dt can be replaced with:

$$\frac{di_L}{dt} = -\frac{\Delta i_L}{t_{off}} = -\frac{\Delta i_L}{T_s - t_{on}} \tag{4.18}$$

The following system is obtained:

$$\begin{cases} V_C - V_{out} = 2 \cdot L \cdot \dfrac{\Delta i_L}{t_{on}} \\[2mm] L \cdot \dfrac{\Delta i_L}{T_s - t_{on}} = V_{out} \end{cases} \tag{4.19}$$

The current variation for the inductor must be the same for T opened and T closed.

$$\frac{V_C - V_{out}}{2 \cdot L} \cdot t_{on} = \frac{V_{out} \cdot (T_s - t_{on})}{L} \tag{4.20}$$

From equation (4.20) the expression of the duty cycle as a function of the output voltage and the voltage drop across the capacitors C_1 and C_2 is obtained:

$$D = \frac{t_{on}}{T_s} = \frac{2 \cdot V_{out}}{V_C + V_{out}} \tag{4.21}$$

Using equation (4.7) in equation (4.21) a second order equation is obtained. A single solution of this second order equation is the expression of the duty cycle as a function of the input and output voltages:

$$D = \frac{V_{in} + 4 \cdot V_{out} - \sqrt{V_{in}^2 + 8 \cdot V_{in} \cdot V_{out}}}{2 \cdot V_{out}} \tag{4.22}$$

The switching period of the transistor:

$$T_s = \frac{1}{f_s} \tag{4.23}$$

Considering the converter efficiency the maximum input power is determined using the following equation:

$$P_{in,max} = \frac{P_{out,max}}{\eta} \tag{4.24}$$

The maximum and minimum values of the input current according to the values of the input voltage are:

$$I_{in,max} = \frac{P_{in,max}}{V_{in,min}} \tag{4.25}$$

$$I_{in,min} = \frac{P_{in,max}}{V_{in,max}} \tag{4.26}$$

The maximum and minimum values of the output current according to the values of the output voltage are:

$$I_{out,max} = \frac{P_{out,max}}{V_{out,min}} \tag{4.27}$$

$$I_{out,min} = \frac{P_{out,max}}{V_{out,max}} \tag{4.28}$$

Converter components dimensioning:

➢ The input inductor (L_{in}):

In this case the value of the input current is equal to the average value of the current through the input inductor, L_{in}:

$$I_{in} = I_{L_{in}} \tag{4.29}$$

The input current is calculated using the following equation, considering the maximum input power and the input voltage:

$$I_{in} = \frac{P_{in,max}}{V_{in}} \tag{4.30}$$

In the t_{off} switching topology the voltage drop across the input inductor has the following expression:

$$V_{L_{in}} = V_{in} - V_C = V_{in} - \frac{V_{in}}{(2-D)} = V_{in} \cdot \frac{(1-D)}{(2-D)} \tag{4.31}$$

We impose an inductor current ripple equal to X_1 % (X_1-constant, chosen value) of the maximum input current:

$$\Delta I_{L_{in}} = X_1\% \cdot I_{in,max} = X_1\% \cdot \frac{P_{in,max}}{V_{in,max}} \tag{4.32}$$

The maximum and minimum values of the current through the input inductor are calculated using:

$$I_{L_{in}, max} = I_{L_{in}} + \frac{\Delta I_{L_{in}}}{2}$$

(4.33)

$$I_{L_{in}, min} = I_{L_{in}} - \frac{\Delta I_{L_{in}}}{2}$$

(4.34)

Knowing that:

$$V_{L_{in}} = L \cdot \frac{\Delta I_{L_{in}}}{\Delta t}$$

(4.35)

results the value of the input inductance:

$$L_{in} = \frac{V_{L_{in}}}{\Delta I_{L_{in}}} \cdot \Delta t$$

(4.36)

$$L_{in} = \frac{V_{in} \cdot (1 - D)}{\Delta I_{L_{in}} \cdot (2 - D)} \cdot \Delta t$$

(4.37)

where: $\Delta t = t_{on}$.

> Capacitors (C_1, C_2):

- $C_1 = C_2 = C$

In the t_{off} switching topology ($V_{C1} = V_{C2} = V_C$) C_1, C_2 are charged in series from the input voltage, and in the t_{on} switching topology they are discharged in parallel.

The voltage drop over the capacitors (V_C) is presented in equation (4.7) and (4.13).

We impose a voltage ripple through capacitor of X_2 % (X_2-constant, chosen value) from the maximum input voltage:

$$\Delta V_C = X_2\% \cdot V_{in, max}$$

(4.38)

Knowing that:

$$i_C = C \cdot \frac{\Delta V_C}{\Delta t}$$

(4.39)

and in switching topology t_{on},

$$i_C = \frac{1}{2}(I_{out} - I_{in})$$

(4.40)

results the capacitor's capacity:

$$C = i_C \cdot \frac{\Delta t}{\Delta V_C}$$

(4.41)

➢ <u>Diodes (D$_1$, D$_2$, D$_{12}$):</u>

• D$_1$, D$_2$

During t$_{on}$ switching topology the current through diodes D$_1$ and D$_2$ is equal with the current through capacitors C$_1$ and C$_2$. The current through diode D$_{12}$ during t$_{on}$ switching topology is equal with zero.

The current (i$_D$) through diodes D$_1$ and D$_2$ is expressed with the following equation:

$$i_D = \frac{1}{2} \cdot \left(i_{L1,min} + \left(\frac{\Delta I_{L1}}{t_{on}} \right) - i_{Lin,min} + \left(\frac{\Delta I_{Lin}}{t_{on}} \right) \right) \tag{4.42}$$

• D$_{12}$

During t$_{off}$ switching topology the current through diodes D$_1$ and D$_2$ is equal with zero. The current through diode D$_{12}$ during t$_{off}$ switching topology is equal with the current through C$_1$ and L$_{in}$. The current through diode D$_{12}$ is expressed with the following equation:

$$i_{D12} = \left(i_{Lin,max} - \left(\frac{\Delta I_{Lin}}{t_{off}} \right) \right) \tag{4.43}$$

➢ <u>Transistor (T):</u>

The average value of the current through T during t$_{on}$ is equal to the average value of the current through the output inductors during t$_{on}$:

$$I_{T_{on}} = I_{L1,on} = I_{L2,on} = I_{out} \tag{4.44}$$

The average value of the current through transistor during the entire switching period T$_s$ can be calculated from I$_{T,on}$ using equation (4.45):

$$I_T = I_{T_{on}} \cdot D = I_{out} \cdot D \tag{4.45}$$

Considering:

$$V_{in} \cdot I_{in} = \frac{V_{out} \cdot I_{out}}{\eta} \tag{4.46}$$

$$I_{out} = \frac{V_{in}}{V_{out}} \cdot I_{in} \cdot \eta \tag{4.47}$$

and from equation (4.14):

$$I_{out} = \frac{(2-D)^2}{D} \cdot I_{in} \cdot \eta \tag{4.48}$$

$$I_{T_{on}} = \frac{I_T}{D} = \frac{(2-D)^2}{D} \cdot I_{in} \tag{4.49}$$

The average value of the current through transistor is given by equation (4.50):

$$I_T = (2 - D)^2 \cdot I_{in} \tag{4.50}$$

The voltage drop over the transistor is:

$$V_T = V_{out} + 2 \cdot V_C = V_{out} + 2 \cdot \frac{V_{in}}{2 - D} = V_{in} \cdot \frac{4 - D}{(2 - D)^2} \tag{4.51}$$

> The output inductors (L$_1$, L$_2$):

The value of the average output current is equal to the average value of the current through the output inductors, L_1 and L_2:

$$I_{out} = I_{T_{on}} = I_{L_{1,on}} = I_{L_{2,on}} = I_{L_{on}} \tag{4.52}$$

$$I_{out} = \frac{P_{out,max}}{V_{out}} \tag{4.53}$$

In the t_{on} switching topology the voltage drop across the output inductor has the following expression:

$$V_L = \frac{V_C - V_{out}}{2} = \frac{\dfrac{V_{in}}{(2 - D)} - V_{out}}{2} = V_{in} \cdot \frac{1 - D}{(2 - D)^2} \tag{4.54}$$

We impose an inductor current ripple equal to X$_3$ % (X$_3$-constant, chosenvalue) of the maximum output current:

$$\Delta I_L = X_3\% \cdot I_{out,max} = X_3\% \cdot \frac{P_{out,max}}{V_{out,max}} \tag{4.55}$$

The maximum and minimum values of the current through the output inductors are calculated using:

$$I_{L_{max}} = I_L + \frac{\Delta I_L}{2} \tag{4.56}$$

$$I_{L_{min}} = I_L - \frac{\Delta I_L}{2} \tag{4.57}$$

Knowing that:

$$V_L = L \cdot \frac{\Delta I_L}{\Delta t} \tag{4.58}$$

results the value of the input inductance:

$$L = \frac{V_L}{\Delta I_L} \cdot \Delta t \tag{4.59}$$

$$L_{in} = \frac{V_{in} \cdot (1 - D)}{\Delta I_L \cdot (2 - D)} \cdot \Delta t \tag{4.60}$$

where: $\Delta t = t_{on}$.

The average current through transistor, I_T, is equal with the value of the input current and C-switching cell output current and can be calculated with:

$$I_T = I_{in} + \frac{1}{2} \cdot (I_{out} - I_{in}) = \frac{1}{2} \cdot (I_{out} + I_{in}) \tag{4.61}$$

$$I_{L,on} = I_{T,on} = \frac{I_T}{D} = \frac{1}{2} \cdot \frac{(I_{in} + I_{out})}{D} \tag{4.62}$$

$$I_{L,max} = \frac{1}{2} \cdot \frac{(I_{in,max} + I_{out,max})}{D} \tag{4.63}$$

$$\Delta I_L = I_{L,max} - I_{L,min} = \frac{(V_C - V_{out})}{2 \cdot L} \cdot D \cdot T_S \tag{4.64}$$

$$I_{L,max} = I_{L,on} + \frac{\Delta i_L}{2} = \frac{L \cdot (I_{in} + I_{out}) + D^2 \cdot (V_C - V_{out}) \cdot T_S}{2 \cdot D \cdot L} \tag{4.65}$$

$$I_{L,min} = I_{L,on} - \frac{\Delta I_L}{2} = \frac{L \cdot (I_{in} + I_{out}) - D^2 \cdot (V_C - V_{out}) \cdot T_S}{2 \cdot D \cdot L} \tag{4.66}$$

The maximum current through transistor $i_{T,max}$ is equal to $i_{L,max}$.

$$iI_{T,max} = I_{L,max} \tag{4.67}$$

➢   The output diodes (D_3, D_4):

Each of the two diodes D_3 and D_4 must be able to resist a maximum forward current equal to the maximum inductor current.

The average forward current of one diode:

$$I_D = \frac{I_{D,off} \cdot t_{off}}{T_S} = \frac{I_L \cdot (T_S - D \cdot T_S)}{T_S} = I_L \cdot (1 - D) \tag{4.68}$$

The reverse voltage across one diode when the power switch T is closed is given by:

$$V_D = L \cdot \frac{di_L}{dt} + V_{out} = \frac{V_{in}}{(2 - D)^2} \tag{4.69}$$

➢   The output capacitor (C_{out}):

We impose a voltage ripple through capacitor of X_4 % (X_4-constant, choosen value) from the maximum output voltage:

$$\Delta V_{C_{out}} = X_4\% \cdot V_{out,max} \tag{4.70}$$

Knowing that:

$$\Delta V_{out} = \frac{\Delta Q}{C} \tag{4.71}$$

$$\Delta Q = \frac{\dfrac{\Delta I_L \cdot T_s}{2}}{2} \tag{4.72}$$

$$\Delta V_{out} = \frac{\Delta Q}{C} = \frac{1}{C} \cdot \frac{1}{2} \cdot \frac{T_s}{2} \cdot \frac{\Delta I_L}{2} \tag{4.73}$$

results:

$$C_{out} = \frac{T_s}{8} \cdot \frac{\Delta I_L}{\Delta V_{C_{out}}} \tag{4.74}$$

The current through the output capacitor is equal with the alternative component of the current through the output inductor switching cell.

$$i_{C_{out}} = i_L - I_L = i_L - I_{out} \tag{4.75}$$

4.3. HBDC-C/L digital simulation and experimental results

In this section, digital simulations and experimental results of HBDC-C/L converter will be presented.

The values used for the HBDC-C/L prototype components (in simulations and experimental setup) are:

L_{in}=13 [μH]
L_1=L_2=13 [μH]
$C_{1,2}$ = 29.92 [μF]
C_{out} =47.6 [μF].
f_s=50 [kHz].

To validate the theoretical analysis of HBDC-C/L, digital simulations and experimental measurements were carried on.

The simulations were made using PSim simulation program, in open-loop. The experimental measurements were taken using a HBDC-C/L prototype (Fig. 4.5) built for this purpose.

The simulated and experimental results were obtained for: V_{in}=42 [V], V_{out}=12.5 [V], I_{out}=18.41 [A], D=62 % and a switching frequency f_s=50 [kHz]. The converter was operating in CCM.

Fig. 4.4 presents the PSim simulation model of the HBDC-C/L.
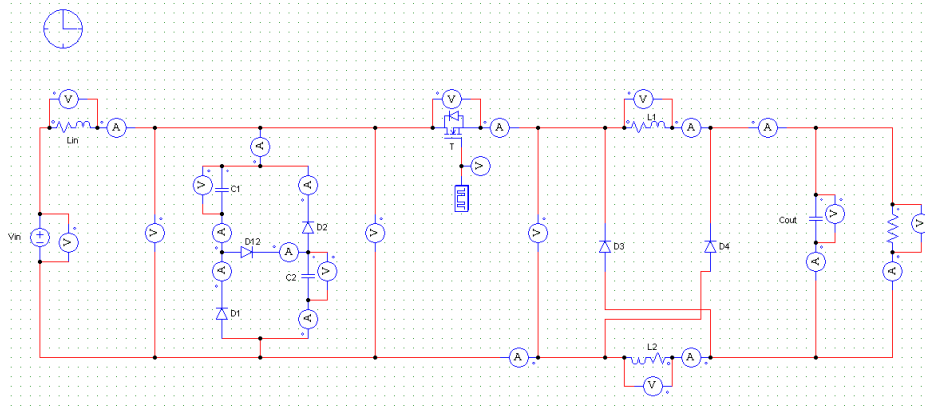
Fig.4.4. HBDC-C/L PSim model for open-loop simulation.

Fig. 4.5 presents the HBDC-C/L prototype. The simulated waveforms presented in Fig. 4.6-4.19 in comparison with the measured waveforms, were obtained using realistic simulation models for the HBDC-C/L components.

Fig.4.5. HBDC-C/L prototype.

In Figs.4.6, 4.7 the current through the input inductor is presented, Figs. 3.8 and 3.9 presents the voltage across the C-switching cell. The voltage across the transistor is presented in Fig. 4.10 and Fig. 4.11. In Fig. 4.12-4.13 the current through the output inductors is presented. The output current of the L-switching cell, or the sum of the currents through the output inductors, is presented in Figs. 4.14 and 4.15. The current through the diodes of the L-switching cell is presented in Figs. 4.16 and 4.17.
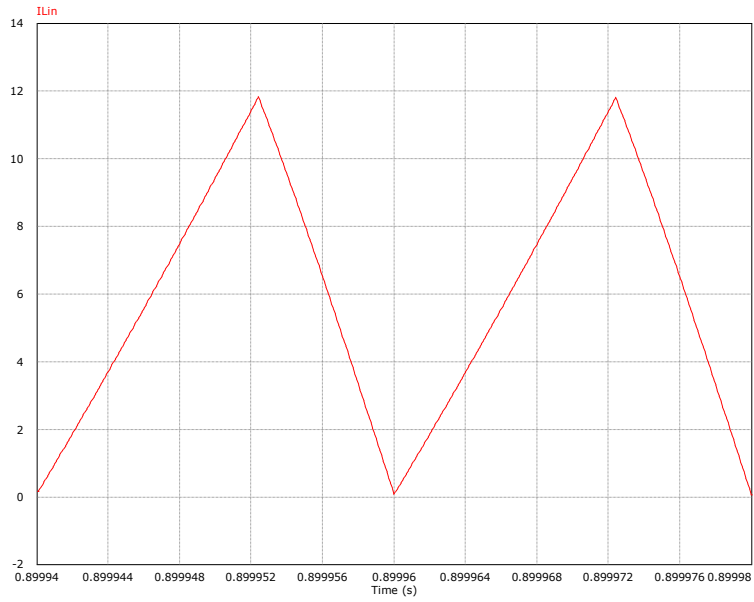
Fig.4.6. HBDC-C/L simulated waveform of the current through the input inductor L_{in}.
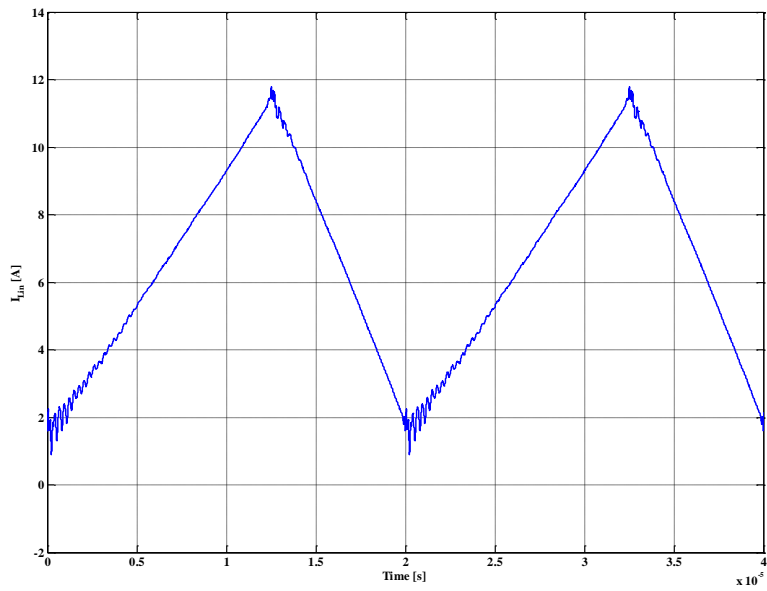
Fig.4.7. HBDC-C/L experimental waveform of the current through the input inductor L_{in}.
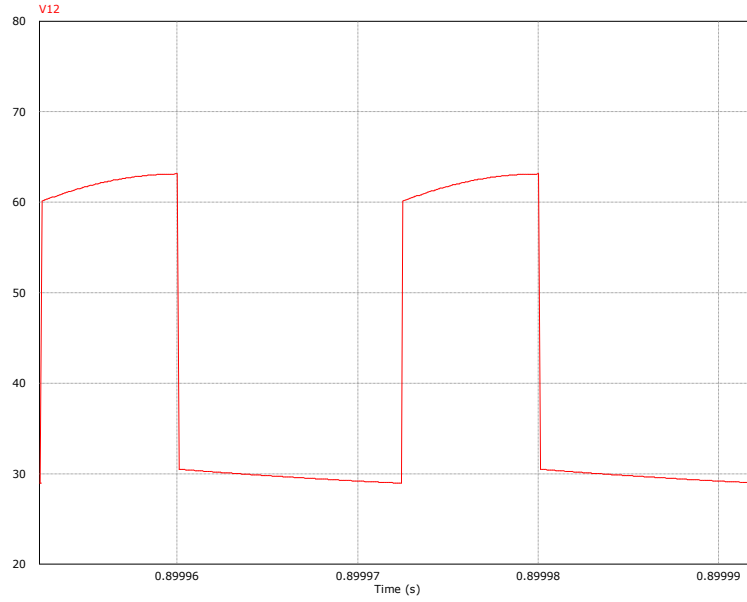
Fig.4.8. HBDC-C/L simulated waveform of the voltage across the C-switching cell.
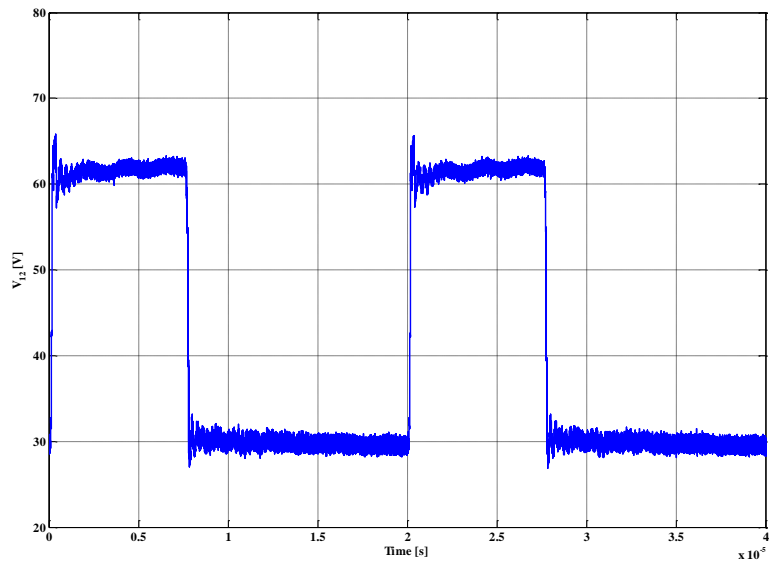
Fig.4.9. HBDC-C/L experimental waveform of the voltage across the C-switching cell.
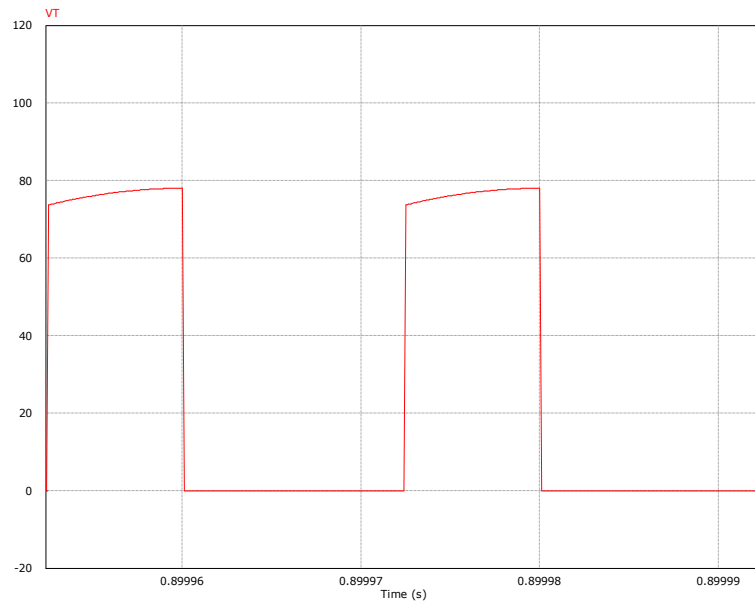
Fig.4.10. HBDC-C/L simulated waveform of the voltage across the transistor.
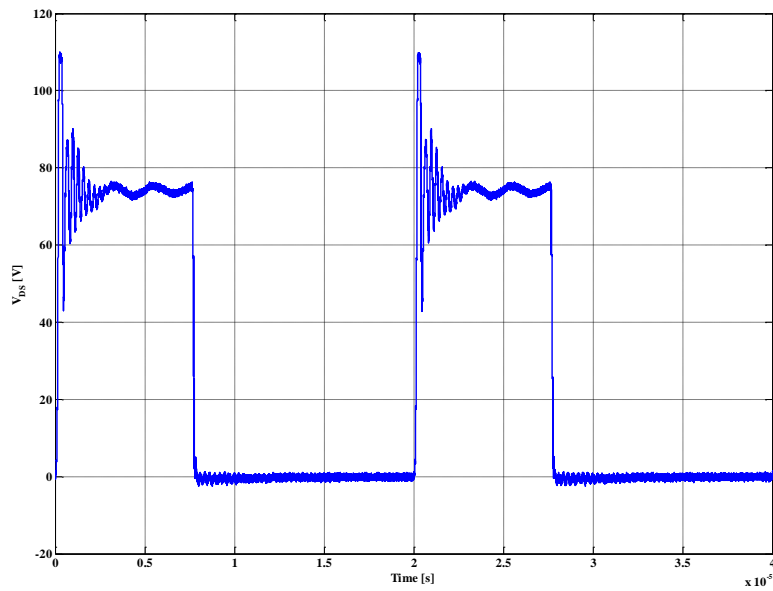
Fig.4.11. HBDC-C/L experimental waveform of the voltage across the transistor.
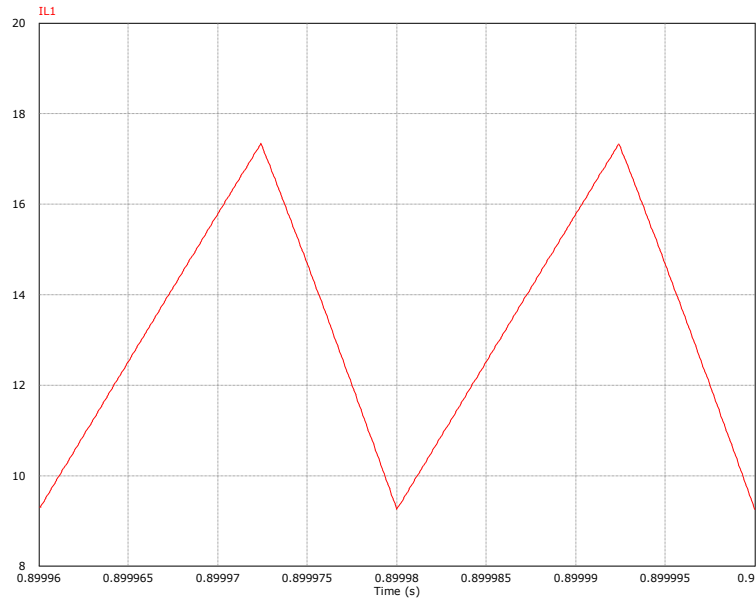
Fig.4.12. HBDC-C/L simulated waveform of the current through the output inductors.
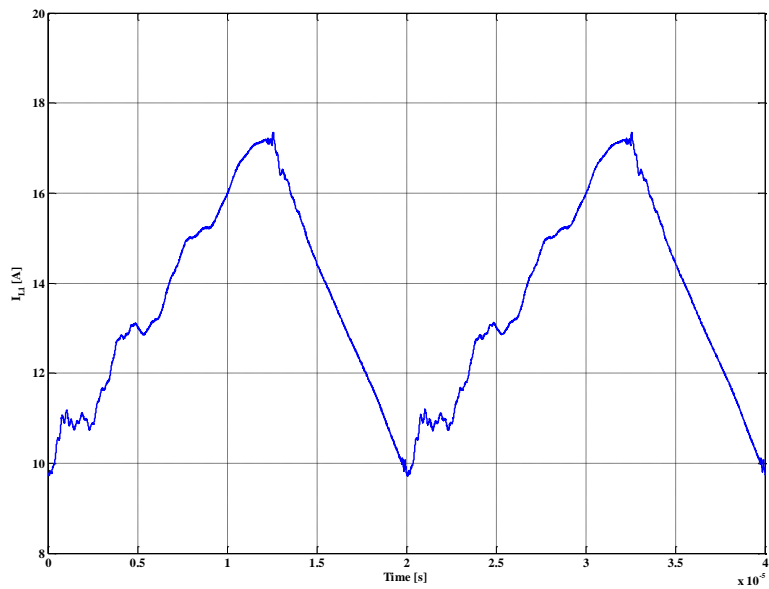
Fig.4.13. HBDC-C/L experimental waveform of the current through the output inductors.
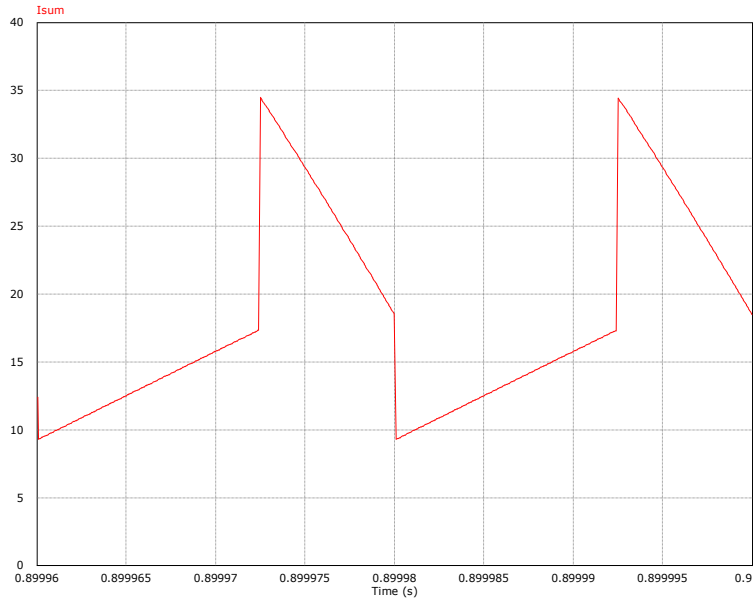
Fig.4.14. HBDC-C/L simulated waveform of the L-switching cell output current.
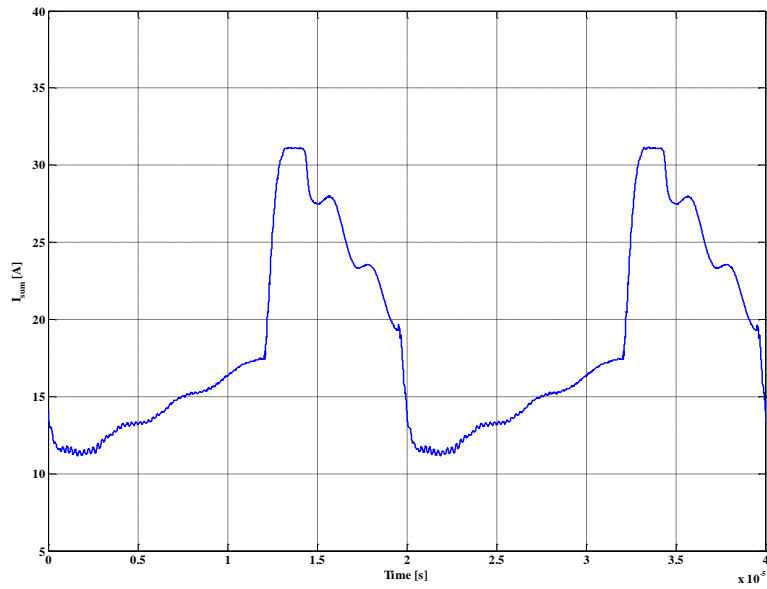
Fig.4.15. HBDC-C/L experimental waveform of the L-switching cell output current.
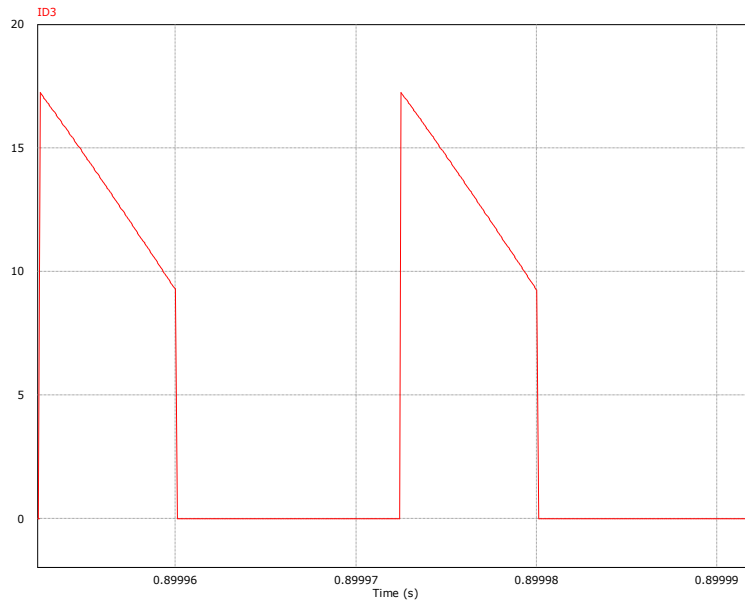
Fig.4.16. HBDC-C/L simulated waveform of the current through diode D_3.
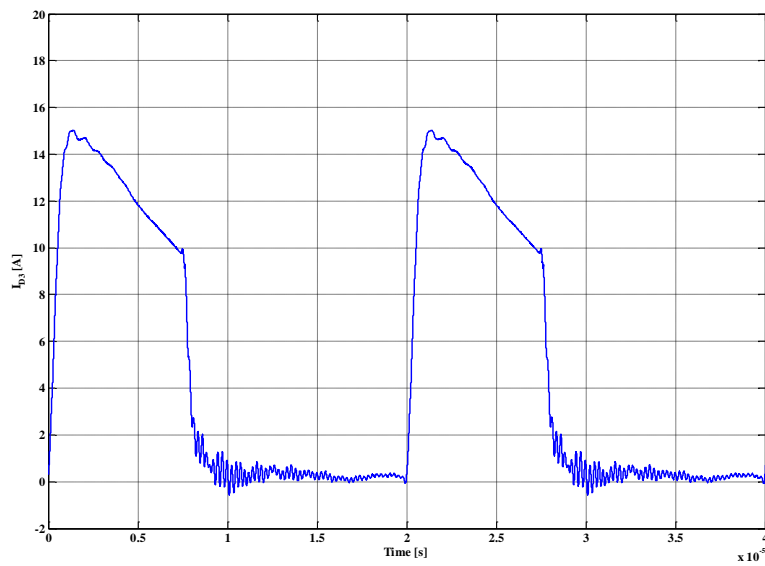
Fig.4.17. HBDC-C/L experimental waveform of the current through diode D_3.

4.4. Conclusion

For a higher step-down voltage conversion ratio, even higher than the one of the HBDC-L and HBDC-C converters, at the input of the BDC a switched-capacitor cell, formed by two identical capacitors and three diodes, was inserted and the inductor and the output diode of the BDC were replaced with a switched-inductor cell, formed by two identical inductors and two diodes. Or can be said that by mixing together the HBDC-C and HBDC-L converters, the HBDC-C/L was proposed. The output voltage of the HBDC-C/L is reduced (2-D) times than the output voltage of the HBDC-L and HBDC-C converters and $(2-D)^2$ times more than the output voltage of the BDC.

A full analysis and design of the HBDC-C/L was made.

Equations for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor currents are presented.

Main current and voltage waveform, simulation and experimental waveforms were presented and compared.

A real prototype of the HBDC-C/L was built. For the comparison between the experimental and the simulation waveforms, obtained with PSim simulation program, a model with realistic electronic components was used.

All the simulation waveforms of HBDC-C/L are in good agreement with the experimental waveforms confirming the theoretical study.

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5. COMPARATIVE EVALUATIONS OF HYBRID BUCK DC-DC CONVERTERS

5.1. Introduction

For a higher step-down voltage conversion ratio hybrid structures of Buck DC-DC converter (HBDC), using switched-capacitors or switched-inductors, were presented in the literature [5.1-5.12].

A comparative study of HBDC-C, HBDC-L and HBDC-C/L converters, with BDC is the object of this chapter, in order to have a practical guide needed to a correct choice of these structures for various applications [5.8-5.12].

5.2. Comparative evaluation of BDC and HBDC-L converters.

This subchapter is focused on a comparative study of BDC and a HBDC-L, in CCM and at the boundary (BCM) between CCM and DCM.

A comparative analysis of the BDC and HBDC-L in CCM and BCM, taking into account the average and RMS values of the input, output and inductors currents, and the maximum voltage and current stresses of the transistor, are presented. We assume that the HBDC-L doesn't operate in DCM therefore DCM is not analyzed.

The input-output relation between V_{out} and V_{in} is obtained from the steady-state analysis of the HBDC-L converter, as in equations (2.1) and (2.2).

$$V_{out} = \frac{D}{2-D} \cdot V_{in} \qquad (5.1)$$

In the case of the BDC, the input-output relation between V_{in} and V_{out} is given by the following expression:

$$V_{out} = D \cdot V_{in} \qquad (5.2)$$

In this case the output voltage of the HBDC-L converter is reduced by (2-D) times more than in the case of the BDC converter.

The voltage stress of the HBDC-L transistor is given by (5.3) and it shows the voltage stress of the HBDC-L transistor is bigger, but in applications that require a high conversion ratio the maximum voltage across the transistor of HBDC-L is not drastically increased.

$$\hat{V}_T = V_{in} + V_{out} \qquad (5.3)$$

The voltage stress of the BDC transistor is given by (5.4):

$$\hat{V}_T = V_{in} \qquad (5.4)$$

The approximate values of the transistor RMS current are given in (5.5) and (5.6) for BDC and HBDC-L respectively; I_{out} is the load (output) current.

$$I_{T,rms} \cong \sqrt{D} \cdot I_{out} \qquad (5.5)$$

$$I_{T,rms} \cong \frac{\sqrt{D}}{2-D} \cdot I_{out} \qquad (5.6)$$

The HBDC-L output capacitor current waveform is very different compared with BDC due to the action of the switching inductor cell. In addition, the HBDC-L, output capacitor current ripple, $I_{Cout,ripple}$ depends on the load, as the following equation shows:

$$I_{C_{out},ripple} = 3 \cdot \frac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1-D) + \frac{I_{out}}{2-D} \qquad (5.7)$$

where f_s is the switching frequency.

Table 5.1 presents a synthetic comparison between BDC and HBDC-L converters, a comparison already presented with the equations above.

TABLE 5.1. Synthetic comparison between BDC and HBDC-L converters.

Converter / Function		Buck (BDC)	Hybrid Buck (HBDC-L)
$\dfrac{V_{out}}{V_{in}}$		D	$\dfrac{D}{2-D}$
Transistor Maximum Voltage $\hat{V}_T$		V_{in}	$V_{in} + V_{out}$
Transistor Current	$I_{T,rms}$	$\cong \sqrt{D} \cdot I_{out}$	$\cong \dfrac{\sqrt{D}}{2-D} \cdot I_{out}$
	I_T	$D \cdot I_{out}$	$\dfrac{D}{2-D} \cdot I_{out}$
Output Capacitor Current Ripple	$V_{out} = const.$	$\dfrac{V_{out}}{L_{out} \cdot f_s} \cdot (1-D)$	$3 \cdot \dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1-D) + \dfrac{I_{out}}{2-D}$

The duty cycles of both converters, as function of the ratio between the output and input voltages, are presented in Fig. 5.1.

Using HBDC-L, at the same input voltage and D as BDC, the output voltage is reduced by (2-D) times more, or the same output voltage is obtained for a higher value of D, which results in smaller peak transistor current.

Fig. 5.2 presents the p.u. of the transistor RMS currents (relative to the output current), for both converters.
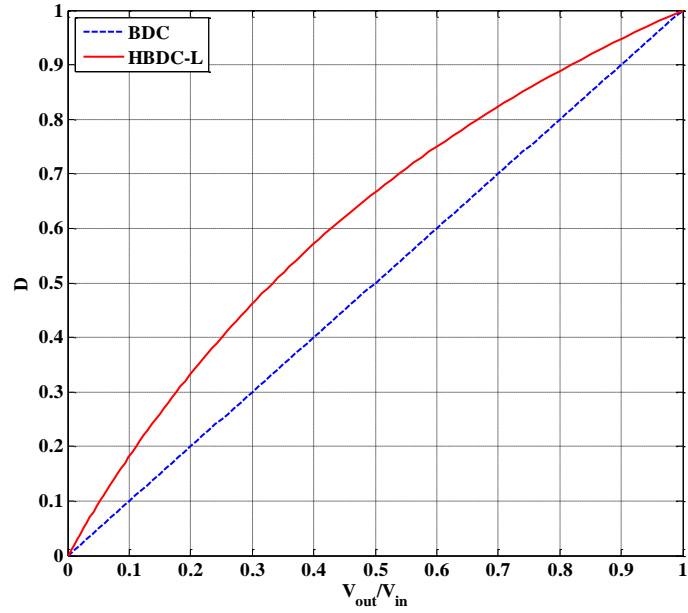
Fig.5.1. The duty cycle as function of the conversion ratio for BDC and HBDC-L.
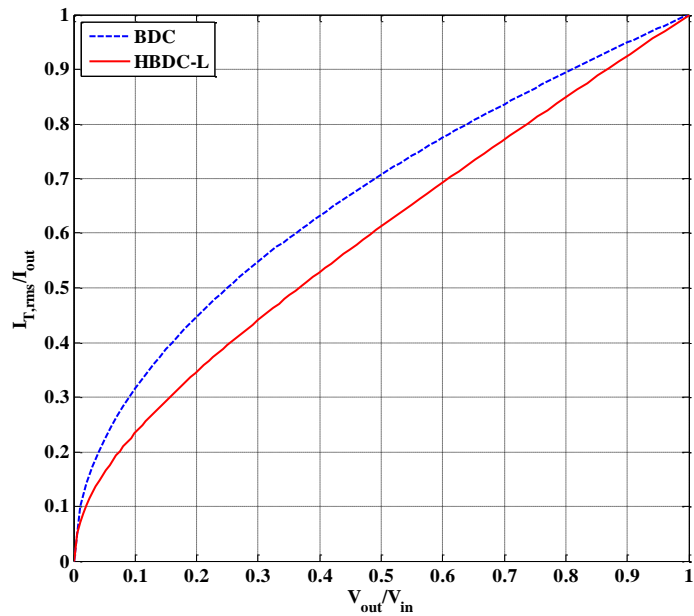
Fig.5.2. P.u. transistor RMS current for BDC and HBDC-L.

Smaller RMS current values of HBDC-L give reduced conduction losses in transistor for this converter. In addition, the peak transistor current is lower due to the bigger value of HBDC-L duty cycle. This leads to smaller commutation losses if the hard switching is used.

When HBDC-L operates at the BCM, the average value of each inductor current, $I_{L,lim}$, is:

$$I_{L,lim} = \frac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) \tag{5.8}$$

if V_{out} is kept constant.

The maximum value of (5.8) is obtained for D→0 and is given by:

$$I_{L,lim,max} = \frac{V_{out}}{2 \cdot L_1 \cdot f_s} \tag{5.9}$$

To always ensure that HBDC-L operates in CCM or at least at BCM, the minimum output current has to be equal with (5.9), for any value of D.

For BDC, the average value of the inductor current, $I_{L,lim}$, is given by the same equation. Assuming that the equivalent BDC needs to operate at the same minimum output current as HBDC-L, without reaching the DCM, $I_{L,lim,max}$, obtained for D→0, is given by:

$$I_{L,lim,max} = \frac{V_{out}}{2 \cdot L_{out} \cdot f_s} \tag{5.10}$$

where L_{out} is the BDC inductor.

The two values of $I_{L,lim,max}$ given in (5.9) and (5.10) have to be equal, which means that the inductors of BDC and HBDC-L converters have the same inductance.

Fig. 5.3 presents the p.u. average inductor current (relative to $I_{L,lim,max}$) at BCM, as a function of the voltage conversion ratio at V_{out}=constant, for both converters.

When V_{in} is kept constant, $I_{L,lim}$ and $I_{L,lim,max}$ for HBDC-L can be obtained from:

$$I_{L,lim} = \frac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot \left(\frac{1 - D}{2 - D} \right) \tag{5.11}$$

The maximum of $I_{L,lim}$ is obtained for D=0.586. Replacing D with this value in (5.11), we obtain (5.12) for $I_{L,lim,max}$ calculation.

$$I_{L,lim,max} = \frac{V_{in}}{11,66 \cdot L_1 \cdot f_s} \tag{5.12}$$

For BDC, $I_{L,lim}$ and $I_{L,lim,max}$, obtained for D=0.5, are given by:

$$I_{L,lim} = \frac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D) \tag{5.13}$$

$$I_{L,\,lim,\,max} = \frac{V_{in}}{8 \cdot L_{out} \cdot f_s} \tag{5.14}$$

As in the previous case (V_{out}=constant), to ensure that the minimum output current is the same for both converters, the two maximum average inductor currents must be equal, which gives the following relation between L_1 and L_{out}:

$$L_1 = 0.686 \cdot L_{out} \tag{5.15}$$

The p.u. average inductor current (relative to $I_{L,lim,max}$), for both converters, at BCM, are presented in Fig. 5.4, as a function of the voltage conversion ratio, when V_{in} = constant.
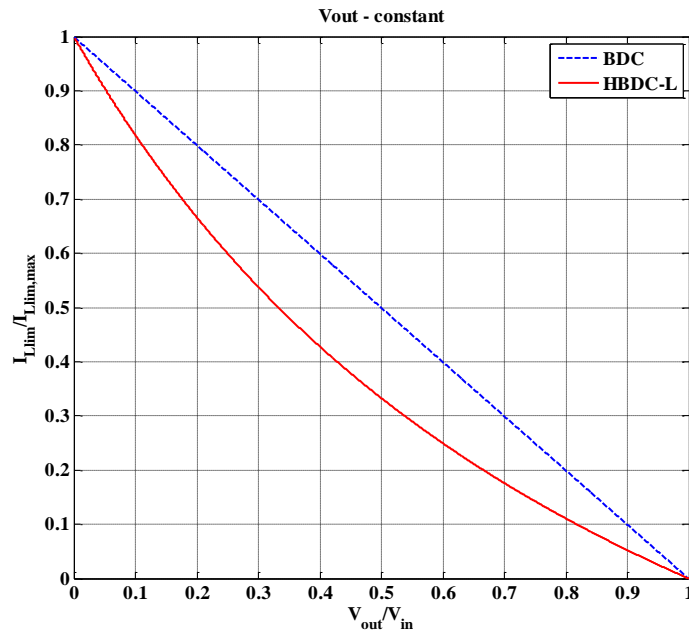
Fig.5.3. BDC and HBDC-L p.u. average inductance current in BCM, at V_{out}=constant.

The peak inductor currents $\hat{I}_L$ and the corresponding p.u. expressions (relative to $I_{L,lim,max}$ at BCM) are presented in (5.16), (5.17) for BDC and (5.18), (5.19) for HBDC-L:

$$\hat{I}_L = \frac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D) + I_{out} \tag{5.16}$$

$$\frac{\hat{I}_L}{I_{L,\,lim,\,max}} = \frac{I_{out}}{I_{L,\,lim,\,max}} + \left(1 - \frac{V_{out}}{V_{in}}\right) \tag{5.17}$$

$$\hat{I}_L = \frac{V_{out}}{2 \cdot L_1 \cdot f_S} \cdot (1-D) + \frac{I_{out}}{2-D} \tag{5.18}$$

$$\frac{\hat{I}_L}{I_{L,lim,max}} = \left(\frac{1 - \dfrac{V_{out}}{V_{in}}}{1 + \dfrac{V_{out}}{V_{in}}} \right) + \frac{I_{out}}{I_{L,lim,max}} \cdot \left(\frac{1 + \dfrac{V_{out}}{V_{in}}}{2} \right) \tag{5.19}$$
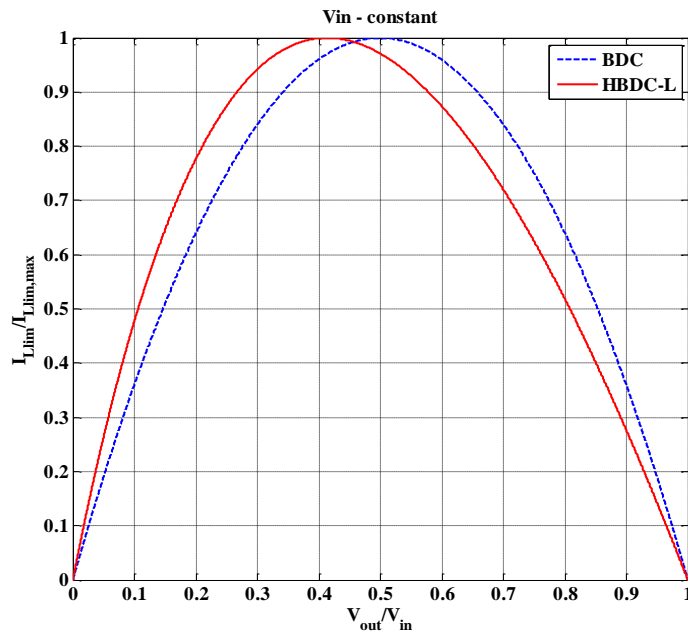
Fig.5.4. BDC and HBDC-L p.u. average inductance current in BCM, at V_{in}=constant.

Fig. 5.5 presents the p.u. values of $\hat{I}_L$ for $I_{out}=I_{L,lim,max}$, when V_{out}=constant.

Considering the same operation conditions (the same input and output voltages and equal output power), the average transistor currents are the same, although the equations used to calculate them are different.

If V_{out}=constant, HBDC-L enters DCM at a lighter load current.

If V_{in}=constant, in the range of voltage conversion ratio $V_{out}/V_{in}<0.4$, where HBDC-L is normally used, it reaches DCM at lower output currents than BDC.

In Fig. 5.5, for V_{out}=constant, and $0<V_{out}/V_{in}<0.6$ the peak inductor current of HBDC-L is at least 25% smaller than that of BDC.

Because of the difference in peak values and in inductance values (which are different if V_{in}=constant) of the converters, it is possible that the two inductors of HBDC-L together are not more expensive than the BDC inductor.

The peak value of HBDC-L inductor current, at low values of conversion ratio, is much smaller.

The HBDC-L output capacitor current ripple depends on the load.

The average input currents for BDC and HBDC-L at boundary condition, for V_{in}=constant and V_{out}=constant respectively, can be obtained from the expressions of the peak values of the input currents in CCM; the equations are given in Table 5.2.

In boundary condition mode, whether the case of V_{in}=constant or V_{out}=constant, the average output currents of both converters are related to the average input currents through the converter's conversion ratio. These can be seen in Table 5.2 when comparing the two sets of equations.

Equations for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor current are presented synthetically in Table 5.1 and Table 5.2. Some of these equations are general, while others have a form which depends on whether V_{in} or V_{out} is kept constant.
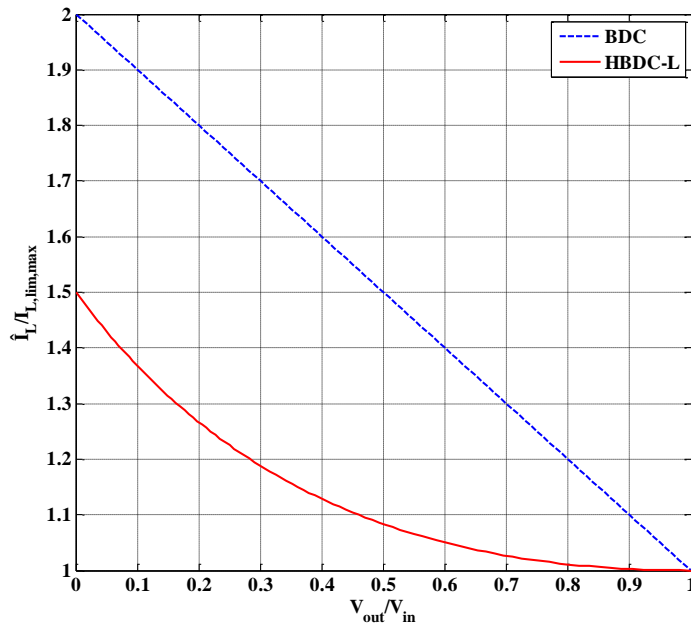
Fig.5.5. BDC and HBDC-L p.u. peak inductor current for V_{out}=constant.

ABLE 5.2. Synthetic comparison between BDC and HBDC-L converters.

Converter / Function			Buck (BDC)	Hybrid Buck (HBDC-L)
Continuous Current Mode	Peak Input Current $\hat{I}_{in} = \hat{I}_T = \hat{I}_L$	$V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D) + I_{out}$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) + \dfrac{I_{out}}{2 - D}$
		$V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D) + I_{out}$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot \left(\dfrac{1 - D}{2 - D}\right) + \dfrac{I_{out}}{2 - D}$
Boundary Operation Mode	Average input current I_{in}	$V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D)$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot (1 - D)$
		$V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D^2 \cdot (1 - D)$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D^2 \cdot \left(\dfrac{1 - D}{2 - D}\right)$
	Average Inductor Current $I_{L,lim}$	$V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D)$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D)$
		$V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D)$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot \left(\dfrac{1 - D}{2 - D}\right)$
	Maximum Average Inductor Current $I_{L,lim,max}$	$V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s}$ for D→0	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s}$ for D→0
		$V_{in} = const.$	$\dfrac{V_{in}}{8 \cdot L_{out} \cdot f_s}$ for D=0.5	$\dfrac{V_{in}}{11.66 \cdot L_1 \cdot f_s}$ for D=0.586
	Average output current I_{out}	$V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D)$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) \cdot (2 - D)$
		$V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D)$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot (1 - D)$

5.3. Comparative evaluation of BDC and HBDC-C converters.

This subchapter discusses the theoretical aspects of the comparison, in analytical and synthetic form, for the main current and voltage waveforms, in CCM and BCM.

The input-output relation between V_{out} and V_{in} is obtained from the steady-state analysis of the HBDC-C converter, as in equations (3.1) and (3.2).

$$V_{out} = \frac{D}{2-D} \cdot V_{in} \tag{5.20}$$

In the case of the BDC, the input-output relation between V_{in} and V_{out} is given by the following expression:

$$V_{out} = D \cdot V_{in} \tag{5.21}$$

In this case the output voltage of the HBDC-C is reduced by (2-D) times more than in the case of the BDC.

The voltage stress of the HBDC-C transistor is given by expression (5.22):

$$\hat{V}_T = 2 \cdot V_{in} \tag{5.22}$$

The voltage stress of the BDC transistor is given by (5.23) and it shows that the maximum voltage across the transistor (in the worst case) is two times higher for HBDC-C converter:

$$\hat{V}_T = V_{in} \tag{5.23}$$

The approximate value of the transistor RMS current is given in (5.24) for BDC and HBDC-C (I_{out} is the load current).

$$I_{T,rms} \cong \sqrt{D} \cdot I_{out} \tag{5.24}$$

The value of the average transistor current for both converters is given by:

$$I_T = D \cdot I_{out} \tag{5.25}$$

Table 5.3 presents a synthetic comparison between BDC and HBDC-C converters, a comparison already presented with the equations above.

Fig. 5.6 shows the duty cycle (D) as a function of the voltage conversion ratio for both converters. For $V_{out}/V_{in}=0.1$ HBDC-C has an almost double D and a corresponding lower maximum value of the peak transistor current.

For the same voltage conversion ratio, HBDC-C works at a higher duty cycle, with positive aspects regarding the converter control.

Fig. 5.7 presents the p.u. approximate value of the transistor RMS current (relative to the output current), as a function of the voltage conversion ratio for both converters. HBDC-C has the disadvantage of a higher RMS transistor current. For $V_{out}/V_{in}=0.1$ $I_{T,rms}$ of BDC is 25% lower.
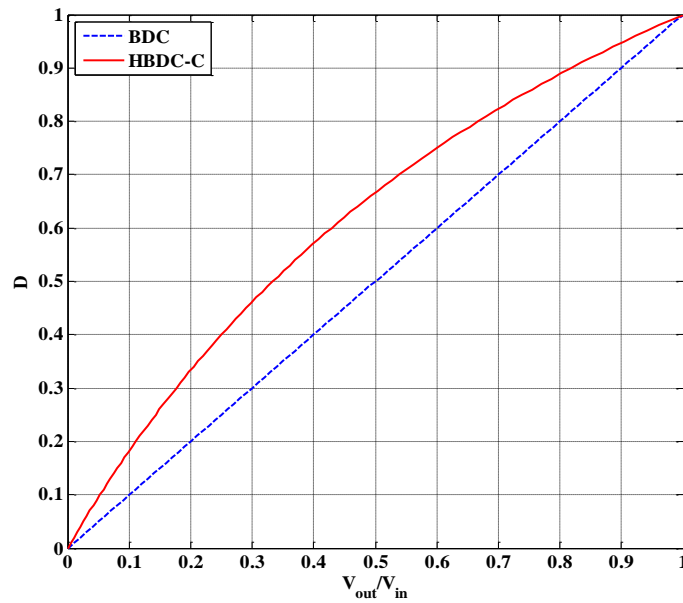
Fig.5.6. BDC and HBDC-C duty cycle as function of the voltage conversion ratio.
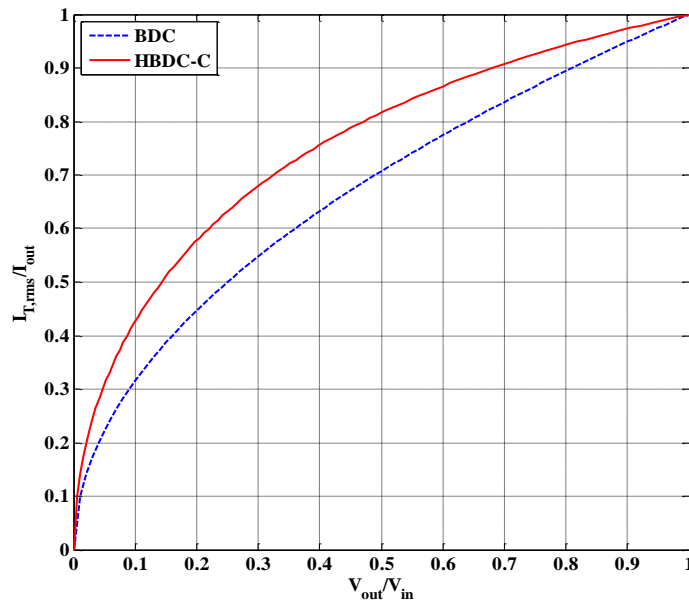
Fig.5.7. The p.u. transistor RMS current for BDC and HBDC-C converters.

TABLE 5.3. Synthetic comparison between BDC and HBDC-C converters.

Converter / Function		Buck (BDC)	Hybrid Buck (HBDC-C)
V_{out} / V_{in}		D	$\dfrac{D}{2-D}$
Transistor Maximum Voltage $\hat{v}_T$		V_{in}	$2 \cdot V_{in}$
Transistor Current	$I_{T,rms}$	$\cong \sqrt{D} \cdot I_{out}$	$\cong \sqrt{D} \cdot I_{out}$
	I_T	$D \cdot I_{out}$	$D \cdot I_{out}$

HBDC-C boundary operation mode (between CCM and DCM) is provided by the following equations, expressing the average values of the "limit" currents through the input and output inductances:

$$I_{L,lim} = \frac{V_{in}}{2 \cdot L \cdot f_s} \cdot D \frac{(1-D)}{(2-D)} \tag{5.26}$$

when V_{in} is kept constant, and:

$$I_{L,lim} = \frac{V_{out}}{2 \cdot L \cdot f_s} \cdot (1-D) \tag{5.27}$$

when V_{out} is kept constant.

Equations (5.26) and (5.27) are valid for both inductors, therefore $I_{L,lim} = I_{Lin,lim}$ if $L = L_{in}$, or $I_{L,lim} = I_{Lout,lim}$ if $L = L_{out}$.

The maximum value of (5.26) and (5.27) is obtained for D=0.586, and D→0, respectively:

$$I_{L,lim,max} = \frac{V_{in}}{11.66 \cdot L \cdot f_s} \tag{5.28}$$

$$I_{L,lim,max} = \frac{V_{out}}{2 \cdot L \cdot f_s} \tag{5.29}$$

From the equation of the output peak inductor current, $\hat{I}_{Lout}$, (5.30) and (5.31) we can write the p.u. equation (5.32) for BDC. The p.u. equation for HBDC-C (5.34) can be obtained using (5.30) and (5.33).

$$\hat{I}_{Lout} = \frac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1-D) + I_{out} \tag{5.30}$$

$$(1-D) = 1 - \frac{V_{out}}{V_{in}} \tag{5.31}$$

$$\frac{\hat{I}_{Lout}}{I_{Lout,lim,max}} = \frac{I_{out}}{I_{Lout,lim,max}} + \left(1 - \frac{V_{out}}{V_{in}}\right) \tag{5.32}$$

$$(1-D) = \left(1 - \frac{2 \cdot V_{out}}{V_{in} + V_{out}}\right) = \left(\frac{1 - \dfrac{V_{out}}{V_{in}}}{1 + \dfrac{V_{out}}{V_{in}}}\right) \tag{5.33}$$

$$\frac{\hat{I}_{Lout}}{I_{Lout,lim,max}} = \frac{I_{out}}{I_{Lout,lim,max}} + \left(\frac{1 - \dfrac{V_{out}}{V_{in}}}{1 + \dfrac{V_{out}}{V_{in}}}\right) \tag{5.34}$$

where I_{out} is the average output current.

From equation (5.20) to equation (5.34), a synthetic comparative form of the main characteristics of both converters (BDC and HBDC-C) is presented in Table 5.3 and Table 5.4.

Figures 5.8 and 5.9 summarize graphically the boundary operation of the converters at V_{in} = ct. and at V_{out} = ct. respectively.

For V_{in}=ct., if the voltage conversion ratio is smaller than 0.45, HBDC-C enters DCM at a higher ratio of $I_{out}/I_{Lout,lim,max}$. According to Table 5.4 the ratio between $I_{Lout,lim,max}$ values of BDC and HBDC-C is 11.66/8=1.4575. Considering this, it is clear that the absolute value of I_{out} at BCM is smaller for HBDC-C for any V_{out}/V_{in}.
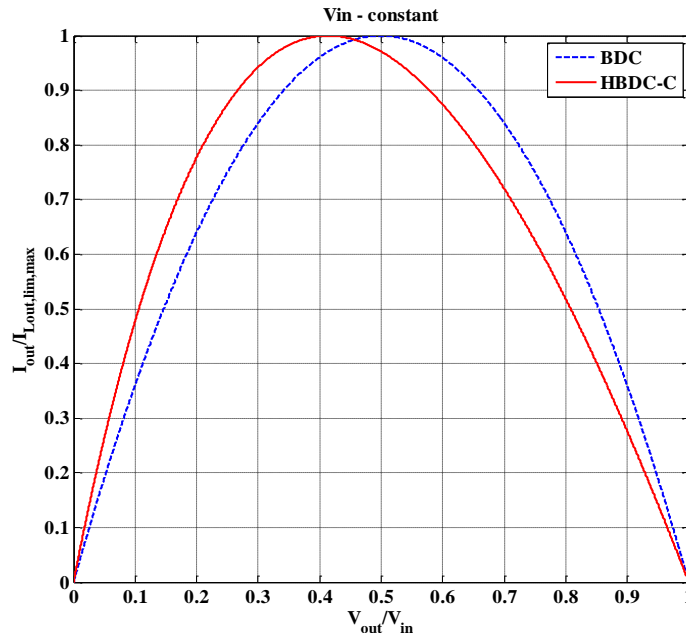
Fig.5.8. BDC and HBDC-C at the boundary operating mode, at V_{in}= constant.
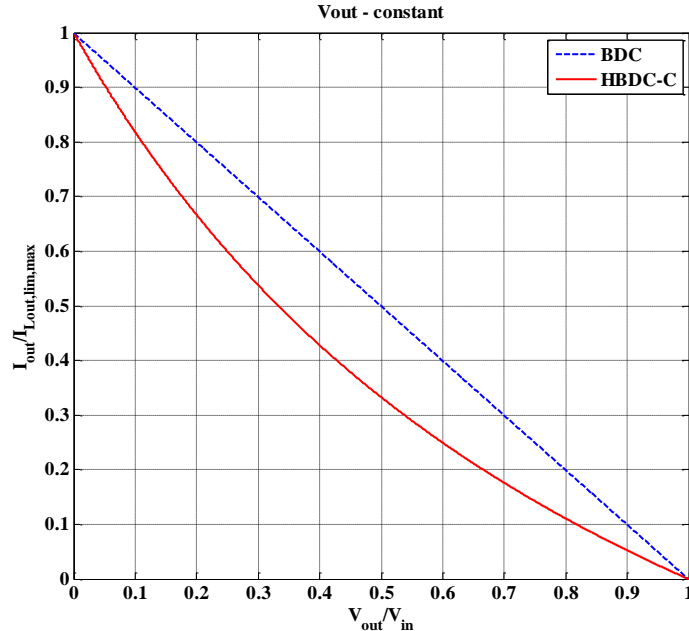
Fig.5.9. BDC and HBDC-C at the boundary operating mode, at V_{out}= constant.

For V_{out}=ct., the two values of $I_{Lout,lim,max}$ are the same as can be seen in Table 5.4 and in this condition Fig. 5.9 shows clearly that HBDC-C enters DCM at a lower output current.

Figure 5.10 presents the comparison between the p.u. values of $\hat{I}_{Lout}$ for I_{out}=$I_{Lout,lim.max}$, when V_{out} = constant. HBDC-C has a lower peak output inductor current for any V_{out}/V_{in}, but the difference between the two converters is only in the range of several percent (the maximum difference is lightly higher 10 %). For V_{out}/V_{in}=0.1 the difference between the two p.u. peak values is about 4%.

HBDC-C boundary conditions are better. If the converter has to operate in CCM or at BCM, at the same output current as BDC a lower output inductance is needed for the HBDC-C converter.

The peak transistor current is lower for HBDC-C converter with positive effects regarding the switching device.

The output inductor of HBDC-C converter can be smaller or for the same value of the output inductance the peak current is slightly reduced.

In Table 5.3 and Table 5.4 the equations for average, RMS and peak transistor current, transistor voltage stress, peak and average values of input and output inductor currents (which depends whether V_{in} or V_{out} is kept constant) are presented. The theoretical equations presented for comparison in this subchapter were verified using simulation models with ideal components.

As a final conclusion HBDC-C ensures a lower peak transistor and output inductor currents; the higher duty cycle value ensures a wider converter control domain in the range of the voltage conversion ratio. Compared to a DC-DC converter with transformer, the elimination of the high frequency transformer decreases the cost, volume and loses for this converter.
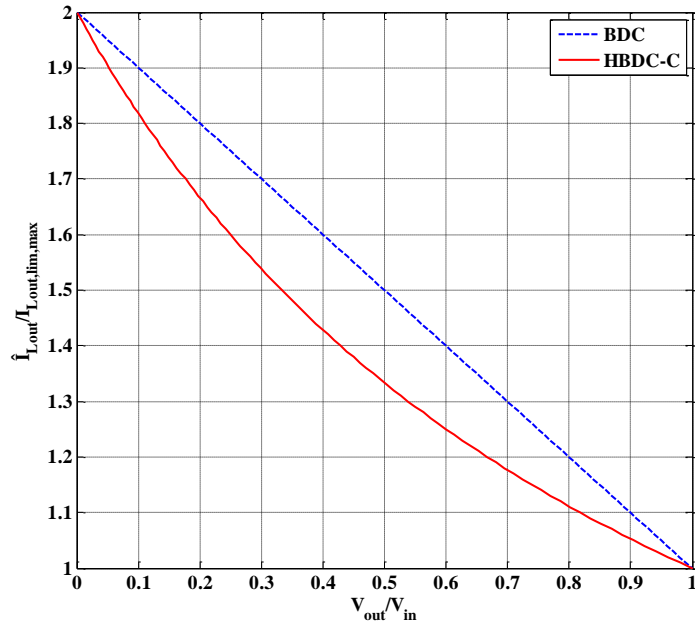
Fig.5.10. The p.u. $\hat{I}_{Lout}$ for BDC and HBDC-C, at V_{out}=constant.

TABLE 5.4. Synthetic comparison between BDC and HBDC-C converters.

Converter / Function			Buck (BDC)	Hybrid Buck (HBDC-C)
Continuous Current Mode	Peak Input Current $\hat{I}_{in}$	$V_{out} = const.$	$\frac{V_{out}}{2 \cdot L_{out} \cdot f_S} \cdot (1 - D) + I_{out}$	$\frac{V_{out}}{2 \cdot L_{in} \cdot f_S} \cdot (1 - D) + I_{out} \cdot \frac{D}{2 - D}$
		$V_{in} = const.$	$\frac{V_{in}}{2 \cdot L_{out} \cdot f_S} \cdot D \cdot (1 - D) + I_{out}$	$\frac{V_{in}}{2 \cdot L_{in} \cdot f_S} \cdot D \cdot \left(\frac{1 - D}{2 - D} \right) + I_{out} \cdot \frac{D}{2 - D}$
	Peak Output Inductor and Transistor Current $\hat{I}_{Lout} = \hat{I}_T$	$V_{out} = const.$	$\frac{V_{out}}{2 \cdot L_{out} \cdot f_S} \cdot (1 - D) + I_{out}$	$\frac{V_{out}}{2 \cdot L_{out} \cdot f_S} \cdot (1 - D) + I_{out}$
		$V_{in} = const.$	$\frac{V_{in}}{2 \cdot L_{out} \cdot f_S} \cdot D \cdot (1 - D) + I_{out}$	$\frac{V_{in}}{2 \cdot L_{out} \cdot f_S} \cdot D \cdot \left(\frac{1 - D}{2 - D} \right) + I_{out}$
Boundary Operation Mode	Maximum Average Input Current $I_{Lin,lim,max}$	$V_{out} = const.$	$\frac{V_{out}}{2 \cdot L_{out} \cdot f_S}$ for D→0	$\frac{V_{out}}{2 \cdot L_{in} \cdot f_S}$ for D→0
		$V_{in} = const.$	$\frac{V_{in}}{16 \cdot L_{out} \cdot f_S}$ for D=0.5	$\frac{V_{in}}{11.66 \cdot L_{in} \cdot f_S}$ for D=0.586
	Maximum Average Output Inductor Current $I_{Lout,lim,max}$	$V_{out} = const.$	$\frac{V_{out}}{2 \cdot L_{out} \cdot f_S}$ for D→0	$\frac{V_{out}}{2 \cdot L_{out} \cdot f_S}$ for D→0
		$V_{in} = const.$	$\frac{V_{in}}{8 \cdot L_{out} \cdot f_S}$ for D=0.5	$\frac{V_{in}}{11.66 \cdot L_{out} \cdot f_S}$ for D=0.586

5.4. Comparative evaluation of BDC and HBDC–C/L converters.

Analytical description, the voltage and current limits of the main components are synthesized in a comparative form, related to the BDC structure in order to emphasis the advantages of the proposed converter. From the first evaluation, HBDC-C/L is expected to be effectively used at input to output voltage ratios higher than 20.

In CCM, the expression of the voltage conversion ratio for the HBDC-C/L converter is given by:

$$\frac{V_{out}}{V_{in}} = \frac{D}{(2-D)^2} \qquad (5.35)$$

In the case of the BDC, the output to input relation between V_{out} and V_{in} is given by the following expression:

$$\frac{V_{out}}{V_{in}} = D \qquad (5.36)$$

In this case the output voltage of the HBDC-C/L converter is reduced by $(2-D)^2$ times more than in the case of the BDC converter.

The voltage stress $\hat{V}_T$ of the HBDC-C/L transistor is given by (5.37):

$$\hat{V}_T = \frac{4-D}{(2-D)^2} \cdot V_{in} \qquad (5.37)$$

The voltage stress $\hat{V}_T$ of the BDC transistor is given by (5.38):

$$\hat{V}_T = V_{in} \qquad (5.38)$$

The approximate values of the transistor RMS current are given in (5.39) and (5.40) for BDC and HBDC-C/L respectively; I_{out} is the load (output) current.

$$I_{T,rms} \cong \sqrt{D} \cdot I_{out} \qquad (5.39)$$

$$I_{T,rms} \cong \frac{\sqrt{D}}{2-D} \cdot I_{out} \qquad (5.40)$$

The value of the average transistor current for BDC and HBDC-C/L converters are given by the following expressions:

$$I_T = D \cdot I_{out} \qquad (5.41)$$

$$I_T = \frac{D}{2 - D} \cdot I_{out} \tag{5.42}$$

The HBDC-C/L output capacitor current waveform is very different compared with BDC due to the action of the switching inductor cell. In addition, the HBDC-C/L output capacitor current ripple, $I_{Cout,ripple}$, depends on the load, as the following equation shows:

$$I_{Cout,ripple} = \frac{V_{out}}{L_{out} \cdot f_s} \cdot (1 - D) \tag{5.43}$$

$$I_{Cout,ripple} = 3 \cdot \frac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) + \frac{I_{out}}{2 - D} \tag{5.44}$$

where f_s is the switching frequency.

Table 5.5 presents a synthetic comparison between BDC and HBDC-C/L converters, a comparison already presented with the equations above.

TABLE 5.5. Synthetic comparison between BDC and HBDC-C/L converters.

Converter / Function		Buck (BDC)	Hybrid Buck (HBDC-C/L)
$\frac{V_{out}}{V_{in}}$		D	$\frac{D}{(2 - D)^2}$
Transistor Maximum Voltage $\hat{V}_T$		V_{in}	$\frac{4 - D}{D} \cdot V_{out}$, $\frac{4 - D}{(2 - D)^2} \cdot V_{in}$
Transistor Current	$I_{T,rms}$	$\cong \sqrt{D} \cdot I_{out}$	$\cong \frac{\sqrt{D}}{2 - D} \cdot I_{out}$
	I_T	$D \cdot I_{out}$	$\frac{D}{2 - D} \cdot I_{out}$
Output Capacitor Current Ripple	$V_{out} = const.$	$\frac{V_{out}}{L_{out} \cdot f_s} \cdot (1 - D)$	$3 \cdot \frac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) + \frac{I_{out}}{2 - D}$

A comparison between the duty cycles of HBDC C/L and BDC, presented in a graphical form in Fig. 5.11, reveals that the proposed converter has a three times higher duty cycle for a voltage ratio of 0,1. If V_{out}/V_{in} is 0,05, HBDC-C/L is operating at D=0.17 which is a reasonable value. The HBDC-C/L voltage capacitor (C_1 or C_2) is only 54.64% of the input BDC capacitor. This can lead, for some applications, to a smaller cost of the entire C-switching cell compared with that of the input capacitors of BDC.

Figure 5.12 shows that the p.u. RMS currents for BDC and HBDC-C/L are the same. The peak transistor current, on the other hand, is always smaller in HBDC-C/L because it operates at a higher duty cycle for any voltage conversion ratio.

Regarding the transistor voltage stress, considering the corresponding equation from Table 5.5, if D=0.17 the maximum voltage across the transistor is $1.14 \cdot V_{in}$, which is 14% higher compared with BDC in CCM.

When HBDC-C/L operates at the BCM, the average value of each inductor current, $I_{L,lim}$, is:

$$I_{L,lim} = \frac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1-D) \tag{5.45}$$

if V_{out} is kept constant.

The maximum value of (5.45) is obtained for D→0 and is given by:

$$I_{L,lim,max} = \frac{V_{out}}{2 \cdot L_1 \cdot f_s} \tag{5.46}$$

To always ensure that HBDC-C/L operates in CCM or at least at BCM, the minimum output current has to be equal with (5.46), for any value of D.

For BDC, the average value of the inductor current, $I_{L,lim}$, is given by the same equation. Assuming that the equivalent BDC needs to operate at the same minimum output current as HBDC-C/L, without reaching the DCM, $I_{L,lim,max}$, obtained for D→0, is given by:

$$I_{L,lim,max} = \frac{V_{out}}{2 \cdot L_{out} \cdot f_s} \tag{5.47}$$

where L_{out} is the BDC inductor.

The two values of $I_{L,lim,max}$ given in (5.46) and (5.47) have to be equal, which means that the inductors of BDC and HBDC-C/L converters have the same inductance.

Fig. 5.13 presents the p.u. average inductor current (relative to $I_{L,lim,max}$) at BCM, as a function of the voltage conversion ratio at V_{out}=constant, for both converters.

When V_{in} is kept constant, $I_{L,lim}$ and $I_{L,lim,max}$ for HBDC-C/L can be obtained from:

$$I_{L,lim} = \frac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot \left(\frac{1-D}{2-D} \right) \tag{5.48}$$

The maximum of $I_{L,lim}$ is obtained for D=0.586. Replacing D with this value in (5.48), we obtain (5.49) for $I_{L,lim,max}$ calculation.

$$I_{L,lim,max} = \frac{V_{in}}{11,66 \cdot L_1 \cdot f_s} \tag{5.49}$$

For BDC, $I_{L,lim}$ and $I_{L,lim,max}$, obtained for D=0.5, are given by:

$$I_{L,lim} = \frac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1-D) \tag{5.50}$$

$$I_{L,lim,max} = \frac{V_{in}}{8 \cdot L_{out} \cdot f_s} \tag{5.51}$$
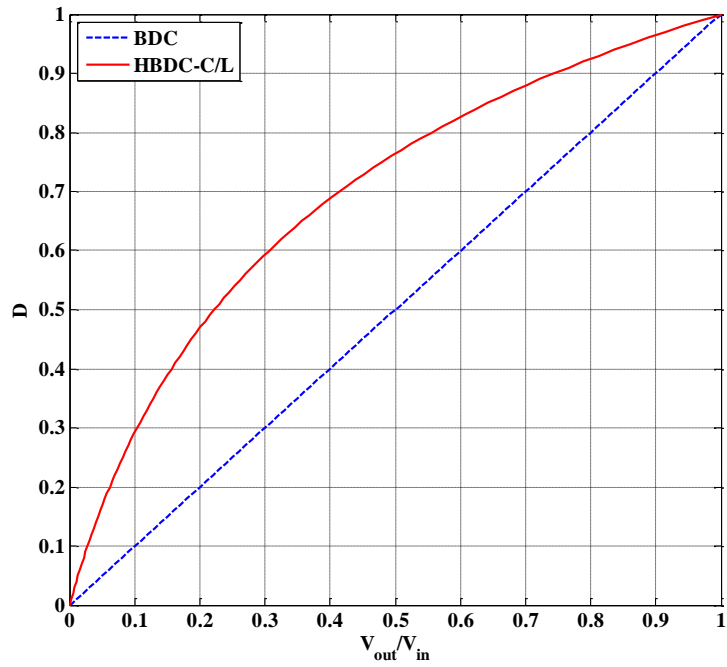
Fig.5.11. The duty cycle as function of the voltage conversion ratio for BDC and HBDC-C/L.
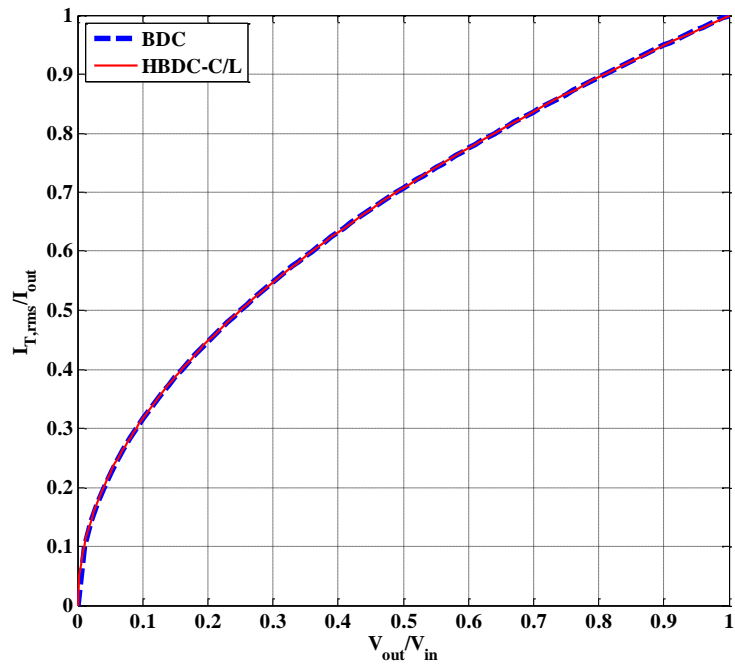
Fig.5.12. Per unit RMS transistor current for BDC and HBDC-C/L as a function of V_{out}/V_{in}.
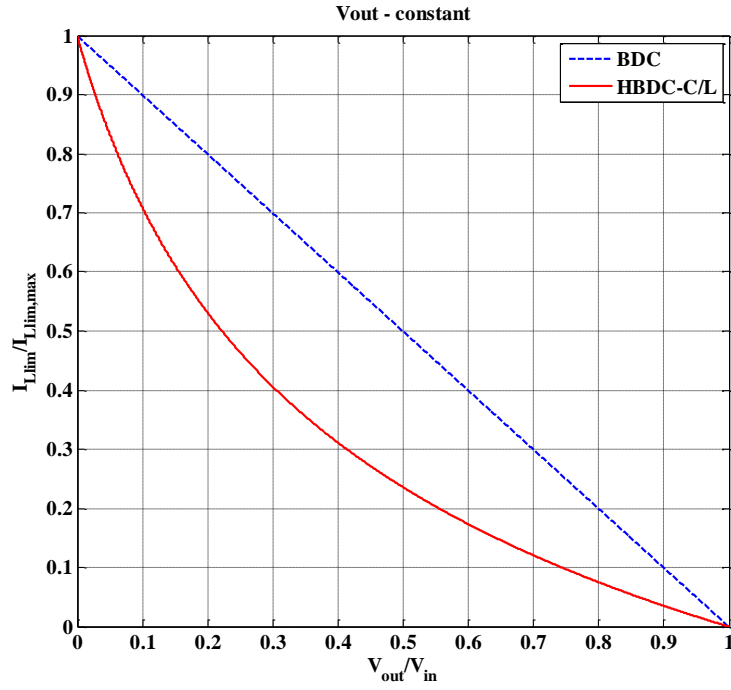
Fig.5.13. BDC and HBDC-C/L at the boundary operating mode, at V_{out}=constant.
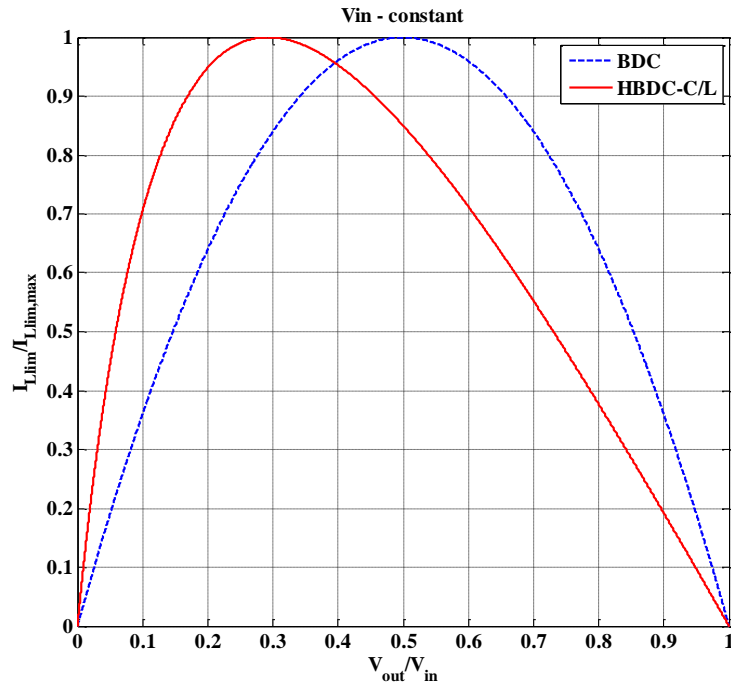
Fig.5.14. BDC and HBDC-C/L at the boundary operating mode, at V_{in}=constant.
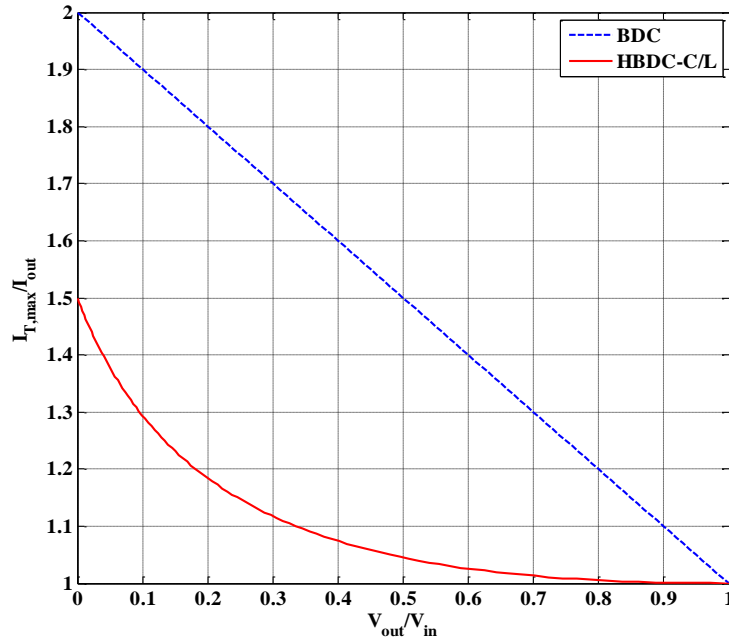
Fig.5.15. Per unit maximum transistor current for BDC and HBDC-C/L as a function of V_{out}/V_{in}.

For V_{out}=ct., the two values of $I_{Llim,max}$ are the same as can be seen in Table 5.6 and in this condition Fig. 5.13 shows clearly that HBDC-C/L enters DCM at a lower output current.

For V_{in}=ct., if the voltage conversion ratio is smaller than 0.29, HBDC-C/L enter DCM at a higher ratio of $I_{Llim}/I_{Llim,max}$.

The peak HBDC-C/L transistor current is much lower than that of BDC as can be seen in Fig. 5.15. If V_{in}/V_{out} is between 10 and 20, the current stress of the BDC transistor is 41,7% to 46,7% higher.

Compared with BDC, the output voltage of HBDC-C/L at the same duty cycle is reduced by a factor of $(2-D)^2$. If the comparison is made with HBDC-C or HBDC-L the reduction factor is $(2-D)$.

HBDC-C/L works at a much higher duty cycle than BDC (up to 3 times) if the conversion ratio is the same, with positive aspects in the converter control.

The equations for average, RMS and peak transistor current, transistor voltage stress, peak and average values of input and output inductor currents (which depends whether V_{in} or V_{out} is kept constant) are presented in Table 5.5 and 5.6; some of them are discussed above.

RMS value of the transistor current for HBDC-C/L can be up to 50% lower compared with the BDC current. However, the voltage stress of HBDC-C/L transistor is slightly higher for high ratio between V_{in} and V_{out}.

A disadvantage of HBDC-C/L is the higher ripple current in the output capacitor, due to the action of the L-switching cell.

Because of the larger number of active and passive components of HBDC-C/L the efficiency is usually lower than in the case of BDC. Depending on the application and especially on the input voltage value, the efficiencies of HBDC-C/L and BDC could be comparable.

TABLE 5.6. Synthetic comparison between BDC and HBDC-C/L converters.

Converter / Function			Buck (BDC)	Hybrid Buck (HBDC-C/L)
Continuous Current Mode	Peak Input Current $\hat{I}_{in} = \hat{I}_{L_{in}}$	$V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D) + I_{out}$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) \cdot (2 - D) + \dfrac{D}{(2 - D)^2} \cdot I_{out}$
		$V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D) + I_{out}$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot \left(\dfrac{1 - D}{2 - D}\right) + \dfrac{D}{(2 - D)^2} \cdot I_{out}$
	Peak Transistor and Output Inductors Current $\hat{I}_T = \hat{I}_{L_1} = \hat{I}_{L_2}$	$V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D) + I_{out}$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) + \dfrac{I_{out}}{2 - D}$
		$V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D) + I_{out}$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot \left(\dfrac{1 - D}{2 - D}\right) + \dfrac{I_{out}}{2 - D}$

Converter / Function		Buck (BDC)	Hybrid Buck (HBDC-C/L)
Boundary Operation Mode	Average input current I_{in} — $V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D)$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) \cdot (2 - D)$
	Average input current I_{in} — $V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D^2 \cdot (1 - D)$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot \left(\dfrac{1 - D}{2 - D} \right)$
	Average Inductor Current $I_{L,lim}$ — $V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D)$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D)$
	Average Inductor Current $I_{L,lim}$ — $V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D)$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot D \cdot \left(\dfrac{1 - D}{2 - D} \right)$
	Maximum Average Inductor Current $I_{L,lim,max}$ — $V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s}$ for $D \to 0$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s}$ for $D \to 0$
	Maximum Average Inductor Current $I_{L,lim,max}$ — $V_{in} = const.$	$\dfrac{V_{in}}{8 \cdot L_{out} \cdot f_s}$ for $D = 0.5$	$\dfrac{V_{in}}{11.66 \cdot L_1 \cdot f_s}$ for $D = 0.586$
	Average output current I_{out} — $V_{out} = const.$	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D)$	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot \dfrac{(1 - D) \cdot (2 - D)^2}{D}$
	Average output current I_{out} — $V_{in} = const.$	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1 - D)$	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D) \cdot (2 - D)$

5.5. Comparative evaluation of BDC, HBDC-C, HBDC-L and HBDC-C/L converters.

In this subchapter some of the earlier presented parameters of the classical and Hybrid Buck DC-DC converters are plotted together in a graphical form in order to provide an accurate overview between them.

Fig. 5.16 presents the duty cycle (D) as a function of the voltage conversion ratio for all four converters.
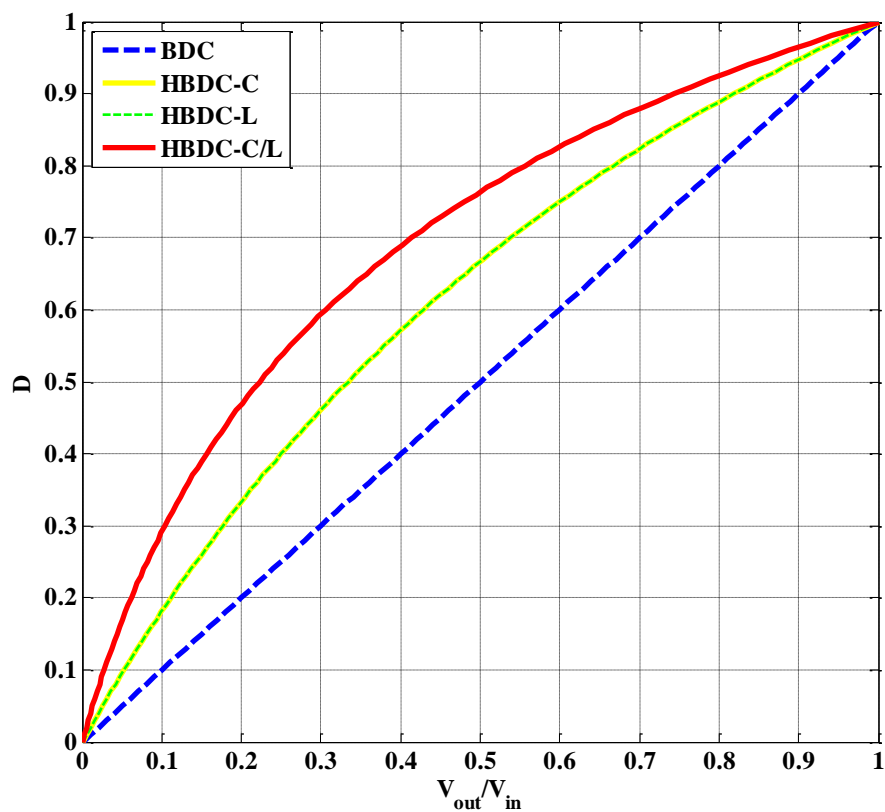
Fig.5.16. The duty cycle as a function of the voltage conversion ratio V_{out}/V_{in}.

Using HBDC-C and HBDC-L at the same input voltage and duty cycle as BDC, the output voltage is reduced by (2-D) times more, or the same output voltage is obtained for a higher value of the duty cycle, which results in smaller peak transistor current.

For V_{out}/V_{in}=0.1 HBDC-C and HBDC-L have an almost double duty cycle with positive aspects regarding the converter control.

Comparing HBDC-C/L with HBDC-C and HBDC-L it can be seen that the duty cycle of the proposed converter is one-third higher than the duty cycle of HBDC-C

and HBDC-L converters for a voltage ratio of 0.1, which results in smaller peak transistor current

Table 5.7 will present the expressions for the input to output voltage conversion ratio for all the convertors.

TABLE 5.7. Synthetic comparison between the voltage conversion ratio of all converters.

Converter / Function	BDC	HBDC-C	HBDC-L	HBDC-C/L
$\dfrac{V_{out}}{V_{in}}$	D	$\dfrac{D}{2-D}$	$\dfrac{D}{2-D}$	$\dfrac{D}{(2-D)^2}$

Fig. 5.17 presents the per unit transistor RMS currents (relative to the output current) as a function of the voltage conversion ratio for all the converters.
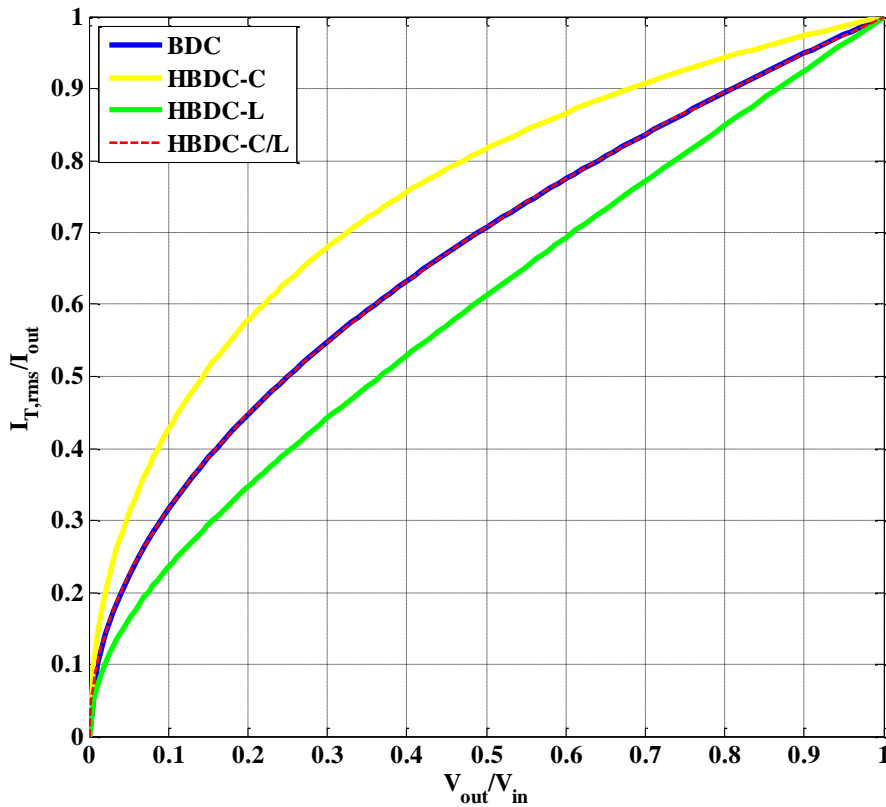
Fig.5.17. The p.u. transistor RMS currents as a function of the voltage conversion ratio V_{out}/V_{in}.

Smaller RMS current values of HBDC-L give reduced conduction losses in transistor for this converter. In addition, the peak transistor current is lower due to the bigger value of HBDC-L duty cycle.

HBDC-L has the advantage of a smaller RMS transistor current. For V_{out}/V_{in}=0.1 $I_{T,RMS}$ of BDC and HBDC-C/L is 25% higher, of HBDC-C is almost two times higher.

HBDC-C has the disadvantage of a higher RMS transistor current. For V_{out}/V_{in}=0.1 $I_{T,rms}$ of BDC is 25% lower.

Figure 5.17 show that the p.u. transistor RMS currents for BDC and HBDC-C/L are the same. The peak transistor current, on the other hand, is always smaller in HBDC-C/L because it operates at a higher duty cycle for any voltage conversion ratio.

Table 5.8 will present the expressions for the transistor RMS current for all the convertors.

TABLE 5.8. Synthetic comparison between the transistor RMS currents of all converters.

Converter / Function	BDC	HBDC-C	HBDC-L	HBDC-C/L
$I_{T,RMS}$	$\cong \sqrt{D} \cdot I_{out}$	$\cong \sqrt{D} \cdot I_{out}$	$\cong \dfrac{\sqrt{D}}{2-D} \cdot I_{out}$	$\cong \dfrac{\sqrt{D}}{2-D} \cdot I_{out}$

Fig. 5.18 and Fig. 5.19 summarize graphically the boundary operation mode of the converters at V_{in}=ct. and at V_{out}=ct. respectively.

Fig. 5.18 presents the p.u. average inductor current (relative to $I_{L,lim,max}$), for all converters, at BCM, as a function of the voltage conversion ratio, when V_{in}=constant.

Table 5.9 present the expression of the average inductor current for all converters, at BCM, when V_{in}=constant.

TABLE 5.9. Synthetic comparison between average inductor current for all converters.

Converter / Function	$I_{L,lim}$
BDC	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_s} \cdot D \cdot (1-D)$
HBDC-C	$\dfrac{V_{in}}{2 \cdot L_{out} \cdot f_S} \cdot D \cdot \left(\dfrac{1-D}{2-D}\right)$
HBDC-L	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_S} \cdot D \cdot \left(\dfrac{1-D}{2-D}\right)$
HBDC-C/L	$\dfrac{V_{in}}{2 \cdot L_1 \cdot f_S} \cdot D \cdot \left(\dfrac{1-D}{2-D}\right)$

If V_{in}=constant, in the range of voltage conversion ratio V_{out}/V_{in} <0.45, where HBDC-C and HBDC-L are normally used, they reach discontinuous current mode at lower output currents than BDC.

If the voltage conversion ratio is smaller than 0.45, HBDC-C enters DCM at a higher ratio of $I_{L,lim}/I_{L,lim,max}$. According to Table 5.2 the ratio between $I_{L,lim,max}$

values of BDC and HBDC-C is 11.66/8=1.4575. Considering this, it is clear that the absolute value of I_{out} at BCM is smaller for HBDC-C for any V_{out}/V_{in}.

HBDC-C and HBDC-L boundary conditions are better. If the converter (HBDC-C or HBDC-L) has to operate in CCM or at BCM, at the same output current as BDC a lower output inductance is needed for the converter.

From Fig. 5.18 can be noticed that HBDC-C/L converter reaches discontinuous current mode at smaller output currents than all of the other converters.
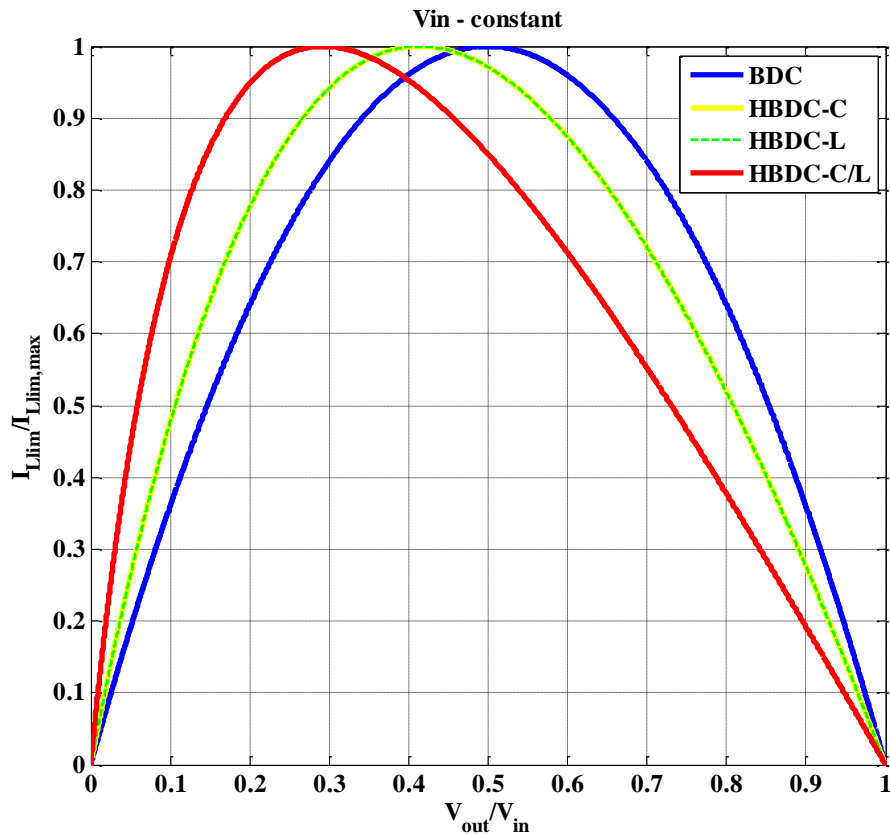
Fig.5.18. P.u. average inductor current for all converters in BCM , at V_{in}=constant.

Fig. 5.19 presents the p.u. average inductor current (relative to $I_{L,lim,max}$), for all converters, at BCM, as a function of the voltage conversion ratio, when V_{out}=constant.

For V_{out}=ct., the values of $I_{L,lim,max}$ for HBDC-C, HBDC-L and BDC are the same as can be seen in Table 5.10 and in this condition Fig. 5.25 shows clearly that HBDC-C and HBDC-L enters DCM at a lower output current.

Table 5.10 present the expression of the average inductor current for all converters, at BCM, when V_{out}=constant.
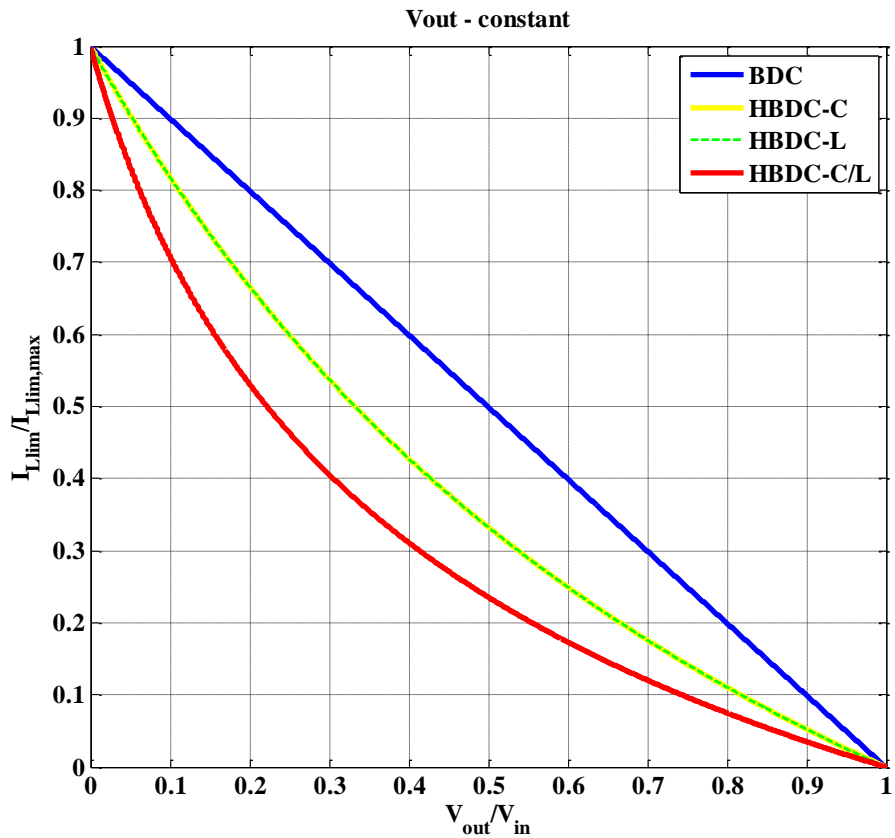
Fig.5.19. P.u. average inductor current for all converters in BCM, at V_{out}=constant.

TABLE 5.10. Synthetic comparison between average inductor current for all converters.

Function Converter	$I_{L,lim}$
BDC	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_s} \cdot (1 - D)$
HBDC-C	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_S} \cdot (1 - D)$
HBDC-L	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D)$
HBDC-C/L	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_s} \cdot (1 - D)$

From Table 5.10 can be seen that the expression for the average inductor current in BCM of the HBDC-C/L converter is the same as for the other converters.

Fig. 5.19 shows that HBDC-C/L converter enters in DCM at a lower load current than all converters.

Fig. 5.20 presents the p.u. maximum transistor current (relative to the output current) for all the converters, at V_{out}=ct., as a function of voltage conversion ratio.
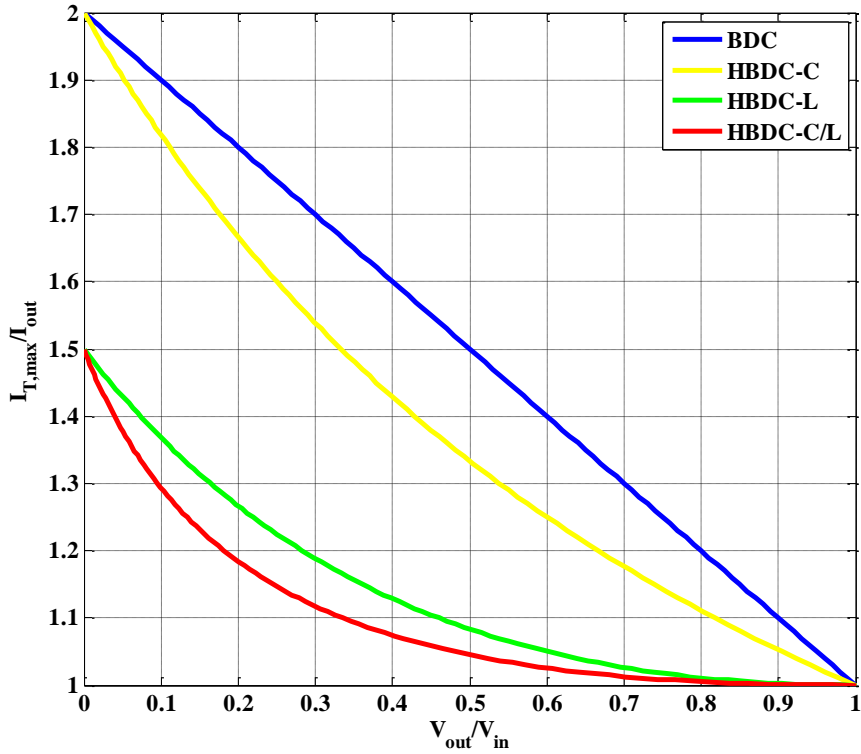
Fig.5.20. P.u. maximum transistor current for all converters, as a function of V_{out}/V_{in}.

TABLE 5.11. Synthetic comparison between maximum transistor current for all converters.

Converter / Function	$I_{T,max}$
BDC	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_S} \cdot (1 - D) + I_{out}$
HBDC-C	$\dfrac{V_{out}}{2 \cdot L_{out} \cdot f_S} \cdot (1 - D) + I_{out}$
HBDC-L	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_S} \cdot (1 - D) + \dfrac{I_{out}}{2 - D}$
HBDC-C/L	$\dfrac{V_{out}}{2 \cdot L_1 \cdot f_S} \cdot (1 - D) + \dfrac{I_{out}}{2 - D}$

Fig. 5.20 presents the comparison between the p.u. values of $\hat{I}_T$ for $I_{out}=I_{Lout,lim.max}$, when V_{out}=constant.

HBDC-C has a lower peak transistor current than BDC for any V_{out}/V_{in}, but the difference between the two converters is only in the range of several percent (the maximum difference is lightly higher 10 %). For V_{out}/V_{in}=0.1 the difference between the two p.u. peak values is about 0.4%.

The peak transistor current is lower for HBDC-C with positive effects regarding the switching device.

In Fig. 5.20, for V_{out}=constant, and $0<V_{out}/V_{in}<0.6$ the peak transistor current of HBDC-L is at least 25% smaller than that of BDC.

Because of the difference in peak values and in inductance values (which are different if V_{in}=constant) of the converters, it is possible that the two inductors of HBDC-L together are not more expensive than the BDC inductor.

The peak value of HBDC-L transistor current, at low values of conversion ratio, is much smaller.

If V_{in}/V_{out} is between 10 and 20, the current stress of the BDC transistor is 41,7% to 46,7% higher for HBDC-C/L converter.

Considering that the peak output inductor current for both converters is the same as the peak transistor current, we expect that the cost of the two HBDC-C/L output inductors together could be close to that of the BDC output inductor.

It can be seen, from Table 5.11, that the expression for the maximum transistor current for BDC and HBDC-C are the same also for HBDC-L and HBDC-C/L are the same.

In Fig. 5.21 a comparative evaluation, in percent, of converters components price is represented.
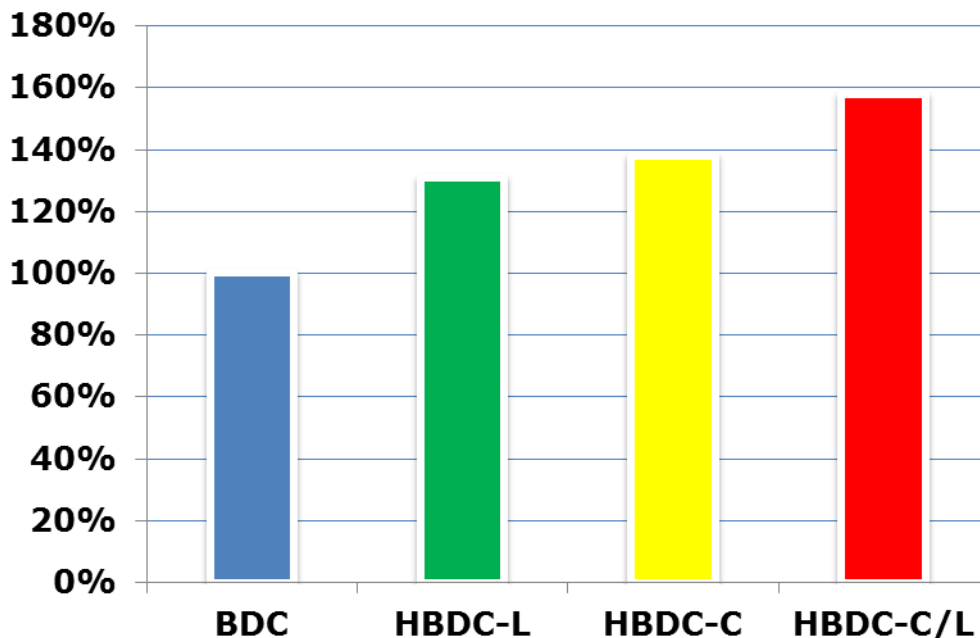
Fig.5.21. Relative price of converters given in percent.

If all four converters: BDC, HBDC-L, HBDC-C and HBDC-C/L would be designed to work at the same input and output power, the price differences would be given by electronic components, heat sinks, PCB size and complexity, dimensions etc.

Because of the fact that these DC-DC converters are not series products the prices are given percent. The prices for the converters were calculated considering the components prices of the prototypes built. Considering the BDC converter the upper price limit (100%) it can be seen form Fig. 5.21 the percentage variation above this upper limit.

The relative price of the BDC converter is exceeded with 31 % by the HBDC-L converter, 38 % by the HBDC-C converter and 58 % by the HBDC-C/L converter.

From this small relative analysis could be concluded that the price variations are no higher than half or a third of the cost considered the upper price limit (of the cheapest converter configuration).

5.6. Conclusion

A comparative study of a HBDC-C, a HBDC-L and a HBDC-C/L converter, in CCM and BCM, with the BDC converter and between all of the converters was made.

Every hybrid Buck DC-DC converter was compared with the BDC converter in order to highlight the advantages and disadvantages of the studied converters.

Equations for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor current are presented synthetically in Table 5.7 – 5.11 and discussed. Some of these equations are general, while others have a form which depends on whether V_{in} or V_{out} is kept constant.

A subchapter is dedicated to a comparative evaluation of all the converters, including the BDC converter, where the differences between them are presented and discussed.

Using visual representations, different characteristics of the compared converters, were presented and discussed.

Visual representations of the duty cycle, p.u. transistor RMS current, p.u. average inductor current, p.u. peak inductor current as a function of the voltage conversion ratio, for constant input or output voltage, were presented in order to highlight the advantages, disadvantages and gains between the converters.

A relative price (components cost), of all the converters, is presented. If all four converters would be designed to work at the same input and output power, the price differences would be given by electronic components, heat sinks, PCB size and complexity, dimensions etc..

From the relative price analysis could be concluded that the price variation is no higher than 50% or 33% of the cost considered the upper price limit (of the cheapest converter configuration, BDC).

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6. HYBRID BUCK DC-DC CONVERTERS APPLICATIONS

6.1. Introduction

Renewable energies like wind power and solar are the most common energy sources nowadays. If in the past, the renewable energy sources were limited by technological short comings and high costs, in our days, because the efficiency and reliability of photovoltaic panels and wind generators have been improved, the costs have been lowered and the equipment started to be used.

Because most of the time the wind and PV sources are complementary and each by themselves cannot supply a system because they depend on the weather condition, wind – PV hybrid systems with high reliability for continuous power distribution (especially for off-grid applications) have been developed [6.1 – 6.10].

Reviews of the main multi-input DC-DC converters and systems presented in the literature highlight the benefits of these hybrid systems [6.11]. New dual-input DC-DC converter topologies based on hybrid [6.12-6.17] and classical structures are studied, validated by simulations, designed, developed and integrated in wind, solar or wind-solar mixing energies systems [6.18, 6.19].

Dual voltage (14/42 [V]) automotive power systems have the possibility to convert the energy from the 42 [V] to 14 [V] batteries/busses. When the power flow is unidirectional a BDC structure is used [6.22-6.24].

6.2. HBDC-L in a small, Off-Grid Wind Turbine Application.

The object of this subchapter is to present the laboratory setup, in which the HBDC-L was integrated, and some experimental results [6.13].

The laboratory setup is in fact a real 5 [kW] Wind Turbine System [6.12, 6.20]. The HBDC-L converter is used as an energy interface between the generator and the conversion and storage equipment.

The used wind energy conversion laboratory setup contains:
➢ dSPACE control board;
➢ voltage source inverter with direct torque control;
➢ induction machine with gearbox-wind turbine equivalent;
➢ permanent magnet synchronous generator (PMSG);
➢ 6 diodes bridge rectifier (DB);
➢ HBDC-L;
➢ 63 [F], 126 [V] Maxwell Supercapacitor (SC);
➢ inverter and charge controller;
➢ 4x12 [V]/100 [Ah] batteries;
➢ 3x10 [Ω] three phase resistor, and a 2 [Ω] resistor.
➢ additional equipment (transducers, signal conditioners etc.).

Fig. 6.1 gives a complete image of the laboratory experimental platform. The operating principle of the experimental laboratory setup can be explained using Fig. 6.2.

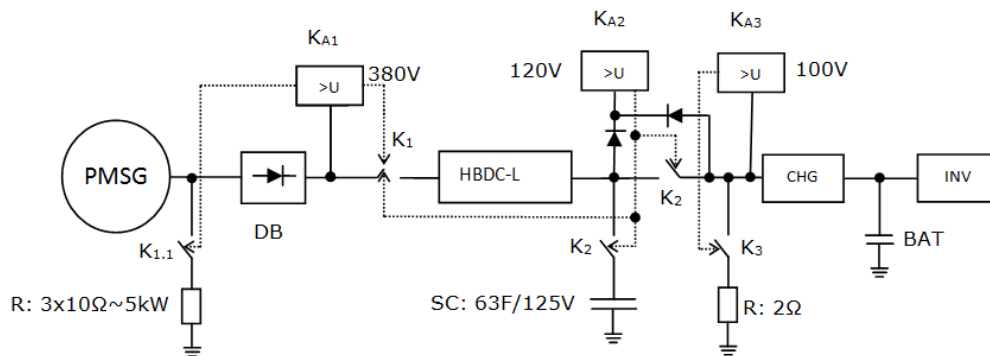Fig.6.1. The complete laboratory setup.

Fig.6.2. Experimental setup diagram.

The input electric power is provided by a PMSG. Using a six diode bridge rectifier (DB), the 3-phased AC power is rectified.

The rectified voltage is now provided to the HBDC-L converter. Using an overvoltage relay (K_{A1}) the rectified voltage, after the DB, is measured in order not to exceed the upper limit of 380 [V].

The energy taken from the input source is now stepped down and a Xantrex Solar Charge Controller (CHG) uses the energy to charge the battery bank (BAT).

The experimental setup also contains a Xantrex Inverter/Charger-XW6048 (INV) which is used to supply the loads.

Xantrex Inverter/Charger-XW6048 can interface with the grid, supply the loads and charge the battery bank from the grid, if a grid connection is available. In off-grid situation the Xantrex Inverter/Charger-XW6048 is used to supply the loads from the energy stored in the battery bank.

The supercapacitor (SC) is used as a bumper with the ability to handle high instantaneous power values.

If the input voltage is in the range of 120-380 [V], the HBDC-L converter starts operating. The Xantrex Solar Charge Controller (CHG) takes the output power of HBDC-L converter and charges the battery bank. The Xantrex Inverter/Charger-XW6048 uses the energy stored in the battery bank to feed the loads.

If the voltage across the supercapacitor (or at the input of the Xantrex Solar Charge Controller) rises above the upper limit 100 [V], measured with K_{A3} overvoltage relay, a 2 [Ω] resistor is inserted in the circuit. The resistor is used in order to reduce the voltage across the supercapacitor (to a 60 [V] limit) and can be replaced in a real life application with a water heat system, for example.

It has to be mentioned that the overvoltage relays K_{A1}, K_{A2}, and K_{A3} are with hysteresis. The 2 [Ω] load will be inserted in the circuit each time the voltage across the SC will raise above 100 [V] and will be take out the circuit when the voltage across the SC will be 60 [V].

K_{A2} overvoltage relay also measures the voltage across the supercapacitor (SC). If the upper limit of 120 [V] across the SC is reached K_{A2} commands the contactors K_1 and K_2 to disconnect the SC from the circuit, disconnect the charging, inverting and battery storage side from the HBDC-L converter and the input voltage (after the DB). In fact K_{A2} overvoltage relay order the disconnection of the HBDC-L from the rest of the power circuit.

During HBDC-L normal operation, if the input power would start to rise, the control strategy of the system would try to obtain the maximum power from the source. If the input voltage, measured with relay K_{A1}, exceeds 380 [V] the control strategy of the system will try to manage the big input power by inserting a 3·10 [Ω] ≈ 5 [kW], resistor. If the voltage across the SC is rising above 100 [V] the control strategy of the system will insert the, 2 [Ω], resistor in the circuit in order to drop down the voltage across the SC. If K_{A2} detects a voltage across the capacitor equal with 120 [V], the HBDC-L is disconnected from the rest of the power circuit. In this moment the output power of the generator is consumed by the 3·10 [Ω] resistor and when the input voltage, measured by K_{A1}, of the HBDC-L converter drops under 380 [V] the system starts operating again.

6.2.1. Experimental setup description

1. dSPACE Control Board

DS1104 R&D Controller Board is a standard board that can be plugged into a PCI slot or a PC. It is specially designed for the development of high-speed multivariable digital controllers and real-time simulations in various fields. For advance I/O purposes, the board includes a slave-DSP subsystem based on the TMS320F240 DSP microcontroller. For rapid control prototyping (RCP), specific interface connector panels provide easy access to all input and output signals on the board. Thus, the DS1103 R&D Controller Board is the ideal hardware for the dSPACE Prototyper development system for cost-sensitive RCP applications [6.25].

Specific interface connector panels, provides easy-to-use connections between the DS1104 R&D Controller Board and devices to be connected to it. Devices can be individually connected, disconnected or interchanged without soldering via BNC connectors and Sub-D connectors. This simplifies system construction, testing and troubleshooting. The Connector/Led Combi Panel provides an array of LEDs indicating the states of the digital signals [6.25].

Real-Time Interface (RTI) provides Simulink® blocks for graphical I/O configuration. It is easy to run function models on the DS1104 R&D Controller Board. All I/O can be configured graphically by inserting the blocks into a Simulink block diagram, and generate the model code via Simulink Coder® (formerly Real-Time Workshop®). The real-time model is compiled, downloaded, and started automatically. This reduces the implementation time to a minimum [6.26].
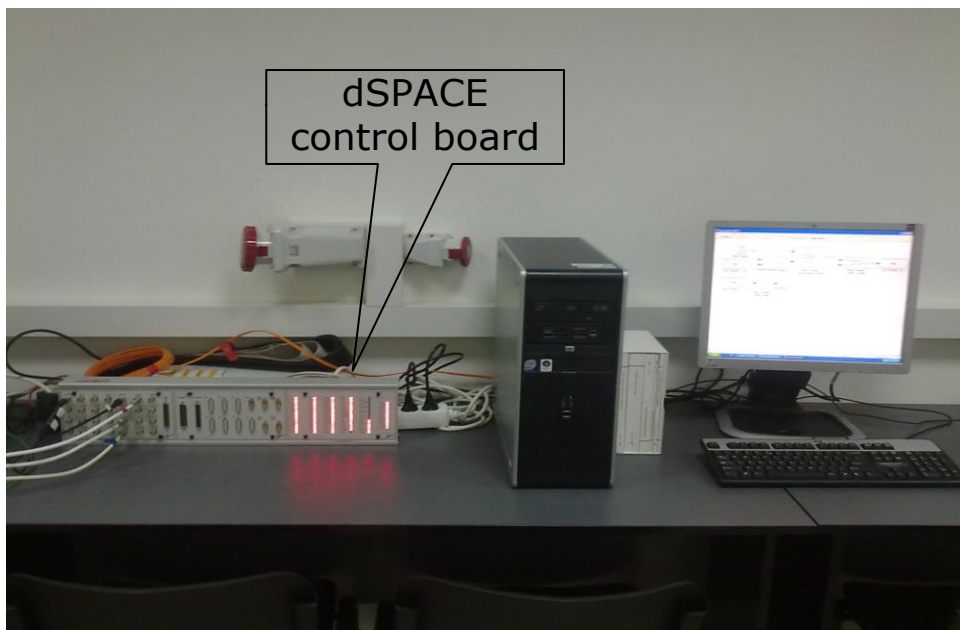
Fig.6.3. DS1104 R&D Controller Board.

4 BNC Connectors from the DS1104 R&D Controller Board have been used (Fig.6.3), 3 for input (estimated) signals and 1 for output (prescribed) signals. Also a digital I/O Connector was used in order to open/close 2 relays, which transmit commands to HBDC L-sw: Run/Stop and Reset.

The experiment interface was designed with Control Desk ® software (Fig. 6.4), which is suitable for real-time and Simulink experiments. The interface enables changing parameter values interactively with input instruments, changing data connections, observing signals with data acquisition instruments, capturing data and saving the results to disk. Multiple data acquisitions can be synchronized to the global time, defined relative to the start of Control Desk's animation mode.
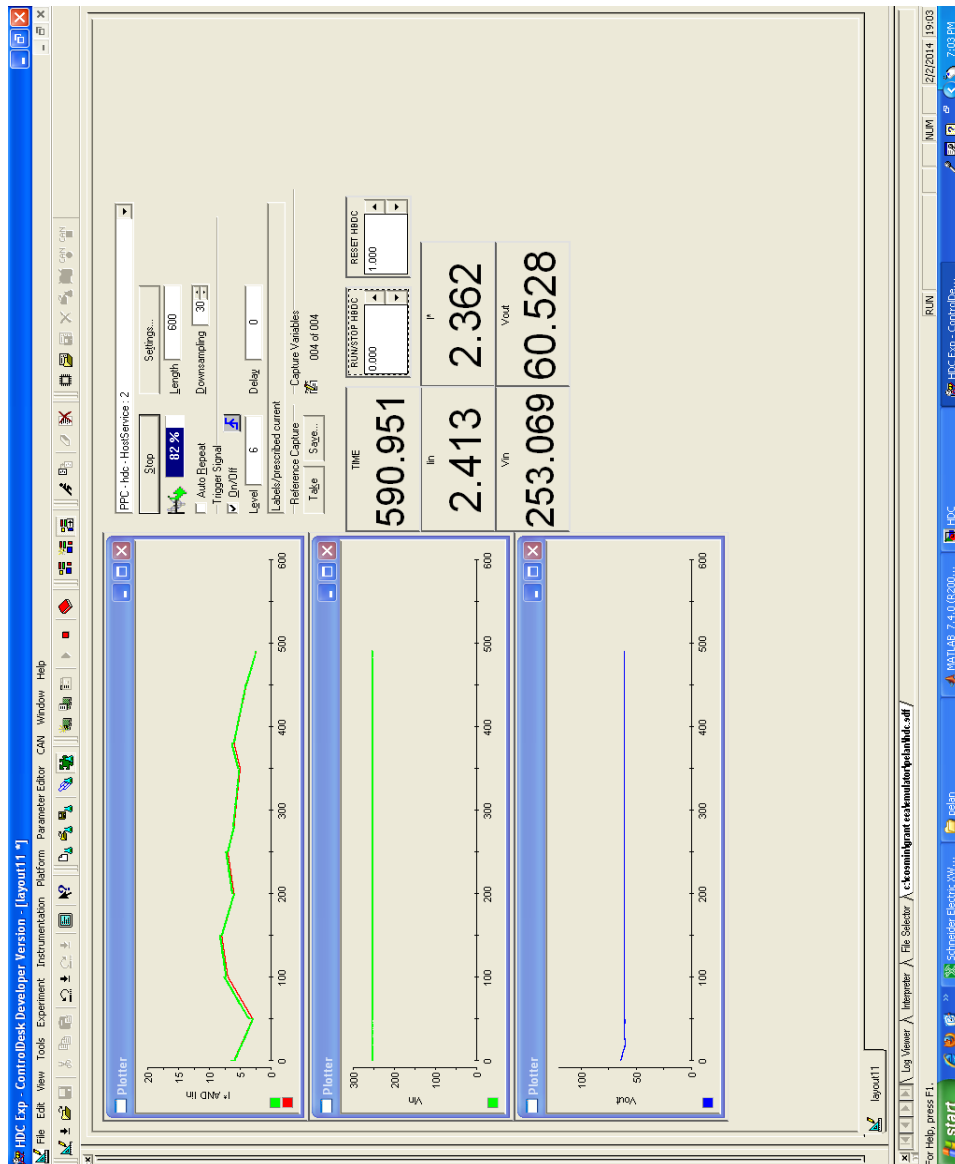
Fig.6.4. Control Desk experiment interface.

2. Hybrid Buck Switched-Inductor DC-DC Converter

The specifications of the HBDC-L are:

➢ Rated power, P=5 [kW];
➢ Input rectified voltage, V_{rect}=120-400 [V];
➢ Output voltage, V_{SC}=(0-)50-120 [V];
➢ Inductors, L_1=L_2=200 [µH];
➢ Switching frequency, f_s=10 [kHz];

Taking into account the complete analysis and design procedure described in Chapter 2 and the HBDC-L converter used in this application, the real design procedure of the HBDC-L converter will be shortly presented below.

Considering the application for which HBDC-L converter was designed, for a small, Off-Grid Wind Turbine Application, the input voltage range was determined using PMSG data and the shaft speed operating range of interest. The output voltage high limit was chosen to be slightly less than the maximum voltage of the supercapacitors which is 130 [V].

The maximum input current, $I_{in,max}$ is the DC current at the output of the diode bridge, which rectifies the current of the PMSG, if the PMSG is operating at nominal current which is 12 [A].

The maximum input power of 5 [kW] is exceeded if the input voltage of the converter is 400 [V] and the input current is 17 [A]. This situation can be accepted for short periods of time if the PMSG is designed to be able to give this power. In normal continuous operation the input current of the converter can be set to maximum 12.5 [A] if the input voltage is 400 [V].

The first step in the design of the HBDC-L is choosing the switching frequency, f_s. We consider a frequency of 10 [kHz] limited by the IGBT transistor data sheet.

The switching period is given by equation (6.1):

$$T_S = \frac{1}{f_s} = \frac{1}{10.10^3} = 100 [\mu s] \tag{6.1}$$

The worst case in regards to the maximum current through the transistor is when the input voltage is $V_{in,max}$= 400 [V] and the output voltage is $V_{out,min}$= 50 [V].

The duty factor is given by equation (6.2):

$$D = \frac{t_{on}}{T} = \frac{2 \cdot V_{out}}{V_{in} + V_{out}} = \frac{2 \cdot 50}{400 + 50} = 0.22 \tag{6.2}$$

Two situations will be presented: in the first one the input current is allowed to reach the maximum value $I_{in,max}$= 17 [A], in the second one it is limited by the maximum power.

A.   If $I_{in,max}$= 17 [A], the electrical power which is taken from the wind turbine for short time is $P_{in,peak}$= 6.8 [kW]. The mean transistor current for the time interval t_{on}, when the transistor is opened can be calculated using equation (6.3).

$$I_{T,on} = \frac{I_{in,max}}{D} = \frac{17}{0.22} = 77.27 [A] \tag{6.3}$$

We chose the current ripple ΔI as 25% from $I_{T,on}$. The inductors value is determined from equation (6.4).

$$\Delta I_L = I_{L,max} - I_{L,min} = \frac{V_{in} - V_{out}}{2 \cdot L} \cdot D \cdot T_S \tag{6.4}$$

$$L = \frac{V_{in} - V_{out}}{2 \cdot \Delta I_L} \cdot D \cdot T_S = \frac{400 - 50}{2 \cdot \frac{25}{100} \cdot 77.27} \cdot 100 \cdot 10^{-6} \cdot 0.22 = 199[\mu H] \tag{6.5}$$

The value obtained is very close to 200 [μH], so two inductors of 200 [μH] each will be used.

We can calculate the average minimum and maximum values of the inductor current.

$$I_L = \frac{I_{in,max}}{D} = \frac{17}{0.22} = 77.27[A] \tag{6.6}$$

$$i_{L,min} = \frac{I_{in,max}}{D} - \frac{V_{in,max} - V_{out,min}}{4 \cdot L} \cdot D \cdot T = $$
$$= \frac{17}{0.22} - \frac{400 - 50}{4 \cdot 200 \cdot 10^{-6}} \cdot 100 \cdot 10^{-6} \cdot 0.22 = 67.65[A] \tag{6.7}$$

$$I_{L,max} = \frac{I_{in,max}}{D} - \frac{V_{in,max} - V_{out,min}}{4 \cdot L} \cdot D \cdot T_S = 86.89[A] \tag{6.8}$$

The maximum transistor current is equal to $I_{L,max}$.

$$I_{T,max} = 86.89[A] \tag{6.9}$$

The mean transistor current, which is also of interest when choosing the transistor, is always equal to the input current:

$$I_T = I_{in,max} = 17[A] \tag{6.10}$$

The maximum voltage which appears across the transistor when it is not in conduction is:

$$V_T = V_{in,max} + V_{out,max} = 400 + 125 = 525[V] \tag{6.11}$$

The mean current of each diode is given by the following equation:

$$I_D = \frac{I_{in,max}}{D} \cdot (1 - D) = \frac{17}{0.22} \cdot (1 - 0.22) = 60.27[A] \tag{6.12}$$

The maximum current is:

$$I_{D,max} = I_{T,max} = 86.89[A] \tag{6.13}$$

The maximum reverse voltage across a diode appears when the input and output voltage have the maximum value.

$$V_{D,max} = \frac{V_{in,max} + V_{out,max}}{2} = 262.5[V] \tag{6.14}$$

B.   If the input current is limited by the maximum input power its value at an input voltage of 400 [V] is:

$$I_{in} = \frac{P_{in,max}}{V_{in,max}} = \frac{5000}{400} = 12.5[A] \tag{6.15}$$

In this case the main values are given bellow:

$$T_s = \frac{1}{f_s} = 100[\mu s] \tag{6.16}$$

$$D = \frac{2 \cdot V_{out}}{V_{in} + V_{out}} = 0.22 \tag{6.17}$$

$$I_{T,on} = \frac{I_{in,max}}{D} = \frac{12.5}{0.22} = 56.81[A] \tag{6.18}$$

$$L = 200[\mu H] \tag{6.19}$$

$$I_L = \frac{I_{in,max}}{D} = 56.81[A] \tag{6.20}$$

$$i_{L,min} = \frac{I_{in}}{D} - \frac{V_{in,max} - V_{out,min}}{4 \cdot L} \cdot D \cdot T_s =$$
$$= \frac{12.5}{0.22} - \frac{400 - 50}{4 \cdot 200 \cdot 10^{-6}} \cdot 100 \cdot 10^{-6} \cdot 0.22 = 47.18[A] \tag{6.21}$$

$$I_{L,max} = \frac{I_{in,max}}{D} - \frac{V_{in,max} - V_{out,min}}{4 \cdot L} \cdot D \cdot T_s = 66.43[A] \tag{6.22}$$

$$I_{T,max} = 66.43[A] \tag{6.22}$$

$$I_T = I_{in} = 12.5[A] \tag{6.23}$$

$$V_T = V_{in,max} + V_{out,max} = 400 + 125 = 525[V] \tag{6.24}$$

$$I_D = \frac{I_{in}}{D} \cdot (1 - D) = \frac{12.5}{0.22} \cdot (1 - 0.22) = 44.31[A] \tag{6.25}$$

$$I_{D,max} = I_{T,max} = 66.43[A] \tag{6.26}$$

$$V_{D,max} = \frac{V_{in,max} + V_{out,max}}{2} = 262.5[V] \tag{6.27}$$

In Fig.6.5 is presented the control HBDC-L characteristic (the reference voltage for a specific reference current). HBDC-L converter is presented in Fig.6.6.
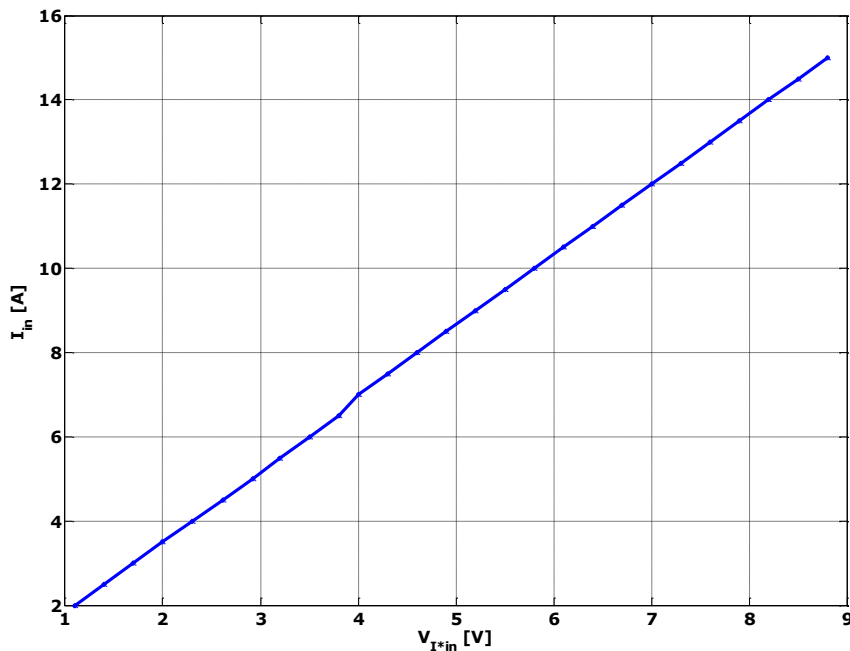
Fig.6.5. HBDC-L converter control characteristic.

3. Supercapacitor

Maxwell Technologies' 125 [V] Heavy Transportation series of supercapacitor modules (Fig.6.7) is a high performance energy storage product line for hybrid buses, trucks, trolleys, light rail, mining, construction and seaport cranes. Each model incorporates balancing, monitoring and thermal management capabilities to ensure industry-leading charge/discharge performance, high reliability and long operational life [6.27].

Features:
➢ Over 1 million charge/discharge cycles;
➢ IP 65 environmental protection;
➢ Operating temperature -40 [°C] to +65 [°C];
➢ CAN bus digital monitoring and communications;

➢ Highest power performance available;
➢ Temperature and voltage monitoring;
➢ Series connection up to 1500 [V].
    Benefits:
➢ Highest performance hybrid power systems;
➢ Survive in nearly any weather/environmental conditions;
➢ All in one solution with digital monitoring and built-in forced air cooling;
➢ Digital feedback enables optimized hybrid control algorithms.
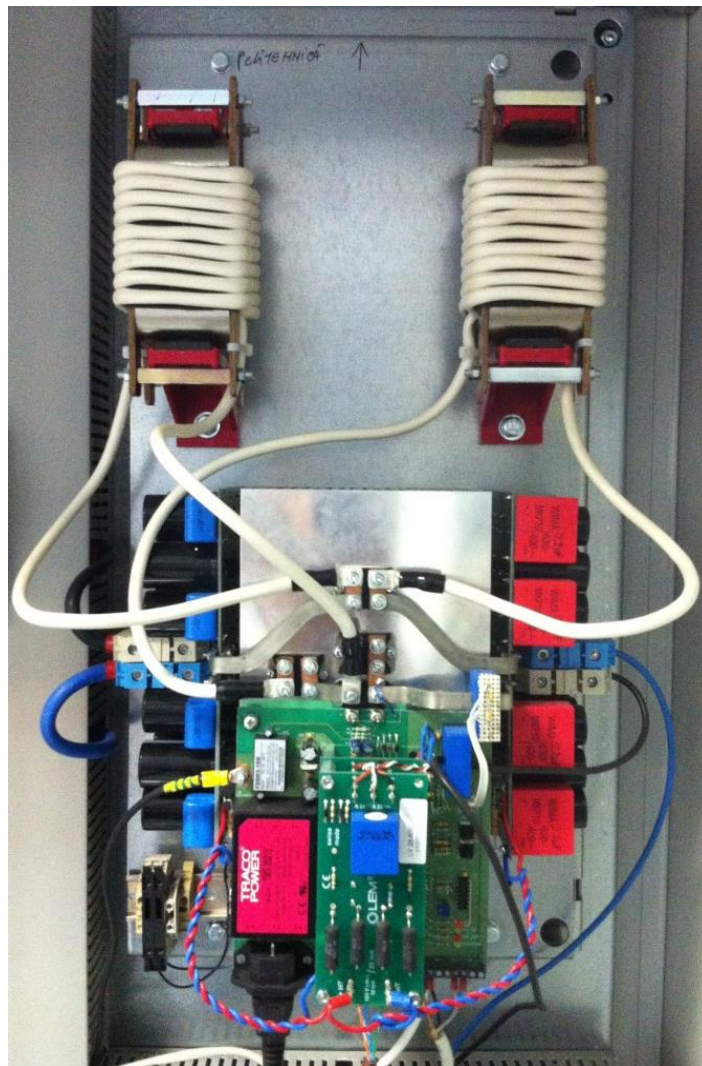
Fig.6.6. HBDC-L industrial prototype.

Fig.6.7. Maxwell SC.

4. Charge Controller with Inverter and Batteries

The inverter used in the proposed WECS was chosen to be a 6 [kW] Xantrex Inverter/Charger XW6048 (Fig.6.8). XW Inverter/Charger is one of the finest inverter/charges on the market today, incorporating state-of-the-art technology, high reliability and convenient control feature [6.28].

XW Inverter/Charger electrical specifications [6.28]:
- Continuous output power, 6000 [W];
- Surge rating, 12000 [W];
- Surge current, 53 [A_{rms}];
- Peak efficiency, 95.4%;
- Full load efficiency, 92 %;
- Waveform: true sine wave;
- Idle consumption – invert mode, no load 28 [W];
- Idle consumption – search mode < 7 [W];
- AC output voltage, 230 [V] ±3%;
- AC input voltage range (bypass/charge mode), 165-280 [V];
- AC input frequency range (bypass/charge mode), 45-55 [Hz] (default), 40-68 [Hz] (allowable);
- AC output continuous current, 26.1 [A];
- AC output frequency, 50±0.1 [Hz];
- Total harmonic distortion <5% at rated power;
- Automatic transfer relay, 56 [A];
- Auxiliary relay output 0-12 [V], maximum 250 [mA] DC;

- DC input voltage (nominal), 50.4 [V];
- DC input voltage range, 44-64 [V];
- DC current at nominal power, 131 [A];
- Continuous charge rate at nominal voltage, 100 [A];
- Power factor corrected charging PF (0.99);
- XW Inverter/Charger mechanical specifications:
- Supported battery types: flooded (default), gel, AGM, custom;
- Battery bank size, 100-2000 [A];
- Nonvolatile memory;
- System network, Xanbus;
- Enclosure type, IP 20, indoor, unheated;
- Rated temperature range, 0-40 [°C];
- Operational temperature range, -25-70 [°C];
- Storage temperature range, -40-85 [°C];
- Inverter dimensions, (H x W x D) 580 x 410 x230 [mm];
- Inverter weight, 55.2 [kg].

The inverter/charger operation can be monitored with the Inverter Information Panel, which displays basic information or with the System Control Panel, with which the inverter can also be configured. Also the batteries connected to the system can be monitored with the two panels [6.29].

Xantrex Solar Charge Controller (Fig.6.8) is a photovoltaic (PV) charge controller that tracks the maximum power point of a PV array to deliver the maximum available current for charging the batteries. The charge controller can be used with 12-, 24-, 36-, 48- and 60-volt DC battery system. The solar charge controller is designed to regulate PV input, but will also work with other DC sources. It can be installed with a Xantrex Inverter/Charger or in stand-alone installation [6.30].

Standard features [6.30]:
- Two or three stage charging process, with manual equalization to maximize system performance and maintain expected battery life;
- True dynamic Maximum Power Point Tracking to deliver the maximum available power from the DC source to the battery bank;
- Integrated PV Ground Fault Protection;
- 60 Amp Capacity;
- 150 volt open circuit input voltage;
- Input over-voltage and under-voltage protection, output over-current protection and reverse current protection;
- Over temperature protection and power derating when output power and ambient temperature are high;
- Battery temperature sensor to provide automatically temperature compensated battery charging;
- Xanbus-enabled. Xanbus is a network communication protocol developed by Xantrex. The charge controller is able to communicate its settings and activity to other Xanbus-enabled devices, such as the XW Series Inverter/Charger, the XW System Control Panel or other XW Charge Controllers.
- Electrical Specifications:
- Maximum PV Array Voltage (operating): 140 [Vdc];
- Maximum PV Array Open Circuit Voltage: 150 [Vdc];
- Array Short Circuit Current: 60 [Adc] maximum;
- Nominal Battery Voltage: 12, 24, 36, 48, 60 [Vdc];
- Battery Voltage Range (operating): 10 [Vdc] to 80 [Vdc];

➢ Maximum Output Current: 60 [A];
➢ Maximum Output Power: 3500 [W];
➢ Auxiliary Output: 5-13 V, up to 200 [mA];
➢ Tare Loss/Nighttime Power Consumption: 2.5 [W];
➢ Charger regulation mode: Three-stage (bulk, absorption, float), two-stage (bulk, absorption).
➢ Mechanical Specifications:
➢ Dimensions (H x W x D): 368 x 146 x 138 [mm];
➢ Weight: 4.8 [kg].

4 Ritar Valve regulated rechargeable batteries have been chosen with 12V/100AH/10AH specifications (Fig.6.8).
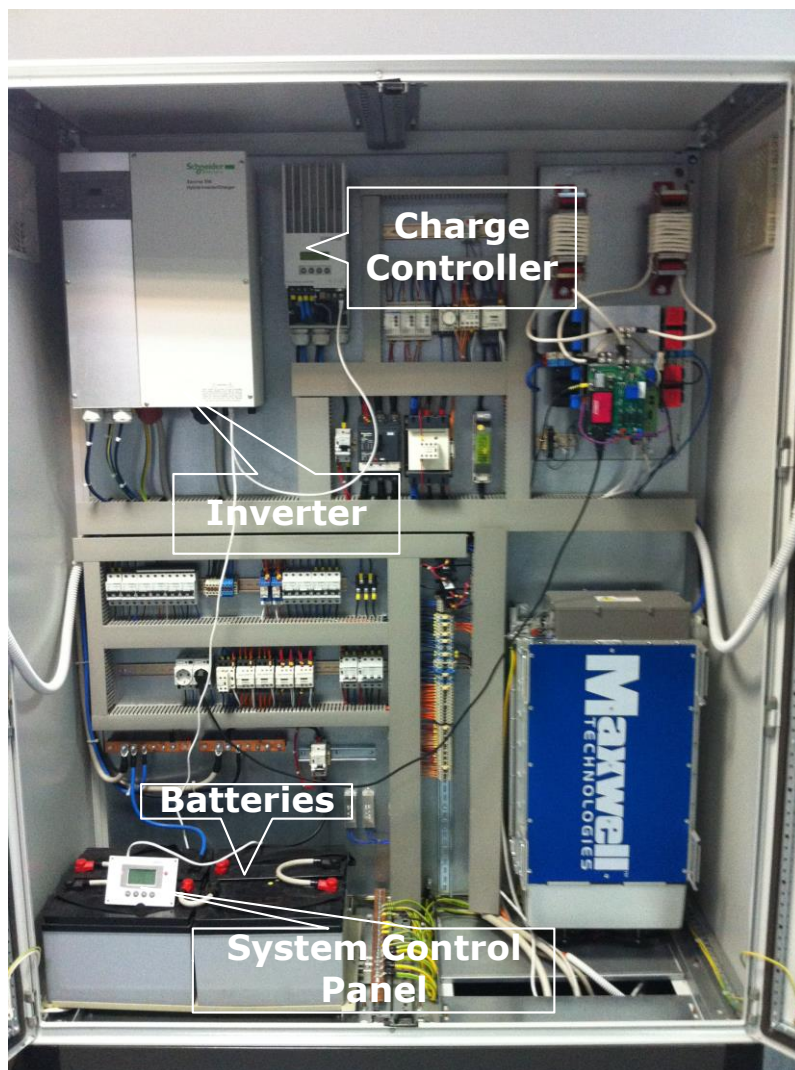
Fig.6.8. Xantrex inverter with charge controller, system control panel and batteries.

6.2.2. Experimental results

In Fig. 6.9 the prescribed current and the input current, of the HBDC-L converter, waveforms are presented. Also the input voltage of the HBDC-L converter and the voltage across the SC are presented.

Fig. 6.9.a presents the operating mode of the HBDC-L converter, when a constant input voltage of 250 [V] is applied to the Wind Turbine system, and when the prescribed HBDC-L current, I*, has a random waveform. From Fig. 6.9 the entire system response can be seen. From the voltage across the SC (Fig. 6.9.c) it can be seen that the input power is used to supply loads and/or to charge the battery bank and the voltage across the SC is maintained to the 60 [V] level, where the control strategy of the system says it should be in normal operating conditions.

Fig.6.9. I* random signal experimental waveforms:
a) HBDC-L converter prescribed and input currents;
b) HBDC-L converter input voltage;
c) voltage across the supercapacitor.

It can be observed the influence of the HBDC-L converter and his power extraction capabilities for a random I*.

Fig. 6.10 presents an experiment where the input voltage is constant and the prescribed HBDC-L converter current has a random shape.

From Fig. 6.10.c it can be seen that the voltage across the SC has an average value of 90 [V] and a triangular waveform. The shape of the waveform is given, as it was presented above in the Wind Turbine system operation mode, by the 2 [Ω] resistor inserted in the circuit (by K_{A3}) to keep the voltage across the supercapacitor at 100 [V] safety level. The connection and disconnection of the 2 [Ω] resistor can be observed also in the waveforms of the prescribed and input currents of the HBDC-L converter as little spikes synchronized with the voltage across the SC. This situation is present if the batteries are fully charged and the inverter is no loaded.

Fig.6.10. I* random signal experimental waveforms:
a) HBDC-L converter prescribed and input currents;
b) HBDC-L converter input voltage;
c) voltage across the supercapacitor.

Fig. 6.11 presents the operating mode of the HBDC-L converter, when a variable input voltage of 250 [V] is applied to the Wind Turbine system, and when the prescribed HBDC-L current, I*, has a random signal waveform. From the voltage across the SC (Fig. 6.11.c) it can be seen that the input power is used to supply loads and/or to charge the battery bank and the voltage across the SC is maintained to the 60 [V] level, where the control strategy of the system says it should be in normal operating conditions.
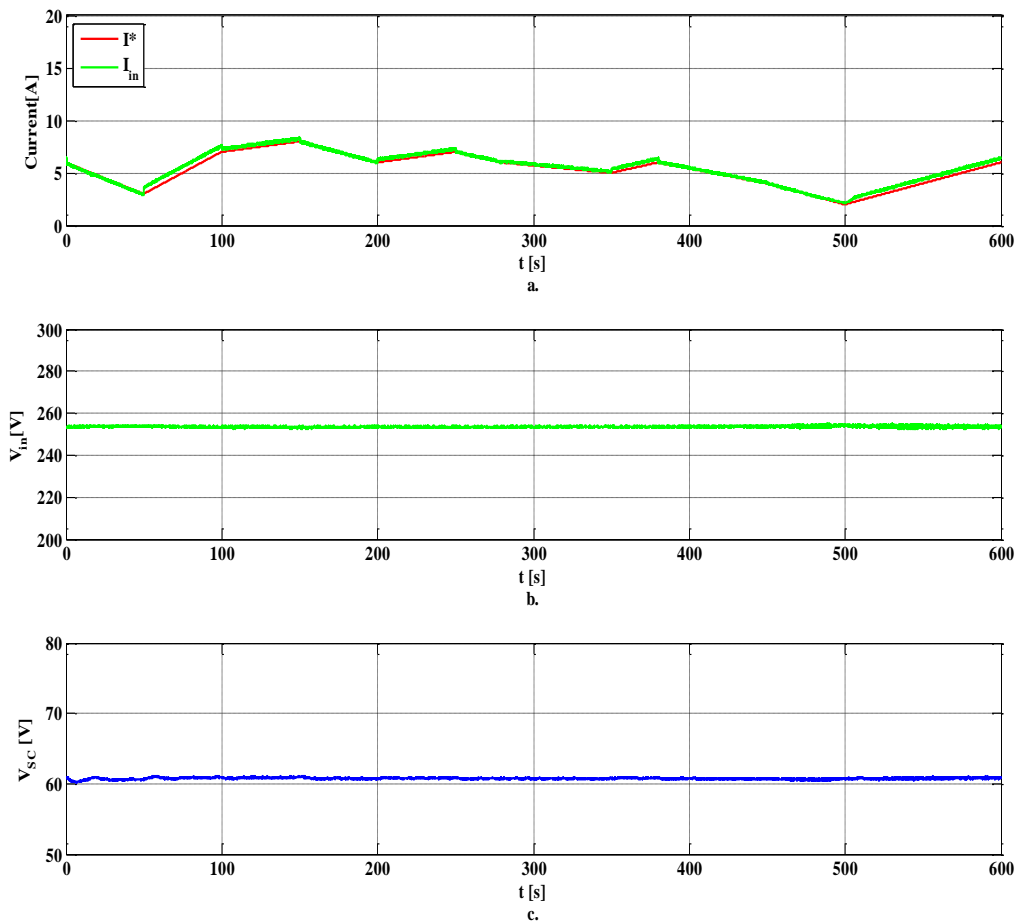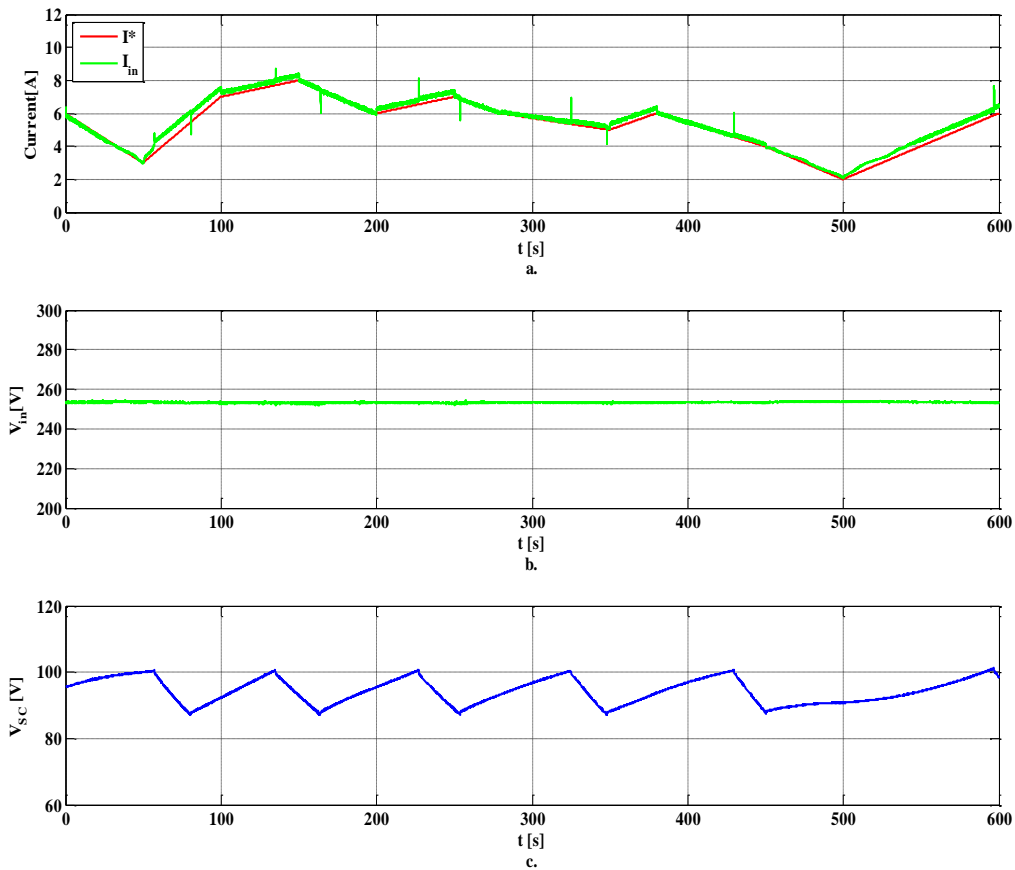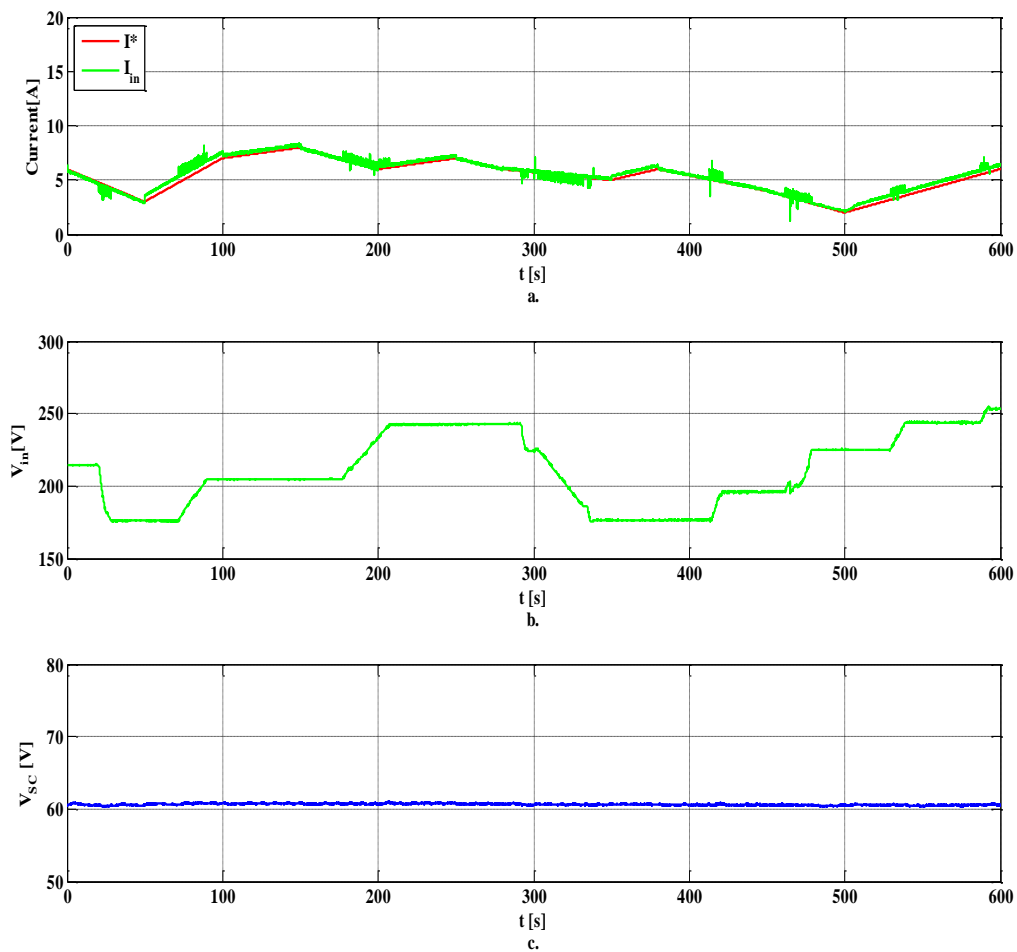

Fig.6.11. I* random signal experimental waveforms:

a) HBDC-L converter prescribed and input currents;

b) HBDC-L converter input voltage;

c) voltage across the supercapacitor.

6.3. HBDC-C in a Dual Voltage Power Automotive System Application

The object of this subchapter is to present the laboratory setup, in which the HBDC-C was integrated, and some experimental results.

The laboratory setup is in fact a dual voltage (42/14 [V]) automotive power system with a HBDC-C converter between the two power busses [6.32].

The used dual voltage automotive power system laboratory setup contains:

➢ dsPIC30F4011 microcontroller;
➢ Regatron TopCon Quadro Power Supply (input voltage source);
➢ HBDC-C;
➢ 1x12 [V]/100 [Ah] Rital Valve regulated rechargeable batteries;
➢ additional equipment (PC, oscilloscope, etc.).

Fig. 6.12 gives a complete image of the laboratory experimental platform.
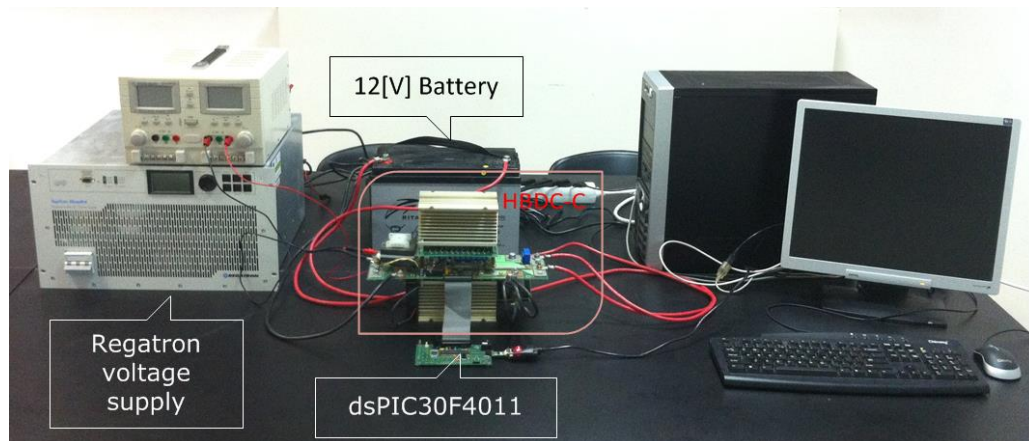
Fig.6.12. HBDC-C experimental setup.

6.3.1. Experimental setup description

1. Regatron TopCon Quadro Power Supply

The development of programmable power supplies with high dynamics allows for new applications in process engineering, testing and laboratory use [6.31].

Power supplies from Regatron (Fig. 6.13) are successfully used for:
➢ Simulation and substitution of real DC sources like:
 - Batteries
 - Solar panels
 - Fuel cell stacks
➢ Supply of:
 - Burn-in- and test-systems

- Plasma loads e.g. surface technology
- Radar modulators (klystron, magnetron)
- Highly dynamic DC applications
- Pulse laser
- Demagnetizing and degaussing systems

Main output specifications:

➢ Output ratings:
- Output power range .... 0 – 10 [kW]
- Output voltage range .... 0 – 400 [Vdc]
- Output current range .... 0 – 31 [A]
- Internal resistance range .... 0 – 1000 [mΩ]
➢ Operating modes
- Voltage regulation (CV) .... 0 – 100 % [U_{max}]
- Current regulation (CC) .... 0 – 100 % [I_{max}]
- Power regulation (CP) .... 5 – 100 % [P_{max}]

Fig.6.13. Regatron TopCon Quadro Power Supply.

2. HBDC-C converter

The specifications of the HBDC-C (Fig. 6.14) are:

➢ Rated power, P=1.5 [kW];
➢ Input voltage, V_{in}=32-50 [V];
➢ Output voltage, V_{out}=12-14 [V];
➢ Input inductor, L_{in}=8 [μH];
➢ Output inductor, L_{out}=6 [μH];
➢ Input capacitors, C_1=C_2=29.92 [μH]
➢ Output capacitor, C_{out}=47.6 [μH]
➢ Switching frequency, f_s=100 [kHz];

Taking into account the complete analysis and design procedure described in Chapter 3, the real design procedure of the HBDC-L converter (presented in this chapter) and the HBDC-C converter used in this application, the real design

procedure of the HBDC-C converter can be done easily. For this reason this design procedure will not be included.
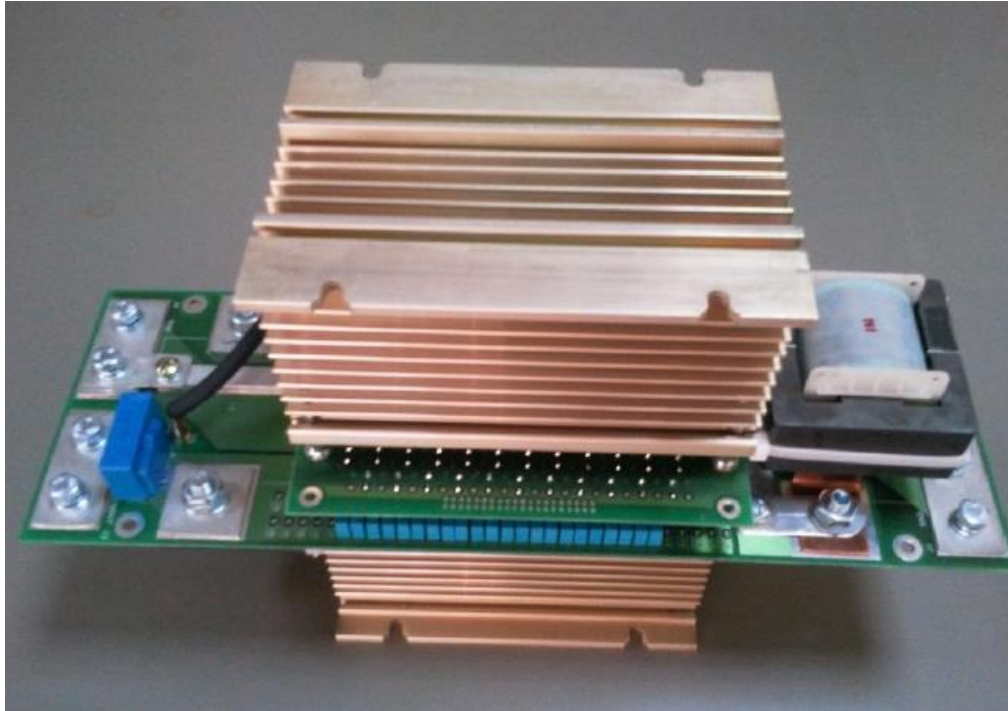
Fig.6.14. HBDC-C prototype.

6.2.2. Experimental results

The experimental setup presents a dual voltage (42/12 [V]) automotive power system (Fig. 6.12). In Fig. 1.3 a diagram similar to the experimental setup is presented.

In the case of conventional cars the traditional 12 [V] bus must supply a substantial number of consumers, number that is tending to grow with automotive technology development leading to large currents. Automotive industry started to investigate the use of busses with larger voltages (48 [V]) for large consumers. In this situation the connection between busses requires a DC-DC converter.

If the input voltage provided by the Regatron voltage supply is considered to be the voltage supplied by the 3~phased alternator through the diode bridge at the input of the HBDC-C which manage the input power to charge a 12 [V]/100 [Ah] battery, the experimental setup is described and presented as a real industry solution [6.22].

Fig. 6.15 presents HBDC-C's experimental waveforms of duty cycle variation, output current (battery charging current) and output voltage (battery voltage).

The experiment was made at a 42 [V] input voltage; the duty cycle was modified during the 19 [s] period of time, presented in Fig. 6.15.a, in order to show

the HBDC-C's capability to charge the 12 [V] battery. The output current (battery charging current) of HBDC-C is presented in Fig. 6.15.b. In Fig. 6.15.c the output voltage, at the terminals of the battery, is presented.
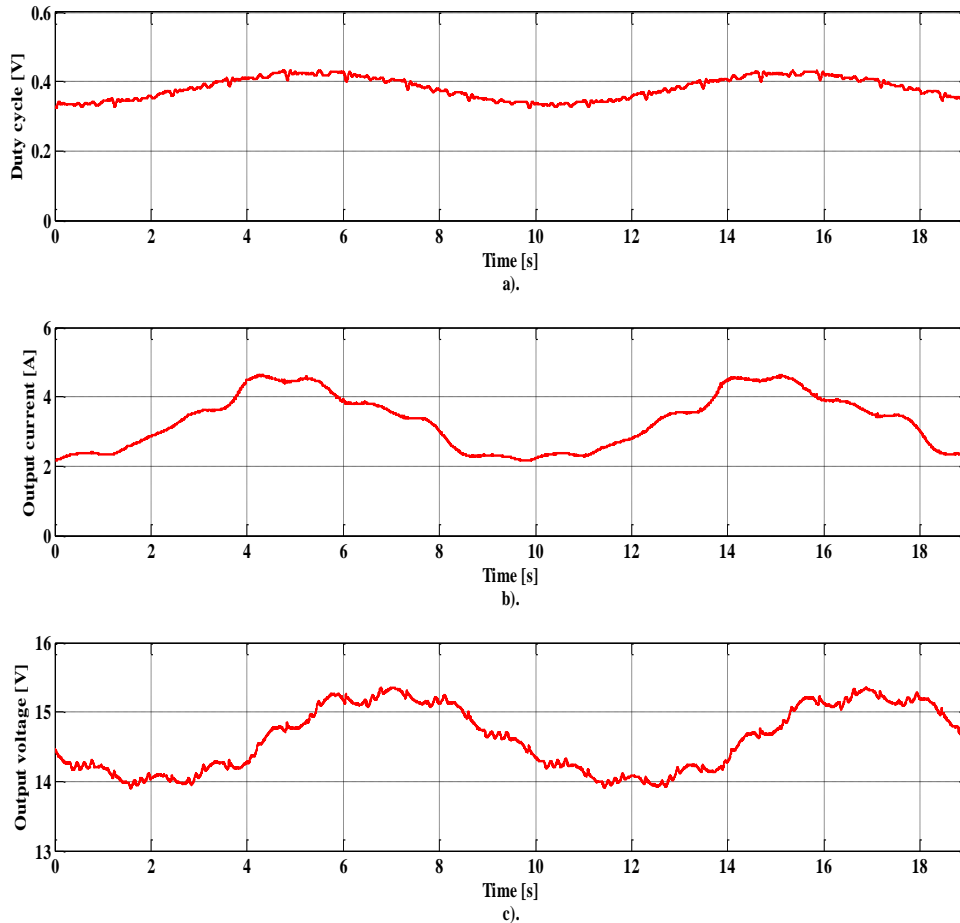
Fig.6.15. HBDC-C experimental waveforms:
a) duty cycle variation; b) charging battery current; c) battery voltage.

6.4. Conclusion

This chapter is dedicated to potential industrial applications of hybrid DC-DC converters. Two systems including HBDC-L and HBDC-C converters have been presented.

The small off-grid Wind Turbine application presents how the HBDC-L converter was designed and integrated in a 5 [kW] Wind Turbine emulator.

The real design procedure and the real values of the HBDC-L converter main components have been presented.

The main components of the experimental setup (Wind Turbine emulator) have been described.

A general description of the experimental setup operating principle was made in order to give a complete image of the presented industrial solution.

Experimental waveforms were presented in order to highlight the power extraction capabilities and influence of the HBDC-L converter in the presented industrial application.

The dual voltage (42/12 [V]) automotive system application presents an industrial HBDC-L converter designed for this purpose.

The experimental setup is presented including a description of the main components and operating principle and by analogy with real situation a complete image of the presented industrial solution is made.

Experimental waveforms were presented in order to validate the application and all the presented theoretical considerations.

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7. CONCLUSION AND CONTRIBUTIONS

7.1. Conclusion

The work presents a research in the field of the DC-DC converters.

After a literature research three Hybrid Buck Step-Down DC-DC converters were studied, simulated, designed, built and integrated in real applications (HBDC-L and HBDC-C).

Starting from the BDC converter and inserting a switched-capacitor and/or a switched-inductor cell in his structure, three Hybrid Buck Step-Down DC-DC converters were developed.

By replacing the inductor and the output diode of the BDC with a switched-inductor cell formed by two inductors and two diodes, the HBDC-L is obtained.

By inserting at the input of the BDC a switched-capacitor cell, formed by two identical capacitors and three diodes, the HBDC-C is obtained. The output voltage of the HBDC-L and HBDC-C converters is reduced (2-D) times than the output voltage of the BDC converter.

For a higher step-down voltage conversion ratio, even higher than the one of the HBDC-L and HBDC-C converters, at the input of the BDC a switched-capacitor cell was inserted and the inductor and the output diode of the BDC were replaced with a switched-inductor cell creating the proposed HBDC-C/L converter. Or can be said that by mixing together the HBDC-C and HBDC-L converters, the HBDC-C/L converter was obtained. The output voltage of the HBDC-C/L is reduced (2-D) times than the output voltage of the HBDC-L and HBDC-C converters and $(2-D)^2$ times more than the output voltage of the BDC.

A full analysis and design procedure of the presented Hybrid Buck Step-Down DC-DC converters was made.

Equations for average, RMS and peak transistor current, transistor voltage stress, output capacitor ripple, average value of input, output and inductor current are presented and discussed. Some of these equations are general, while others have a form which depends on whether the input or the output voltage is kept constant.

The main current and voltage, simulation and experimental waveforms were presented, discussed and compared.

One configurable laboratory model and three real prototypes were built. For the comparison between the experimental waveforms of the Hybrid Buck Step-Down DC-DC converters, built for this purpose, and the simulation waveforms, obtained with PSim program, models with realistic electronic components were used.

All the simulation waveforms of HBDC converters are in good agreement with the experimental waveforms confirming the theoretical description.

Every Hybrid Buck DC-DC converter was compared with the BDC in order to highlight the advantages and disadvantages of the studied converters.

A subchapter is dedicated to a comparative evaluation of all the converters, where the differences between them are presented and discussed.

A relative price (given in percent), of all converters components, is presented. From the price analysis could be concluded that the price variation,

between all the converters, is no higher than 50% or 33% of the cost considered the upper price limit (of the cheapest converter configuration, BDC).

Two industrial applications for renewable energy and automotive systems have been presented. A general description of each experimental setup operating principles was made in order to give a complete image of the presented industrial solutions.

The small off-grid Wind Turbine application presents how the HBDC-L converter was designed and integrated in a real 5 [kW] Wind Turbine System.

The Dual Voltage (42/12 [V]) Automotive System application presents an industrial HBDC-L converter designed for this purpose.

Both applications and theoretical considerations are sustained by experimental results.

7.2. Contribution

The author contributions in this work can be summarized as follows:
- ➢ a general overview of the main DC-DC converters topologies;
- ➢ three hybrid step-down converters were analytically studied, designed and validated through digital simulations made in Psim;
- ➢ one configurable laboratory model and three industrial prototypes were built in order to validate the theoretical considerations;
- ➢ a comparative evaluation of the presented Hybrid Buck Step-Down DC-DC converters was made;
- ➢ preliminary experimental results obtained for each converter in the proposed applications.
- ➢ five papers in international conferences (ACEMP - Electromotion 2011 - TURKEY, OPTIM 2012 - ROMANIA, SPEEDAM 2012 - ITALY , EPE-PEMC 2012 ECCE Europe - SERBIA, ECCE 2013 - USA).

7.3. Future Work

Future work related to the thesis subject could follow the next research direction:
- experimental validation and comparison of the converter efficiencies;
- the implementation of control strategies for each industrial application;
- the integration of the presented converters in other industry applications.

AUTHOR PAPERS RELATED TO THE THESIS

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[5].▪ O. Pelan, N. Muntean, O. Cornea, "Comparative Evaluation of Buck and Switched-Capacitor Hybrid Buck DC-DC Converters", SPEEDAM 2012 - International Symposium on Power Electronics, Electrical Drives, Automation and Motion, Sorrento, Italy, June 2012, pp 1330-1335.

[6].▪ N. Muntean, O. Cornea, O. Pelan, C. Lascu, "Comparative Evaluation of Buck and Hybrid Buck DC-DC Converters for Automotive Applications", 15th International Power Electronics and Motion Control Conference, EPE-PEMC 2012 ECCE Europe, Novi Sad, Serbia, September 2012, pp DS2b.3-1 - DS2b.3-6.

[7].▪ O. Pelan, "High Voltage Conversion Ratio, Switched C and L Cells, Step-down DC-DC Converter", Workshop-ul nr. 3, Interdisciplinaritatea si Managementul Cercetarii, Pitesti, Romania, 30-31 Mai 2013.

[8].▪ Ovidiu Pelan, Nicolae Muntean, Octavian Cornea, Frede Blaabjerg, "High Voltage Ratio, Switched C & L Cells, Step-Down DC-DC Converter", ECCE 2013 - IEEE Energy Conversion Congress & Expo, Denver, Colorado, USA, September 15-19 2013, pp. 5580-5585.

CURICULUM VITAE

PERSONAL INFORMATION

Ovidiu Roman Pelan

📍 34 / 56 A, Aviatorilor, 332110, Petrosani, Hunedoara, Romania

📱 +40 (736) 691 331

✉️ ovidiu.pelan@gmail.com

Sex Male | Date of birth 26/07/1985 | Nationality Romanian

WORK EXPERIENCE

August 2012 - present

Research Assistant

"Politehnica " University of Timisoara, Faculty of Electrical and Power Engineering, Romania

Project name: "Hybrid Renewable Energy Conversion in an Integrated Low Power Micro Grid", no. PN-II-PT-PCCA-2011-3.2-1519.

- Bibliographical research
- Reports preparation
- Simulations and tests
- Research dissemination

Renewable energies sector

July 2012 – October 2012

Guest PhD Student

Institute of Energy Technology, Aalborg University, Denmark

- Hybrid DC-DC Converters for Automotive and Renewable Energies Systems
- Benchmarking of different Hybrid DC-DC Converters
- Bibliographical research
- Reports preparation
- Simulations, design and tests
- Research dissemination

Automotive and Renewable energies sector

February 2010 – May 2011	**Research Assistant**

"Politehnica " University of Timisoara, Faculty of Electrical and Power Engineering, Romania

Project name: "Improvement of the Structures and Efficiency of Small Horizontal Axis Wind Generators with Non-Regulated Blades", no. RO018 EEA Grants.

- Bibliographical research
- Design and simulate a Hybrid Buck switched-inductor DC-DC Converter for a small-scale wind energy conversion system
- Implementation of a complete full scale laboratory installation in order to test designed wind energy conversion system
- Analysis and processing of acquired data
- Research dissemination

Renewable energies sector

EDUCATION AND TRAINING

October 2010 – present	**PhD Student in Electrical Engineering Department**

"Politehnica " University of Timisoara, Faculty of Electrical and Power Engineering, Romania

October 2004 – June 2009	**Electrical Diplomat Engineer Degree**

"Politehnica " University of Timisoara, Faculty of Electrical and Power Engineering, Romania

Power Electronics, Electrical Drives, Automotive Electronics and Systems, Computer Science
Computer skills acquired: Matlab, C++, C, Psim, Labview

October 2000 – June 2004	**Baccalaureate Degree, Average Programmer Certificate**

"Informatics High-School" of Petrosani, Petrosani, Hunedoara, Romania

Mathematics, Computer Science intensive Informatics
Computer skills acquired: Borland Pascal, Fox Pro

Mother tongue(s)   Romanian

Other language(s)

UNDERSTANDING		SPEAKING	WRITING
Listening	Reading		
English	ADVANCED	ADVANCED	ADVANCED	ADVANCED
French	MEDIUM	MEDIUM	MEDIUM	MEDIUM

Communication skills	▪ Good communication and public speaking skills acquired through participation at different international scientific conferences.
Job-related skills	▪ Team working skills gained working in two research projects.
Computer skills	▪ Good command of Microsoft Office™ tools, Microsoft Visio, Matlab, C++, C, Borland Pascal, Psim, Labview.
Other skills	▪ Adaptability to unforeseen circumstances, diligence, dexterity, sociability, punctuality, creativity.
Driving licence	▪ B category since 2005.

ADDITIONAL INFORMATION

Publications	▪ N. Muntean, L. Tutelea, D. Petrila, O. Pelan, „Hardware in the Loop Wind Turbine Emulator", *International Aegean Conference on Electrical Machines and Power Electronics & Electromotion Joint Conference, ACEMP - Electromotion 2011,* Istanbul, Turkey, September 2011, pp. 59 - 64.
	▪ O. Cornea, O. Pelan, N. Muntean, "Comparative Study of Buck and Hybrid Buck "Switched-Inductor" DC-DC Converters", *OPTIM 2012 – 13th International Conference on Optimization on Electrical and Electronic Equipment,* ISSN 1842-0133, Brasov, Romania, 24-26 May 2012, pp. 853 – 858.
	▪ O. Pelan, N. Muntean, O. Cornea' "Comparative Evaluation of Buck and Switched-Capacitor Hybrid Buck DC-DC Converters", *SPEEDAM 2012 - International Symposium on Power Electronics,Electrical Drives, Automation and Motion*, Sorrento, Italy, ISBN: 978-1-4673-1300-1, June 2012, pp 1330-1335.
	▪ N. Muntean, O. Cornea, O. Pelan, C. Lascu, " Comparative Evaluation of Buck and Hybrid Buck DC-DC Converters for Automotive Applications", *15th International Power Electronics and Motion Control Conference, EPE-PEMC 2012 ECCE Europe,* Novi Sad, Serbia, ISBN: 978-1-4673-1971-3, September 2012, pp DS2b.3-1 - DS2b.3-6.
	▪ Ovidiu Pelan, Nicolae Muntean, Octavian Cornea, Frede Blaabjerg," High Voltage Ratio, Switched C & L Cells, Step-Down DC-DC Converter", ECCE 2013 - IEEE Energy Conversion Congress & Expo, Denver, Colorado, USA, September 15-19 2013, pp. 5580-5585.