Proposed Topology of Cascaded Multilevel Inverter Used for Reduced Number of On State Switches

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Abstract: This paper presents a novel topology for cascade multilevel inverter. Multilevel inverter is an alternative within the area of lot of power average voltage energy control. This proposed paper analyses a generalized cascaded inverter topology with minimized number of switching devices. In this proposed work of multilevel inverter, the aim is to reduce the number of dc voltage sources and switches to obtain number of voltage levels. The proposed circuit consists of series connected Switching units and it can generate DC voltage levels similar to other topologies. In this paper, six switches are used to generate 9 level inverter output. Topology of the proposed cascaded multilevel inverter considers some factors such as number of switching devices, number of output voltage levels and the standing voltage on the switches. The quality output voltage depends on the number of voltage level in the inverter. This new inverter shows superior capabilities when compared to other existing topologies. To verify the proposed topology, a 9-level inverter has been simulated. In this work the THD value is reduced to 7.58 % which is very low when compared to other existing topologies. The simulation results are carried out using MATLAB/SIMULINK.

Keywords: Multilevel inverter, Cascaded Circuit.

1. Introduction

Multilevel inverters have emerged because of the industry's selection due to their voltage stress reduction, inherent redundancy. They present a set of options that are suited to use in reactive power compensation. Increasing the amount of voltage levels within the electrical converter, while not using higher ratings on individual devices will increase the ability ratings. As the levels of voltage increases, the harmonics of the output voltage waveform decreases. A Neutral-point-clamped (NPC) inverter composed of main switching devices that operate as switches and auxiliary switches to clamp the output potential to the neutral point potential [1]. Flying Capacitance inverters suffer from capacitor voltage imbalance that results in a power quality deterioration and an increase in blocking voltages. The flying capacitor topology needs larger capacitor banks and additional pre-charging electronic equipment [2].

Cascade MLIs has been mentioned on topologies that need a less number of switches, diodes, gate drives and DC sources as the number of voltage levels will increase. This method is used to reduce voltage stress on switches. This inverter has the series connection of the existing unit to generate solely positive levels in the output [3]. Cascade H bridge Multilevel inverter needs

reduced number of elements to generate the maximum number of levels. This inverter will increase the output waveform level and the low order harmonics will be reduced [4]. E-type of cascade inverter module will generate thirteen levels with a reduced range of components. It reduces the stress on semiconductor devices and improves the reliability [5].

A new non-isolated DC supply with symmetric multilevel inverter with the lesser number of switches that reduces the complexity. It is possible to generate an odd range of output voltage levels. Increase the amount of levels that may reduce the distortion of harmonics [6]. Throughout steady-state operation and transient condition, the stability can be verified by capacitor balancing algorithm. It has the ability to generate the voltages from a one dc-link power supply [7]. In a modular multilevel inverter the four discord algorithms is mentioned and calculate an equivalent value of dc sources [8]. This topology has six level inverter consists of the inner flying capacitor and outer two-level inverter. It has reduced the isolated sources and device requirement [9].

By using stacking multilevel inverter, the space vector voltage to be low to generate the higher number of voltage waveform[10]. Low ripple current waveforms is generated with unity power factor. The converter is controlled using the proposed multilevel active rectifier and improved by MPPT algorithms [11]. Topology with a reversing-voltage element is proposed to enhance the performance of multilevel inverter [12]. In this work, modulation is easily extended to three phase, and using the higher level inverters operates with same structure of the module [13]. The performance of current control is improved with voltage delay compensation and therefore the fault tolerance is increased by using unbalance three-phase control [14]. It includes double frequency operation of output inductance and current that flows through power switches and filter inductance to be equal [15].

The Control algorithmic rule is employed to generate the gating signals for the power switches and maintain the natural balancing of all the capacitors [16]. A multilevel DC link employing a fixed DC voltage source and cascaded half-bridge is connected in such a way that the inverter outputs the desired output voltage levels. The staircase modulation technique is definitely used to generate the appropriate switch gate signals [17]. The proposed topology not solely has lower switches and elements compared with another one, however additionally its full bridge converters operate within the lower voltage [18].

The topology needs lesser number of dc sources and power switches and it consists of lower blocking voltage on switches, which ends in reduced complexity [19]. This inverter need less number of switches, whereas capacitor desires less variety of magnitude of dc voltage sources [20]. Symmetric and asymmetric operational modes, are analyzed during this proposed topology [21]. The main aim of optimization was generating the output voltage levels to be maximum with the minimum range of power electronic components and voltage rating on

switches [22]. The proposed technique is robust against the faults in switches of multilevel converter for dc supply [23].

The main contribution of this work is

1. Novel cascade multilevel inverter is designed using reduced number of on state switches, whereas the existing topology are designed for maximum number of switches.

2. Advantage of using Multilevel Inverter in this research is to reduce the harmonics. To validate this, THD analysis is performed.

3. Novel cascade multilevel inverter is proposed in this research to reduce the harmonics and losses.

The paper highlighting the proposed research is organized as follows:

Section 2 presents the block diagram of proposed system with relevant explanations and presents the n basic unit of cascade inverter. It also compares the semiconductor devices and switches in the current path with the existing topologies. Section 3 introduces the simulation results performed using MATLAB/SIMULINK along with relevant discussions. Finally, the concluding remarks and suggestions for further research are given in Section 4.

2. Proposed Topology

The basic unit of the proposed MLI consists of four unidirectional switches (S1, S2, S3 and S4), two bidirectional switches (S5 and S6) and two direct current sources (Va and Vb). This unit is capable of generating nine-level output voltage. This inverter is cascade to get additional voltage levels. If n basic units are cascaded, the inverter will generate up to $(2^{n+1}+1)$and $(2^{n+1}-1)$, (n = 1,2,3,...) voltage output levels for equal and unequal operations. Avoid short-circuiting in the power sources, left-side switches (S1, S3, S5) is ON at a given time and also right-side switches (S2, S4, S6) is ON at a given instant.

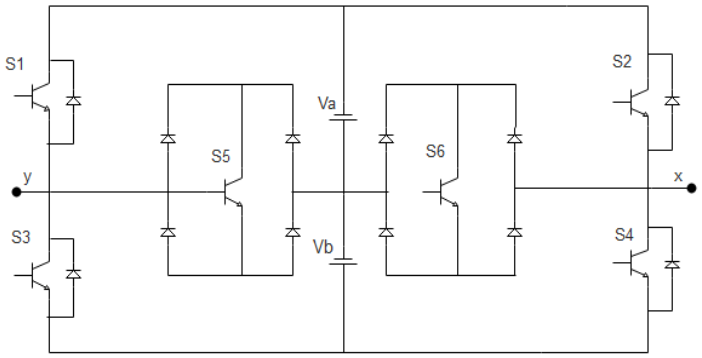


Figure 1 : Basic Block Diagram of Cascade Multilevel Inverter

Where S_j denotes the switching function of switch j (j = 1,2,...,6) and takes the value of 1 when ON and 0 when OFF. Table 1 shows the set of switching states of the fundamental unit and therefore the resulting inverter output voltage. The switching states consist of three null states and six active states. The three redundant null states is used to realize totally different control objectives.

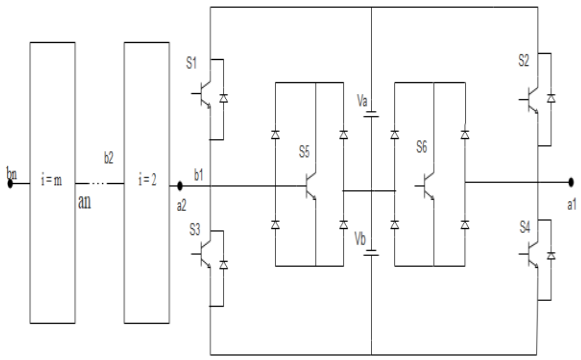


Figure 2: n cascade unit to generate output voltage levels

The bidirectional switches protect the inverter from short-circuit currents when operating in asymmetrical mode. Due to the voltage drop in one of the diodes of the bridge the diodes are forward biased. The bidirectional switches can distort the output wave form at low voltage levels. This topology is not significant in low and medium level voltage applications. Due to drop of voltage in any one of the diode, the bidirectional switches reduce the harmonics in the output voltage waveform.

States	S1	S2	S3	S4	S5	S6	Output Voltage
1	0	0	1	1	0	0	0
2	0	0	1	0	0	1	$+V_b$
3	0	0	0	1	1	0	$-V_b$
4	0	0	0	0	1	1	0
5	0	1	1	0	0	0	$+(V_a + V_b)$
6	0	1	0	0	1	0	$+V_a$
7	1	0	0	1	0	0	$-(V_a + V_b)$
8	1	0	0	0	0	1	$-V_a$
9	1	1	0	0	0	0	0

Table 1 : Switching Topology of Proposed Multilevel Inverter

2.1 Operation of Proposed Topology

It consists of two voltage sources Va and Vb and six semiconductor switches. Every switch consists of a MOSFET/IGBT with anti parallel diode. The output voltage of multilevel is generated on the set of switching states. To produce a nine-level output (Vxy), at least one null state and all the active states are fired in-sequence. For uniform power dissipation among the six switches, two null states are used, wherever State1 is ON throughout the positive half-cycle, whereas State 9 is employed throughout the negative half-cycle. Any PWM method could be used to control the semiconductor switches, tend to choose phase disposition PWM because of its performance.

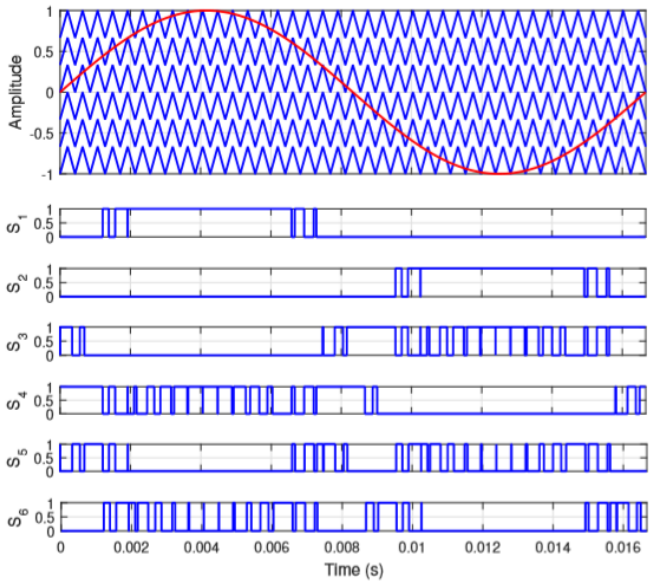


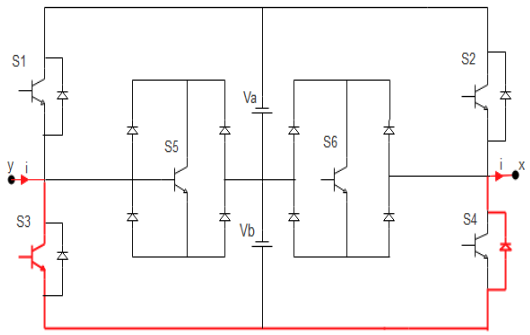
Figure 3 : Phase Disposition Modulation and Gating signals of Nine Level Inverter

The General expression for level number of voltage is

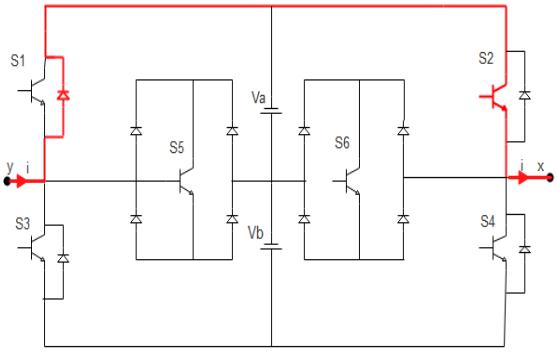
$$l = (2*Sw-3), \quad (1)$$

Where *l* = number of voltage levels in the output

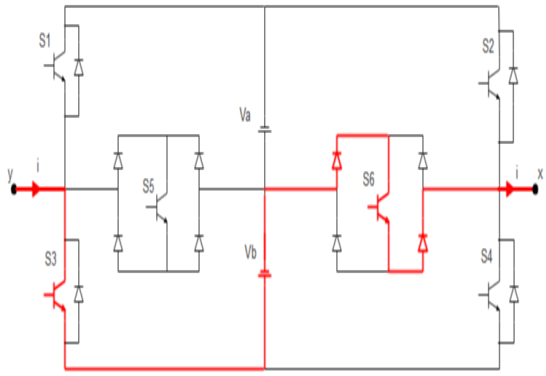
Sw = number of switches



Mode 1: State 1 Vxy = 0, S3 = S4 = 1

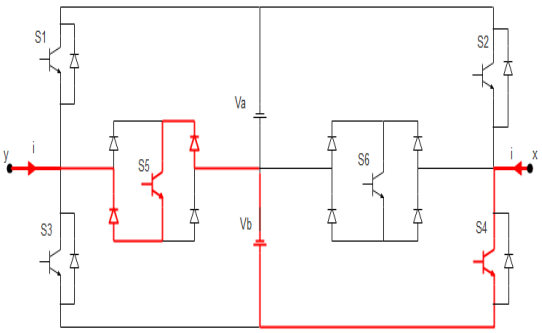


Mode 2: State 9 Vxy = 0,S1 = S2 = 1

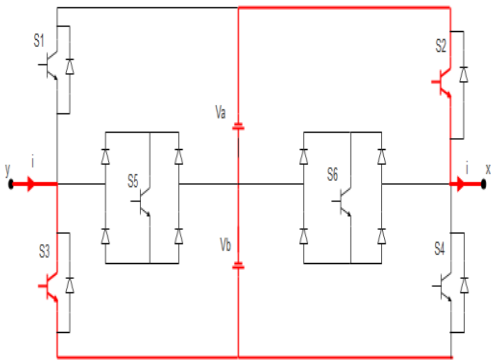


Mode 3: State 2 Vxy = +V2, S3 = S6 = 1,

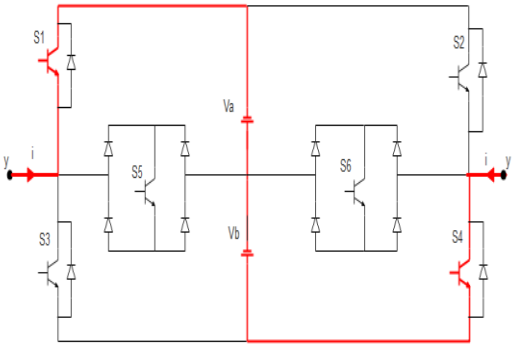
It requires bidirectional switches with the potential of blocking voltage and current conducting in each direction. The unidirectional switches within the inverter and bidirectional switches should operate at the high output voltage and need higher voltage.



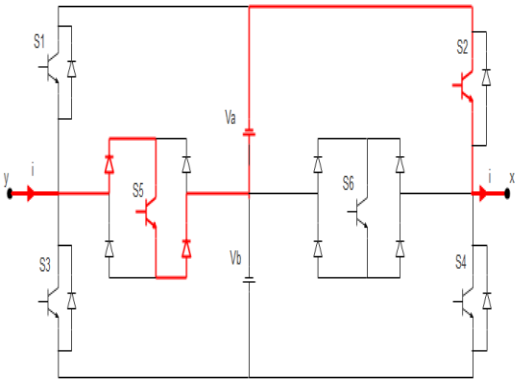
Mode 4: State 3 Vxy = −V2, S4 = S5 = 1



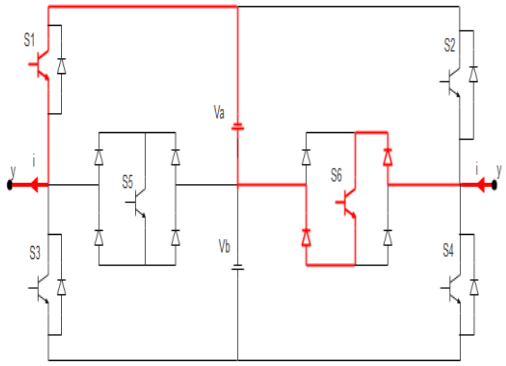
Mode 5:State5 Vxy = + (V1 + V2), S2=S3=1,



Mode 7: State 7 Vxy = − (V1 +V2), S1=S4= 1



Mode 6: state 6 Vxy = +V1, S2 = S5 = 1



Mode 8: state 8 Vxy = −V1, S1 = S6 = 1

Fig 4 : Switching states for generating voltage level output

2.3 Number of Switching Devices in Proposed Inverter

The number of semiconductor devices has a control on value and size or weight of an MLI unit as a result of the ability to get a similar number of voltage output levels by using reduced switches can each lower a unit's cost and physical size. Figure 5 shows the quantity of switches required to generate a similar number of voltage output levels for various topologies. It's clear that the proposed topology out performs the other topologies with the lowest switch count for a similar voltage level.

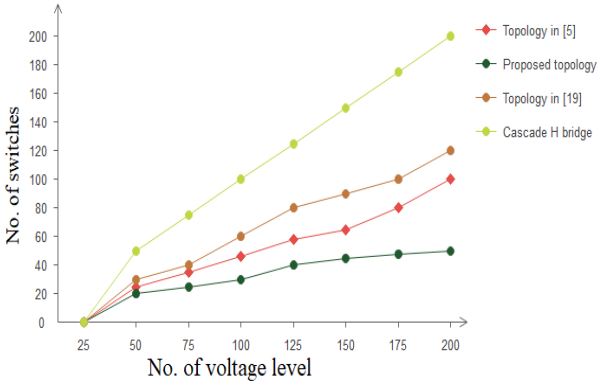


Figure 5: Number of switches versus voltage level of inverter

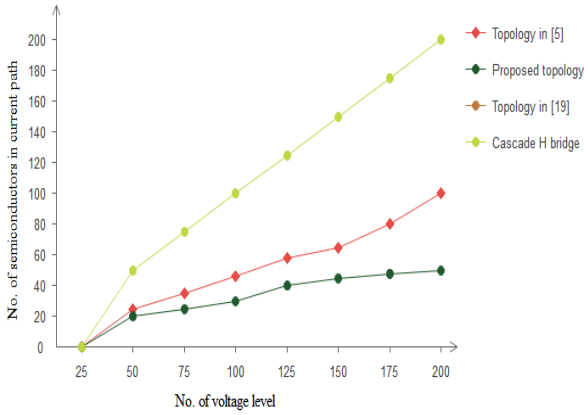


Figure 6: Number of semiconductors in the current path versus output voltage levels

2.4 Number of Semiconductors in the Current Path

When a switch or diode will turn on or off instantly without any power loss, real switches have a finite switching transition time. This finite transition period is accompanied by power loss transients. Hence, a smaller number of needed switches to supply a voltage level implies reduced power losses. Figure 6 shows the number of switches within the current path for identical voltage levels for the various. The proposed topology performs higher than in each modes that can leads to higher efficiency at any output voltage level.

3. Simulation Results and Discussion

Figure 7 shows the schematic diagram of the system with RL load under study. Simulations of six switch 9 level inverter were carried using MATLAB/ Simulink .The semiconductor switches are IGBT with voltage and current ratings of 600 V, 120 A in figure 7.

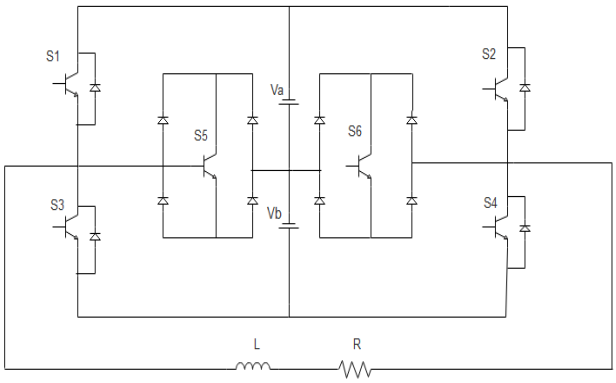


Figure 7: Schematic Diagram with RL load

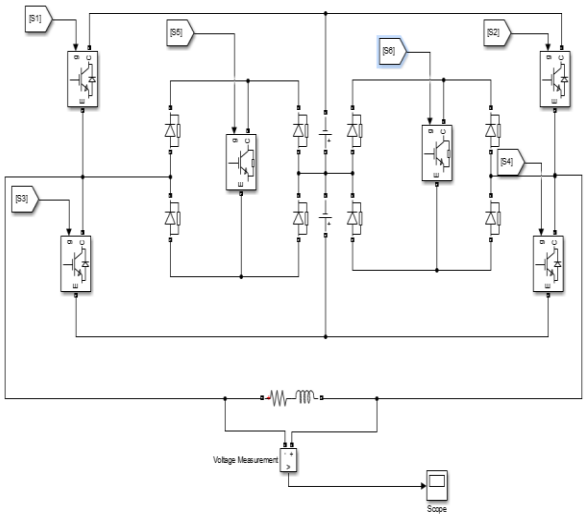


Figure 8 : Simulation circuit of Six-Switch 9 level Inverter

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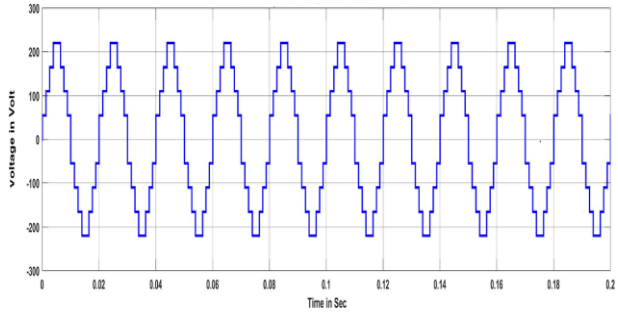

Figure 9 : Simulated 9-level Output Voltage waveform

Figure 9 shows the simulation results of the inverter output voltage waveforms for nine-level operation. Using six switches the nine level output voltage to be determined.

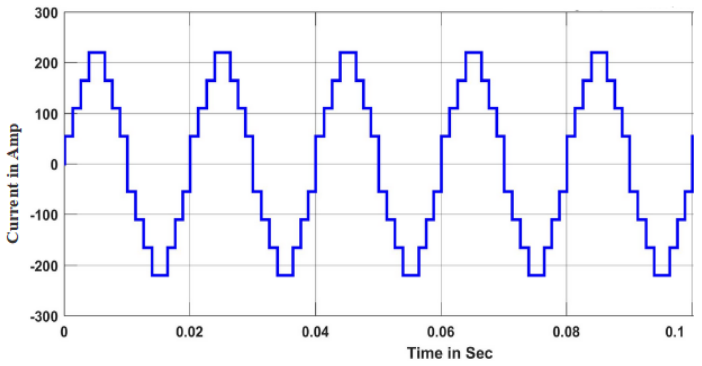

Figure 10: Simulated 9-level Output current waveform

Figure 10 shows the inverter output current waveform for nine level inverter. To generate a desired output with the best quality of the waveform, the number of the voltage steps should be increased.

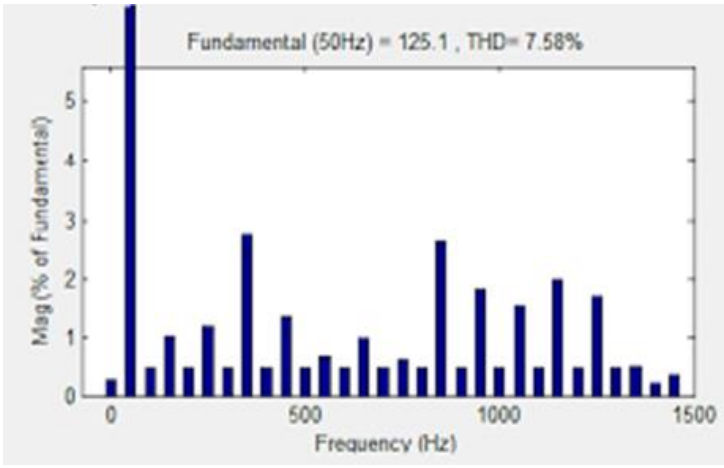

Figure 11 : FFT plot of 9 level Multilevel Inverter

The corresponding THD% are observed using FFT block and the FFT value is shown in figure 11. The THD value is reduced to very low in the proposed topology. It improves the performance of cascaded multilevel inverter.

3.1 Comparative Analysis

Comparative Performance based on THD for 9 level inverter

S.no	Inverter	No.of switches	THD %
1	Proposed work	6	7.58
2	Symmetric Inverter ref no[6]	9	22.27
3	Cascade MLI ref no [21]	8	10.12

4. Conclusion

In this paper, proposed topology for nine level inverter with on state switches to be reduced. The principles of operation of the design are discussed and validated using simulations. The new modulation is compared to two similar modulations in terms of the number of switches needed to generate a voltage level; the number of switches within the current path will be handled by the switches. Here the six switch and 2 dc voltage sources are used to generate the 9 level inverter output. This topology optimization of the proposed cascaded multilevel considering some factors such as number of switching devices, number of output voltage levels is reduced. This topology produces both the positive and negative voltage levels without the necessity for the classical H-bridge circuit and therefore reduces the semiconductor device count. MATLAB/ Simulink simulations are presented for nine level operations of cascade multilevel inverter. In this work, total harmonic distortion value is reduced to very low value when compared to existing topologies.

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