RESEARCH ON SOLDER JOINT LIFETIME OF SURFACE-MOUNTED DEVICES

A thesis submitted for obtaining the scientific title of Ph.D. in Engineering from Politehnica University Timișoara in the field of Mechanics by

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Foreword

This thesis has been elaborated during my activity in the Department of Mechatronics of the Politehnica University Timișoara, Romania.

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I conclude by thanking my partner Dan and my parents for their unlimited love, care, and support.

Timișoara, July 2023 Iulia – Eliza Ținca

To Dan, Mom, and Dad.

ȚINCA, Iulia - Eliza

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Abstract

This research focuses on improving solder joint reliability in electronics, specifically in the automotive industry, through applied methods such as virtual prototyping, simulation-based reliability assessment, and the development of practical guidelines. The study employs a combination of experimental and theoretical approaches, including board-level reliability tests, analytical calculations, and finite element analysis. The research contributes enhancing reliability in electronic devices through the implementation of a PCBA low-cycle fatigue assessment workflow.

CONTENTS

NOTATIONS, ABBREVIATIONS, ACRONYMS

ADAS	Advanced Driver Assistance Systems
ADCU	Assisted & Automated Driver Control Unit
ATC	Accelerated Thermal Cycling
BLR	Board Level Reliability
CAE	Computer Aided Engineering
CDF	Cumulative Distribution Function – Probability Function
CTE	Coefficient of Thermal Expansion
CTH	Combined Time Hardening
DFR	Design for Reliability
DMA	Dynamic Material Analysis
DoE	Design of Experiments
E	Young's Modulus
FC-BGA	Flip-Chip Ball Grid Array
FE	Finite Element
FEA	Finite Element Analysis
HCF	High-cycle Fatigue
IC	Integrated Circuit
IMC	Intermetallic Compound

LCF	Low-cycle Fatigue
PC	Power Cycling
PCB	Printed Circuit Board
PT	Project Team
SEDR	Strain Energy Density Ratio
SLR	System-Level Reliability
SMD	Surface Mounted Devices
SMT	Surface Mounted Technology
Tg	Glass transition temperature
THT	Through Hole Technology
TIM	Thermal Interface Material
TMA	Thermal Material Analysis
v	Poisson’s ratio

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1 INTRODUCTION

1.1 Background

Worldwide government initiatives for safer roads and the demand for safe and efficient vehicles are significant factors driving the growth of the Advanced Driver Assistance Systems or ADAS market [1]. ADAS technology includes sensors such as camera, radar, and lidar, as shown in Figure 1, that take information about the vehicle's environment and transmit it to various actuators or a multi-processing platform, the ADCU (Assisted & Automated Driver Control Unit) [2].

Figure 1 "The six building blocks of automated driving." Image reproduced from Continental Press Release Web Page [3].

The sensor systems or control units are electronic devices consisting of one or more printed circuit boards (PCBs) with various electronic components populating their surface, as in Figure 2, where the PCB lies within a housing and a plastic cover protects them from outside factors.

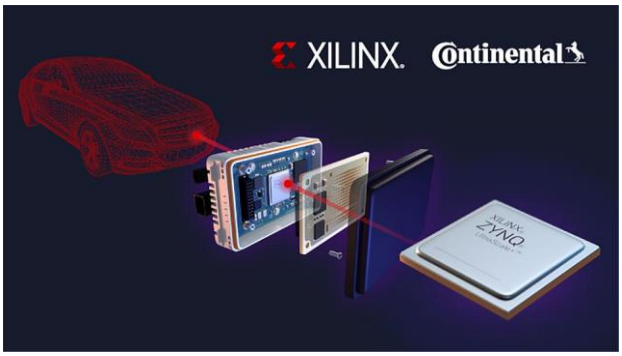


Figure 2 Representation of radar sensor assembly parts (housing, PCB, antenna, cover) and zoom-in on the Radar System Chip. Image reproduced from Forbes Web Page [4].

The solder joints, shown in Figure 3 (left), create the mechanical and electrical connection between the electronic part and the PCB.

During their lifetime, the electronic devices undergo slow-changing temperature variations – thermal cycling, rapidly changing temperature variations – thermal shock cycles, and vibration cycles. The leading cause of failure of the integrated circuit (IC) components mounted on the surface of the PCB is thermal cycling [5]. Figure 3 (right) shows how the assembly expands and contracts during thermal cycling.

Because the materials in the IC – PCB assembly expand differently, stress develops in the solder joints. As a result, the solder joints respond through time-dependent plastic deformation, which accumulates over time, eventually leading to the apparition of cracks [6], shown in Figure 4, and product malfunction.

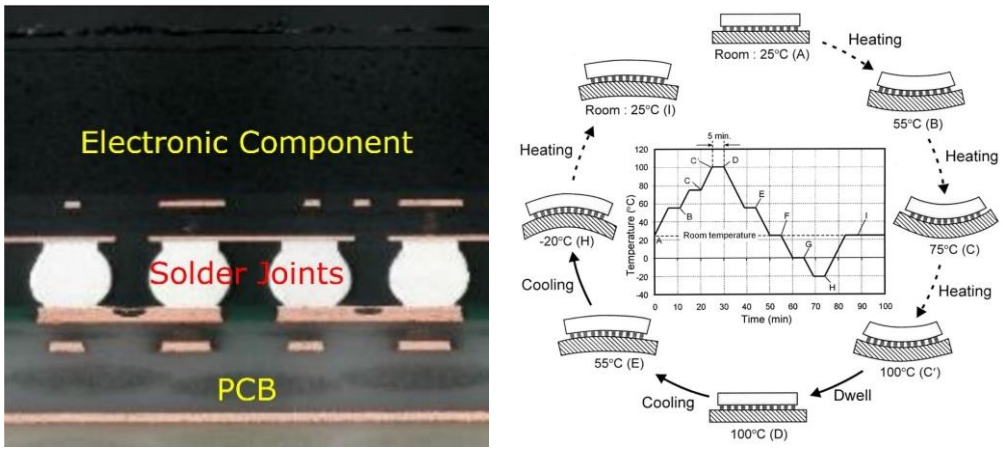


Figure 3 Cross-section of an electronic part mounted on a PCB (left). Illustration of the deformation of an IC – PCB assembly during thermal cycling. Reproduced with permission from ASME from Journal of Electronic Packaging, 2004, vol. 126(1): 41-47 [7] (right).

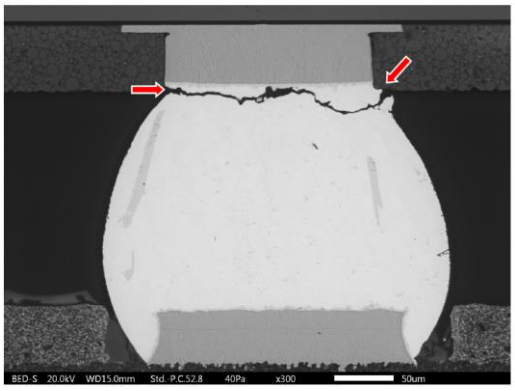


Figure 4 Solder joint fatigue crack. Image used courtesy of Continental AG.

1.2 Motivation

Across the electronics industry, solder joint-related issues cause 13% of failures [8], and high-temperature conditions and temperature cycling is the main reason [5]. In the past twenty years, with the increasing complexity of vehicles, the number of auto recalls doubled, and in 2015, electronics covered 6% of vehicle recalls. Furthermore, autonomous driving imposes a zero-defect mindset, which underlines the need for quality strategy improvement, focused on prevention and defect elimination [9].

Recalls and field failures trigger corrective actions from the original equipment manufacturer (OEM) across the supply chain, such as finding root causes, solution development, implementation, revalidation, and testing. Implementing changes in a product's late lifecycle comes with a significant cost increase. Reengineering is time-consuming and expensive. It often leads to modifications of tooling and manufacturing processes, which in turn require more testing and validation. A modified product must go through quality control again, finally leading to an innovative marketing and sales strategy.

Virtual prototyping and digital twins are two quality improvement strategies with enormous potential to avoid the far-reaching implications of late-stage changes. Compared to a reliability test for one electronic part, one thermal cycling test simulation costs up to ten times less. Although simulations do not fully characterize a product's reliability, they help increase its reliability. Through simulations, engineers optimize products by testing different scenarios, identifying, and addressing potential issues, and tailoring design aspects according to the use environment. In addition, simulations offer a visualization of the design, allowing for better communication and understanding between the stakeholders. More cost-efficient than physical testing, simulations also reduce the cost of various stages of product development. Virtual prototyping methods bring manufacturers a competitive advantage, and here lies the reason for continuous research and development in virtual technologies.

The motivation for this work comes from the need for a continuous quality improvement strategy in developing electronics for autonomous driving. Electronic part manufacturers evaluate their products based on current standards [10] and for their intended use through board-level reliability testing. However, when Tier 1 suppliers or OEMs mount these components on a PCB as part of a product, the stress state in the solder joints changes due to added loads such as fixations [11] [12]. The increased mechanical stress can accelerate the solder joint failure. Therefore, recent studies emphasize the need to evaluate electronic components in the context of the system they are part of, making the transition from board-level to system-level reliability assessment [11] [12].

The proposed process involves understanding modeling intricacies and building a material and knowledge database through board-level experimental, analytical, and numerical analysis. The goal is to develop a standardized simulation workflow for predictive system-level reliability assessment. This approach developed for automotive load-case applies to the broader electronics reliability field.

1.3 Thesis Outline

The thesis consists of five chapters, as follows:

1. **Introduction:** outlines the position of the research in the industry, shows the researched niche, and underlines the unanswered aspect along with the motivation behind the study, proposed goal, and strategy towards fulfillment.

2. **Literature review** of the current research in the field, showing fundamental theories and concepts related to the research problem.

3. **Methodology and Results** describes the research design, data collection, and analysis methods. The research process first aims for an experimental, analytical, and numerical board-level analysis for three ball–grid array (BGA) parts, followed by a system-level analysis. The board-level analysis outputs critical modeling and analysis aspects. In the system-level analysis, external loads create tension in the PCB to emulate the system-level effects. The goal is to compare the accumulated creep work in the two setups and understand the factors driving down the component's lifetime when mounted in the final product. The chapter presents the experimental board-level reliability test results, analytical and numerical analysis results, and the system-level analysis results. This chapter compares the two analyzed setups and relevant graphics for improved data processing. Finally, it proposes a simulation workflow approachable by finite element analysis engineers. The created workflow allows the design verification teams to analyze diverse designs and output consistent results regardless of the engineers performing the task.

4. **Discussion:** interprets and relates the results to the research goals and questions. The chapter discusses critical modeling aspects at the board-level and the integration of the board-level model in the complete product model. It evaluates the constraints and limitations and their impact on predictive system-level reliability assessment. The chapters also suggest areas for future research.

5. **Conclusion:** summarizes the essential findings of the research and emphasizes its contributions. The study created a valuable knowledge base and issued it to a global community of engineers from various disciplines. Developing a simulation workflow is the main contribution, now a daily practice for a global Finite Element Analysis Team. The workflow includes tutorials, a curated materials database, an electronic part library, and FE software scripts for automated pre- and post-processing. The research addressed a practical problem in the automotive parts manufacturing industry by supplying practice guidelines for predictive reliability assessment.

6. **References:** lists all the sources cited in the thesis.

2 LITERATURE REVIEW

2.1 Introduction to Surface Mount Technology

The thesis addresses the reliability of surface mount devices assembled to the PCB through surface mount technology (SMT).

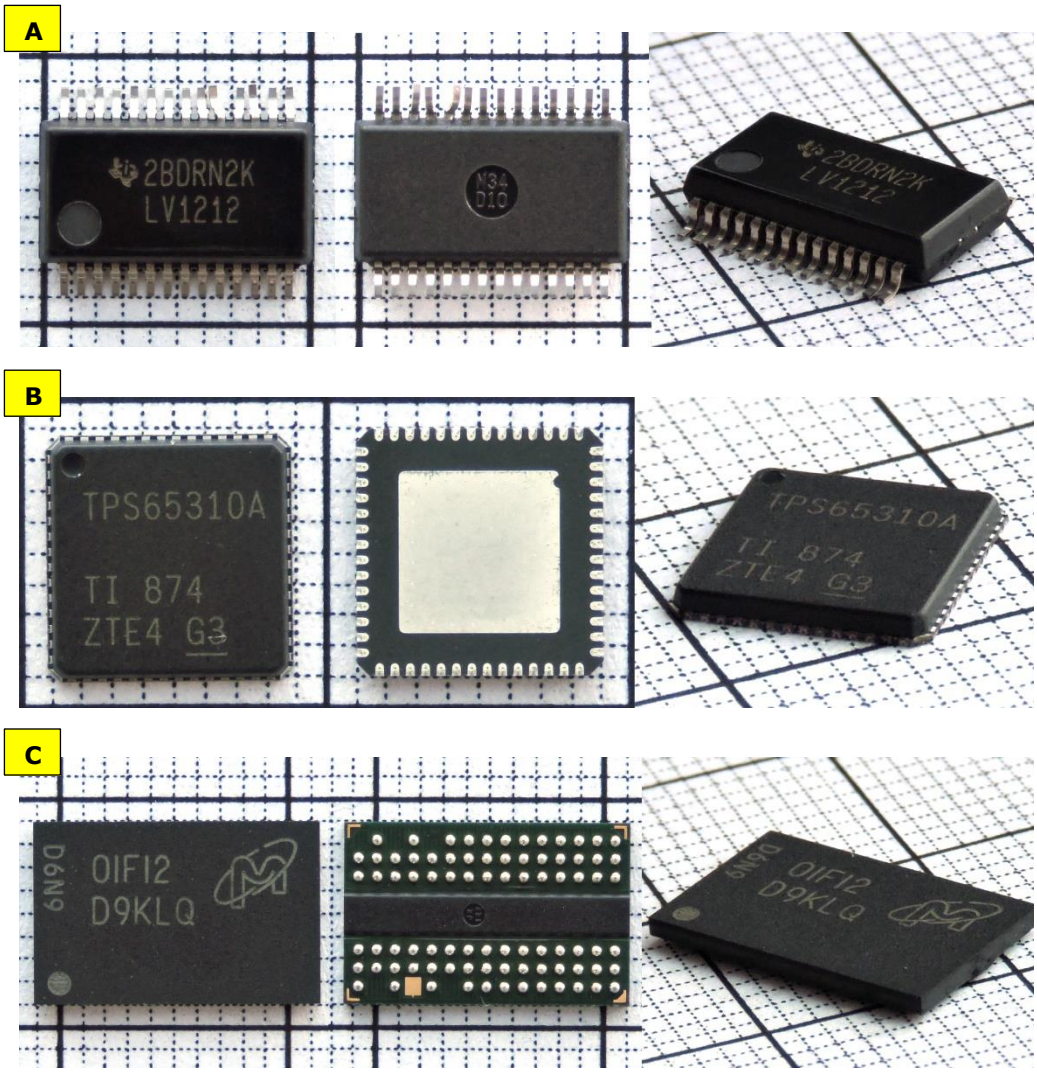


Figure 5 A – Shrink Small Outline Package (SSOP), B – Quad Flat No-lead Package (QFN), C – Ball Grid Array Package (BGA). Images used courtesy of Continental AG.

SMT connects all terminals of a part to the PCB by soldering them to the face of the PCB. Thus, SMT allows the realization of smaller printed circuit boards than

through hole technology (THT), where the part terminals pass through the thickness of the board through holes. The electronic components specific to surface mount technology are small and thus allow for more components on the target surface compared to THT. Components mounted on the surface of printed circuit boards are known as Surface Mounted Devices, SMD. They can be dual (dual), with terminals on two sides, quad (quad), with terminals on all four sides, or they can have terminals arranged in a matrix on one face. Although no standardized classification exists, most components have an acronym writing down the mounting technology, power, and technology used [13]. For example, Figure 5 illustrates three medium-sized components: SOP, QFN, and BGA. The apparent terminals of the SOP, as opposed to the QFN, can be seen, as well as the arrangement of terminals on two or four sides. In the case of the BGA, the terminals are not visible. Instead, they are solder paste balls arranged in a matrix on the back of the component.

Electronics manufacturers use reflow soldering to attach surface-mounted components to printed circuit boards (PCBs). The process involves applying a solder paste to the PCB as in Figure 6, placing the components on top of the paste using a "Pick and Place" machine, and then subjecting the assembly to a temperature profile in an oven to melt and flow the solder paste, forming a permanent bond between the components and the PCB [14].

The temperature profile used in the reflow process is critical to ensure a reliable solder joint formation. The profile typically consists of three stages: preheat, soak, and reflow [15]; see Figure 7. In the preheat stage, the temperature gradually increases to activate the flux, which removes oxides from the metal surfaces and prepares them for bonding. The soak stage follows, during which the temperature stays constant for a specified period to allow the flux to activate fully and to ensure that all components reach the same temperature. The final stage is the reflow, where the temperature increases, causing the solder alloy to flow and form the connection between the components and the PCB. Once the reflow process is complete, the PCB undergoes a cooling stage, during which the temperature decreases to allow the solder to solidify and form a strong bond [14].

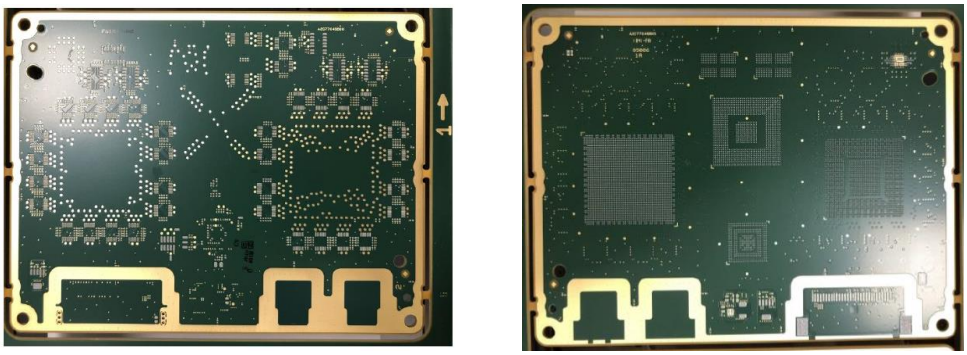


Figure 6 Non-populated PCB with stencil shape dispensed solder paste (bottom and top sides). Images used courtesy of Continental AG.

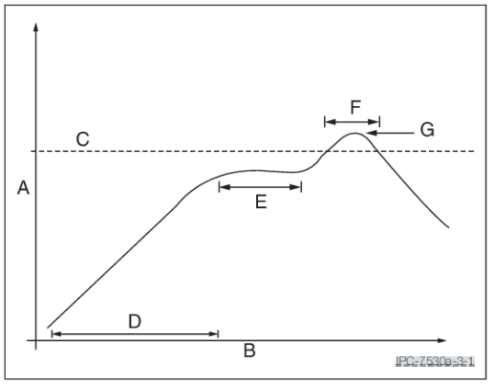


Figure 7 Reflow thermal profile schematic as in IPC7350A [15] Figure 3-1, where A is the temperature, B is the time, C is the alloy liquidus temperature, D is the preheat time, E is the soak time, F is the time above liquidus and G is the peak temperature.

The fully automated reflow process in an industrial setting carefully controls the temperature profile to ensure consistent and reliable solder joint formation. The temperature profile considers several factors, such as the solder alloy's composition, the PCB, and the components' properties, to minimize defects such as flux splashes or volatile compounds in the solder paste [14]. Following recrystallization, electronic parts populate the PCB - see Figure 8.

A disadvantage of SMT is the problematic inspection and testing of components due to complex or no access to the terminals [14]. In addition, following recrystallization, in the case of a BGA package, the geometry of the solder balls changes due to the solder alloy's composition, the balls' size and spacing, and the temperature profile considered in the reflow process. Therefore, to guarantee the quality and reliability of the solder joints, quality inspectors use non-invasive and invasive procedures to analyze the changes in the solder geometry and dimensions.

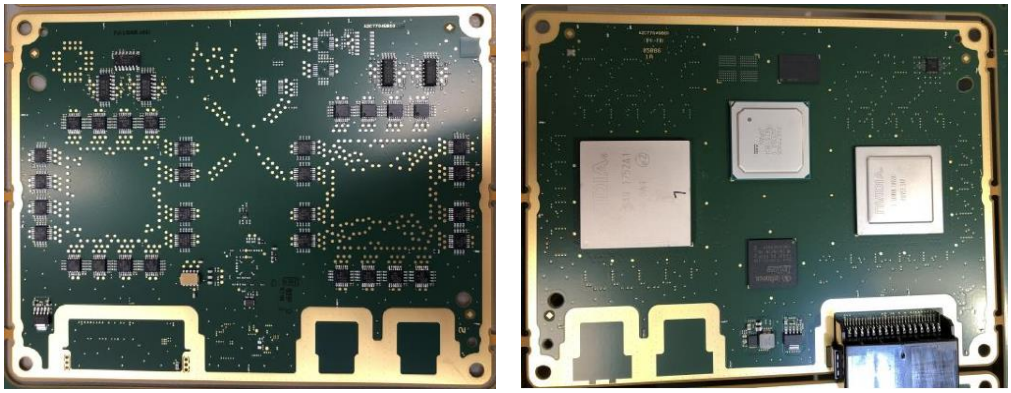


Figure 8 Populated PCB (bottom and top sides). Images used courtesy of Continental AG.

Non-invasive procedures, such as optical or X-ray inspection in Figure 9B, can provide high-resolution images of the BGA component and its solder joints. X-ray inspection is particularly useful in detecting voids, cracks, or other defects in the solder joints.

Invasive procedures, such as microscopic cross-section analysis shown in Figure 9A, involve cutting the BGA component and encapsulating it in resin to reveal the internal structure of the solder joints. The microscopic cross-section analysis allows for a detailed examination of the solder integrity at the solder-component and solder-PCB interfaces and the shape and dimensions of the joints, as in Figure 9C. The equipment used for microscopic cross-section analysis typically includes a high precision cutting tool, a resin encapsulation system, and a microscope with high magnification and resolution capabilities. The cross-sectional images obtained from this analysis can provide valuable information about the quality and robustness of the solder joints and help identify any defects or issues that may need addressing in the manufacturing process.

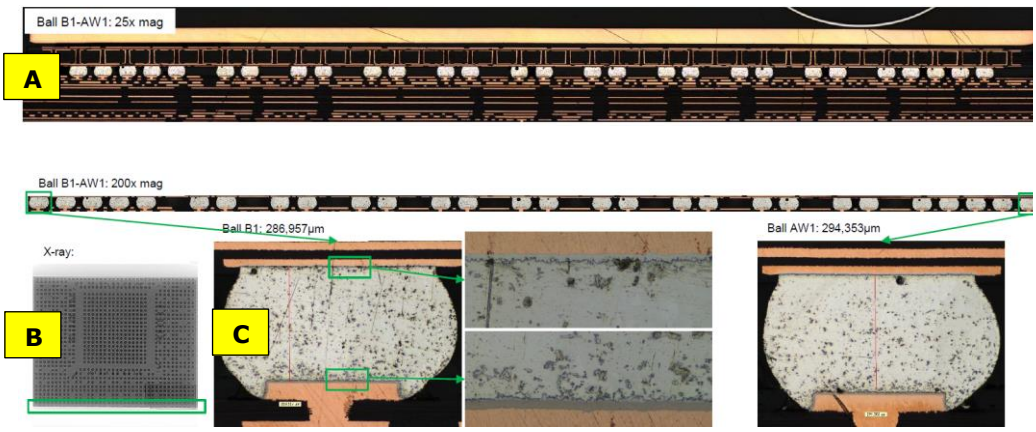


Figure 9 A – cross section of the solder ball row marked in B – the X-ray image of a BGA component, C - analysis of the first and last solder ball of the row. Images used courtesy of Continental AG.

New packages, such as quad flat no-lead (QFN) and chip scale packages (CSPs), are becoming increasingly common. Manufacturers are developing new techniques for placing and soldering these tiny components. Another trend in SMT is the use of more advanced materials. For example, researchers develop new solder pastes for more robust joints with improved performance, such as higher melting points. In addition, manufacturers use new substrate materials, such as high-temperature ceramics, to increase the performance and reliability of electronic devices. One of the most significant advances in using convection reflow ovens is providing more consistent heating and better temperature control than traditional infrared (IR) ovens. This allows for more precise soldering process control, resulting in better joints and fewer defects. Another innovation in reflow soldering is the use of vacuum reflow technology. Lau in [16] identifies the keywords describing SMT trends starting Industry 4.0 to be high automation, miniaturization, performance, reliability, efficiency, and environmentally friendly.

2.2 Lead-Free Solder Alloys

Traditionally, the electronics industry used tin-lead (SnPb) soldering alloys. However, due to concerns over the toxicity of lead and its impact on the environment, legislators in North America have made efforts to ban lead since 1992. In addition, Japanese manufacturers voluntarily reduced the use of lead through the 1990s, and in 2006 the European Union, prohibited the use of lead in electronics. Hence a transition towards lead-free solder alloys followed [17]. Common lead-free solders are Tin-Silver-Copper (SnAgCu or SAC), Tin-Copper (SnCu), Tin-Silver (SnAg), and Tin-Zinc (SnZn). However, lead-free soldering presents challenges such as higher melting points, lower wetting ability, higher voiding behavior, and a dull aspect compared to SnPb solder joints requiring new inspection specifications [18].

The structure of a typical solder joint consists of the solder bulk and the metallization or intermetallic compound (IMC) on the component and PCB side, as in Figure 10. Fractures appear at the interface regions due to shock, drop, or vibration loads. On the other hand, thermal fatigue damage due to the different expansion between the materials in contact causes cracks in the solder bulk [18].

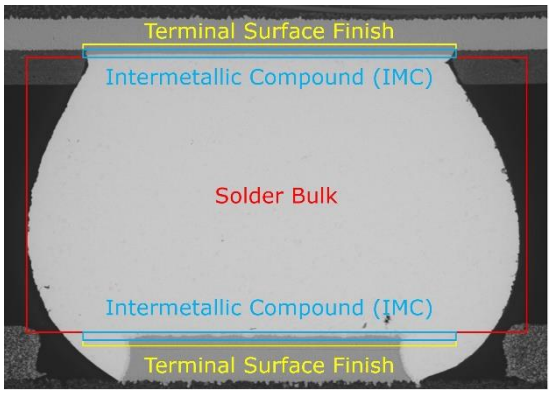


Figure 10 Structure of a solder joint. Image used courtesy of Continental AG.

The thermomechanical properties of solder joints can vary even when made using the same solder alloy. Microstructural differences such as grain size and orientation caused by a difference in the cooling rate or thermal profile during soldering can change the solder's mechanical properties. In addition, terminal surface finishes impact the adhesion of the solder and lead to variations in mechanical stress [19]. Clech et al. [20] identify 12 geometry and material parameters that influence the reliability of the solder joints illustrated in Figure 11, where α stands for coefficient of thermal expansion, E for the modulus of elasticity, v for Poisson's ratio, h for height, P is the pitch distance between the solder joints and A is the area of the solder joint in contact with the component. Subscript C stands for the component and B for the PCB. Variations in the soldering process can also affect the joint's mechanical strength and reliability.

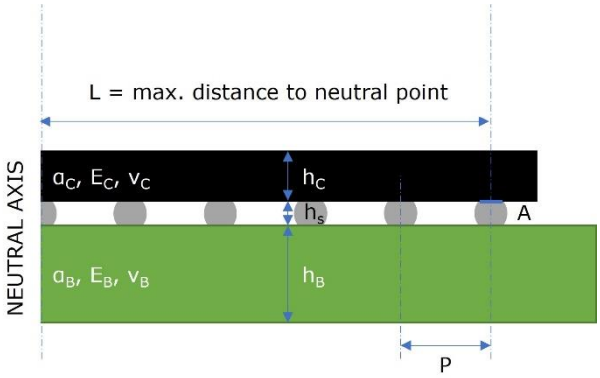


Figure 11 Schematic of geometry and material parameters that influence the reliability of the solder joints as in [20].

Table 1 sums the approximate values of the essential characteristics of solder alloys [19] [21]. These values vary depending on the solder alloy's composition and manufacturing processes - for example, harsh environmental conditions demand alloys capable of withstanding high temperatures and deformation rates [22]. High-reliability alloys emerged from this need in the form of SAC family solders, formulated with the addition of bismuth (Bi), antimony (Sb), and indium (In) [23].

Property	**Unit**	**SnPb**	**SnAgCu**	**SnAg**
Melting Temperature	°C	183	217	221
CTE 20-100°C	ppm/°C	24	16 – 20	19 – 20
CTE 100-150°C	ppm/°C	27	18 – 22	21 – 23
Yield Strength (strain rate 10^{-4} s^{-1})	MPa	22	20	15
Yield Strength (strain rate of 10^{-3} s^{-1})	MPa	32	30	20
Young's Modulus at 20°C	GPa	30	48	35
Poisson's Ratio	-	0.38	0.35	0.35

Table 1 Mechanical properties of soldering alloys [19].

Homologous temperature is a dimensionless parameter that describes the temperature of a material relative to its melting temperature. It is the ratio of the absolute temperature of the material and its melting temperature in absolute units (usually Kelvin). The exact threshold depends on the material and its specific properties, but it is typically in the range of 0.4 to 0.6 for metallic materials. When the homologous temperature of a material exceeds a certain threshold, creep deformation is likely to occur [19]. For example, the homologous temperature of a typical SAC solder at room temperature would be 25°C[K]/218°C[K] = 298K/491K = 0.61, showing that at room temperature, the material is already operating at a high homologous temperature, which suggests that it may be more prone to creep deformation if subjected to stress or other environmental factors.

Lead-free alloys exhibit a nonlinear, loading rate-dependent mechanical behavior. Additionally, these alloys experience rupture at strains above 20% after the yield point, which occurs at 0.2% strain. Regarding the elastic modulus, both lead, and lead-free mixtures exhibit a linear variation with temperature. However, lead-free alloys are stiffer than leaded alloys, even at elevated temperatures, and they also have a higher melting point than SnPb alloys [19].

The elastic-plastic-creep analysis treats the total deformation of a material as the sum of the elastic, plastic (time-independent), and creep (time-dependent) components in (1) [24]:

$$\varepsilon_{total} = \varepsilon_{elastic} + \varepsilon_{plastic} + \varepsilon_{creep} \quad (1)$$

Elastic deformation occurs when a loaded and then unloaded material returns to its original shape. The Young's modulus and Poisson's ratio characterize this type of deformation.

Plastic deformation occurs when a material undergoes permanent deformation under loading above its yield strength. This type of deformation occurs over a relatively short time and is irreversible.

In the case of long-term loading, a material can undergo visco-plastic deformation, which is a combination of plastic deformation and creep. *Creep* is a time-dependent deformation that appears at stresses lower than the yield strength and results from rearranging atoms and molecules in the material over time. Creep deformation in metals goes through three stages: primary, secondary, and tertiary. Primary creep occurs immediately after elastic and plastic deformation, with a descending strain rate. In the secondary stage, the deformation follows a constant rate, while the third stage rapidly increases the strain rate, leading to material failure, as shown in Figure 12. Under thermal cycling, both primary and secondary creep deformations are relevant. Since the temperature profiles used in reliability tests typically change slowly, the secondary component, or stabilized creep dominates the creep behavior of the solder paste. Therefore, constitutive models for solder alloys follow a visco-plastic law and include both elastic and plastic components from stabilized creep. These models are essential in predicting the long-term reliability of solder joints under cyclic loading conditions [19].

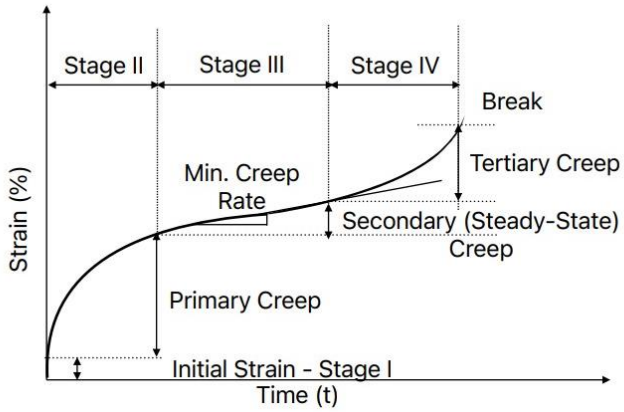


Figure 12 Creep deformation stages under constant load and temperature.

Solder alloys undergo aging processes over time. These processes change the solder microstructure, reducing mechanical strength and increasing susceptibility to failure. The aging mechanism in lead-free solders consists of intermetallic compounds' growth at the connection interface. For SAC305, Ma et al. [25] observed an increase in the creep strain rate up to seventy-three times during 63 days of room temperature aging. Zhang et al. observed a "cross-over point" at which the lead-free solders creep faster than tin-lead solders [26]. Basit et al. [27] propose an analysis methodology that incorporates the effects of solder paste aging by correlating with experimental data. Their experiments show a decrease in the lifetime of up to 53% for samples pre-aged for 12 months.

Lead-free solders exhibit microstructural effects, which can affect their performance in various applications. One effect is the appearance of intermetallic compounds (IMCs) at the connection interface, which can increase the mechanical strength but may also cause brittle fracture or corrosion. Another effect is the coarsening of precipitates, which can reduce mechanical properties and increase susceptibility to cracking under thermal cycling or mechanical loading. Additionally, the formation of a granular structure network in regions with high strain can lead to the formation of cracks through recrystallization. Optimizing the solder alloy composition by adding bismuth, antimony, or indium addresses some of the above-mentioned effects [20]. Bismuth doping improves mechanical properties, including ductility, and reduces brittleness.

Regarding aging performance, bismuth-doped SAC solders show increased thermal cycling reliability compared to lead-free solder alloys [28]. In addition, bismuth acts as a grain refiner and inhibits intermetallic compounds (IMCs) growth at the solder/substrate interface during thermal cycling, which can cause solder joint failure over time [29]. Athamneh and Hamasha [30] investigated the fatigue behavior of a SnAgCuBi alloy compared to SnAgCu, including the aging phenomenon. The bismuth-doped alloy's fatigue life and shear strength increased, regardless of aging and stress state. Therefore, the reported impact of aging on the Bi-alloy is significantly lower.

2.3 Board-Level Reliability

The first-level interconnect shown in Figure 13 refers to the connection between the die and the terminal or substrate, typically involving wire or flip-chip bonding. This level of interconnect is essential for establishing electrical connections between the active components of the integrated circuit and the outside world [14].

The second-level interconnect, on the other hand, refers to the connection between the electronic component and the printed wiring board (PWB / PCB), as in Figure 13. Typically solder joints create this connection [14].

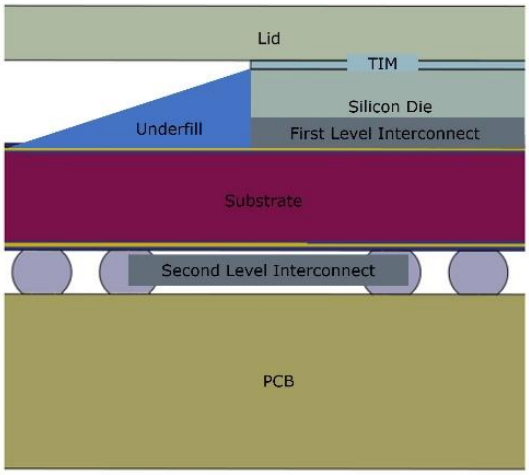


Figure 13 Schematic of a BGA cross-section, showing the first- and second-level interconnects.

Microelectronics production defects can occur due to several factors, such as design flaws, material impurities, manufacturing process issues, and environmental factors. Some examples mentioned in [31] are:

- Delamination at interfaces occurs when the properties of the materials in contact differ, leading to separation or cracking. Using materials with similar properties, proper bonding techniques, and buffer layers prevents such issues.

- Cracks in the silicon die can occur due to accumulated strains and stresses exceeding the material's tensile strength. Optimizing the component's design and using materials with better mechanical properties minimizes this risk.

- Fatigue or breakage of wires connecting the silicon die to the terminals leads to a loss of function or reduced performance. Using high-quality materials, designing robust connections, and reducing stress concentrations prevent such failures.

- Cracks or crevices in the component body can occur due to moisture and vapor pressure build-up during the recrystallization bonding process. Careful control of the bonding process and the use of moisture-resistant materials minimizes this issue.

- Gas bubbles or voids can form during cooling due to the compression of materials. Optimizing the manufacturing process, controlling the cooling process, and using materials with better thermal properties addresses this issue.

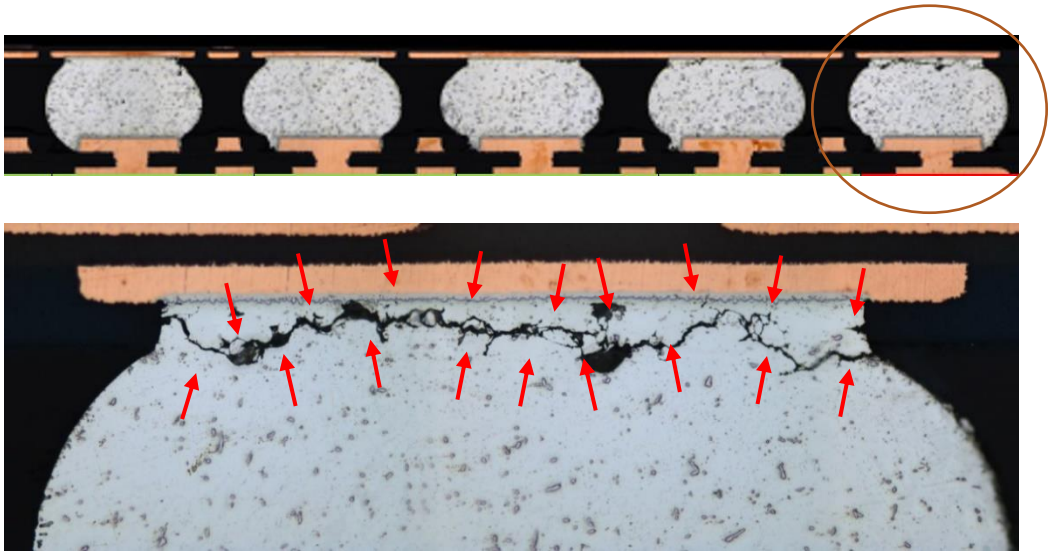


Figure 14 Thermal cycling induced failure in the corner solder ball of a BGA. Images used courtesy of Continental AG.

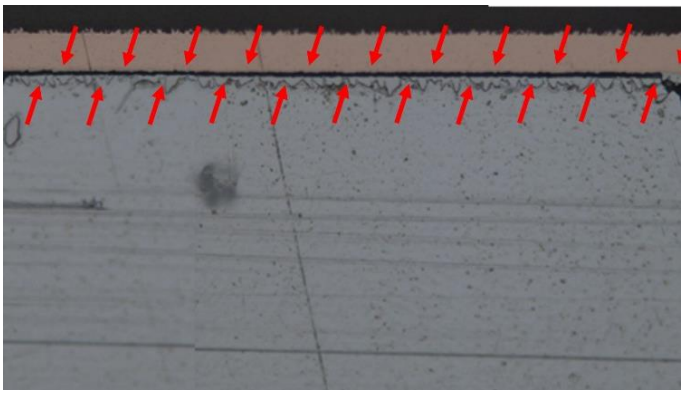


Figure 15 Mechanical fracture in the solder ball of a BGA. Image used courtesy of Continental AG.

In the context of thermal expansion, Clech et al. [20] define two types of deformation that can occur in the second-level interconnect: global CTE mismatch and local CTE mismatch. Global CTE mismatch refers to the deformation when the entire PCB expands or contracts due to temperature changes, causing stresses in the solder-PCB interface. Local CTE mismatch, on the contrary, refers to the deformation that occurs when a particular component on the PCB expands or contracts at a different rate than the surrounding materials, causing stresses in the component-solder interface.

Due to cyclic temperature loads at various stages of the finished product life cycle, different thermal expansions of the materials in contact will produce a state of significant stresses and strains. In addition, solder joints positioned at the corners of components are most susceptible to failure, sometimes resulting in solder failure or loss of electrical connection [31], see Figure 14. Thermal cycling cracks are distinguished from mechanical fractures due to poor handling of samples, shock, vibration, or drop by their distinctive aspect and propagation through the solder mass. Mechanical fractures appear in the IMC layer and follow a straight path, as shown in Figure 15. SMD's prevalent failure mode and reliability concern is fatigue damage due to CTE mismatch [32]. Electronics manufacturers work closely with their component suppliers to ensure the reliability of the finished product. While for some products, such as home computers, the reliability of the electronic components will mostly stay the same when assembled in the final product, in industries with harsher environmental conditions, the mechanical stresses that develop in the solder joint can accelerate their failure.

Dudek [19] defines two fundamental approaches in solder joint reliability assessment: a theoretical approach and an experimental approach, while Lau [33] divides reliability engineering into three main tasks based on the product development process:

- Design for reliability (DFR) ensures that a product, system, or process can perform its intended function over its expected lifetime without requiring excessive maintenance or repair. Design for Reliability implies a theoretical approach. The next chapter will discuss this approach.
- Reliability testing and data analysis aim to identify any potential issues before the product is released to the market or put into use.
- Failure analysis determines the root cause of failures.

The reliability of an interconnect is a measure of its ability to perform its intended function under a given set of conditions over a specified period without failure [32], numerically expressed as in (2),

$$R(x) = 1 - F(x) \tag{2}$$

where R(x) is the reliability function and F(x) is the cumulative distribution function (CDF) determined through reliability testing.

The scope of the reliability test is to obtain failures on a statistically significant number of samples and determine the life distribution, F(x). The statistical distribution of solder joint failures follows a two-parameter Weibull distribution defined by the scale parameter, θ, and the slope or shape parameter, β. The scale parameter represents the quality of the product, and the shape parameter characterizes its uniformity. The Weibull probability density function, the cumulative failure distribution, reliability, failure rate, and mean time to failure characterize the statistical data. Reliability tests should not be confused with qualification tests. Qualification tests evaluate if a product passes or not a specific test threshold. They have a predefined duration and aim to qualify a particular design. Qualification tests include a smaller sample size than reliability tests and render fewer failures. They have different duration and setups [33].

Typically, solder reliability testing considers different accelerated temperature profile in a test called Accelerated Thermal Cycling (ATC). ATC considers a homogenous temperature distribution through the assembly. An electronic device generates heat, the primary source being the silicon die. The integrated circuit dissipates this heat on one side through the joints, but also on the opposite side through the encapsulation material to the environment or various cooling devices. As a result, the temperature has an uneven distribution in the integrated circuit. In Power Cycling (PC), the silicon die is the only heat source [34], and the assembly is under thermoelectric stress.

The reliability test must produce the proper failure mechanism. For example, thermal shock tests do not accelerate fatigue failure mechanisms. Instead, they aim to generate unequal warpage of components and substrate through a rapid transition between hot and cold environments [32]. Figure 16 shows two test profiles, a thermal cycling profile (left) and a thermal shock profile (right). IPC9701B [10] specifies the thermal cycling test method for fatigue life characterization of SMD. Different temperature conditions apply depending on the intended use environment of the final product. The test duration should allow a minimum of 63% of the samples to fail. High and low-temperature dwell times should be no less than 10 minutes, and the temperature ramp rate should not exceed twenty °C/min.

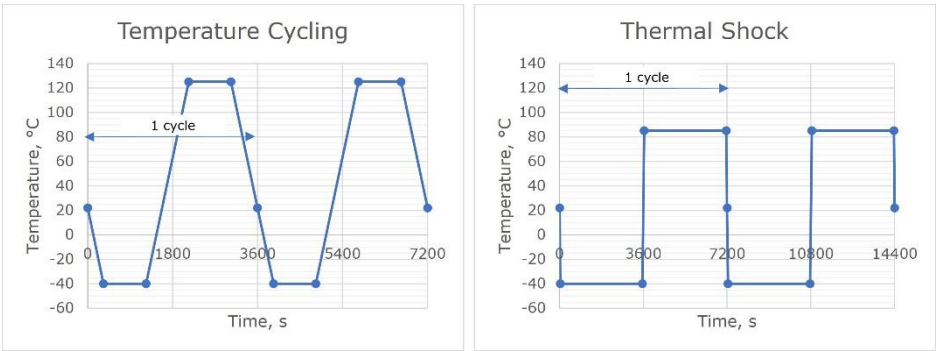


Figure 16 Left – temperature cycling profile (-40 ↔ +125°C, 11K/min, 10 min dwell) and right - thermal shock profile (-40 ↔ +105°C, 104K/min, 59 min dwell).

Accelerated reliability assessment tests aim to cause a failure mechanism to occur prematurely without inducing other mechanisms not specific to the environmental conditions of the tested device. The acceleration factors use the time to failure for a given stress level specific to a failure mechanism to determine the equivalent time to failure for a stress level specific to the environmental/use conditions. The acceleration factor, AF, can be determined with (3) [35].

$$AF = \frac{Time\ to\ failure\ (\sigma 1)}{Time\ to\ failure\ (\sigma 2)}, \qquad where\ \sigma 2 > \sigma 1 \tag{3}$$

Since the CTE varies slightly in the working range of electronics, the model in (4) is suitable for determining the acceleration factor. It considers only the temperature difference between the use environment and accelerated test conditions [35].

$$AF = \left(\frac{\Delta T_{use\ environment}}{\Delta T_{stress\ environment}}\right)^{-n} \tag{4}$$

where ΔT is the temperature excursion, and n is the material coefficient.

The Norris-Landzberg [36] acceleration factor accounts for the time-dependent behavior of materials. A common form is (5) [37], where ΔT is the temperature range in Celsius, f is the temperature cycling frequency, and T is the maximum temperature in Kelvin. The subscript T stands for test condition and o for operating condition. For example, for lead solders, q = 1/3, and c is between 1.9 and 2.0. Lall and Arunachalam [38] developed constants for lead-free assemblies. In [33], Lau summarizes variations proposed over time and constants for different solders and components.

$$AF = \left(\frac{f_o}{f_T}\right)^q \left(\frac{\Delta T_T}{\Delta T_o}\right)^c exp\left[1414\left(\frac{1}{T_o} - \frac{1}{T_T}\right)\right] \tag{5}$$

IPC-SM-785 [39] defines the acceleration factor as a function of the potential cyclic fatigue damage at complete stress relaxation, ΔD, in (6).

$$AF = \frac{N_f(use, 50\%)}{N_f(test, 50\%)} = \frac{[\Delta D(use)]^{\frac{1}{c(use)}}}{[\Delta D(test)]^{\frac{1}{c(test)}}} \tag{6}$$

In a board-level study, Denria et al. [34] analyzed the reliability of BGA IC solder joints under combined ATC and PC conditions. The study compares two types of dielectric materials used in printed circuit board construction, namely FR-4 and the Megtron series of materials used in high-frequency applications. The study also looks at the different deformations caused by PC versus ATC. For example, PC accentuates

in-plane bending due to uneven temperature distribution. Finally, they propose to analyze the reliability of solder joints by combining ATC with PC to obtain realistic and, at the same time, accurate results.

The experimental approach for determining solder joint reliability involves significant economic and time resources. Reliability tests can take anywhere from 1 to 6 months, depending on the tested component, and require many samples for analysis. The effort involved in preparing and analyzing these samples can be intensive and costly. However, it is essential to distinguish between reliability tests and quality tests. Reliability tests are necessary to determine the life distribution of a component, while quality tests focus on ensuring that the component meets specific performance requirements.

Accelerated tests are an important aspect of reliability testing. Accelerated tests simulate long-term use effects in a shorter period. The acceleration factors in the literature are linear, but it is essential to investigate other factors since they impact the cost-efficiency of reliability testing [33]. While reliability testing can be resource-intensive, it ensures that the solder joints in electronic components are reliable over their expected lifespan is necessary.

Virtual design enables engineers to create digital prototypes of electronic devices to optimize designs before building physical prototypes. Digital twins can monitor and analyze device behavior in real-time and predict future performance. Finally, machine learning can analyze large amounts of data generated during testing, identify patterns and correlations, and develop predictive models of device behavior. Combining these technologies makes it possible to accelerate the development of reliable electronic devices, reduce testing time and costs, and improve overall product quality.

Product-level reliability testing is a challenging process compared to board-level reliability testing due to the increased complexity and variability of the tested product. The testing process for a product includes environmental testing to simulate everyday use and ensure the product meets industry standards for reliability. However, this testing can be expensive, time-consuming, and complicated due to the many components involved. Additionally, when a product fails during testing, it can be challenging to isolate the source of the problem.

Design for reliability (DFR) is an approach that can help mitigate the challenges associated with product-level reliability testing. DFR aims to design more reliable and durable products, simplifying the assembly process, reducing the number of components, and using consistent materials and processes across multiple production runs. This approach can reduce the complexity of testing, improve consistency, shorten testing times, and reduce costs. Additionally, DFR aims to design products that are easier to diagnose and repair, making it easier to isolate the root cause of failures during reliability testing.

Product-level reliability testing is challenging due to the complexity, variability, and cost. However, by adopting a DFR approach, manufacturers can design more reliable and durable products, making it easier to pass reliability tests and reducing costs associated with testing and warranty claims.

2.4 Design for Reliability

DfR in solder joint lifetime assessment involves selecting reliable materials, appropriate design and assembly processes, and proper testing methods to ensure that the solder joints meet the desired lifetime requirements. It also involves identifying and managing potential failure modes and factors that could affect the performance and durability of the joints. This analysis can compare different components and configurations through parametric studies [27], [34], [40], [41]. Furthermore, the assessment can identify critical solder joints susceptible to cracking based on accumulated deformation during temperature cycles, providing thus a basis for informed decisions during both circuit board design and testing stages and for investigating defects that arise during testing.

The theoretical board-level reliability assessment approach uses a fatigue model to predict the failure of solder joints. This model must define a physical measure that indicates failure, such as plastic strain or dissipated energy, and correlate it to a critical number of cycles.

The deformation mechanism described in [42] defines the maximum shear strain in (7), where ΔT represents the difference between the maximum and minimum temperature of the temperature cycle. Figure 11 shows the graphical representation of the rest of the parameters. Clech et al. [42] note that tangential strain values do not exceed 1° under low-cycle fatigue conditions, but it is sufficient to produce cracks in the solder joint. Thus, electrical defects occur at several hundred to several thousand cycles.

$$\Delta\gamma_{max} = \frac{L \cdot |\alpha_B \cdot \alpha_C| \cdot \Delta T}{h_s} \tag{7}$$

The literature provides several analytical and numerical approaches to determine the shear strain in solder joints stemming from different expansion behavior during temperature cycling and predict the solder joints' fatigue life.

According to Lau's definition in [33], "design for reliability" goals include improving reliability tests, optimizing cost, understanding the assembly's behavior, and comparing designs. Furthermore, the author emphasizes that the predicted life of a solder joint highly depends on modeling assumptions regarding geometry, materials, boundaries, structures' response, and the life prediction model. In conclusion, the predicted life is incomparable to life from reliability tests, considering the current literature's need for successful experimental verification. However, despite these limitations, modeling, and simulation can still be valuable tools for understanding the behavior of solder joints under different conditions and for comparing distinctive design options. It can also help guide the selection of materials and assembly processes to optimize reliability and reduce the risk of failure.

2.4.1 Analytical Approach

The Engelmaier – Wild [32] model presented in (8) estimates the mean fatigue life of leadless components by considering the cyclic total plastic shear strain range in the solder after complete relaxation, as shown in equation (9) [43]:

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma}{2\varepsilon'_f}\right]^{\frac{1}{c}} \tag{8}$$

$$\Delta\gamma = C\frac{L_D}{h}\Delta(\alpha\Delta T) \tag{9}$$

$$c = c_0 + c_1 * \overline{T_{SJ}} + c_2 * 10^{-2}\ln\left(1 + \frac{t_0}{t_D}\right) \tag{10}$$

$$L_D = \frac{1}{2}\sqrt{L^2 + W^2} \tag{11}$$

where ε'_f is the fatigue ductility coefficient, c is the fatigue ductility exponent determined with (10), T_{SJ} is the mean cyclic solder joint temperature, $T_{SJ} = 1/4(T_c + T_s + 2T_0)$, T_c, T_s are the steady-state temperatures for component (c) and substrate (s), T_0 is the temperature during off half-cycle, t_D is the half-cycle dwell time, C is an empirical "nonideal" factor, L_D is the distance from the neutral axis of the assembly to the outermost solder joint as in (11) and Figure 11, h is the solder joint height, α is the coefficient of thermal expansion and ΔT is the temperature range. References [6] and [20] discuss model constants in detail and offer an overview of sources that fit the model constants for various solder alloys. The IPC-D-279 [44] design guidelines cover the Engelmaier model and its limitations.

The Ansys® Sherlock software calculates the shear strain range according to (9) and then calculates the shear force on the solder joint using equation (12) [43].

$$(\alpha_2 - \alpha_1)\Delta T L_D = F\left(\frac{L_D}{E_1A_1} + \frac{L_D}{E_2A_2} + \frac{h_s}{A_sG_s} + \frac{h_c}{A_cG_c} + \left(\frac{2-\nu}{9G_ba}\right)\right) \tag{12}$$

where α, ΔT and L_D are the same parameters as in (9), E is the elastic modulus, G is the shear modulus, A is the area, h is the height (thickness), and a is the edge length of the bond pad. Subscripts 1 stand for component, 2 and b for the PCB, s for solder joint, and c for bond pad [45]. Combining these analytical strain determination models with FEA-based prediction models, such as Ansys Sherlock does, is an attractive approach due to its rapidity, lack of 3D modeling requirements, and ability to address certain caveats of the Engelmaier model, such as local expansion mismatch, die shadow area and package corners, and stiffness of assembly parts [43].

2.4.2 Numerical Approach

The reliability analysis of solder joints is a complex process that involves a nonlinear transient thermomechanical finite element analysis (FEA). During the pre-processing stage, the engineer creates the finite element model, which includes complex geometries and materials. The material properties modeling includes temperature dependence, isotropic or anisotropic plastic, or viscous behavior. Additionally, the modeler defines the multiaxial loads the solder joint will experience during its lifetime. In the processing stage, the analysis determines the development of plastic strain, stress, and temperature in the joint. Lastly, the engineer evaluates the FEA results in the post-processing stage to determine the solder joint's reliability. The analysis indicates the accumulated plastic strain and fatigue life through appropriate fracture mechanisms and criteria. Overall, the reliability analysis of solder joints is a highly specialized and technically demanding process. Producing accurate and reliable results requires careful diligence and expertise in materials science, engineering mechanics, and numerical modeling [19].

Engineers often use simplified geometries and material models that only partially capture the complexity of the real-world components to simplify the analysis. However, one of the main challenges is dealing with the nonlinear behavior of the materials involved, which can lead to significant changes in their properties under different loads, especially when dealing with complex phenomena like particle migration, oxidation, or polymerization. In addition, FEA typically only considers a limited number of loading cycles, which may reflect a different duration of cyclic loads experienced by the components in real-world applications [19].

At the product level, stresses caused by board bending, vibrations, or drop can cause cracks in the intermetallic phases. However, the leading cause of crack initiation and propagation remains the uneven expansion of materials due to temperature changes. Therefore, FEA considers temperature cycling as the conditions driving the stress and strain state changes. However, given the complexity of the finite element analysis and the simplifying assumptions implemented, the accuracy of the prediction models is challenging to achieve [19].

Syed [46] summarizes the development of a life prediction model for four elements, namely:

- A constitutive equation and material properties within the stress range applied.
- A methodology based on an appropriate fracture mechanism corresponding to the constitutive material model.
- Experimental results on actual components that include the considered fracture mechanism.
- Finite element analyses that calculate the response of the adhesive under different loading conditions.

The prediction models depend highly on the FEA results, so engineers must minimize or eliminate variations in mesh refinement, element type, and simplifying assumptions. In this direction, Syed proposes a set of rules in [47]:

- to model all solder joints with nonlinear behavior.

- to avoid sub-modeling and nodal constraints.

- to consider a coarse mesh for noncritical solder joints.

- to finely discretize critical solder joints, with at least two elements through the 25-μm layer at each interface.

Syed recommends considering creep strain energy density as the strength criterion, observing similar prediction model parameters regardless of the constitutive solder equation considered [47].

The materials commonly used in integrated circuit fabrication are silicon, metals (such as copper and aluminum), encapsulation materials, ceramics, solder alloys, and resin. Literature recommends including Ignoring the anisotropic behavior of silicon, as it can significantly impact stress levels. Anisotropy reduces stress by 15% compared to the assumed isotropic behavior of the silicon die. The properties of resins and thermoplastic materials can be determined through Dynamic Material Analysis (DMA) and Thermal Material Analysis (TMA), which can provide information on properties such as glass transition temperature, coefficient of thermal expansion, and stiffness as a function of temperature [31]. Injecting material between the component and the PCB is known as underfilling and protects the solder in vibration or drop conditions. However, the filler material expands and contracts under temperature cycling, causing axial stresses in the solder joints. Conventional lifetime prediction methods work well for board-level analysis without underfill. However, they do not work as expected with underfill because conventional prediction methods do not consider the axial stress state that occurs at the glass-transition temperature of the underfill, which plays a significant role in solder joint failure [40] [48]. Metals should follow an elastoplastic constitutive law.

Different creep laws describe the behavior of metals under different conditions, but no single law can accurately represent all types of creep behavior. For example, the power-law creep model describes the secondary creep behavior for solder alloys. In addition, equation (13) describes the steady-state creep strain rate [24].

$$\dot{\varepsilon_{ss}} = A\sigma^n e^{\frac{-Q}{RT}} \tag{13}$$

where A is a material constant, σ is the applied stress, n is the stress exponent, Q is the creep activation energy, R is Boltzmann's constant, and T is the absolute temperature [24]. Researchers employed various empirical models to obtain a solder material model, such as the Norton, the double power, and the hyperbolic sinusoidal creep models, or the Anand Viscoplasticity model.

The Norton Power Creep constitutive equation (14) describes the steady-state creep stage. The creep rate reaches a constant value and stays constant over time because strain hardening, and recovery effects are in equilibrium [33]. Table 2 shows the parameter values for several lead-free solder alloys. Equation (15) is the corresponding model in classic computer-aided engineering (CAE) tools, such as Ansys. The model parameters depend on alloy composition and sample preparation, as shown for the SAC405 flip-chip for new and aged [49] samples or sample types such as the SnAg PCB or flip-chip [49].

$$\frac{d\varepsilon_{cr}}{dt} = A\sigma^{n}\exp\left(\frac{-Q}{RT}\right) \tag{14}$$

$$\frac{d\varepsilon_{s}}{dt} = C_1\sigma^{C_2}exp\left(\frac{-C_3}{T}\right) \tag{15}$$

Parameter σ_n = 1 MPa	**A (s^{-1})**	**n**	**Q/R**
	C1	**C2**	**C4**
Sn4.0Ag0.5Cu Flip-Chip [49]	2.00E-21	18	9995
Sn4.0Ag0.5Cu Flip-Chip Aged [49]	1.00E-11	12	8996
Sn3.8Ag0.7Cu [50]	1.50E-09	8.2	9321
Sn3.8Ag0.7Cu0.03Ce [50]	6.20E-09	8	10503
Sn3.5Ag PCB [49]	4.00E-05	7	8455
Sn3.5Ag Flip-Chip [49]	5.00E-06	11	9598

Table 2 The Norton constitutive equation (14) (15) and parameter values.

The Double-Power Law (16) changes the Norton model by including a term describing the primary creep stage. During this phase, the strain rate decreases with time as the material undergoes strain hardening. At the same time, the material may undergo annealing or recovery, which is the process of reducing the internal stresses and defects in the material through thermal or mechanical means. The net effect of strain hardening, and recovery is the increase in the creep rate over time [33]. The combined time hardening creep model in (17) is the corresponding Ansys creep model. Table 3 shows the Wiese [49] [51] parameters for SAC and SnAg solder tested on PCB and bulk samples. For SAC405 parameters [49], Syed [47] developed two life prediction models discussed later in this chapter.

$$\frac{d\varepsilon_{cr}}{dt} = A_1 exp\left(\frac{-Q_1}{RT}\right)\left(\frac{\sigma}{\sigma_n}\right)^{n1} + A_2 exp\left(\frac{-Q_2}{RT}\right)\left(\frac{\sigma}{\sigma_n}\right)^{n2} \quad (16)$$

$$\frac{d\varepsilon_{cr}}{dt} = \frac{C_1 \sigma^{C_2} t^{C_3+1} exp\left(\frac{-C_4}{T}\right)}{C_3+1} + C_5 \sigma^{C_6} t exp\left(\frac{-C_7}{T}\right) \quad (17)$$

Parameter C3 = 0 σ_n = 1 MPa	**A1 (s^{-1})** **C1**	**n1** **C2**	**Q1/R** **C4**	**A2** **C5**	**n2** **C6**	**Q2/R** **C7**
Sn4.0Ag0.5Cu PCB [49]	4.00E-07	3	3223	1.00E-12	12	7385
$N_f = (0.1968\varepsilon_{cr}^{acc})^{-1}$ [47] $N_f = (0.0066w_{cr}^{acc})^{-1}$ [47]						
Sn4.0Ag0.5Cu bulk [51]	1.00E-06	3	4161	1.00E-12	12	7349
Sn3.5Ag bulk [49]	7.00E-04	3	5629	2.00E-04	11	11197

Table 3 The Double power law (Combined time hardening) constitutive equation (16) (17), parameter values, and related life prediction models.

The Hyperbolic Sine (18) or Garofalo – Arrhenius model (19), has the parameter values in Table 4 for some lead-free alloys. For the same alloy, researchers fitted different constants, as is the example for Sn3.9Ag0.6Cu and Sn3.5Ag in Table 4. Parameter values depend on the test method, strain rate, stress state, and temperature conditions. For the constitutive model developed by Schubert et al. [52], both the original authors and Syed [47], developed life prediction models shown in Table 4. The Garofalo-Arrhenius hyperbolic sine creep law models the secondary creep best, as it considers for the effects of temperature and stress on the steady-state deformation rate. However, it may not be proper for modeling the earlier stages of creep. The deformation behavior during those stages is typically more complex and dependent on other factors, such as microstructural changes and material properties.

In [46], Syed compared different creep curves [52] [49] [53] for SAC alloys and found that stabilized creep falls in a narrow range, despite differences in methodology and alloy composition. Syed noted that the models proposed by Schubert et al. [52] and Zhang et al. [53] predicted similar behavior at low stresses but diverged at stresses above 30 MPa. The double-power law model proposed by Wiese [49] predicted a reduced creep rate at low stresses but an increased creep rate at high stresses compared to the Schubert et al. [52] hyperbolic sine model, as shown in Figure 17. Given the narrow range over which the models varied, Syed concluded that either creep model suits the behavior of SAC alloys.

$$\frac{d\varepsilon_{cr}}{dt} = A_1[sinh(\alpha\sigma)]^n exp\left(\frac{-Q_1}{RT}\right) \quad (18)$$

$$\frac{d\varepsilon_{cr}}{dt} = C_1[sinh(C_2\sigma)]^{C_3} exp\left(\frac{-C_4}{T}\right) \quad (19)$$

Parameter	**A1 (s^{-1})**	**α (MPa^{-1})**	**n**	**Q1/R**	**E (MPa)**
	C1	**C2**	**C3**	**C4**	**v; α (ppm/K)**
Sn4Ag0.5Cu [54]	0.17	0.14	4.20	6875	
Sn3.8Ag0.7Cu Sn3.5Ag0.75Cu Sn3.5Ag0.5Cu Castin™ [52]	277984	0.02447	6.41	6500	E=61251–58.5T v=0.36; α=20
$N_f = 345(w_{cr}^{acc})^{(-1.02)}$ [52] $N_f = 4.5(\varepsilon_{cr}^{acc})^{(-1.295)}$ [52] $N_f = (0.0019w_{cr}^{acc})^{-1}$ [46] $N_f = (0.0069w_{cr}^{acc})^{-1}$ [47]					
Sn3.9Ag0.6Cu [53]	143.40	0.108	3.79	7567	E=24224–0.0206T α=16.66+0.017T
Sn3.9Ag0.6Cu [55]	441000	0.005	4.20	5412	E=74840–0.08T v=0.30
Sn3.8Ag0.7Cu [50]	3.25E+05	0.05	5.30	5800	3.25E+05
Sn3.8Ag0.7Cu0.03 Ce [50]	2.84E+05	0.02	6.10	6400	2.84E+05
Sn3.5Ag [56]	1.70E+10	22.30	11.30	H1=93 kJ/mol	
Sn3.5Ag [57]	18(553-T)/T	1/(6386-11.55T)	5.50	5802	

σ in psi

Table 4 The Hyperbolic sine (Garofalo) constitutive equation (18) (19) and parameter values, and related life prediction models.

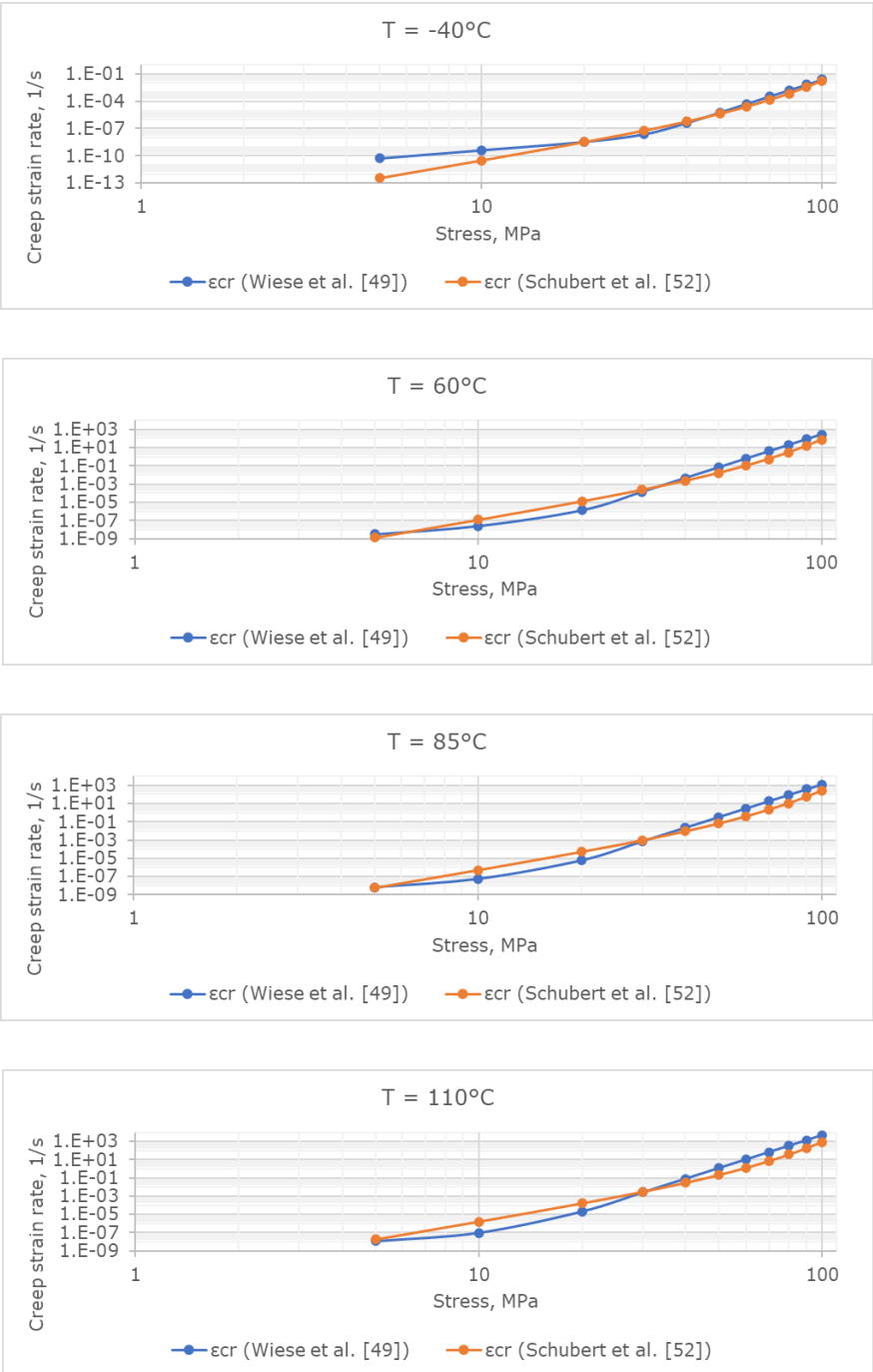


Figure 17 The predicted creep strains for Wiese et al. [49] SAC405 PCB double-power law model and Schubert et al. [52] hyperbolic sine model at -40, +60, +85 and +110°C.

The Anand Viscoplasticity [58] model is an internal variable-based model used to describe the deformation behavior of materials under both rate-dependent and rate-independent plasticity and temperature effects [33]. The model takes into account the deformation behavior of materials, including strain rate history effects, isotropic strain hardening, and dynamic recovery. The unified rate-dependent model uses nine parameters A, Q/R, ξ, m, h_0, $\hat{s}$, n, a, and s_0 [59]. Table 5 shows the Anand model parameter values for some lead-free solder compositions.

Equation (20) is the flow equation, linking the stress to the strain rate, where ξ is the multiplier of stress and m is the strain rate sensitivity. The model accounts for the material's previous deformation history by introducing an internal state variable, denoted by s, representing the material's deformation resistance. The constitutive equations for creep include an internal state variable, which reflects the material's previous deformation history [59]. Equation (21) is the evolution equation for the internal state variable s, where h_0 is a hardening/softening constant, and a is the strain rate sensitivity of hardening/softening. The model accounts for the hardening/softening effect through the initial value of the deformation resistance, s_0, which is the ninth Anand model parameter [59]. Equation (22) gives the value of B, where s* is the saturation value of deformation resistance s, associated with a set of given temperatures and strain rate as in (23), where $\hat{s}$ is a coefficient and n is the strain rate sensitivity for the saturation value of deformation resistance [59].

$$\frac{d\varepsilon_p}{dt} = Aexp\left(\frac{-Q}{RT}\right)\left[sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \tag{20}$$

$$\frac{ds}{dt} = \left\{h_0(|B|)^a\frac{B}{|B|}\right\}\frac{d\varepsilon_p}{dt} \tag{21}$$

$$B = 1 - \frac{s}{s^*} \tag{22}$$

$$s^* = \hat{s}\left[\frac{d\varepsilon_p}{Adt}exp\left(\frac{-Q}{RT}\right)\right]^n \tag{23}$$

Researchers determined the Anand Viscoplasticity model parameters by fitting the model to experimental data. They typically use for parameter estimation stress-strain curves obtained at different strain rates and temperatures. However, some researchers also used creep curves [60] obtained at various stresses and temperatures [33]. Therefore, to accurately predict the deformation of solders, it is needed to determine the model parameter values that best match the experimental data as in Figure 18. Figure 19 (right) shows the predicted stress for SAC405 compared to SAC305 from stress-strain and creep tests. Figure 19 (left) shows the predicted behavior for SAC-Q composition. Besides the alloy composition, the sample type influences the behavior as well.

Introducing the Anand model parameters into a finite element software, such as Ansys and Abaqus, allows the engineers to analyze the deformation of solder under different loading conditions.

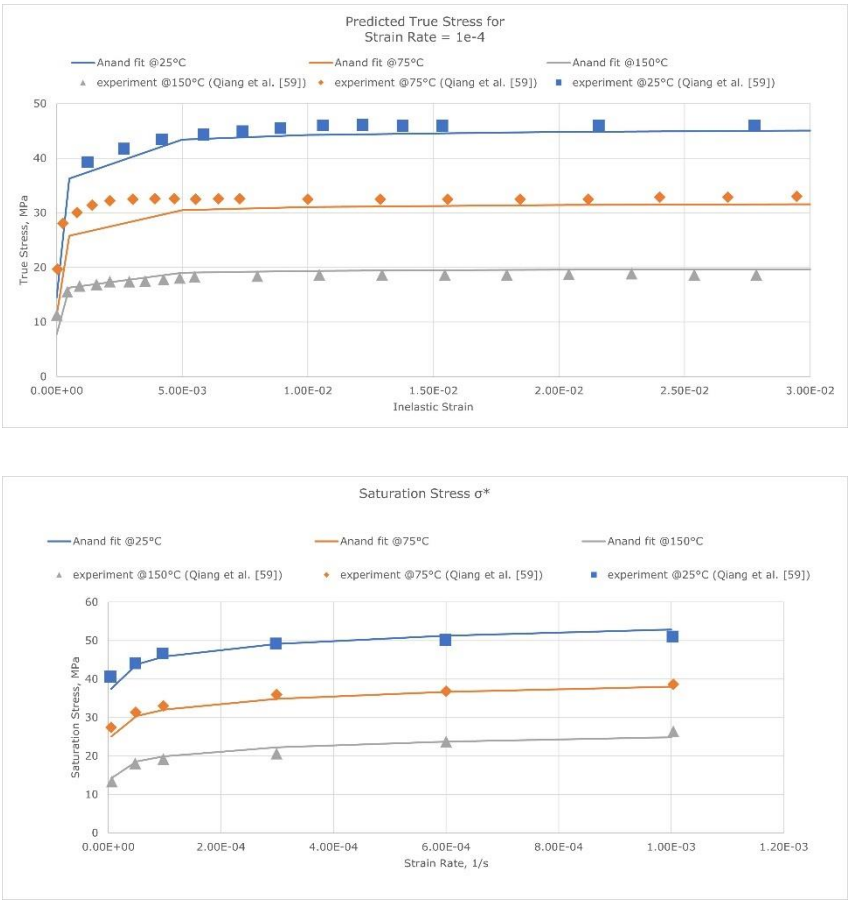


Figure 18 The predicted true and saturation stress at 25, 75 and 150°C for a strain rate of 1E-04/s of the Qiang et al. [59] SAC405 Anand model.

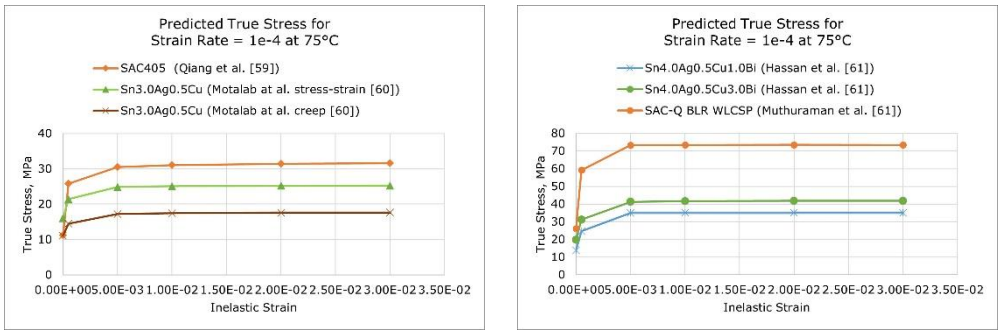


Figure 19 Predicted true stress for a strain rate of 1E-04 at 75°C for SAC405 [59], respectively SAC305 from stress-strain and creep data [60] (left) and for SAC-Q alloys with different contents of bismuth on bulk [61] and WLCSP [62] samples (right).

Parameter	s_0	Q/R	A	ξ	m	h_0	$\hat{s}$	n	a
Sn4.0Ag0.5Cu [59]	20	10561	325	10	0.32	8.00E+05	42.1	0.02	2.57
Sn4.0Ag0.5Cu [63]	22.25	10561	7128	10	0.8181	3.14E+04	30.45	0.00109	1.6
Sn3.0Ag0.5Cu stress-strain [60]	21	9320	3501	4	0.25	180000	30.2	0.01	1.78
Sn3.0Ag0.5Cu creep [60]	18.07	9096	3484	4	0.2	144000	26.4	0.01	1.9
Sn3.4Ag0.5Cu3.4Bi 10/s [22]	1.306	8256	2298	5.742	0.549	75794	37.231	0.0042	1.2805
Sn4.0Ag0.5Cu3.0Bi [61]	15.20	11400	11000	6	0.50	70000	31.40	0.0015	1.40
Sn4.0Ag0.5Cu2.0Bi [61]	26.50	9820	10200	6	0.31	95000	59.50	0.0044	1.08
Sn4.0Ag0.5Cu1.0Bi [61]	21.80	9950	8000	6	0.30	80000	53.00	0.0038	1.02
SAC-Q BLR WLCSP [62]	0.41	13509	2.45E+08	0.068	0.36	3522	0.64	0.056	1.24

$N_f = (14.1046E6w_{cr}^{acc})^{-0.4064}$

Table 5 The Anand model parameter values. Units: MPa, K, s-1.

Thambi [64] proposes a creep model capable of describing the creep deformation of a SAC alloy through mechanical dependence on microstructural characteristics. Equation (24) includes the sub grain size and Table 6 gives the term values for Sn3.8Ag0.7Cu. The mechanisms occurring when the solder paste dislocations interact with the Ag3Sn and Cu6Sn5 hardened particles drive the investigated behavior. Through microstructural analysis, Thambi presents the "Orowan climbing mechanism" and the "mechanism of dislocations separation from intermetallic compound particles" together with the interaction at the sub granular level as the apparatus controlling the strain rate of SAC alloys [64].

$$\dot{\varepsilon}_s = C_4 \frac{E}{T} (\lambda_{ss})^{-n_1 p} \left[1 + C_2 \left(\frac{\sigma}{E} \right)^{n_2} \exp\left(- \frac{(Q_c - Q_l) - (\alpha - \beta)\left(\frac{\sigma}{E}\right)}{RT} \right) \right] exp\left(- \frac{Q_l - \beta \left(\frac{\sigma}{E}\right)}{RT} \right) \quad (24)$$

Parameter	**Value for R^2 = 0.988**
α [kJ/mol]	79887
β [kJ/mol]	89465
Q_c [kJ/mol]	98.73
Q_l [kJ/mol]	114.67
Norm C_1/C_4 [-]	1.2E3
Norm C_2 [-]	4.5E3
n_1	3.51
n_2	1.8
R [kJ/mol.K]	0.008314
λ_{ss} [μm]	12.2
p	0.098

Table 6 The parameter values in equation (24) as determined by Thambi [64].

Table 4 shows some equations for the elastic modulus as a function of temperature. As Figure 20 shows, elastic properties depend on alloy composition, test methods, and sample preparation – see SAC405 [52] compared to [59]. Bismuth-doped alloys also show strain rate dependency, exhibiting higher modulus at higher strain rates [22]. Solder alloys lose up to 50% strength from room temperature to 125°C [61].

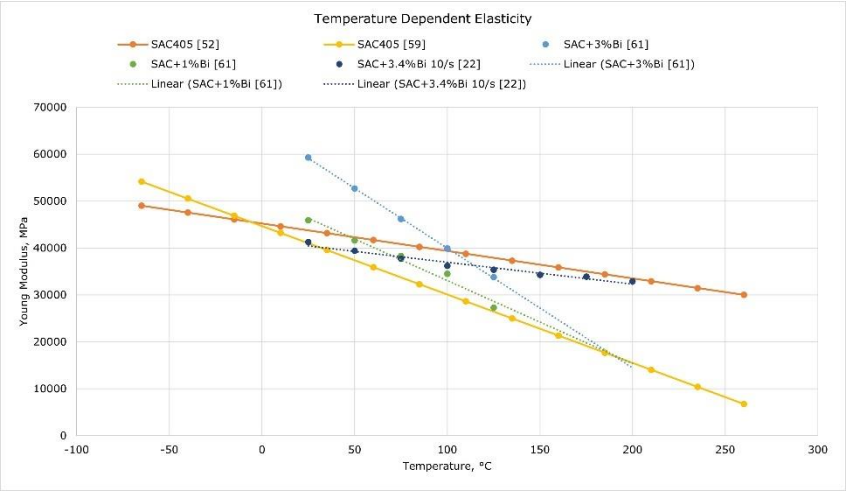


Figure 20 Temperature dependent elasticity of SAC solder alloys.

Metasch et al. [65] justify the need to consider primary creep due to the temperature changes, deformations caused by the CTE mismatch, and the stiffness of adjacent geometries and materials in the final product. Also, modern alloys have higher strength, showing reduced temperature-induced deformations, hence primary creep rather than secondary creep dominates the stresses in solder joints. Clech et al. [20] observed the need for models that incorporate the phenomena occurring at the microstructural level. Lead-free solders exhibit several microstructural effects, which can affect their performance in various applications. One effect is the formation of intermetallic compounds (IMCs) at the joint interface, which can increase the mechanical strength but may also cause brittle fracture or corrosion. Another effect is the coarsening of precipitates, which can reduce mechanical properties and increase susceptibility to cracking under thermal cycling or mechanical loading.

Additionally, the formation of a granular structure network in regions with high strain can lead to the formation of cracks through recrystallization. Optimizing the solder alloy composition by adding bismuth, antimony, or indium addresses some of the abovementioned effects. However, large-scale adoption of such alloys also requires characterizing these modern alloys, such as in [22], [61], and [62].

Table 3, Table 4, and Table 5 list only a small amount of the parameter values available in the literature for different alloys. Further references such as [63], [64], and [66] list inexhaustive parameter models for the aforementioned constitutive laws.

2.4.3 Fatigue Life Prediction

The constitutive equations implemented in the numerical analysis directly influence the results. Thus, the constitutive equation drives the choice of the empirical fatigue model [19]. Life prediction models are deterministic, probabilistic, and empirical simultaneously. The implementation of structural analysis generates the deterministic nature of the prediction models. Probabilistic models can determine the number of cycles up to a certain percentage of defects. The empirical nature of prediction models consists of introducing material constants and calibrating the models with experimental tests [35]. Syed [46] fits prediction models for SAC alloys based on the constitutive equations proposed by Wiese et al. [49] as in Table 3 and Schubert et al. [52] as in Table 4, respectively. First, using finite element analysis, Syed determines the creep strain accumulated during one temperature cycle and the creep strain energy. Next, he introduces the strength criteria in equations (25) and (26), where N_f is the number of cycles to failure, ε_{cr}^{acc} is the accumulated inelastic creep strain during one temperature cycle, $C' = 1/\varepsilon_f$ is the inverse of creep ductility, w_{cr}^{acc} is the accumulated creep strain energy density during one temperature cycle, W' is the creep strain energy density at failure and m' and m'' are exponents.

$$N_f = (C'\varepsilon_{cr}^{acc})^{-m'} \tag{25}$$

$$N_f = (W'w_{cr}^{acc})^{-m''} \tag{26}$$

Finally, he determines the parameters of the equations by fitting the curves to the experimentally obtained average lifetimes. Then, in [47], Syed updates the parameters to remove the variations brought about by finite element modeling while providing modeling guidelines. Muthuraman and Canete [62] fitted the SAC-Q WLCSP solder balls Anand model for the accumulated plastic energy density, as in Table 5.

The assumption underlying the prediction models proposed by Syed [47] is that the failure of solder joints under thermal cycling is primarily due to deformation accumulated during stabilized creep.

However, the Ansys Sherlock software analytically calculates with (27) the dissipated energy in the solder joints as a function of the shear force on the solder joint from (12) [43]. The application then determines the cycles to failure with (28) as determined by Syed in [46]. Nonetheless, the application lets the users update the fatigue coefficients based on their measurements, if necessary.

$$\Delta W = 0.50\Delta\gamma\frac{F}{A_s} \tag{27}$$

$$N_f = (0.0019\Delta W)^{-1} \tag{28}$$

Another widely used empirical approach is the application of a Coffin-Manson equation, based on either the accumulated creep strain in (29) or the creep strain

energy in (30), where θ_1 and θ_2 are the creep ductility coefficients and c1 and c2 are the fatigue exponents [52]. Schubert et al. [52] fitted the parameters for both criteria, as shown in Table 4.

$$N_f = \Theta_1(\varepsilon_{cr}^{acc})^{-c1} \tag{29}$$

$$N_f = \Theta_2(W_{cr}^{acc})^{-c2} \tag{30}$$

The strain energy density ratio (SEDR) approach is a commonly used method for predicting the lifetime of solder joints. In this approach, the failure of a solder joint occurs when the accumulated strain energy density ratio exceeds a specific critical value. The SEDR approach considers the strain energy density accumulated in the solder joint due to various loading conditions. Based on (30), SEDR takes the form in (31), where the subscript FailBaseCycle denotes the critical failure cycle and corresponding dissipated energy density [67]. The SEDR approach can be applied to different solder joints and consider the effects of different material properties, geometries, and loading conditions. The method involves calculating each loading cycle's strain energy density ratio and comparing it to the critical value. The critical value is typically determined experimentally using accelerated or simulation-based testing methods. One advantage of the SEDR approach is its simplicity, as it only requires knowledge of the material properties and loading conditions. However, its accuracy depends on the material properties' accuracy and assumptions made in the modeling process. Therefore, it is essential to point out that the approach has constraints and should be used with other techniques to assess solder joint reliability comprehensively.

$$N_f = N_{FailBaseCycle}\left(\frac{W_{cr}^{acc}}{W_{cr,FailBaseCycle}^{acc}}\right)^{-c2} \tag{31}$$

Reference [68] surveys the fatigue models used in solder joint lifetime prediction based on numerically determined solder joint response. Lau [33] points out several modeling assumptions and parameters that go into predicting a structure's life, including geometry, materials, boundary conditions, and the chosen life prediction model. These factors can significantly impact the accuracy of the predicted life and make it difficult to compare the predicted life to results from reliability tests. Additionally, there currently needs to be more successful experimental verification in the literature for these predictions, further complicating the issue. Given the numerous factors involved in predicting the reliability of a structure, it is essential to carefully consider each modeling assumption and parameter and their potential impact on the accuracy of the predicted life. Furthermore, experimental verification is necessary to ensure that the predicted life matches the actual life of the structure. Therefore, it is necessary to continue refining and improving life prediction models and to conduct more experimental tests to validate the accuracy of the predictions. Literature also proposes bending tests as an alternative to thermal cycling tests in [69] [70] [71].

2.4.4 System-Level Reliability

While board-level reliability focuses on the reliability of the second-level interconnects, system-level reliability considers the reliability of all parts, including the complete PCB assembly and the other mechanical parts which create the electronic device. System-level reliability testing is challenging and expensive, and therefore, design for reliability seeks to identify and mitigate potential failure modes and risks during the design phase.

The European project TRACE included studies about the superimposing effect of the mounting conditions on the electronic components' reliability, showing the major impact on the solder fatigue life [72]. Research on the impact of system-level constraints on the fatigue life of electronics show a possible reduction in life up to 60% [73].

One common application of SEDR is the system-level reliability analysis. For example, the critical failure cycle and strain energy density value are the board-level reliability evaluated lifetime and numerically determined solder joint response [67]. Board-level reliability analysis was also used as a baseline for layout optimization in [74].

Schempp et al. [11] [12] [75] propose the correlation of solder deformations with solder lifetime to propose a new methodology for lifetime prediction. The authors consider that system-level solder joint analysis could be more efficient for PCBs with high population densities, and designers must account for system-level effects. Thus, the new method would involve a parameter accounting for solder deformation at the solder-component and solder-PCB interfaces. The proposed parameter in [12] approximates the solder deformation by correlating the translations and rotations at the two interfaces. The authors demonstrate that the proposed system-level measurements can serve as a metric for a prediction model. Therefore, this approach can simplify the system-level analysis and reduce the cost and time required for lifetime prediction.

$$\Delta D = \Delta U + \Delta R \tag{32}$$

FEA is a powerful tool for predicting the behavior of complex systems, but it can also present challenges in system-level reliability analysis. One of the biggest challenges is the computational expense and difficulty in managing the models, which may involve multiple parts and materials. To overcome these challenges, engineers often turn to automation and use a combination of tools like Sherlock, Ansys, or Abaqus for pre-and post-processing to streamline the analysis and make it more efficient [76]. However, even with these tools, developing scripts to automate specific tasks is necessary [77]. One way to reduce the computational expense of FEA is to coarsen the mesh and find an appropriate technique without cutting back too much on numerical accuracy, which can compromise the results' quality. Therefore, it is crucial to balance accuracy and computational efficiency [78].

Another essential aspect to consider when using FEA for reliability analysis is PCB modeling. The challenges in PCB modeling involve capturing realistic warpage

and deformation in the solder joints, which can be crucial for predicting the system's reliability [79] [80]. The latest research in this field departs from the traditional Rule-of-Mixture methods and focuses on deep-learning modeling of the homogenized orthotropic material properties of the PCB. The deep learning approach involves training a neural network using substantial amounts of data to predict the material properties of the PCB. This method can capture the complex behavior of the PCB more accurately and efficiently than traditional methods [81]. In addition to the deep-learning approach, there is also interest in developing simulation methods and workflows within existing finite element analysis (FEA) software to standardize and shorten product development cycles [82] [83]. These methods can include assumptions of equivalent sections and copper trace mapping or modeling [84] [85].

Reference [86] discusses the impact of material modeling assumptions which happen inevitably due to the difficult communication along the value chain. Although even simplified models correctly predict the critical mounting position in the PCBA, non-linear and temperature-dependent characterization of the parts within the electronic package result in the most accurate prediction.

Reliability testing is an integral part of product development, as it helps achieve the required performance and safety standards. However, the cost of reliability testing can be high, especially for complex systems. Simulation plays thus a valuable role, as it allows engineers to predict the behavior of a system without the need for costly physical testing.

While theoretical analysis can provide valuable insights into system behavior, there are advantages and disadvantages to both theoretical analysis and testing. Theoretical analysis is faster and less expensive than physical testing, allowing engineers to explore various scenarios and design options. However, it is essential to validate theoretical analysis with physical testing to ensure accuracy.

On the other hand, physical testing provides real-world data on system behavior and can be used to validate theoretical models. However, it can be expensive and time-consuming, and testing every scenario or design option may be challenging.

The Heterogenous Integration Roadmap on Modeling and Simulation [87] emphasizes the challenges in the microelectronics industry, focusing on the importance of digital twin development. The microelectronics industry faces challenges in creating digital twins that can enable health assessment and management of electronic systems. Failures in microelectronics are often due to temperature-induced loads that lead to stress accumulation and eventual failure. Digital twins are needed to capture temperature and time-dependency effects, nonlinear behavior, multi-field/multi-domain requirements, multi-scale effects, and further standardization of the exchange format for model exchange. Deployment of the digital twin also requires consideration of the enormous volume of data generated, autonomous execution of simulation models, and life cycle management of the digital twin. Degradation criteria and performance indicators must predict specific parameters that may lead to failure. Researchers must consider the interaction of multi-degradation states and the potential degradation of the systems. In summary, much research must address these challenges in creating digital twins for microelectronics, enabling practical health assessment and management of electronic systems.

3 METHODOLOGY AND RESULTS

3.1 Research Design

The research aims to improve the reliability assessment of electronics for autonomous driving by developing a standardized simulation workflow beyond current methods, such as experimental testing and final product qualification. The focus is improving solder joint reliability to prevent recalls, field failures, and optimize the cost of design validation and quality testing. This research is significant because it addresses the growing demand for quality improvement strategies in the electronics industry, particularly for autonomous driving. By developing a standardized simulation workflow for predictive system-level reliability assessment, this research will enable engineers to optimize products by testing different scenarios, identifying potential issues, and tailoring design aspects according to the use environment, reducing the cost of ad-hoc testing. In order to develop a solution for the identified problem, the research methodology aims to answer the following research questions:

- How can virtual prototyping be used to improve the reliability of electronics?
- How can the stress state in solder joints be evaluated in the context of the system they are part of, moving from board-level to system-level reliability assessment?
- Can a simulation workflow be developed for system-level reliability assessment?

The research hypothesis is that one can create a simulation workflow for system-level reliability assessment by validating the simulation models at the board level. Following the developed workflow, the system-level analysis can identify the solder connections at risk of failure and suggest improvements.

The methodology involves experimental and theoretical board-level reliability assessment, system-level simulation, and the standardization and implementation of the proposed simulation workflow.

The experimental board-level reliability assessment includes three BGA parts. The parts are part of a Continental Automotive research project investigating the impact of various temperature ramp rates on solder fatigue cycles to failure. The samples were prepared and assembled at the prototype line in Seguin, Texas, United States of America, at a Vitesco facility and then tested at the Continental Automotive Qualification Laboratories in Deer Park, Michigan, United States of America. The scope of the experimental part is to understand the reliability test and data analysis and calibrate and validate the theoretical solder fatigue prediction methods.

The theoretical approaches involve the analytical BGA fatigue life prediction described in the former chapter. The goal of the analytical approach is first to understand the "classic" Engelmaier model and then to understand the applicability and accuracy of the Ansys Sherlock tool, which claims to semi-automatically assess solder fatigue. Further on follows the recommended FEA-based approach. This approach aims to understand component modeling intricacies and evaluate the accuracy of empirical life prediction models available in the literature.

In the system-level simulation, the aim is to assemble the parts on a PCB, emulate the boundary conditions of a housing and asses the influence of system-level factors over the fatigue life of the BGA parts.

In addition, the chapter addresses the simplifications considered, such as PCB homogenization, PCB population modeling, contact formulation and meshing choices. In order to validate the proposed workflow, throughout the study, we performed solder joint reliability assessments of several parts on different projects. Finally, we compared the simulation assessment to the design validation test results and discussed the actions triggered by simulations and their consequences.

Following the validation period, the integration of the proposed simulation workflow took place in the form of a process addressing decisions such as selecting parts for simulations, interactions within the different disciplines and providing step-by-step training materials for the simulation engineers performing the task.

In addition, to develop the workflow, the research collects qualitative data and combines quantitative and qualitative research methods. The qualitative research methods used in this study include interviews and discussions with experts within the Continental organization (Romania, Germany, USA, Singapore, and India) and industry (NXP, Infineon, Xilinx, Micron, Renesas, AT&S), and academic and research members (Fraunhofer Institute, PCCL, Politehnica University from Bucharest, Politehnica University Timisoara), focus group discussion within Continental, and a document analysis of relevant literature. The focus group discusses the challenges and approaches in solder joint reliability assessment. The document analysis involved reviewing relevant literature on the reliability assessment of electronics. The network within the company involves experts in various disciplines, such as FEA, simulation and validation, thermal analysis, complex packaging, soldering and new product launch. The focus groups include FEA specialists and experts. Within the research activities, a communication channel opened with part suppliers, packaging experts and experienced simulation engineers on the suppliers' side. The interviews focused on the following topics:

- electronic components and PCB modeling,
- post-processing techniques,
- sanity checks techniques,
- component types, their parts and known behavior,
- manufacturing processes,
- data storage and supply chain,
- material measurements and test design.

The author did not perform all experiments included in the thesis but worked for three weeks in the quality assurance laboratory at Continental Temic, Ingolstadt, Germany to learn the test and cross-section analysis procedures.

A potential research limitation includes the need for previous experience in the field, potentially leading to overlooking specific factors that more experienced researchers might have considered and formulating inaccurate assumptions due to lack of experience. Most data collection and analysis is cost-effective as independent research without specific funding or research project.

The mitigation of this potential bias included consulting with experts in the field and attending conferences and courses to broaden the understanding of the research area. However, another potential bias in this study is the selection bias in the qualitative research methods. For example, the experts and the focus group were chosen based on their availability and willingness to participate, which may have resulted in a sample not representative of the entire population of experts in the field. Another potential bias is the confirmation bias in the quantitative research methods, where preconceived ideas about the performance of the packages may have influenced the analysis. To mitigate these biases, we tried to ensure that the research methods were rigorous, and objective and that the data was analyzed and interpreted carefully.

Overall, the combination of quantitative and qualitative research methods provides a comprehensive understanding of the reliability assessment of electronics. In addition, the potential biases were considered and addressed to the best of our ability.

3.2 Board-Level Reliability Assessment

3.2.1 Experimental Approach

The experimental approach in this thesis aims to determine the board-level reliability of three BGA parts. The parts are part of a Continental Automotive research project investigating the impact of various temperature ramp rates on solder fatigue cycles to failure. Although the project includes many types of components, different solder pastes and tests under different thermal cycling, this thesis considers only three components mounted with one solder paste under one thermal cycling profile. The samples were prepared and assembled at the prototype line in Seguin, Texas, at a Vitesco facility and then tested at the Continental Automotive Qualification Laboratories in Deer Park, Michigan, United States of America.

The test included 16 PCB boards having two of each of the selected parts mounted with SAC305 solder alloy. Thus, the test included thirty-two samples of each part. Figure 21 shows the Continental test board and the parts included in this research. The printed wiring board in Figure 21 is a 135x65x1.60 mm board, with six conductive layers as shown in Figure 22.

CVBGA and CTBGA are very thin, respectively thin Chip Array Packages, and WLP is a Wafer-Level Package. The number indicates the inputs and outputs (I/O) – solder balls. In all packages, the I/O follows a perimeter pattern and not a full array of connections, meaning there are no solder balls under the silicon die area. Table 7 shows the package parts dimensions.

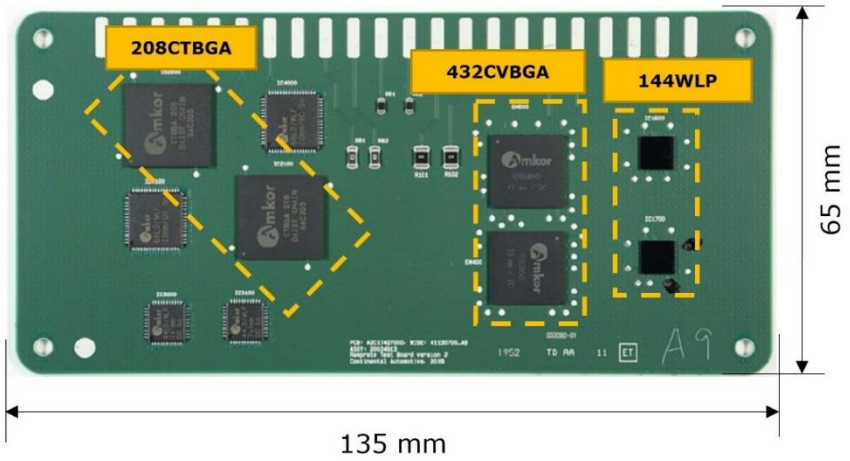


Figure 21 The test board with marked components included in this study. Image used courtesy of Continental AG.

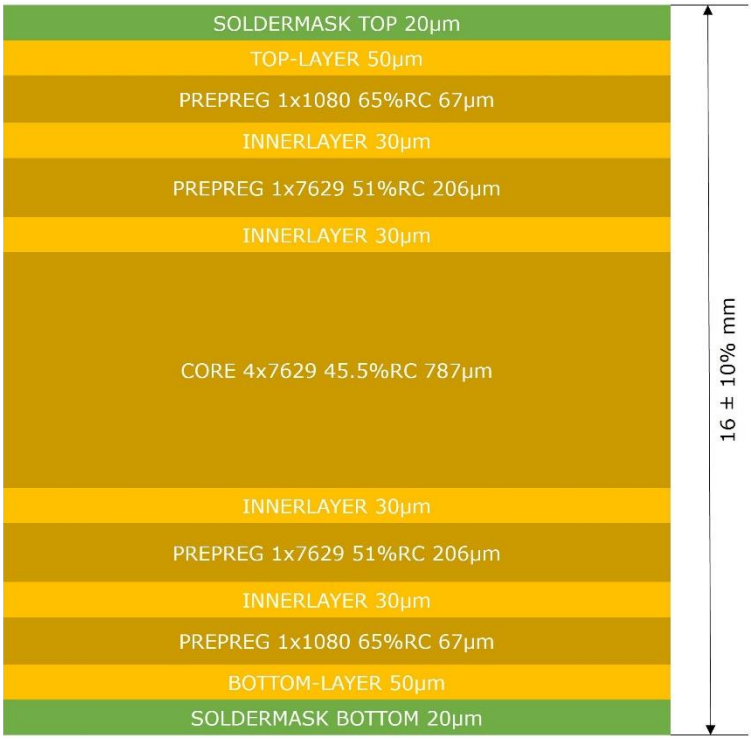


Figure 22 Test board stack-up, layer construction and thickness.

Package	Substrate	Die	Mold	Solder Ball	Pads		Pitch
	LxWxt	LxWxt	t	Dxh	D_{pkg}	D_{PCB}	
WLP144	n/a	5.96x5.96x0.400	n/a	0.256x0.192	0.199	0.247	0.40
CVBGA432	13x13x0.198	9.92x9.92x0.175	0.452	0.254x0.180	0.225	0.200	0.40
CTBGA208	15x15x0.250	12.84x12.84x0.22	0.580	0.419x0.277	0.385	0.331	0.80

Table 7 Package Attributes. All dimensions are in millimeters, mm. L = length, W = width, t = thickness, h = height, D = diameter.

Wafer Level Packaging technology creates the package for the chip directly on the silicon wafer rather than creating it separately and then attaching it to the chip as shown in Figure 23 top. As a result, WLP allows for a compact size, ideal for applications with limited space, such as high-density mounting. WLP also eliminates wire bonding, simplifying thus the packages. Instead, it uses copper posts to form the electrodes as in Figure 23 bottom [88].

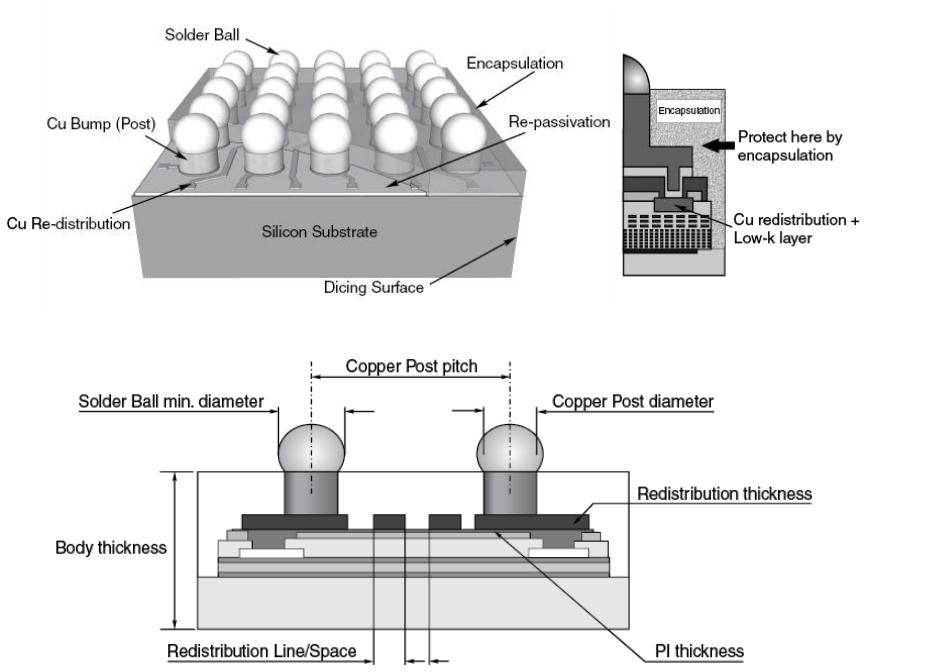


Figure 23 Top: Wafer Level Packaging schematic. Bottom: Detail view showing the cross-section schematic [88].

The thin and very-thin BGA packages feature a thin core substrate and ultra-thin mold caps, resulting in an overall thin package, as shown in Figure 24 top. Wire bonds connect the silicon die to the solder balls grid array as in Figure 24 bottom [89].

The experiment used dummy, non-functional components for prototyping, testing, and qualification purposes. These dummy components have the same form factor as their functional counterparts, allowing engineers to evaluate the performance of the package in their designs without the cost and complexity of using a functional device. In addition, the components come with a daisy chain net topology for testing purposes, as shown in Figure 25 in the bottom view of the 144WLP.

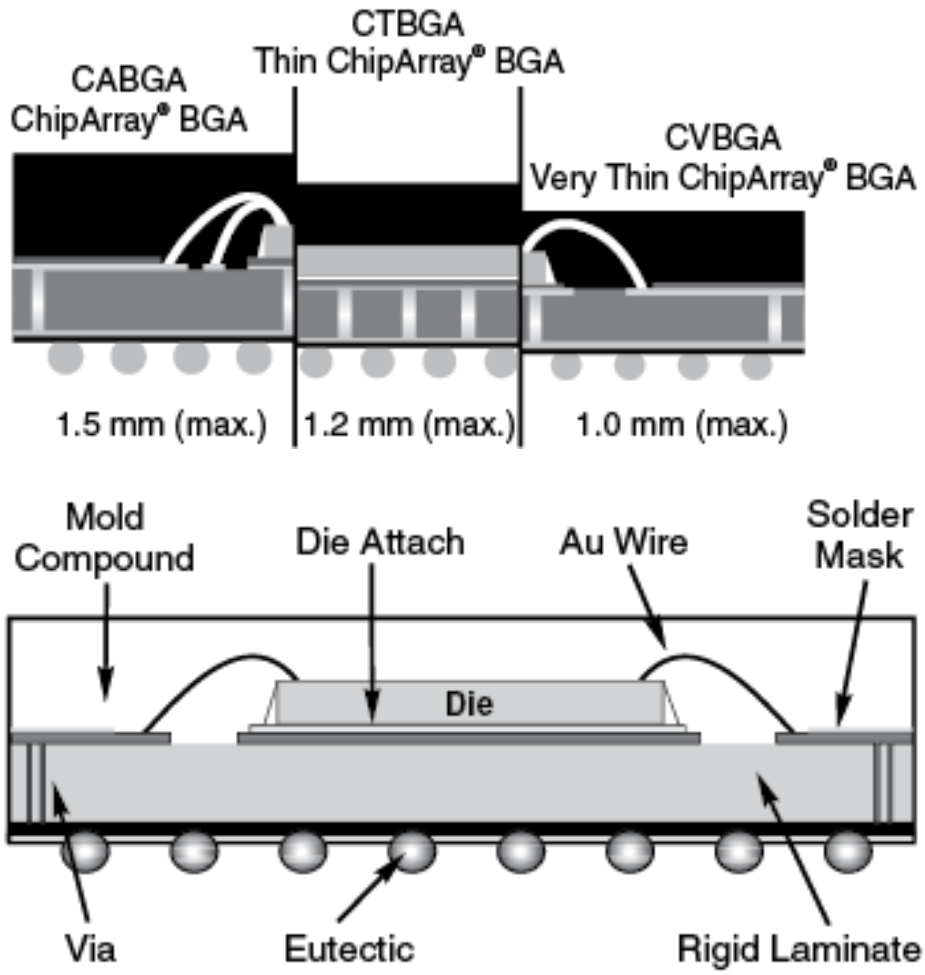


Figure 24 Top: BGA schematic showing different thickness packages (CABGA, CTBGA and CVBGA). Bottom: Schematic of a BGA cross-section [89].

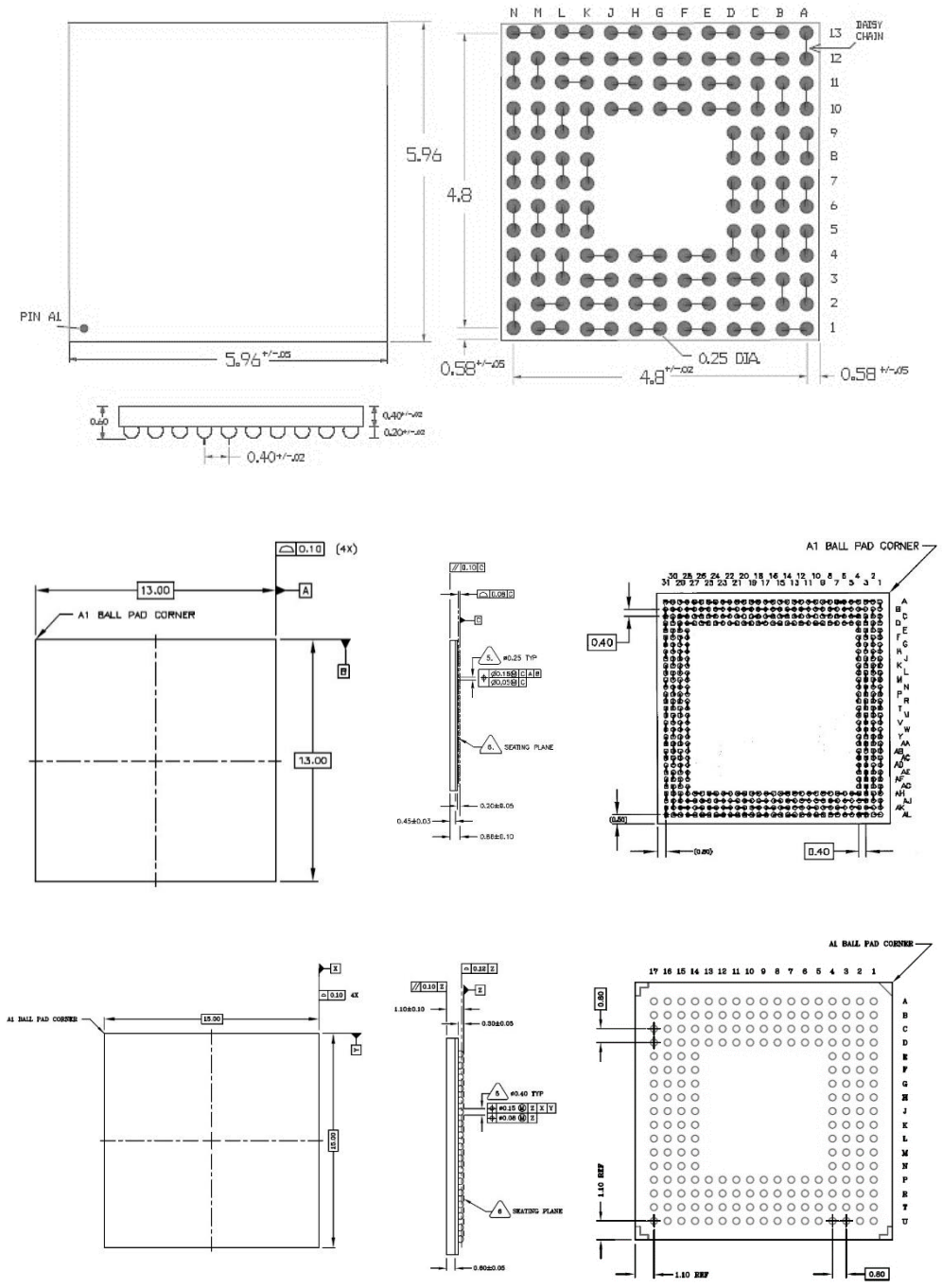


Figure 25 Package drawings showing the top, bottom, and side view for WLP144 (top) [88], CVBGA432 (middle), and CTBGA208 (bottom) [89].

A daisy chain connection is an electrical connection where multiple devices or components are connected in a series using a single wire or conductor as in Figure 26. In this case, the daisy chain connection monitors the electrical failure of a specific test point by linking it through solder joints to the ground. Figure 27 shows the daisy chain connections of the test board.

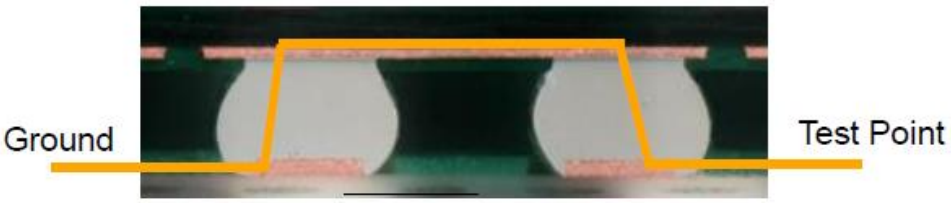


Figure 26 Schematic of a daisy-chain connection. Image used courtesy of Continental AG.

The set-up takes readings of the electrical resistance of the test point every 10 seconds. The event threshold is 300 Ohms, which means that if the electrical resistance of the test point rises above this level, it will be considered a failure. IPC-785 [39] standard defines the failure criteria for this test. Specifically, it must detect ten opens (i.e., discontinuities in the electrical connection) within 10% of the cycle number at the first failure on that channel. So, for example, if the first opening happens at 100 cycles, the subsequent 9 opens must occur before 110 cycles to meet the failure criteria. This failure criterion helps to eliminate noise from being detected as a failure, ensuring that all ten failures occur within the same cycle. However, if the failures occur over an extended time, they may be due to environmental factors or other issues unrelated to the specific test point.

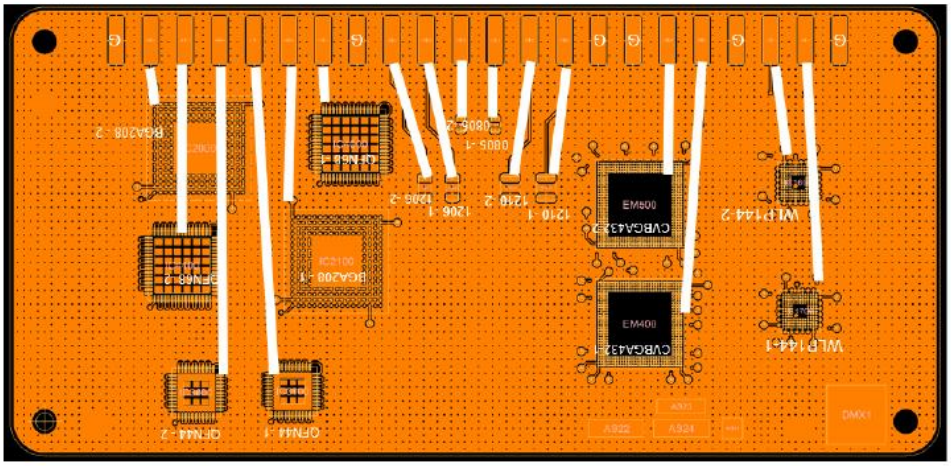


Figure 27 Schematic representation of the daisy-chain connections on the test board. Image used courtesy of Continental AG.

Figure 28 shows the thermal cycling test used in the BLR test. The temperature cycles is from -40°C to +125°, with a ramp rate of 5°C/min. The minimum and maximum dwell times are 15 min, resulting in a 96-minute cycle, typical for most European car manufacturers (VW 80000, BMW GS 95024-3-1, MBN LV 124-1). The test vehicles sit in a thermal chamber with rapid thermal cycling capability for the thermal cycling test, as in Figure 29.

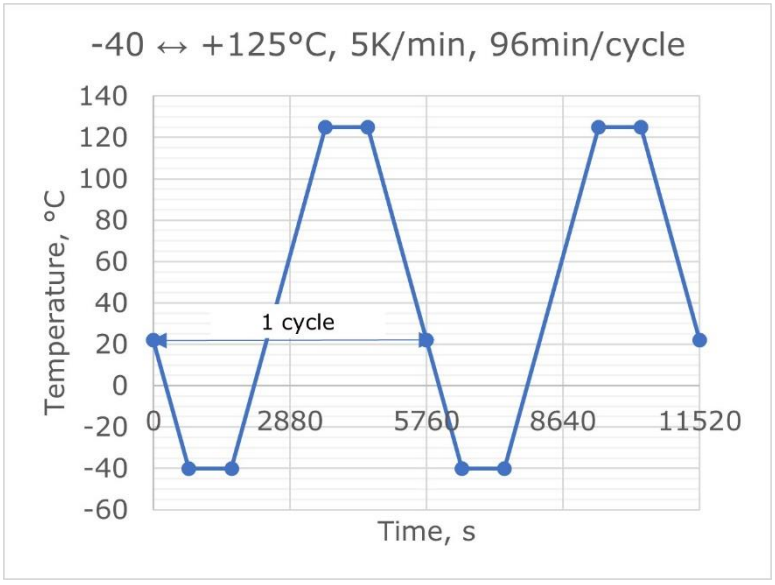


Figure 28 The thermal cycling test condition used in the BLR tests.

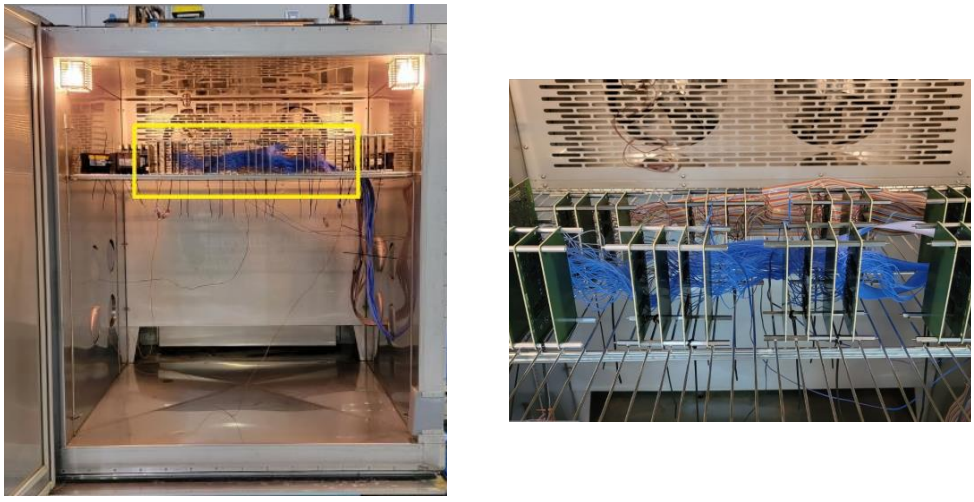


Figure 29 Left: Image of the test chamber with boards mounted inside. Right: Zoom in on the test vehicles in the test position. Images used courtesy of Continental AG.

The Weibull distribution is a statistical model commonly used to describe solder fatigue failure distributions. The distribution allows for predicting the percentage of failures at a given time through two parameters, namely the shape and scale parameters. The shape parameter indicates the type of failure mode, ranging from early failures to wear-out failures. In contrast, the scale parameter measures the average time to failure and is the 63.2 percentile of the distribution.

Figure 30 plots the test failure data (Weibull Probability Plot) processed in the Minitab® Statistical Software 18. In analyzing test failure data, a 95% confidence interval determines the upper and lower bounds. The 63.2 percentile gives the characteristic life of the parts, as shown in Figure 31. The Anderson – Darling parameter indicates the goodness of fit for the selected statistical distribution. Table 8 shows the parameter estimates for the two-parameter Weibull distribution considered.

The experimental BLR test results' data analysis indicates a characteristic life of 162 cycles for the WLP144, 512 cycles for the CVBGA432, respectively of 786 for the CTBGA208. The shape parameters greater than 4 for the WLP144 and CVBGA432 indicate that a wear-out mechanism drives the failures. However, the slope of 3.55 for the CTBGA208 suggests that the distribution is between a "normal" distribution (slope of 1) and a "wear-out" distribution (slope greater than 4) and may indicate that the failure mechanism is a combination of factors. An AD parameter lower than 1 suggests that the chosen two-parameter Weibull distribution fits the experimental data well. The AD parameter higher than one suggests that the data deviates slightly from the expected Weibull distribution, but the deviation is insignificant. The shape of 3.55 and the Anderson-Darling parameter of 1.15 suggest that the CTBGA208 data may exhibit a combination of random and wear-out failure modes. However, overall, the data fit the Weibull distribution well. The lack of overlapping confidence intervals suggests that the three tests differ significantly.

Typically, cross-section analysis confirms the failure modes identified by the statistical analysis. For this particular project, because of its actual size (four temperature cycles, two solder pastes and twenty-one parts), cross-section analysis results at the time of drafting the thesis are available only for one of the temperature conditions, which is not the one considered in this thesis. However, Figure 32, Figure 33, and Figure 34 show examples of cross-section analysis indicating the fractures in the A1 solder ball of each part.

Part	Shape	Scale	Lower Bound	Upper Bound	AD
WLP144	6.05	162	151	173	0.756
CVBGA432	7.24	512	487	537	0.962
CTBGA208	3.55	786	710	869	1.149

Table 8 2-P Weibull Parameter Estimates.

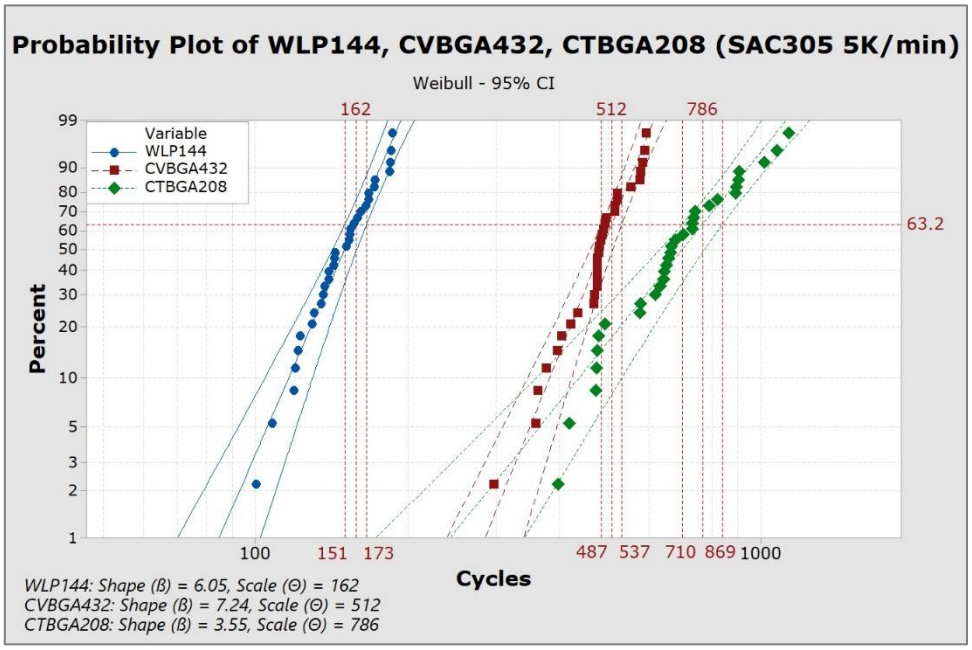


Figure 30 Weibull probability plot of the WLP144, CVBGA432 and CTBGA208 failure data for SAC305 under the thermal cycling condition -40 ↔ +125°C, with a ramp rate of 5K/min. The reference lines show the scale parameter values and upper and lower bounds.

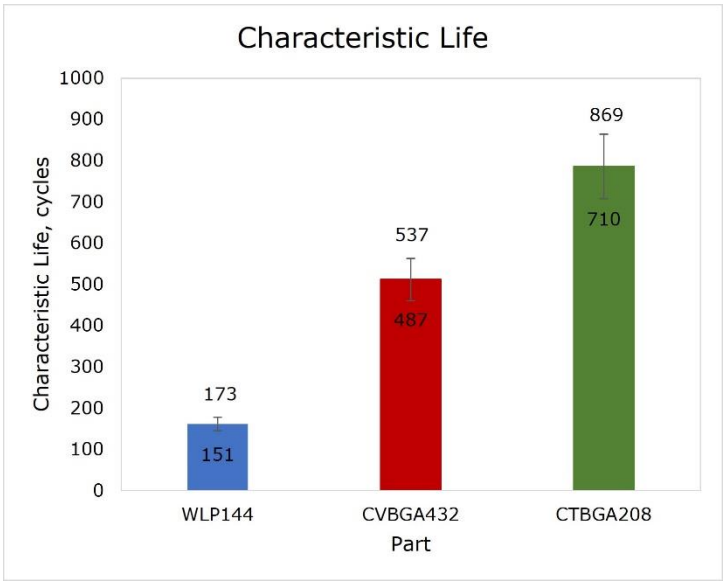


Figure 31 Characteristic life of the tested parts. The error bars indicate the lower and upper bounds of the scale parameter for a confidence interval of 95%.

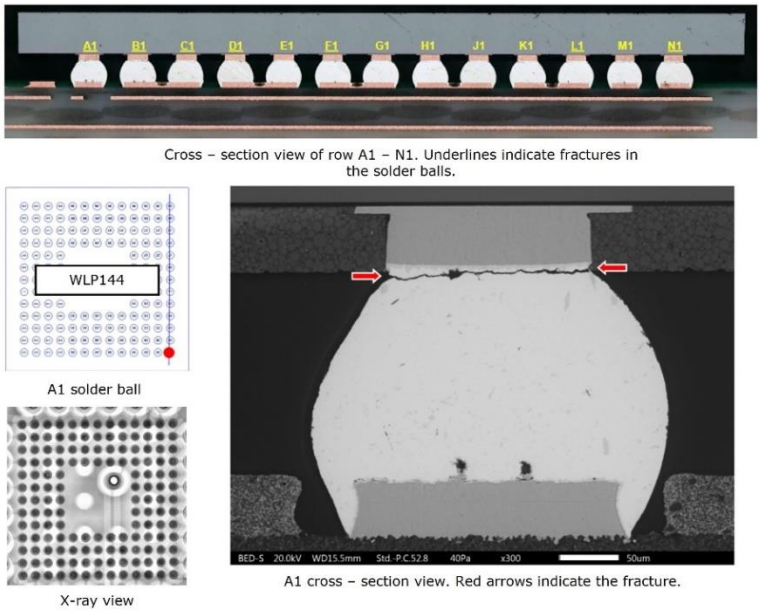


Figure 32 Cross-section analysis of solder ball A1 in WLP144. Image used courtesy of Continental AG.

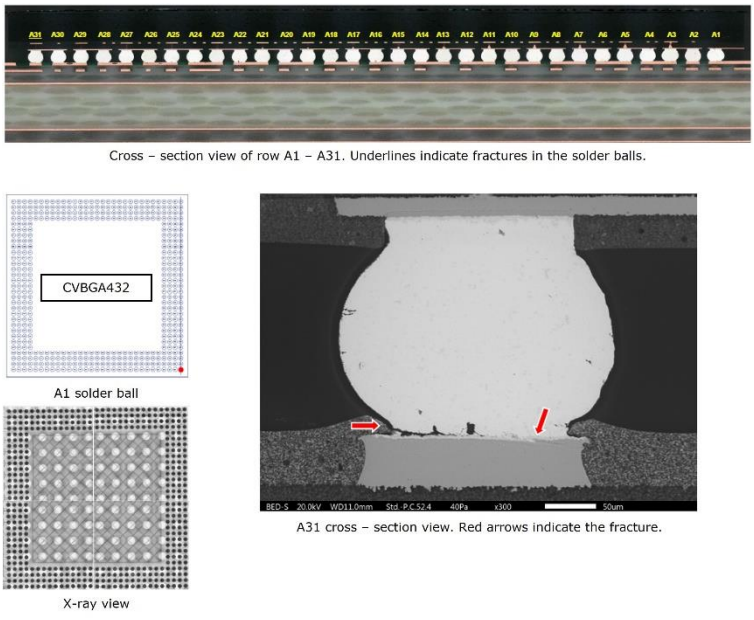


Figure 33 Cross-section analysis of solder ball A31 in CVBGA432. Image used courtesy of Continental AG.

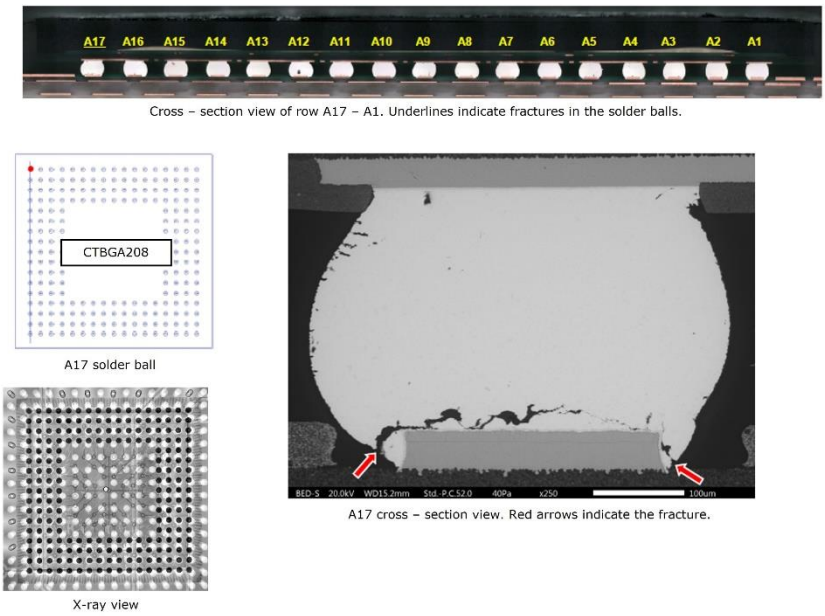


Figure 34 Cross-section analysis of solder ball A17 in CTBGA208. Image used courtesy of Continental AG.

Besides the lifetime test, the laboratory determined the mechanical properties of the parts through experimental procedures. DMA (Dynamic Mechanical Analysis) determined the in-plane storage modulus of the PCB on a representative sample for the average copper density and the mold compounds of the CVBGA432 and CTBGA208. TMA (Thermomechanical Analysis) determined the CTE and glass transition temperature, Tg.

In a tensile DMA test, the storage modulus, E', represents the material's stiffness under dynamic loading conditions, specifically in tension, and the loss modulus, E", measures the dissipated energy. E' characterizes the elastic behavior. At the same time, E" defines the viscoelastic behavior. The phase angle, δ, is the ratio of the loss modulus to the storage modulus. It indicates the relative amount of energy converted into heat during cyclic deformation [90]. A higher tan(δ) value indicates a higher damping capacity or energy dissipation of the material, while a lower tan(δ) value indicates a more elastic or less dissipative behavior.

The laboratory reported a tan(δ) between 0.01 and 0.1 in the 25 to 220 °C temperature range, suggesting that the loss factor is small. In this case, we assume linear elastic behavior and the storage modulus, E', to be an approximation of the elastic modulus, E. Figure 35 shows the temperature dependency of the in-plane E-modulus of the PCB. The reported Tg of the PCB is 190°C, out of the considered temperature cycling range, and the in-plane CTE before Tg is 15.20 ppm/°C, respectively 24.9 ppm/°C for the out-of-plane orientation.

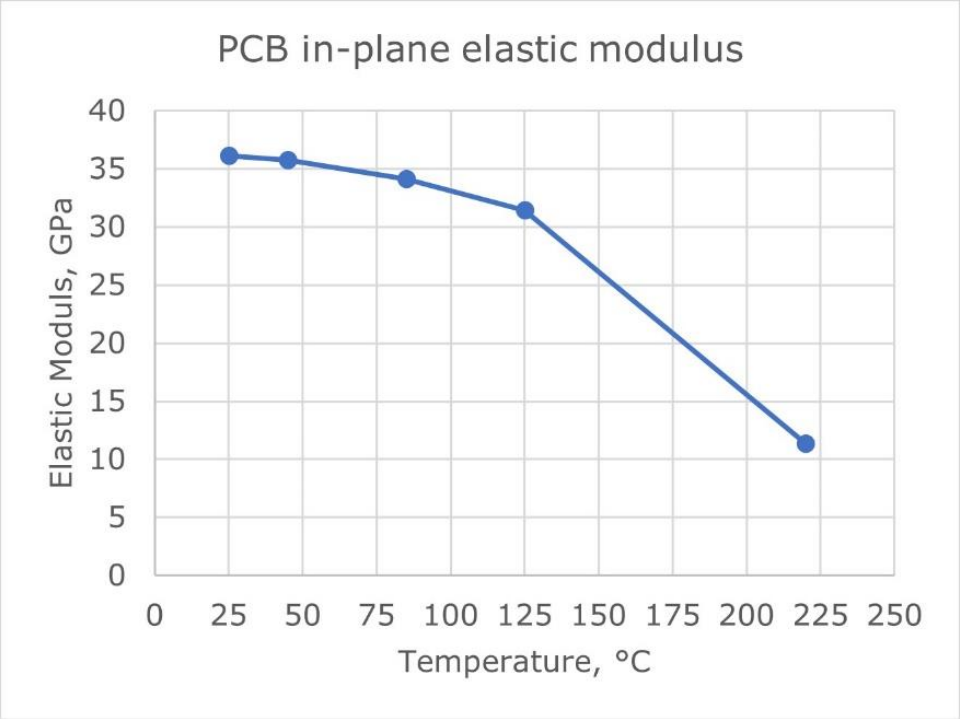


Figure 35 Approximation of the in-plane elastic modulus based on the tensile DMA test of a representative sample.

Table 9 shows the measured material properties for the PCB and plastic molded BGA parts. The encapsulation material for the plastic molded BGAs presents a temperature – dependent behavior within the thermal cycling temperature range.

Part	**CTE, ppm/°C**	**Tg, °C**	**E, MPa**
PCB (25°C, before Tg)	XY: 15.20	190	XY: 36134
Overmold CVBGA432 (before Tg)	25-85°C: 8.9 115-127°C: 14.3	129	15000
Overmold CTBGA208	before Tg: 9.1 after Tg: 24.10	118	20000

Table 9 Measured material properties.

3.2.2 Theoretical Approach

Under the theoretical approach, we first determine the fatigue life of the parts described in 3.2.1 using the analytical Engelmaier model described in 2.4.1. We also use the Ansys Sherlock tool, which determines the shear strain with a modified Engelmaier equation as in 2.4.1. Further, we use FEA to determine the failure criteria and estimate the fatigue life of the parts, as described in 2.4.2 and 2.4.3.

Table 10 compares the input parameters of the considered approaches, and Figure 36 schematically represents the assumed geometries. The orange checkmark in Table 10 suggests that the method accounts for the respective property, but in a simplified manner, or not for all the listed properties under the category. For example, the Engelmaier model accounts for the length and width of the package in the distance to the neutral axis parameter. It considers the CTE but not the Young's modulus and Poisson's ratio regarding material properties.

The Engelmaier model considers only the external dimensions of the part. Regarding material properties, it considers one overall CTE for the part and one for the PCB. It accounts for a specific solder through various empirical coefficients, totaling three material parameters. Apart from the other two approaches, it accounts for the operating temperature of the part through the mean solder joint temperature parameter. Although Sherlock is still an analytical method, it accounts for more parameters than the classic Engelmaier. Sherlock also considers a second failure location in the die shadow joint. The FEA approach is the most complex, and the input parameters depend on the level of detail considered.

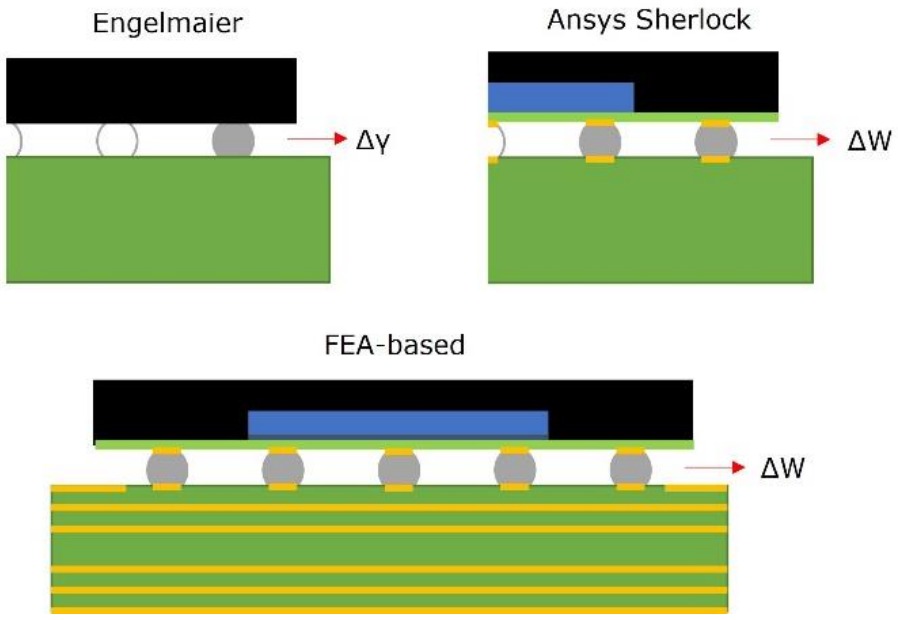


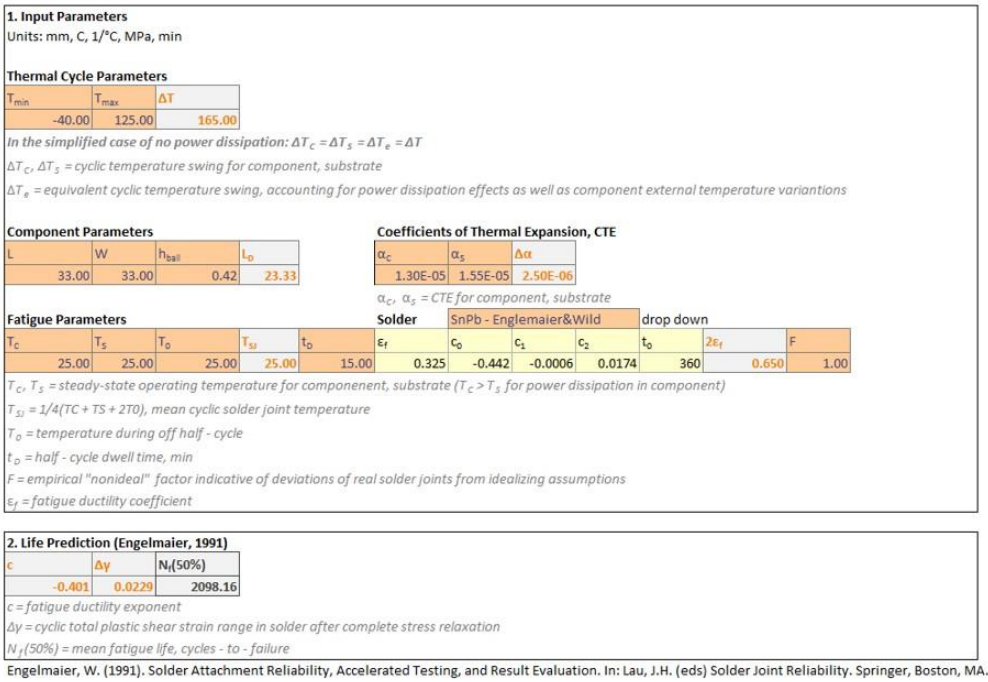
Figure 36 Schematic of the geometry models in the theoretical approaches.

Input Parameters	Engelmaier	Ansys Sherlock	FEA-based
Geometry			
Substrate (L, W, h)	✓	✓	✓
Die (L, W, h)	✗	✓	✓
Overmold / Lid (h)	✗	✓	✓
Solder ball (D, h)	✓	✓	✓
Pads (D_{PKG}, D_{PCB})	✗	✓	✓
Number of joints	✗	✓	✓
PCB (h)	✗	✓	✓
Other (die attach, TIM etc.)	✗	✗	✓
Material			
Substrate CTE, E, v	✓	✓	✓
Die CTE, E, v	✓	✓	✓
Overmold CTE, E, v	✓	✓	✓
PCB CTE, E, v	✓	✓	✓
Solder Composition	✓	✓	✓
Creep	✗	✗	✓
Temperature dependency	✗	✗	✓
Viscoelasticity	✗	✗	✓
Anisotropy	✗	✗	✓
Boundary Conditions			
Peak temperatures	✓	✓	✓
Dwell time	✓	✓	✓
Operating status	✓	✗	✗
Ramp rate	✗	✗	✓

Table 10 Comparison of the considered input parameters in the theoretical approaches. L = length, W = width, h = height or thickness, D = diameter.

3.2.2.1 Engelmaier Life Prediction

The first step in using the Engelmaier life prediction model was implementing the formulas (8) through (11) in 2.4.1 in the spreadsheet calculator shown in Figure 37. Next, we checked the correctness of the implementation by reproducing a result in the literature. In this case, we used the reported input parameters in [91] and compared the outputs with the reported values in Table 11.



1. Input Parameters

Units: mm, C, 1/°C, MPa, min

Thermal Cycle Parameters

T_{min}	T_{max}	ΔT
-40.00	125.00	165.00

In the simplified case of no power dissipation: $\Delta T_c = \Delta T_s = \Delta T_e = \Delta T$

ΔT_c, ΔT_s = cyclic temperature swing for component, substrate

ΔT_e = equivalent cyclic temperature swing, accounting for power dissipation effects as well as component external temperature variantions

Component Parameters

L	W	h_{ball}	L_D
33.00	33.00	0.42	23.33

Coefficients of Thermal Expansion, CTE

α_c	α_s	$\Delta\alpha$
1.30E-05	1.55E-05	2.50E-06

α_c, α_s = CTE for component, substrate

Fatigue Parameters

Solder: SnPb - Englemaier&Wild (drop down)

T_C	T_S	T_0	T_{SJ}	t_D	ε_f	c_0	c_1	c_2	t_0	$2\varepsilon_f$	F
25.00	25.00	25.00	25.00	15.00	0.325	-0.442	-0.0006	0.0174	360	0.650	1.00

T_C, T_S = steady-state operating temperature for componenent, substrate ($T_C > T_S$ for power dissipation in component)

T_{SJ} = 1/4(TC + TS + 2T0), mean cyclic solder joint temperature

T_0 = temperature during off half - cycle

t_D = half - cycle dwell time, min

F = empirical "nonideal" factor indicative of deviations of real solder joints from idealizing assumptions

ε_f = fatigue ductility coefficient

2. Life Prediction (Engelmaier, 1991)

c	$\Delta\gamma$	$N_f(50\%)$
-0.401	0.0229	2098.16

c = fatigue ductility exponent

$\Delta\gamma$ = cyclic total plastic shear strain range in solder after complete stress relaxation

$N_f(50\%)$ = mean fatigue life, cycles - to - failure

Engelmaier, W. (1991). Solder Attachment Reliability, Accelerated Testing, and Result Evaluation. In: Lau, J.H. (eds) Solder Joint Reliability. Springer, Boston, MA.

Figure 37 Implementation of the Engelmaier model in a spreadsheet calculator. Orange cells represent the input parameters, grey cells represent calculations and outputs, and yellow cells contain the solder material related parameters.

Output Parameter	**c**	**Δγ**	**$N_f(50\%)$**
Reported [91]	-0.400	0.0229	2146.20
Calculated	-0.401	0.0229	2098.16
Difference (%)	0.250	0.00	-2.238

Table 11 Validation of the implementation of the Engelmaier model.

Although we get a 0.25% difference in the c parameter calculation and identical strain range, Δγ, the predicted life is 2.24% smaller than the reported value in the cited article. After thoroughly checking the model and formulas, we determine the difference from decimals and consider the implementation correct.

Further on, for the three BGAs described in 3.2.1, we assume unpowered thermal cycling under T_{min} = -40°C and T_{max} = +125°C, and $T_S = T_C = T_0$ = 42.50°C, resulting in T_{SJ} = 42.50°C and ΔT = 165. Table 12 shows the solder material parameters for the SAC305 considered alloy. Table 13 shows the other input and output parameters for the WLP144, CVBGA432 and CTBGA208 [43].

Parameter	**Value**
ε_f'	0.425
c_0	-0.480
c_1	-0.00093
c_2	0.0192
t_0	500
C	1

Table 12 Engelmaier model parameters for SAC305 [92].

First, for the WLP144, we assume the package CTE to be the CTE of silicon [93] because, as shown in Figure 23 , the package is a bare-die, wafer-level package. Then we consider the effective properties of the other two plastic molded packages considering the three-layer die region stack-up as in Figure 38. Finally, we determined the effective material properties considering the proportion of the layers using the formulas given in the Ansys Sherlock Theory Guide available in the Ansys Help Portal.

Figure 38 Schematic of the die region molded BGA stack-up and material properties of each layer.

Parameter	Unit	WLP144	CVBGA432	CTBGA208
Engelmaier Input Parameters				
t_D	min	15	15	15
L	mm	5.96	13.00	15.00
W	mm	5.96	13.00	15.00
h	mm	0.19	0.18	0.28
α_C	1/°C	2.60e-6	5.51e-6	7.40e-6
α_S	1/°C	1.52e-5	1.52e-5	1.52e-5
Engelmaier Calculated Parameters				
c (10)	-	-0.452	-0.452	-0.452
L_D (11)	mm	4.21	9.19	10.61
$\Delta\alpha$	1/°C	1.26e-5	9.69e-6	7.80e-6
Engelmaier Output Parameters				
$\Delta\gamma$ (9)	-	0.0457	0.0817	0.0494
$N_{f(50\%)}$ (8)	**cycles**	**324**	**89**	**272**

Table 13 Engelmaier model input and output parameters.

We observe that the difference between the predicted life of the WLP144 and CVBGA432 comes from the difference in the distance to the neutral axis, L, and the difference between the predicted life of the CVBGA432 and CTBGA208 is due to the solder ball height, h. A smaller package and higher solder volume lead to an increased lifetime. However, a lower CTE mismatch between the part and PCB makes up for the larger part size, as is the case for the CTBGA208 compared to the WLP144.

3.2.2.2 Ansys Sherlock Life Prediction

Ansys Sherlock is a stand-alone application in the Ansys mechanical simulations toolkit. It is also available as a component in Ansys Workbench for pre and postprocessing electronics simulations. Sherlock focuses on PCB and components modeling, simulation and life prediction. It uses the PCB layout data as the primary input. The user defines the part properties and PCB stack-up. Behind the scenes, Sherlock calculates the effective properties of the components and PCB based on lamina theory and the proportion of the layers. The user can use Sherlock as a preprocessor to define the PCB and components' properties. The user can import the PCB assembly in Ansys Mechanical for an FEA analysis. However, for a fast reliability analysis of the PCB or specific components, the user can perform a Solder Fatigue analysis, determining the shear force caused by the CTE mismatch between the PCB and part and then predicting the characteristic life as in 2.4.1. In this section, we focus on the analytical approach embedded in Sherlock. The user can perform a solder fatigue analysis for all the components on the PC in a single analysis or can choose to analyze just one component at a time by accessing the stand-alone Solder Fatigue Tool, as in Figure 39. We used the Ansys Release 22.2.

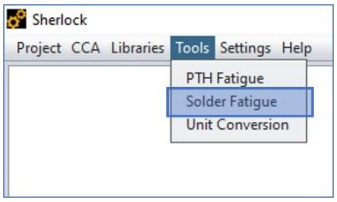


Figure 39 Accessing the Solder Fatigue Tool. Image used courtesy of ANSYS, Inc.

We checked the correctness of implementation by running the worked example in the Sherlock Theory Guide available in the Ansys Help Portal. The Help [94] provides all the background formulas we implemented in a spreadsheet calculator to gain insight on the calculations and use of parameters. However, copyright law and nondisclosure provisions protect the Online Help and documentation under the license agreement. Thus, we did not publish the worked example and background formulas.

Section 3.2.1, respectively Table 7 describe all the geometry parameters Sherlock requires for the fatigue calculation and the material properties of the PCB and mold compounds. We used the isotropic definition of silicon properties in [95] for the silicon dies. The WLP144 copper redistribution layer connects the die to the solder joints. The CVBGA432 and CTBGA208 have a laminate substrate between the die and solder joints. Because the substrate measurements are not available, we assume the elastic properties. Table 14 shows the material properties implemented in Sherlock. We used the implicit definition for SAC305 solder material properties and fatigue parameters available in the tools' Solder Library.

Screenshots in Figure 42, Figure 41, and Figure 42 show the implementation of all the parameters in the tool for each part. The yellow cells show the output parameters.

Implicitly, the tool determines the cycles to failure, the stress, and the strain energy in the joint. For further comparison, we also calculate the strain range as the ratio between strain energy and stress and summarize the results in Table 15.

Part	Property	WLP144	CVBGA432	CTBGA208
Substrate	CTE	n/a	*12*	*12*
	Tg	n/a	n/a	n/a
	E	n/a	*23000*	*23000*
	v	n/a	*0.20*	*0.20*
Die [95]	CTE	2.60	2.60	2.60
	E	130000	130000	130000
	v	0.28	0.28	0.28
Overmold	CTE	n/a	14.30	24.10
	Tg	n/a	129	118
	E	n/a	15000	20000
	v	n/a	*0.25*	*0.25*
PCB	CTE	15.20	15.20	15.20
	Tg	190	190	190
	E	36134	36134	36134
	v	*0.15*	*0.15*	*0.15*

Table 14 Package Parts and PCB Properties. Units: ppm/°C, °C, MPa. Italic font marks the estimated values.

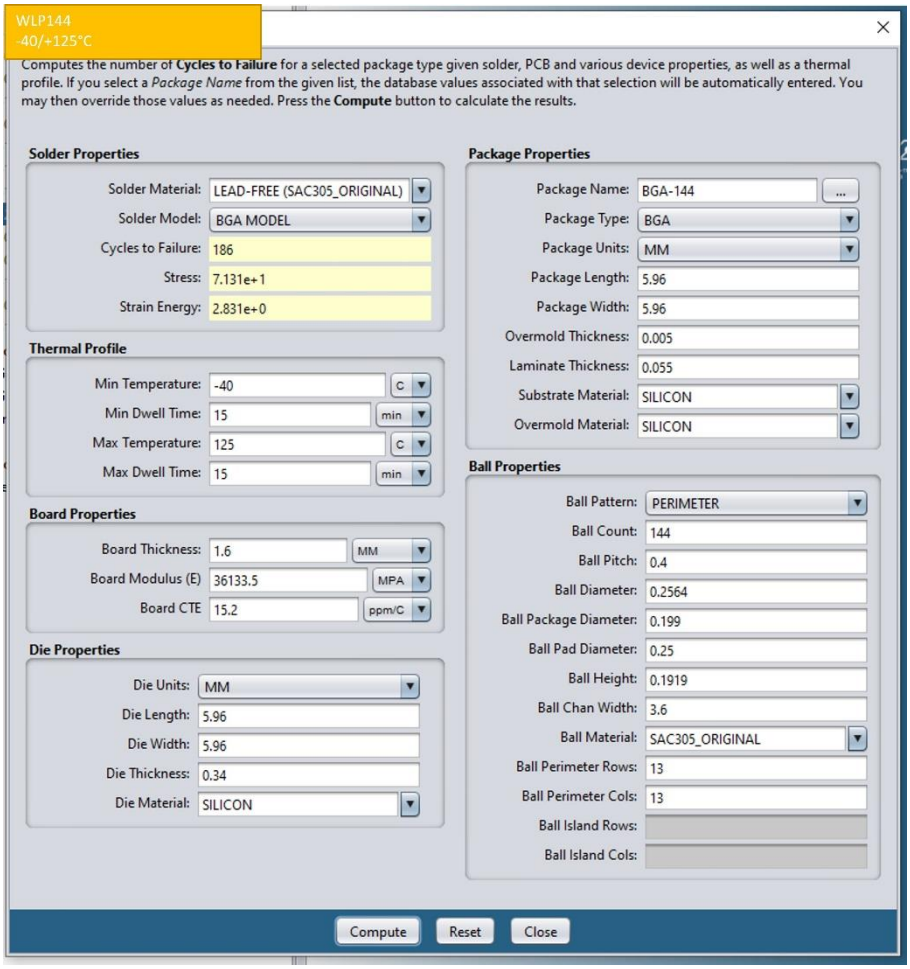


Figure 40 Screenshot of the Sherlock Solder Fatigue calculation for WLP144. Image used courtesy of ANSYS, Inc.

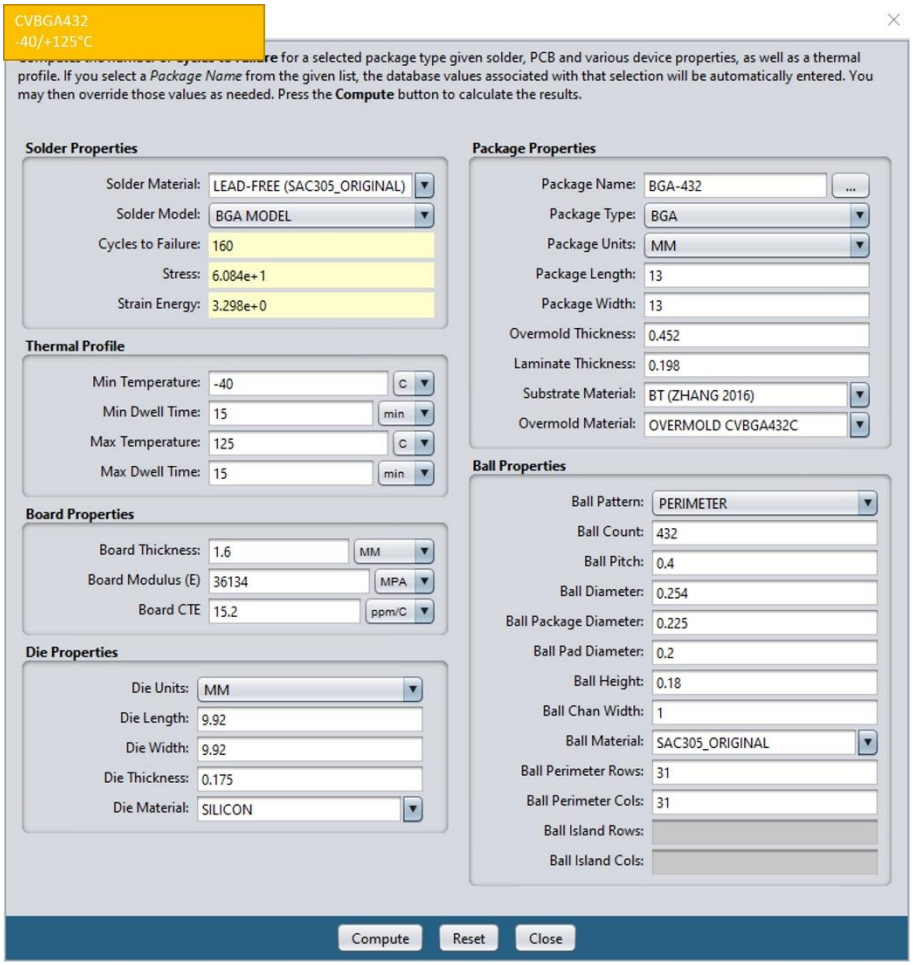


Figure 41 Screenshot of the Sherlock Solder Fatigue calculation for CVBGA432. Image used courtesy of ANSYS, Inc.

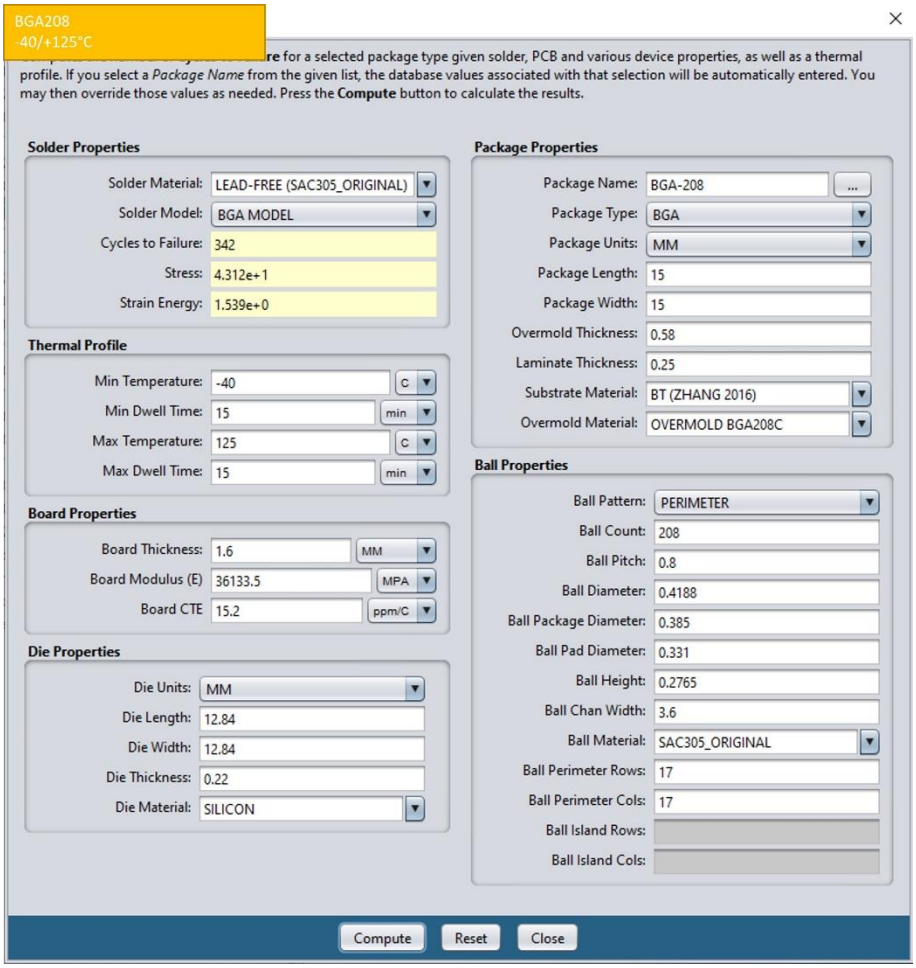


Figure 42 Screenshot of the Sherlock Solder Fatigue calculation for CTBGA208. Image used courtesy of ANSYS, Inc.

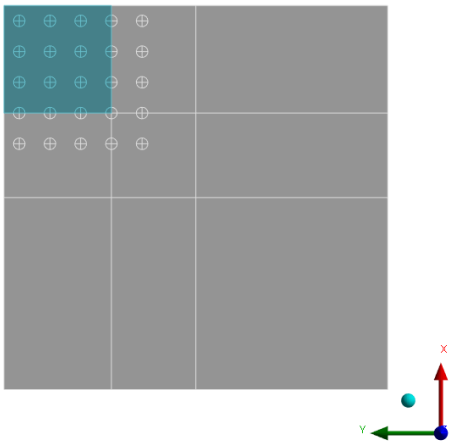
Parameter	**Unit**	**WLP144**	**CVBGA432**	**CTBGA208**
σ	MPa	71.31	60.84	43.12
ΔW	mJ/mm^3	2.831	3.298	1.539
Δγ	-	0.0397	0.0542	0.0357
$N_{f(63\%)}$	**cycles**	**186**	**160**	**342**

Table 15 Ansys Sherlock Solder Fatigue Outputs.

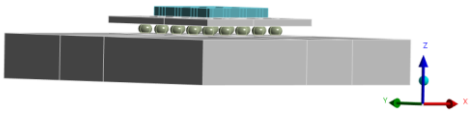
3.2.2.3 FEA Based Life Prediction

Like in the analytical approaches, the first step in attempting the life prediction of the BGA parts based on FEA calculated solder joint response is to calibrate with a literature or help example. In this case, we reproduce two textbook applications: Reflow Cooling [96] and Temperature Cycling [97].

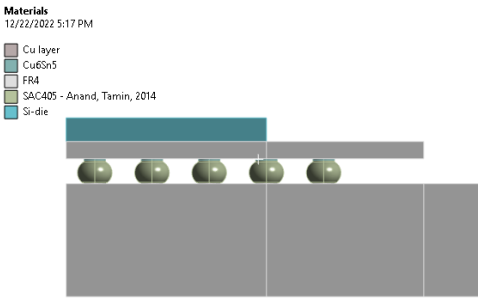
First, we build the quarter model shown in Figure 43 - 1 and 2 according to the dimensions given in [96]. The model is a bare-die on FR4 substrate BGA mounted on an FR4 PCB with SAC405 [63] solder balls, Cu pads on the PCB side, respectively CuSn5 pads on the substrate side, as in Figure 43 - 3. Because the model is symmetric, the authors create a quarter model and impose symmetry conditions as in as in Figure 43 - 4. In addition, we constrain one point in the Z-direction in Figure 43 - 5 to avoid rigid body motion.



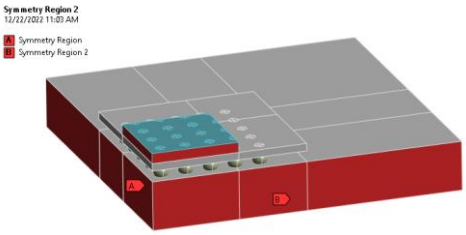
1 Top view



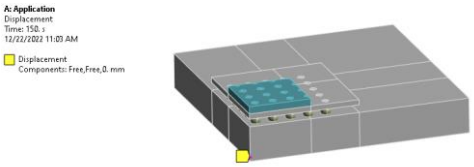
2 3D view



3 Side view and material assignments



4 Symmetry condition



5 Boundary condition

Figure 43 Quarter model textbook example for FE methodology calibration as in [96]. Images used courtesy of ANSYS, Inc.

Secondly, we define shared topology between all bodies and thus create a conformal mesh following the indications given in the textbook. Per the instructions, we only refine the corner joint mesh to reduce the model size. Finally, we create the FE model in Ansys Workbench 2022 R2 and use first-order elements as in the textbook. Figure 44 shows the 48537 nodes mesh.

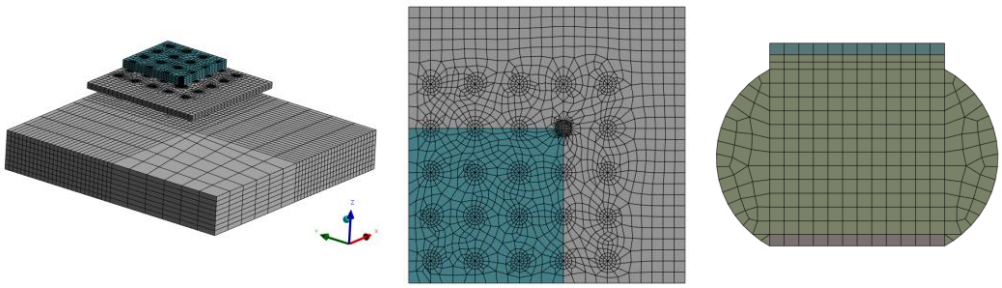


Figure 44 Quarter model textbook example mesh: 3D view, top view, and solder joint detail. Images used courtesy of ANSYS, Inc.

The application assumes a perfectly flat assembly in a stress-free state at 220°C. Lastly, we apply the loading condition in Figure 45, representing the cooling from the peak reflow temperature of 220°C to 25°C at a cooling rate of 80°C/min.

After a couple of iterations and fine adjustments to the FE mesh, pad dimensions and load incrementations, we obtained satisfactory results, although not a perfect match.

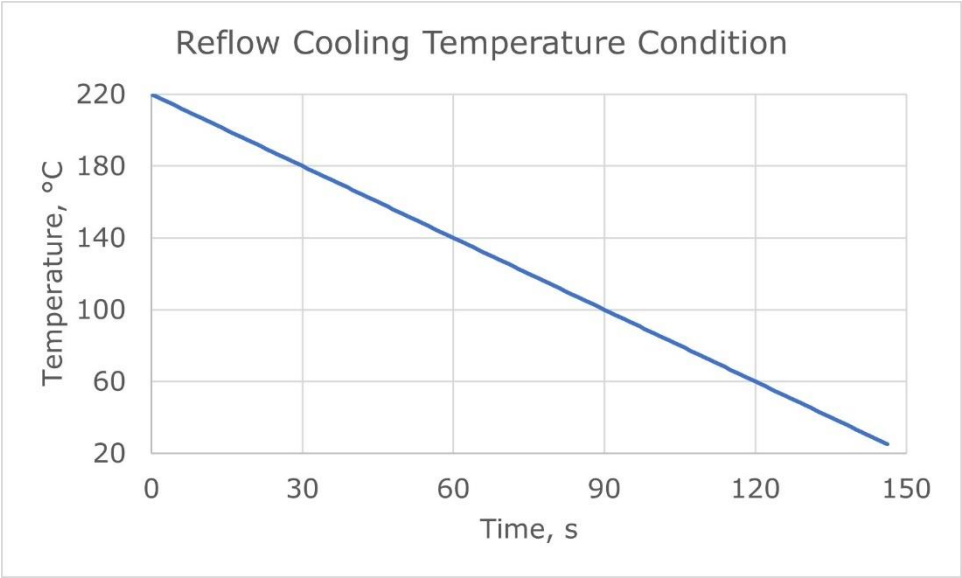


Figure 45 Quarter model example temperature condition.

Figure 46 shows the warpage of the assembly in the textbook [96], and Figure 47 shows the warpage in our analysis at the same scale. The absolute maximum (negative Z) deformation is 7% less than the textbook result, while the absolute minimum value is one order of magnitude higher. However, the minimum value depends on the constrained node; otherwise, the deformation plot is similar.

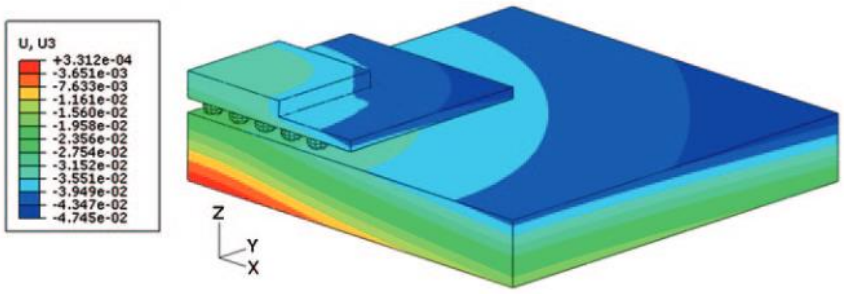


Figure 46 Warpage of the quarter model at 25°C as in Fig. 5.5 in [96], page 81.

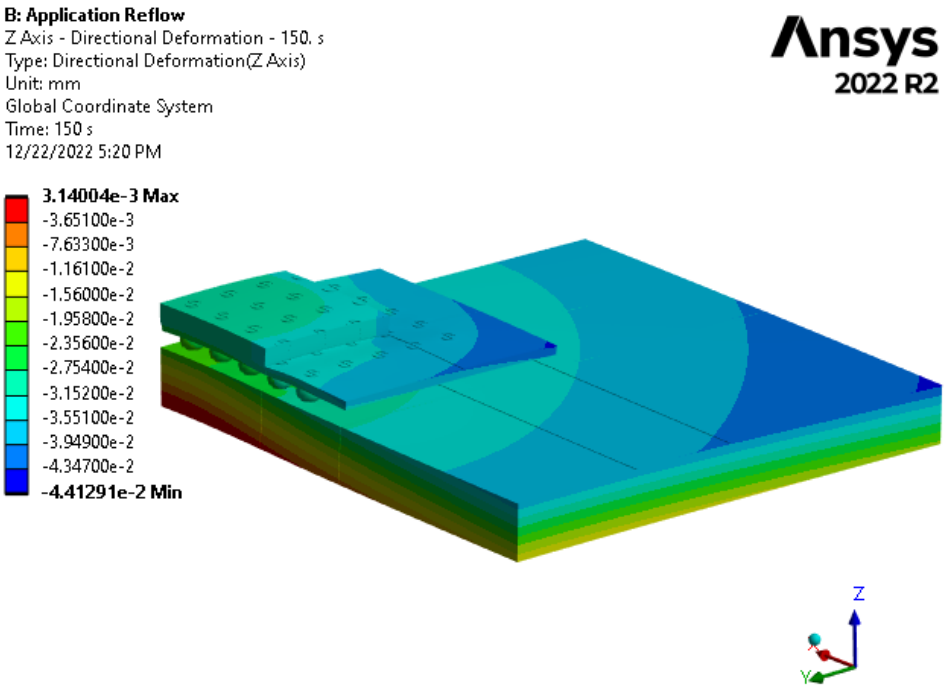


Figure 47 Warpage of the quarter model at 25°C resulted in own analysis. Image used courtesy of ANSYS, Inc.

Further, in Figure 48 and Figure 49 we analyze the von Mises stress output. We obtain the maximum stress result within 1% from the reported value in the textbook and the minimum value one order of magnitude smaller. Lastly, we digitize the textbook stress and strain evolution curves and compare them with our results in Figure 50. Both stress and inelastic strain deviate from the reference values in [96] at lower temperatures but remain within ±10%.

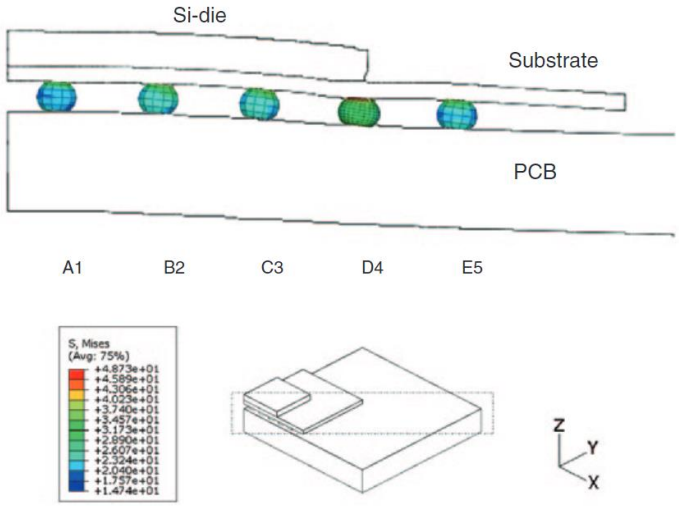


Figure 48 "The deformed row of solder joints along the diagonal plane of the assembly at 25°C following the solder reflow cooling process" as in Fig. 5.7 in [96], page 82.

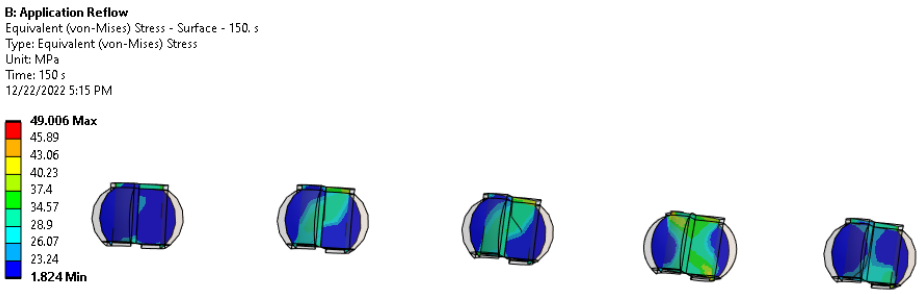


Figure 49 The deformed row of solder joints along the diagonal plane of the assembly at 25°C resulted in own analysis. Image used courtesy of ANSYS, Inc.

We calibrated the FE mesh with this example by matching the deformation results. We found the stress response most sensitive to pad diameter, which the textbook did not specify. We matched the stress and strain development in the critical joint by adjusting the time increment. Overall, this exercise provided a good insight into package modeling and outputs analysis.

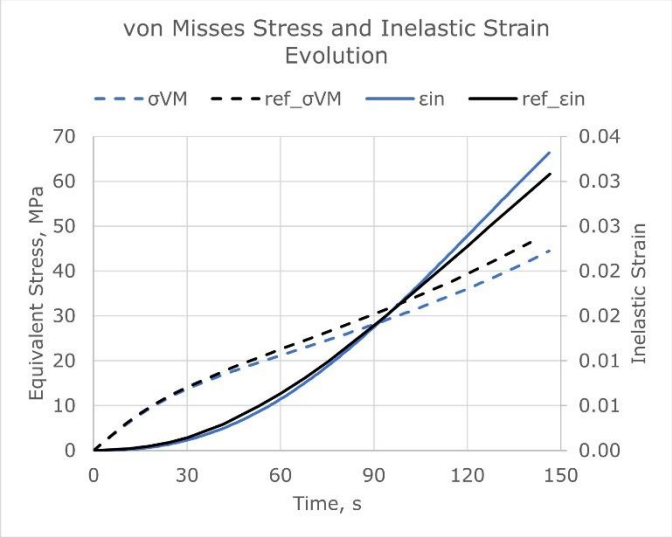


Figure 50 Comparison of own and textbook [96] results of von Misses stress and inelastic strain evolution in the critical solder joint.

We continue with the following exercise application - Thermal Cycling [97], where we change the temperature load in the previous model with a temperature profile consisting of two cycles for 60 minutes each. The temperature ranges from -40°C to +125°C, with a ramp rate of 11°C/min and a dwell period of 900 seconds [97]. Next, we refine the mesh of the copper pads and define a critical region at the solder–package interface. As instructed, we discretize this 25μm region with four elements through the thickness as in Figure 51. The scope of this region is to volume-average the relevant variables.

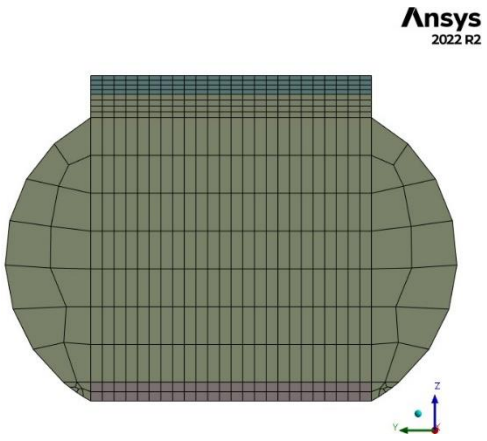


Figure 51 Refined critical solder mesh for thermal cycling in textbook application. Image used courtesy of ANSYS, Inc.

As before, we digitized the evolution of the von Mises stress and inelastic strain plots in [97] and compared with our results. Figure 52 shows the calculated stress compared with the reference value from the textbook, and Figure 53 shows the same comparison for the inelastic strain. After a few mesh refinement iterations, we obtain close results to the reference values.

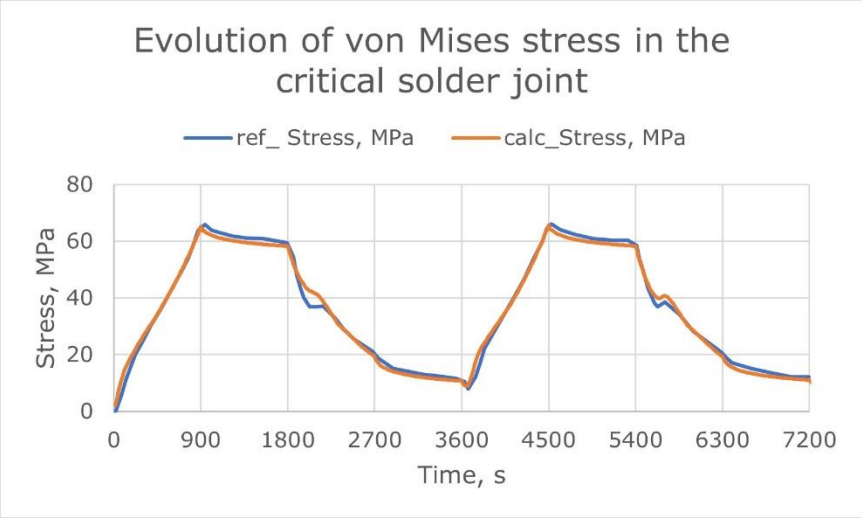


Figure 52 Comparison of own and textbook [97] results of von Misses stress evolution in the critical solder joint.

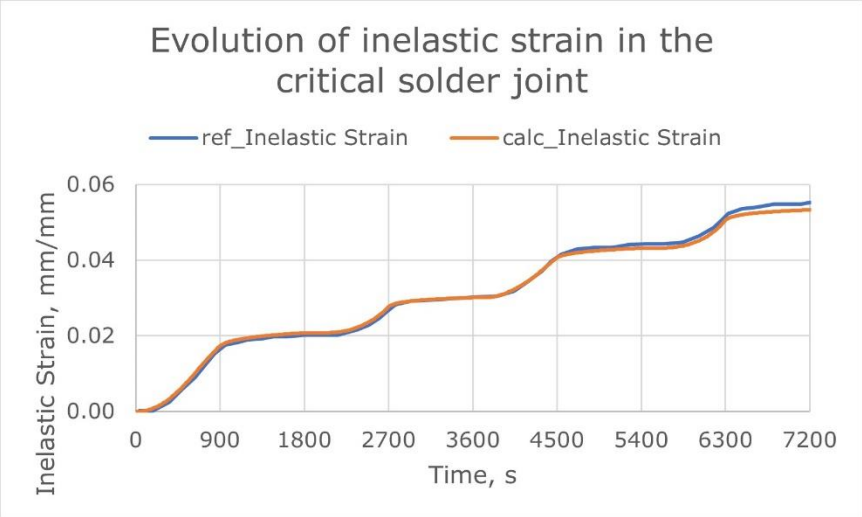


Figure 53 Comparison of own and textbook [97] results of inelastic strain evolution in the critical solder joint.

Solving the two applications above showed that fatigue-relevant variables such as stress, inelastic strain and accumulated inelastic work density per cycle [97] are mesh dependent and sensitive to solder joint geometry. Syed [47] discusses the modeling-related challenges. He proposes a methodology for BGA packages to remove any modeling assumptions from the prediction model, which we applied in [67], where we analyzed different life-prediction approaches which would suit system-level analysis. We found out that the best approach is to do a comparative study between BLR and SLR and apply the strain energy density ratio (SED-R) to determine the lifetime in the system, as described in 2.4.3. In [78], we proved that when using the SED-R approach to determine the system-level lifetime, we can simplify the mesh if we keep the same component model between BLR and SLR.

We do not know which corner joint is critical in SLR because of the uneven PCB deformation. This situation raises modeling challenges such as:

- The need for modeling the entire component.
- The need to analyze results from all solder joints.

To analyze all solder joints, they should all have the same mesh. In this case, one could determine the critical solder through a warpage analysis with a rougher mesh. Then one could determine the critical solder and refine the mesh for lifetime prediction. However, for the SLR, we aim to determine critical solder joint rows for cross-sectioning and determine the impact of the system conditions on the reference BLR lifetime. Another challenge is ensuring consistency over different tasks and FEA specialists performing the task. Thus, absolute lifetime prediction in SLR is not a goal considering Lau's recommendations in [33] , where he emphasizes the fact that besides prediction models being susceptible to FE modeling, they predict one life which is statistically insignificant given all the uncertainties related to the variables going in the empirically determined constants.

Further on, we aim to create a reasonable FE model for the three BGAs and predict lifetime using the Schubert et al. [52] and Syed [46] [47] accumulated inelastic work density per cycle based models discussed in 2.4.2 Table 4, second line and 2.4.3. We start the analysis by determining the transverse isotropic properties of the PCB. In [79] and [84], we discussed different modeling approaches for the PCB. As a result, we determined that a transverse isotropic definition, where we assume Ex = Ey, vxy = vxz = vyz = 0.15 and determine the shear moduli assuming von-Mises elasticity as in (33), based on the elastic moduli calculated with Ansys Sherlock Stack-up provides a static response within 5% when compared with experimental data. Finally, we input in Sherlock Stack-up, see Figure 54, the layers shown in Figure 22. As a result, in Table 16, we obtain the CTExy 13% lower than the measured value and the Exy 3% higher than the measured values. Therefore, we expect some deviation from the TMA / DMA results, considering the ±10% tolerance of the thickness layers and the tolerances in the laminate datasheet reported material properties.

$$G = \frac{E}{2(1+\nu)} \tag{33}$$

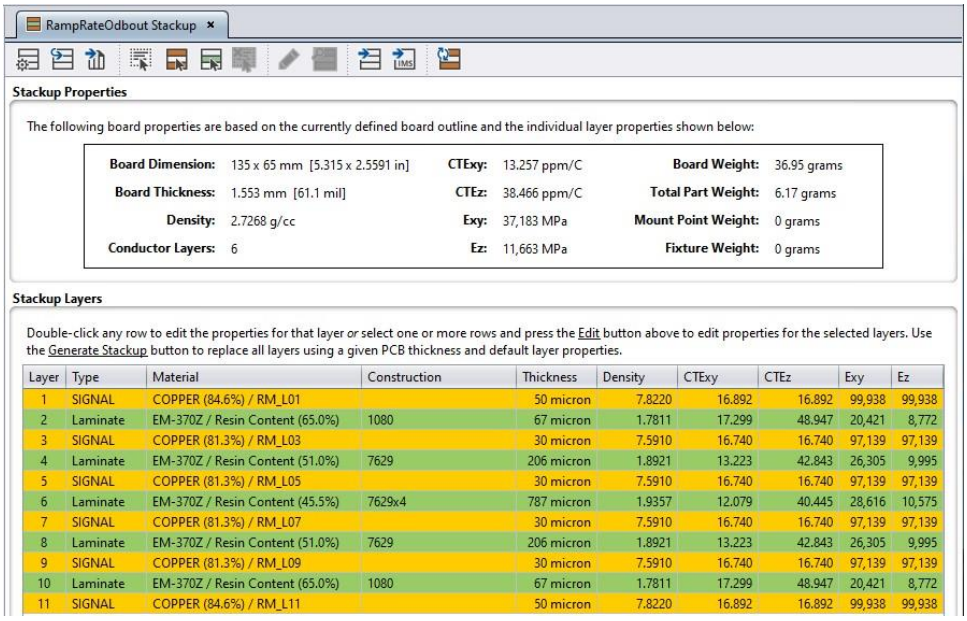


Figure 54 Calculated PCB stack-up with Sherlock, given the supplier proposed stack-up. Image used courtesy of ANSYS, Inc.

Variable	CTExy (ppm/°C)	CTEz (ppm/°C)	Exy (MPa)	Ez (MPa)
Measured	15.20	n/a	36134	n/a
Calculated	13.25	38.47	37183	11663
Error	-13%	n/a	+3%	n/a

Table 16 Measured vs. Calculated PCB properties.

With the available data, we have no means of calibrating the Z direction properties, so given the acceptable correlation for the in-plane properties, we continue the PCB material modeling by considering the measured in-plane variable values and calculated out-of-plane variable values to determine the shear moduli. We assume the Poisson's ratio to be 0.15 in all directions and determine the shear moduli with (33) as in Figure 55.

We imported the ECAD ODB++ file in Sherlock to create the PCB geometry. After defining the stack-up and part properties for all the components, we import the PCBA in Ansys Mechanical using the Sherlock(Pre) Component. This workflow assigns a custom homogenized component-specific material to each part on the PCB. In [80], we found this approach accurate and efficient.

PCB

measured / calculated

Structural	
Orthotropic Elasticity	
Young's Modulus X direction	36134 MPa
Young's Modulus Y direction	36134 MPa
Young's Modulus Z direction	11663 MPa
Poisson's Ratio XY	0.15
Poisson's Ratio YZ	0.15
Poisson's Ratio XZ	0.15
Shear Modulus XY	15710 MPa
Shear Modulus YZ	5071 MPa
Shear Modulus XZ	5071 MPa
Orthotropic Instantaneous Coefficient of Thermal Expansion	
Coefficient of Thermal Expansion X direction	1.52e-05 1/°C
Coefficient of Thermal Expansion Y direction	1.52e-05 1/°C
Coefficient of Thermal Expansion Z direction	3.847e-05 1/°C

Figure 55 PCB material card. Image used courtesy of ANSYS, Inc.

We define the materials for the parts of the BGA components. Since the prediction models use the Schubert et al. [52] hyperbolic sine creep law, we define the SAC305 solder material as temperature-dependent elastic isotropic with Generalized Garofalo creep. Figure 56 shows the solder material card. We defined the temperature dependency of the elastic modulus as in Table 4, line 2.

SAC387/358/355 - Garofalo

Schubert et al. (2003)

Density	7.4e-09 tonne/mm³

Structural	
Isotropic Elasticity	
Isotropic Secant Coefficient of Thermal Expansion	2.22e-05 1/°C
Generalized Garofalo	
Reference Units (Length, Time, Temperature, Force)	mm, s, K, tonne mm s^-2
Creep Constant 1	2.7798e+05
Creep Constant 2	0.02447
Creep Constant 3	6.41
Creep Constant 4	6500

Figure 56 Solder material card. Image used courtesy of ANSYS, Inc.

We consider the copper pads made of temperature-dependent elastic isotropic thin-film copper. Further, we define the silicon elastic orthotropic for the silicon chips as shown in [95] and Figure 57.

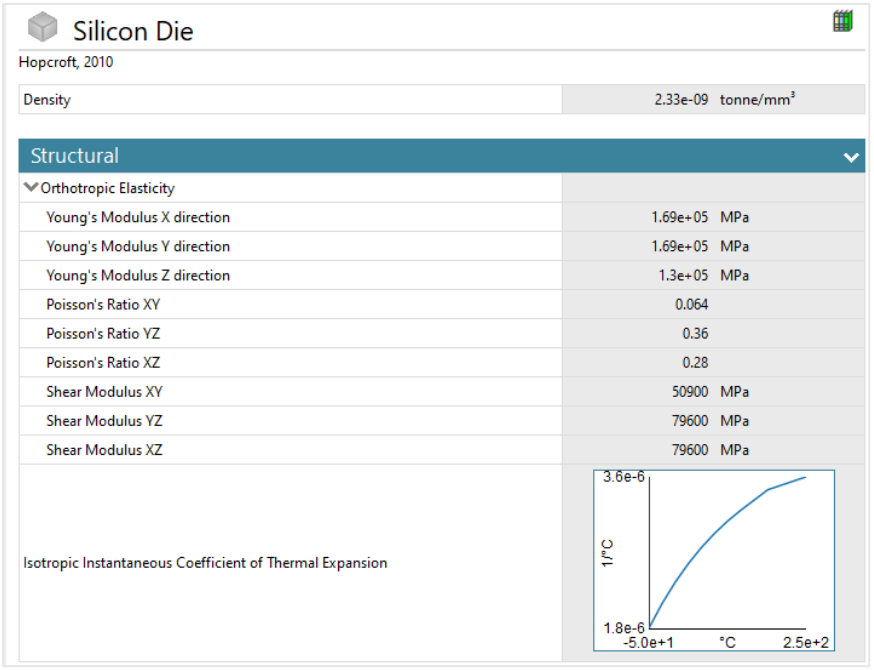


Figure 57 Silicon die material card. Image used courtesy of ANSYS, Inc.

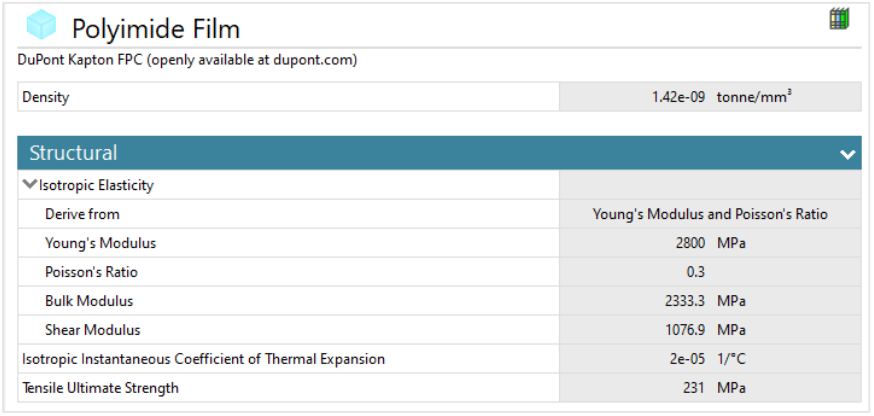


Figure 58 Polyimide film material card. Image used courtesy of ANSYS, Inc.

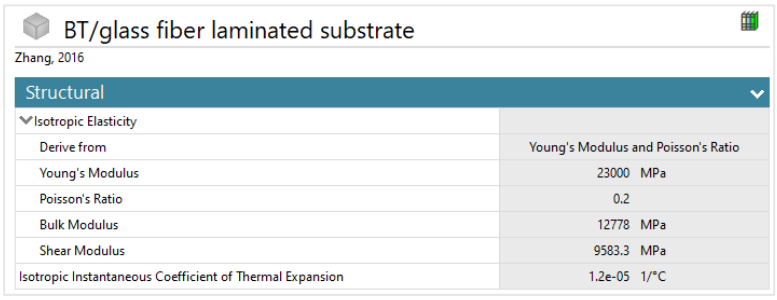


Figure 59 BGA substrate material card [98]. Image used courtesy of ANSYS, Inc.

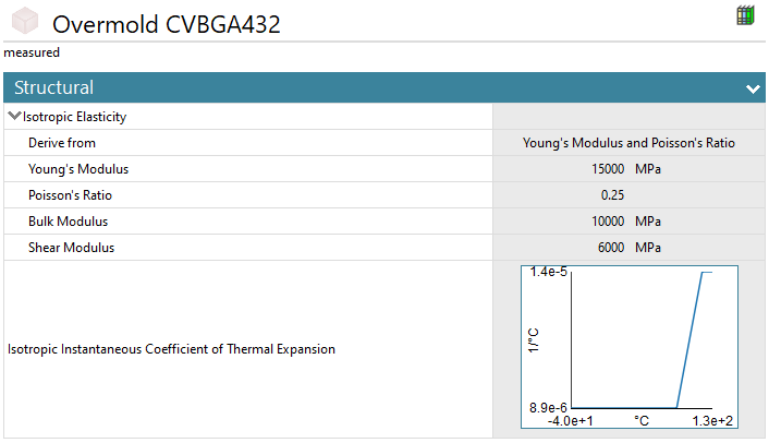


Figure 60 CVBGA432 overmold material card. Image used courtesy of ANSYS, Inc.

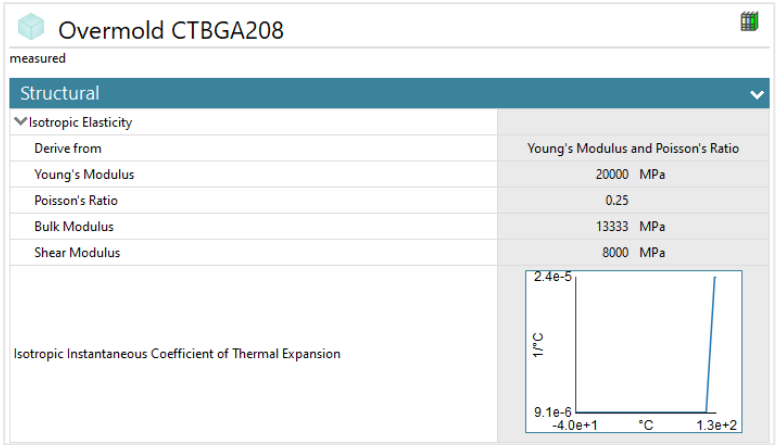


Figure 61 CTBGA208 overmold material card. Image used courtesy of ANSYS, Inc.

We create the WLP144 as a stack-up from top to bottom made of the silicon die, copper redistribution layer and a polyimide layer encapsulating the copper pads. Information such as polyimide film producer and mechanical properties is proprietary to the package producer and rarely available to third parties. In this case, we assume generic information is openly available online, as shown in Figure 58. For the plastic molded BGAs, we consider the material definitions in Table 9 and Table 14, shown in the material cards in Figure 59, Figure 60, and Figure 61.

We detailed only one part and simplified the other as a solid block. Figure 62 shows the top view of the PCB and indicates the detailed and simplified BGA parts. We also considered the PCB underneath an independent body for the detailed parts because we will refine the mesh in this area. This cutout small PCB shares topology with the large PCB part. A bonded contact connects the simplified component to the PCB body.

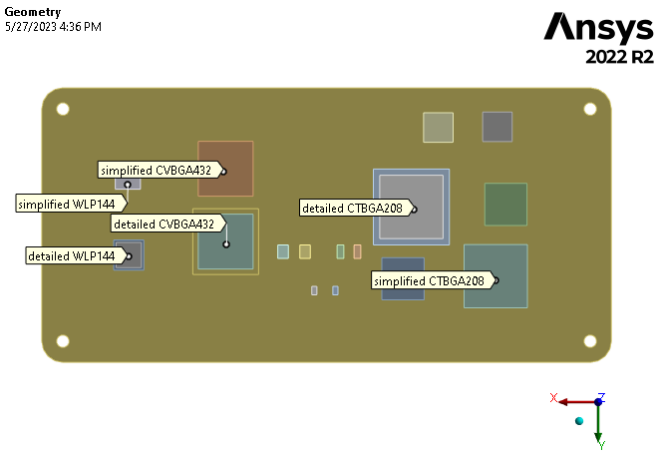


Figure 62 PCBA Top view. Image used courtesy of ANSYS, Inc.

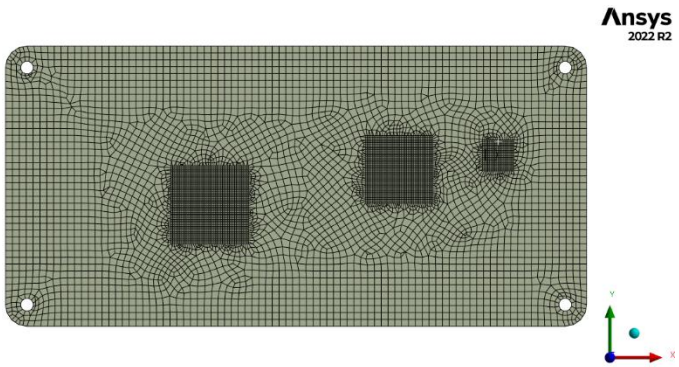


Figure 63 PCB mesh showing the cutouts underneath the detailed components (bottom view). Image used courtesy of ANSYS, Inc.

We created a swept mesh for the PCB bodies, with a 1.60 mm element size for the large PCB part, respectively 0.4 mm element size for the PCB cutouts underneath the detailed component, as in Figure 63. The PCB has three quadratic hex elements (SOLID186) through its thickness. The simplified components on the PCB have two SOLID186 0.8-1.6 mm elements through their thickness and sweep method controls.

We created the geometry of the detailed parts according to the dimensions described in the previous sections using scripting in Ansys SpaceClaim. For the WLP144, we created non-solder mask defined (NSMD) pads at both interfaces, as in Figure 64. For the CVBGA432, the pads are solder mask defined (SMD) at both interfaces, as in Figure 66 and lastly, for the CTBGA208, the pads at the package interface are SMD and at the PCB interface are NSMD, as shown in Figure 68. For all solder joints, we consider a 15% solder volume at each interface which we will use for variables averaging. The solid bodies in the solder joints, solder, and copper pads, have a shared topology. We defined a bonded contact with multipoint constraint formulation between the copper pads and substrate, respectively PCB. The parts in the package – substrate, die, and overmold, respectively polyimide, redistribution layer and silicon in WLP144, also share topology.

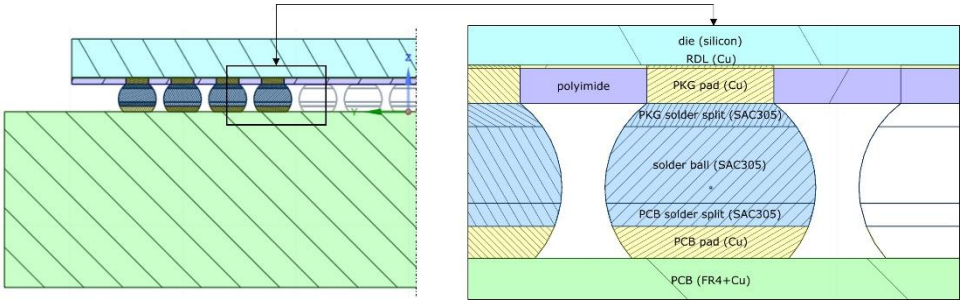


Figure 64 WLP144 cross-section detail. Images used courtesy of ANSYS, Inc.

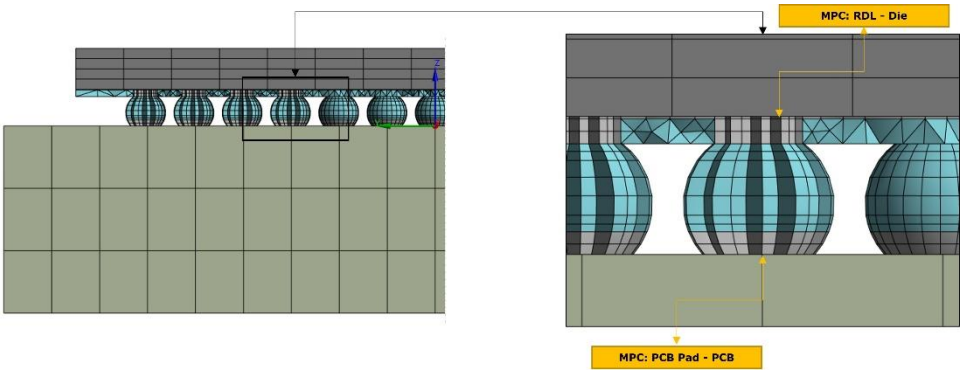


Figure 65 WLP144 mesh cross-section detail. Images used courtesy of ANSYS, Inc.

From a model size perspective, we created the mesh with second-order elements for the package and PCB, respectively, and first-order elements for the solder joints. Each body has at least two elements through its thickness. Figure 65 shows the mesh and contact regions for the WLP144. Except for the polyimide and RDL layers, all parts have hexahedral elements. Figure 67 and Figure 69 show the mesh and contact regions for the molded parts.

To mesh the detailed parts, we used Multizone and edge sizing mesh controls for the package bodies, sweep for the pads and splits, and mesh copy to ensure identical mesh for all solder joints. Package parts have 0.4 mm elements. Solder joints have 0.05 mm for the WLP144, 0.04 mm for the CVBGA432, and 0.06 mm for the CTBGA208.

To create the mesh for the whole assembly, we recorded 45 sequences, starting from the small PCB bodies, followed by the large PCB body and simplified components. Then we created the mesh for each detailed part starting with one solder joint, followed by mesh copy on all the other solder joints and lastly, meshing the package parts from inside out. The resulting mesh in Figure 70 has 977079 nodes.

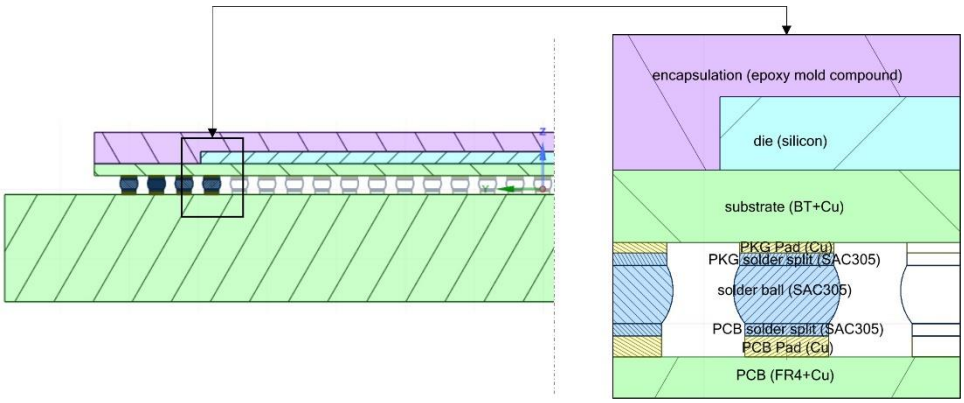


Figure 66 CVBGA432 cross-section detail. Images used courtesy of ANSYS, Inc.

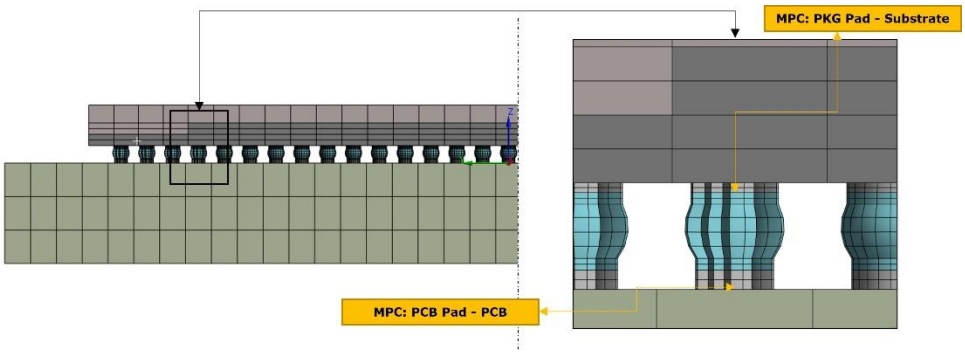


Figure 67 CVBGA432 mesh cross-section detail. Images used courtesy of ANSYS, Inc.

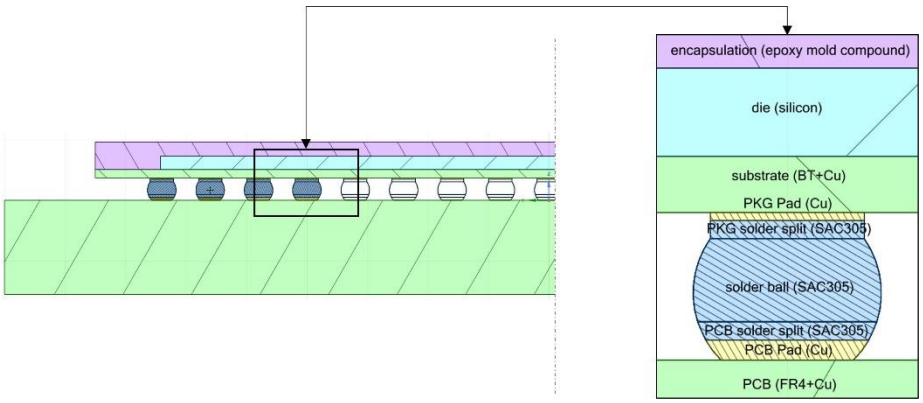


Figure 68 CTBGA208 cross-section detail. Images used courtesy of ANSYS, Inc.

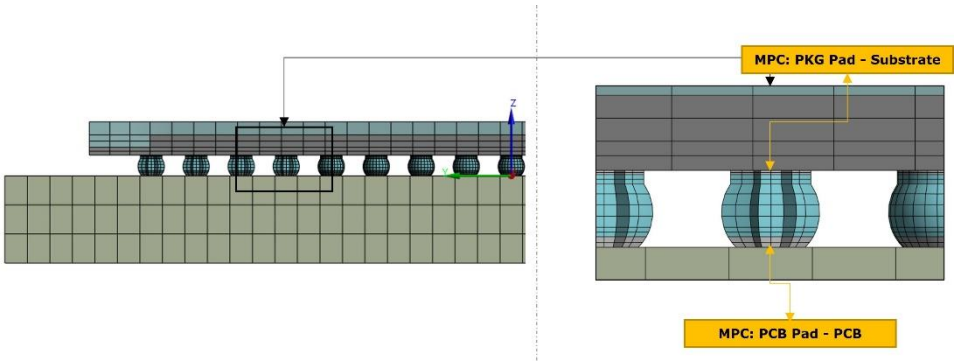


Figure 69 CTBGA208 mesh cross-section detail. Images used courtesy of ANSYS, Inc.

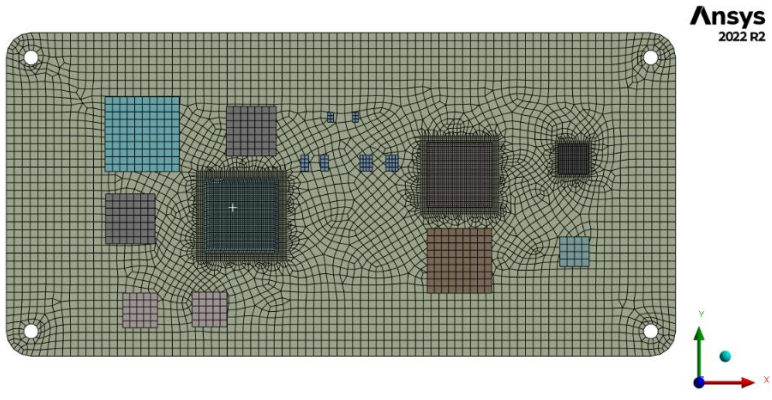


Figure 70 Assembly mesh. Image used courtesy of ANSYS, Inc.

Further, to avoid rigid body motion, we apply the boundary conditions on three vertices as in Figure 71: a fixed support in point A, a displacement in point B blocking the translation of the PCB body toward the Y axis and another displacement in point C blocking the vertical translation. We apply the temperature condition in Figure 28 in 10 steps, as two thermal cycles, each step being a stage in the temperature profile. We use time stepping to control the load incrementation, with a minimum time step of 1 second and a maximum time step of 60 seconds. In Analysis Settings, we also choose a direct solver, turn on creep controls and large deflection for each step. We also choose to save nonlinear data for post-processing and save only the last time step result to reduce the model size. The 2554575 DOF analysis was solved in 7h 25 min on an HP Z840 Workstation, using 22 out of 24 physical cores and 33GB out of 192GB RAM available, the results occupying 12GB disk space.

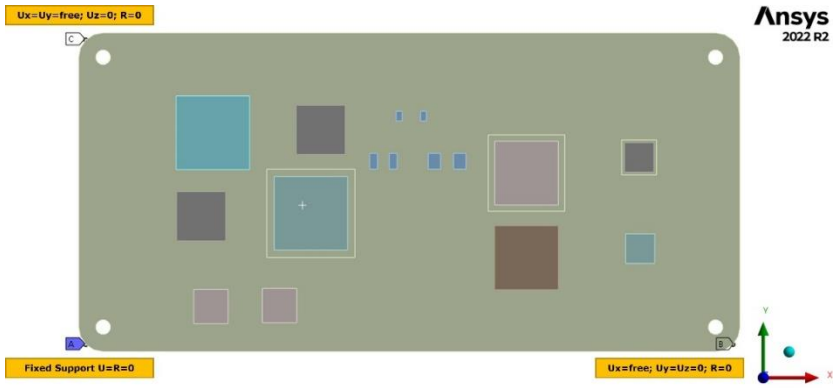


Figure 71 BLR boundary conditions. Image used courtesy of ANSYS, Inc.

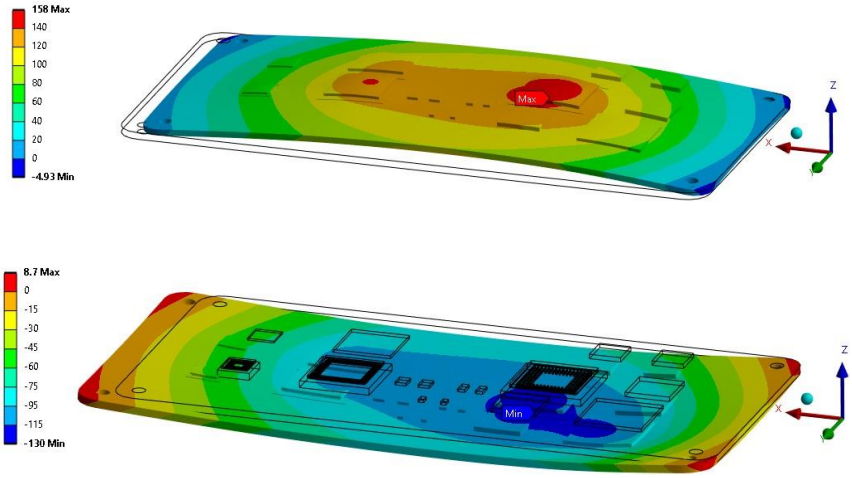


Figure 72 Directional deformation of the BLR PCBA in Z direction at -40°C (top) and 125°C (bottom). The wireframe shows the undeformed shape. Legend units: μm. Deformation scale factor: 35. Images used courtesy of ANSYS, Inc.

Figure 72 shows the warpage of the PCB assembly. The maximum deformation of 158 µm occurs at negative 40°C in the second cycle, at the beginning of the dwell period. At 125°C, the board expands, resulting in a 130 µm deformation at the beginning of the high-temperature dwell period of the first cycle. The zero coordinates are at the top face of the PCB. At both temperatures, the absolute maximum warpage occurs at the CTBGA208. Figure 73 shows the equivalent stress in the solder and the elemental averaged creep work (NLCRWK) accumulated during one cycle. The maximum nodal stress and maximum elemental mean creep energy locations are the same for each package.

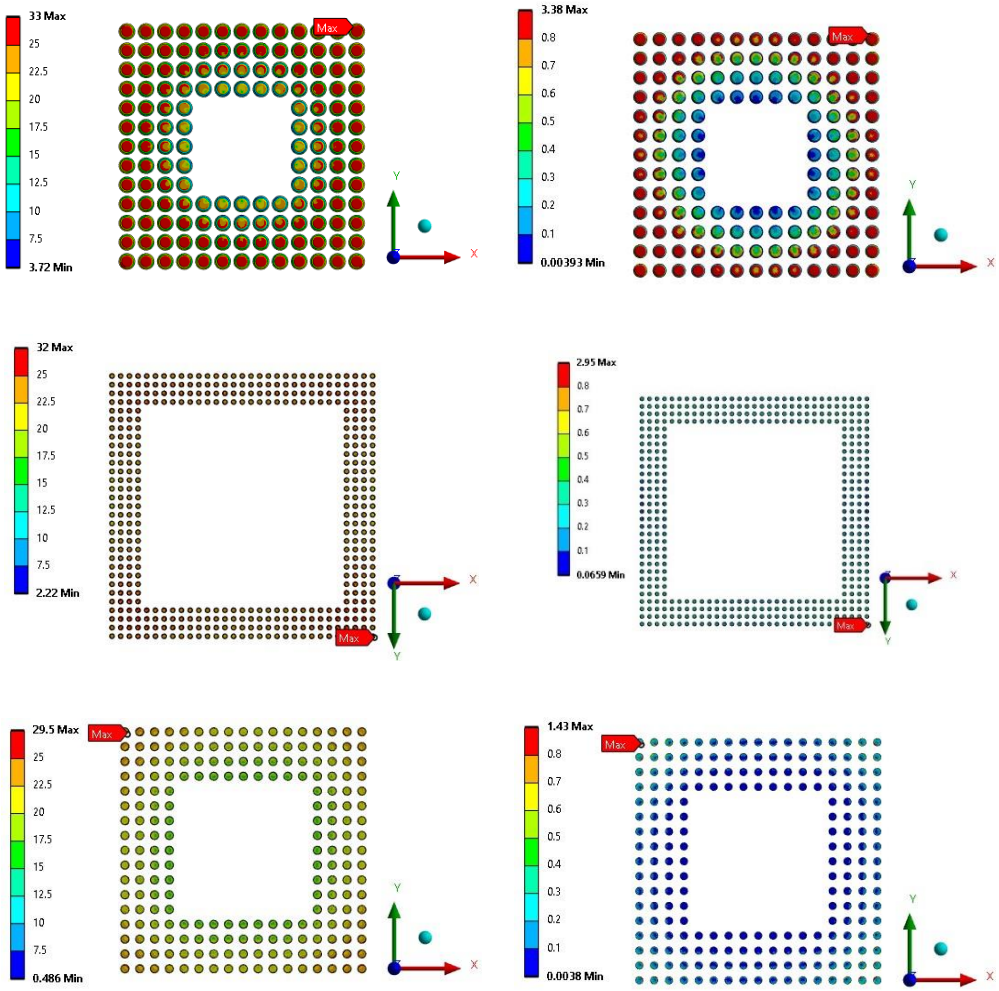


Figure 73 BLR stress (left) and inelastic strain, NLCRWK, (right) distribution in the solder joints in WLP144 (top), CVBGA432 (middle), CTBGA208 (bottom). Legend units: MPa, mJ/mm^3. Images used courtesy of ANSYS, Inc.

The higher stress and creep work results indicate that the WLP144 would fail first, followed by the CVBGA432 and CTBGA208. In the WLP144 and CTBGA208, the damage occurs at the solder–package interface, while in the CVBGA432, the damage occurs at the solder – PCB interface, as shown in Figure 74.

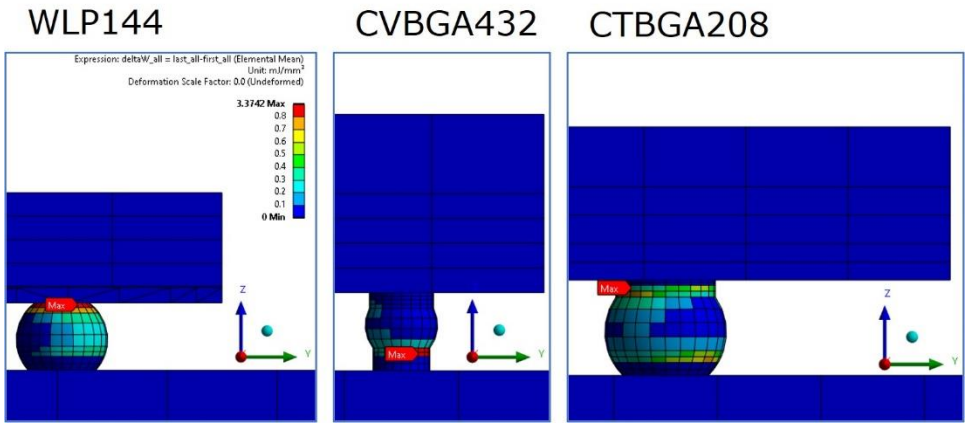


Figure 74 BLR elemental-averaged accumulated creep energy density (NLCRWK, mJ/mm^3) in the critical solder joints. All plots have the same scale and legend as for WLP144. Images used courtesy of ANSYS, Inc.

The life-prediction models use the accumulated creep strain or energy density volume-averaged along the damage path as in (34) [99]. A flexible way that offers an overview of all solder joints is to create a script (APDL for Ansys), that volume-averages a specific output across layers of mesh elements. In this way, the user can choose the damage path after solving the model instead of pre-defining the split in the geometry prior to solving. In this regard, we built such a script with Ansys Customer Support and component manufacturer representatives. We found the maximum accumulated creep work per cycle to be in one layer of elements for the WLP144 and two layers of elements in the other two parts. Thus, the averaging layer has a thickness of 25 µm for the WLP144, 30 µm for the CVBGA432, respectively 45 µm for the CTBGA208, as shown in Figure 75.

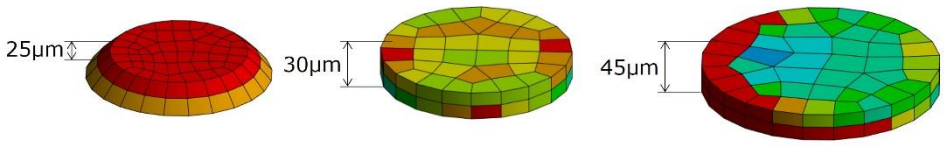


Figure 75 Output integration volumes and layer thickness. All plots have the same legend. Images used courtesy of ANSYS, Inc.

$$\Delta W_{acc,cr} = \frac{\sum \Delta (W_i * V_i)}{\sum \Delta V} \tag{34}$$

The script outputs in a *.csv file the solder joints' nomenclature, coordinates, and volume-averaged output, as in Figure 76, columns A through D. Further on, we determine the minimum and maximum accumulated creep energy density per cycle and normalize the values using (35) [100] in column E. By plotting in a "Bubble Plot" the coordinates and normalized output, we visualize the critical solder joint and damage in the all the other joints as in Figure 77, Figure 78, and Figure 79. The bubble plots indicate the same critical solder joints as Figure 73.

Given the complexity of the model, a mesh convergence study is a research topic on its own. The most straightforward check compares the unaveraged and averaged nodal stress results as in Table 17. The maximum error of 15% is acceptable for the present study, as there is no recommendation as to how much it should be.

	A	B	C	D	E
1	ball	x	y	Wacc_PKG	NWacc_PKG
2	A1	2.40	-2.40	1.35	0.91
3	B1	2.40	-2.00	1.13	0.75
4	C1	2.40	-1.60	0.93	0.61
5	D1	2.40	-1.20	0.76	0.49
6	E1	2.40	-0.80	0.64	0.41
7	F1	2.40	-0.40	0.57	0.36
8	G1	2.40	0.00	0.55	0.35
9	H1	2.40	0.40	0.59	0.38
10	J1	2.40	0.80	0.69	0.44
11	K1	2.40	1.20	0.83	0.55
12	L1	2.40	1.60	1.03	0.68
13	M1	2.40	2.00	1.25	0.84
14	N1	2.40	2.40	1.48	1.00

*Figure 76 Screenshot of the *.csv output file.*

$$X_N = \frac{X - X_{min}}{X_{max} - X_{min}} \tag{35}$$

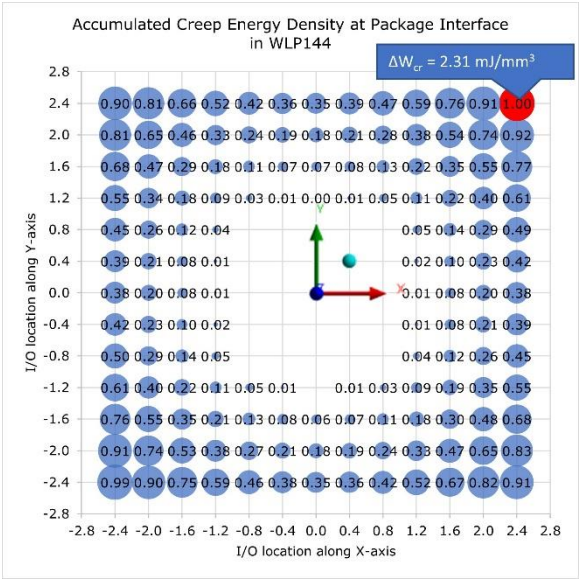


Figure 77 BLR bubble plot of the WLP144 showing the normalized accumulated creep energy density in the package interface solder volume.

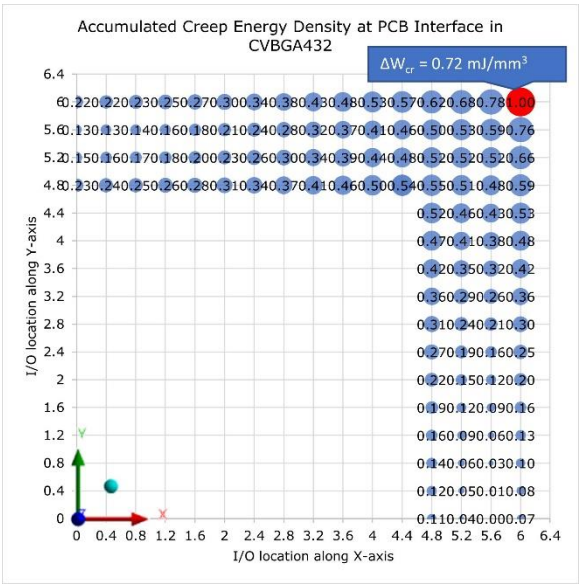


Figure 78 BLR bubble plot of the CVBGA432 (quarter package) showing the normalized accumulated creep energy density in the PCB interface solder volume.

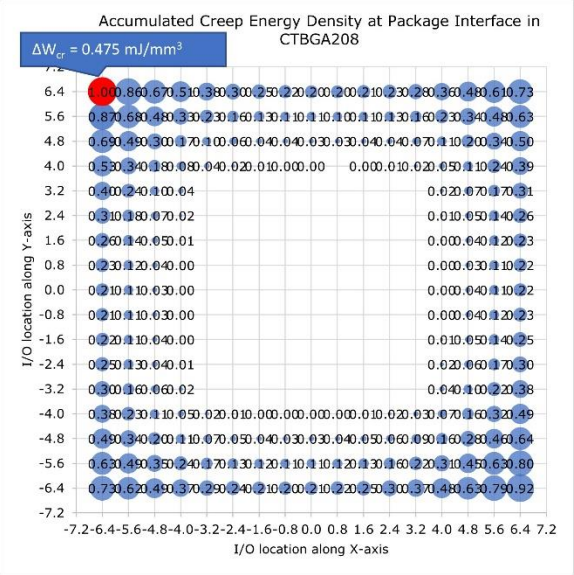


Figure 79 BLR bubble plot of the CTBGA208 showing the normalized accumulated creep energy density in the package interface solder volume.

Part	$\sigma_{max\_averaged}$	$\sigma_{max\_unaveraged}$	$e = \frac{\sigma_{max\_unaveraged} - \sigma_{max\_averaged}}{\sigma_{max\_unaveraged}} * 100$
WLP144	33	33.5	1%
CVBGA432	32	35.5	10%
CTBGA208	29.5	32.4	9%

Table 17 Maximum equivalent stress in the solder joints: nodal averaged vs. nodal unaveraged results.

Table 18 shows the energy-based life prediction of the three BGA parts based on the equations in Table 4 for the Garofalo creep model. The failure criteria, ΔW_{cr}, represents the accumulated creep strain energy density in the selected volume during one thermal cycle.

The critical solder joints indicated by the FEA analysis are consistent with the cross-sectioning results in Figure 32, Figure 33, and Figure 34 for all parts: N1 for WLP144, A31 for CVBGA432, and A17 for CTBGA208. However, for CTBGA208, the analysis indicates the package interface to be critical. Otherwise, stress and accumulated creep work in the solder joints indicate that WLP144 would have the lowest lifetime, followed by the CVBGA432 and CTBGA208.

Part	ΔW_{cr}	$345(\Delta W_{cr})^{-1.02}$ **Schubert** [52]	$(0.0019\Delta W_{cr})^{-1}$ **Syed, 2004** [46]	$(0.0069\Delta W_{cr})^{-1}$ **Syed, 2006** [47]
WLP144	2.3146	147	227	63
CVBGA432	0.7180	484	733	202
CTBGA208	0.4752	737	1108	305

Table 18 BLR energy-based life prediction of the BGA parts.

3.2.3 BLR Results

Figure 80 compares the analytical, numerical, and experimental results. Figure 81 shows the percentage error to the test result from the prediction methods.

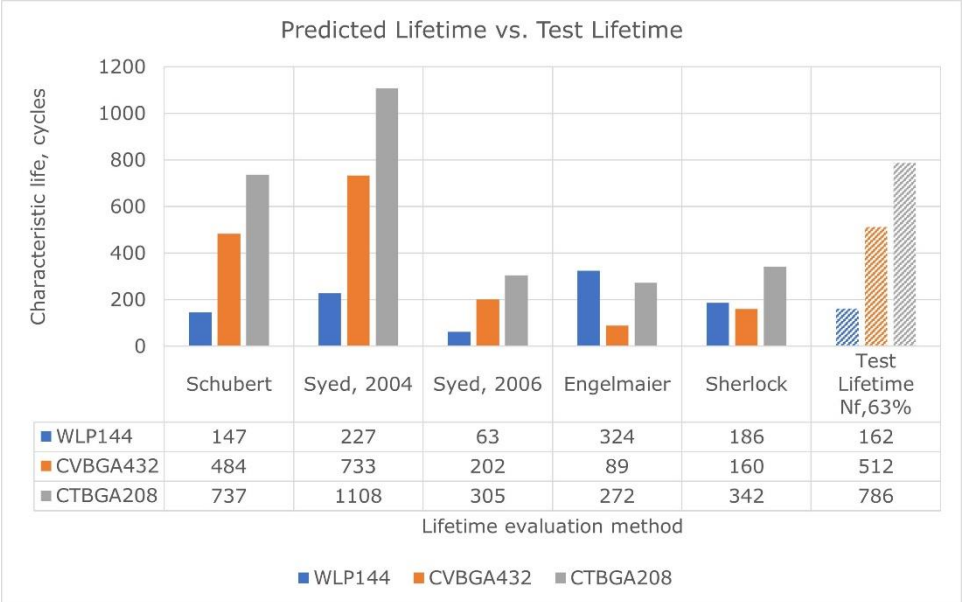


Figure 80 BLR characteristic life evaluation by the different methods considered.

Both analytical methods overpredict the lifetime of the WLP144. Engelmaier predicts 2X, while Sherlock is within 15%. For the plastic BGAs, the analytical methods remain very conservative. Reference [43] discusses the key differences between the two analytical approaches. Although Sherlock uses the Engelmaier strain range at its core, it modifies it to account for the solder material. Further, the life prediction equation is different from the Engelmaier model.

From the FEA-based predictions, Schubert's model fits the experimental data best. The Syed 2004 overpredicts the lifetime by 40%. However, Syed updated the model in 2006. The latest Syed model underpredicts the lifetime by 61% for all parts. The use of MPC constraints and a coarse mesh are critical modeling aspects that could explain the significant difference in the experimental data. In [47], Syed shows the over-constraining effect brought by MPC constraints close to the joint region and the mesh density effects. Comparing the characteristic life to the mean life predicted by the Syed and Engelmaier models also adds a 5-10% deviation.

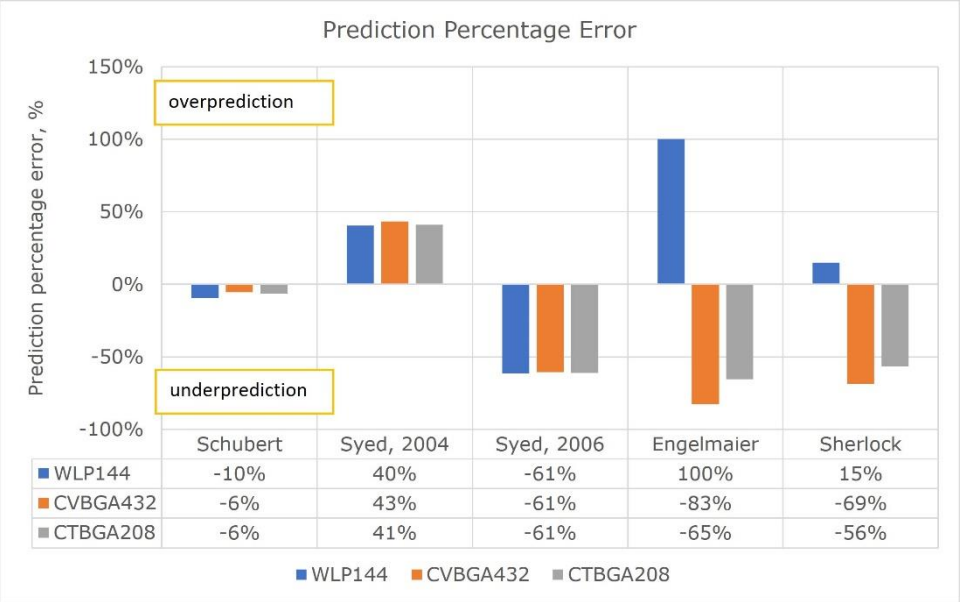


Figure 81 BLR prediction percentage error to test result.

While the analytical methods provide a fast assessment, they require a deeper analysis of all internal parameters and a more extensive data set for validation. The FEA-based prediction models show consistency across the considered components. Although the Schubert model best fits the data set, a different modeling approach would result in a better fit for the Syed models.

3.3 System-Level Reliability Assessment

The main effect that a system integration brings is the PCBA-constrained deformation due to its fixations. To emulate system-level effects, we fix the four holes of the PCBA as in Figure 82 and re-solve the model without any other changes. Figure 83 shows the warpage of the PCB assembly under system-level boundary conditions. The maximum deformation occurs at 125°C at the beginning of the dwell period. The PCBA center expands, resulting in a 2.70 mm deformation. At negative 40°C, the board returns to its original shape, with a maximum warpage of 46 µm. At both temperatures, the maximum warpage occurs at the CTBGA208.

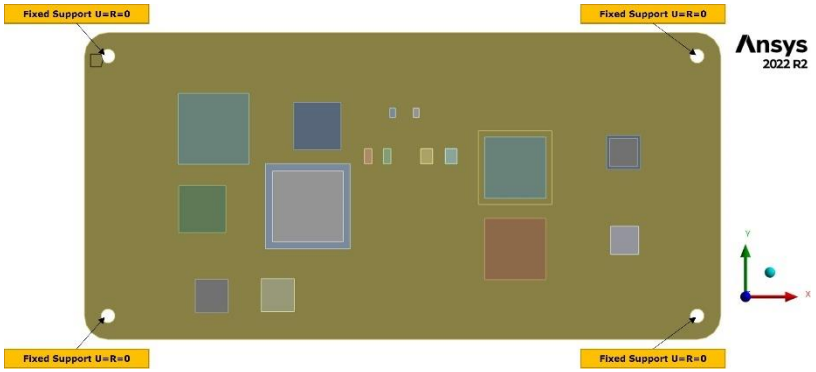


Figure 82 SLR boundary conditions. Image used courtesy of ANSYS, Inc.

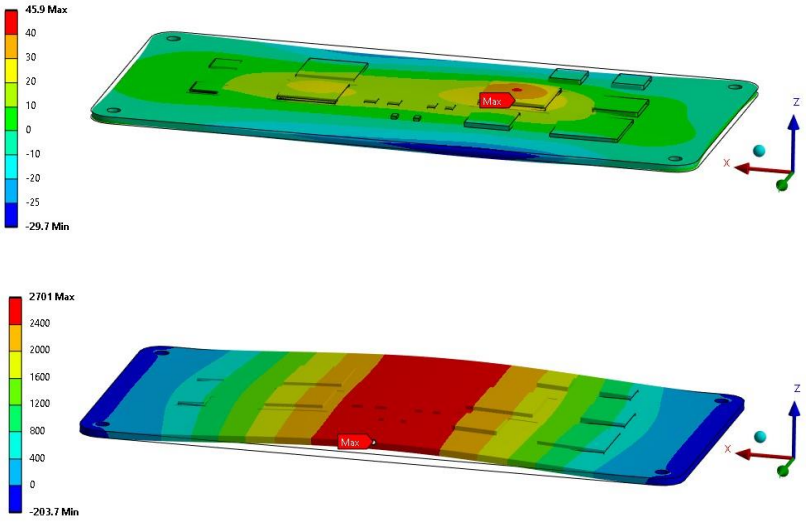


Figure 83 Directional deformation of the SLR PCBA in Z direction at -40°C (top) and 125°C (bottom). The wireframe shows the undeformed shape. Legend units: µm. Deformation scale factor: 35 for -40°C and 1 for 125°C. Images used courtesy of ANSYS, Inc.

Figure 84 shows the equivalent von Misses stress in the solder joints and the elemental averaged creep strain energy density (NLCRWK) accumulated during one thermal cycle. Although the critical interface remains the same as in BLR, see Figure 85, the distribution of stresses and strains differs from the BLR results in Figure 73. Under SLR boundary conditions, the solder joints in all parts are under slightly lower stress than in BLR. However, the elemental NLCRWK output, except for WLP144 is significantly higher. The averaging volumes remain as in BLR, in Figure 75.

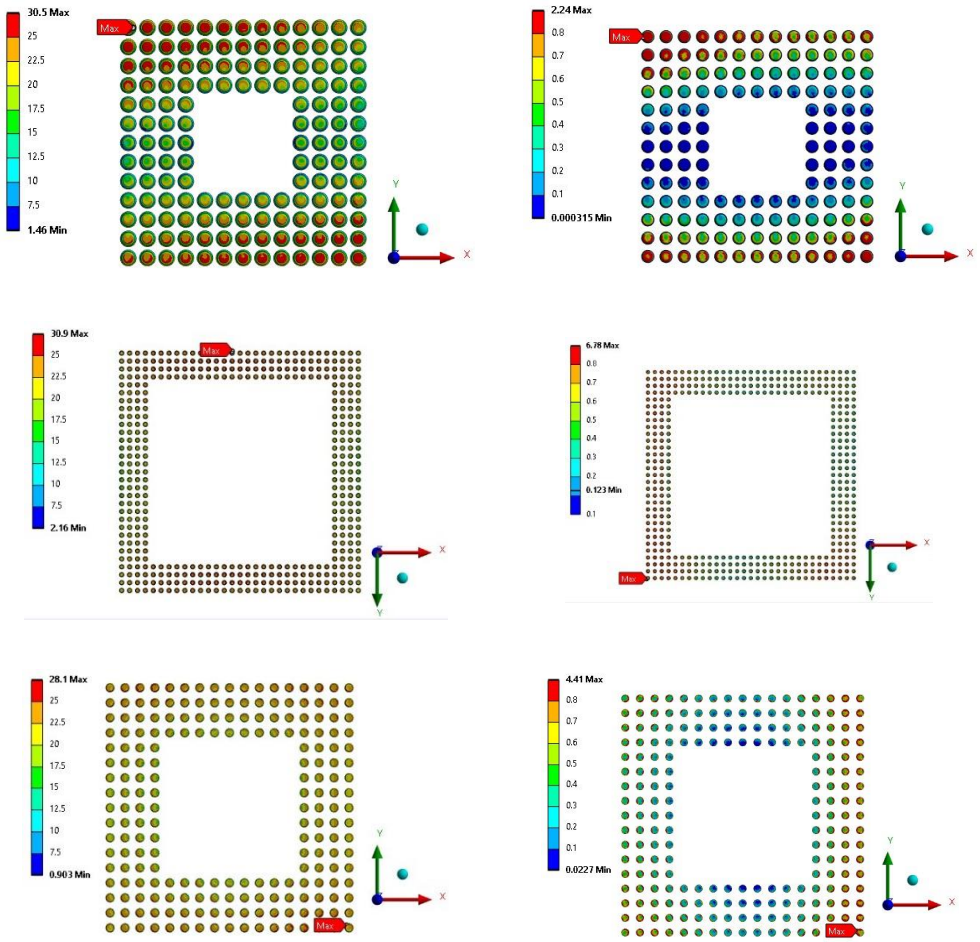


Figure 84 SLR stress (left) and inelastic strain, NLCRWK, (right) distribution in the solder joints in WLP144 (top), CVBGA432 (middle), CTBGA208 (bottom). Legend units: MPa, mJ/mm^3. Images used courtesy of ANSYS, Inc.

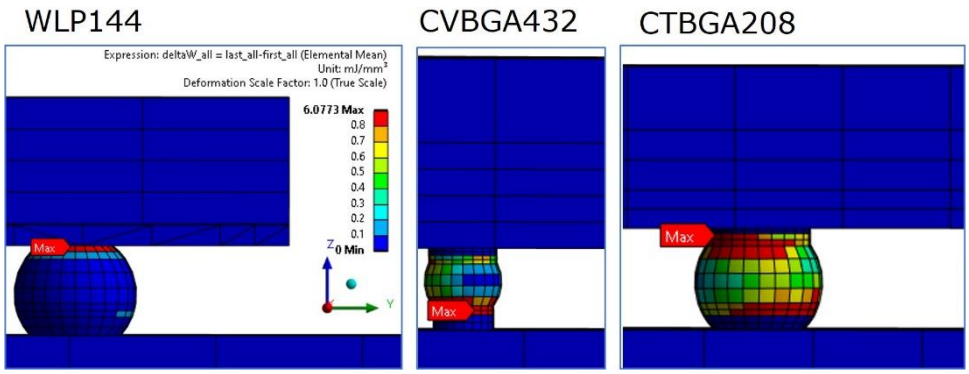


Figure 85 SLR elemental-averaged accumulated creep energy density (NLCRWK, mJ/mm³) in the critical solder joints. All plots have the same scale and legend as for WLP144. Images used courtesy of ANSYS, Inc.

For the SLR assessment, we plot ΔW_{cr} from both BLR and SLR setups. Figure 86 shows higher creep deformation in BLR than in SLR for the WLP144. In SLR, the critical solder joint is now on the opposite edge of the array. Figure 87 shows more significant creep damage in all joints in the SLR configuration for CVBGA432. In this case, the critical joint is also at the opposite corner. Figure 88 shows the same behavior for the CTBGA208 as described for the CVBGA432.

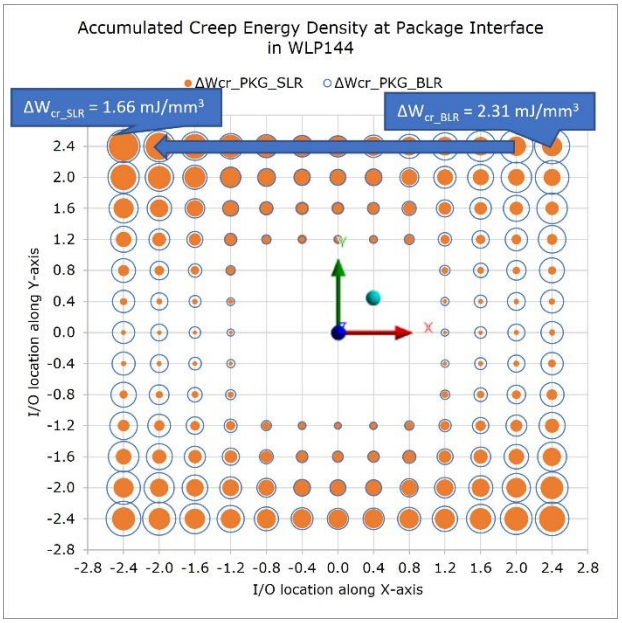


Figure 86 SLR vs. BLR bubble plot of the WLP144 showing the accumulated NLCRWK in the package interface solder volume.

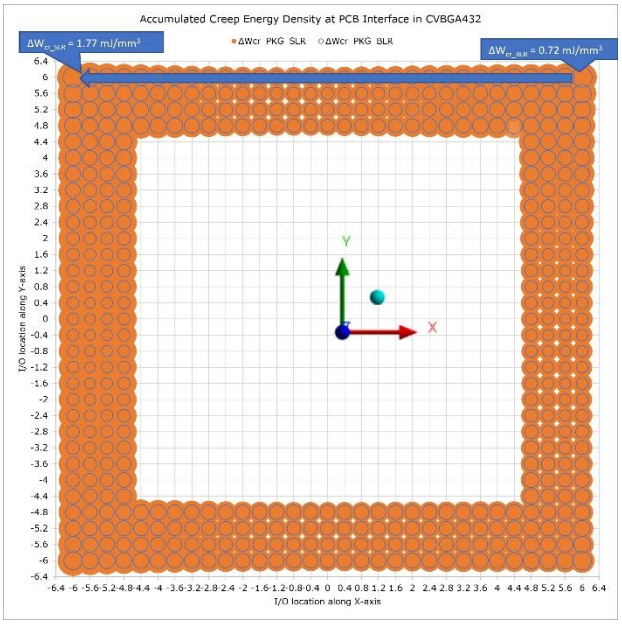


Figure 87 SLR vs. BLR bubble plot of the CVBGA432 (quarter package) showing the accumulated NLCRWK in the PCB interface solder volume.

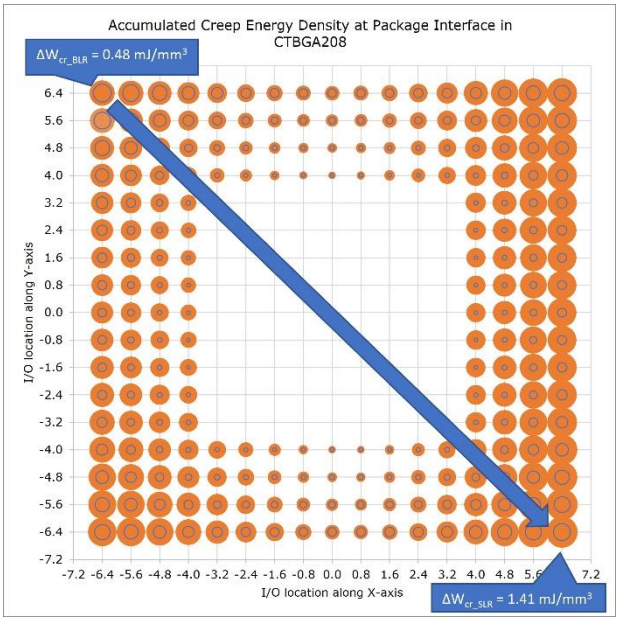


Figure 88 SLR vs. BLR bubble plot of the CTBGA208 showing the accumulated NLCRWK in the package interface solder volume.

Output	WLP144	CVBGA432	CTBGA208
$\Delta W_{cr,SLR}$, mJ/mm^3	1.66	1.77	1.41
$\Delta W_{cr,BLR}$, mJ/mm^3	2.31	0.72	0.48
$D = \Delta W_{cr,SLR}/\Delta W_{cr,BLR}$	0.72	2.46	2.97
Nf,63% (BLR)	162	512	786
Schubert, cycles (SLR)	206	193	243
SED-R (31), cycles (SLR)	227	204	259

Table 19 SLR damage and energy-based life prediction of the BGA parts.

Table 19 shows the failure criteria in SLR and life predictions. In the BLR analysis, the Schubert model provided the best results, so we further compare the Schubert prediction and the strain energy density ratio prediction in (31) based on BLR lifetime and damage. In the fixed PCB, the CVBGA432 have the lowest lifetime, followed by the WLP144 and CTBGA208 and, as shown in Figure 89. However, the WLP144 lasts longer in the SLR setup according to all prediction methods. Considering the damage to be the creep strain energy ratio, the WLP144 shows improvement from BLR with D lower than 1, while the other two parts show deterioration from BLR, with D higher than 1. In Figure 90, the Schubert et al. [52] and SED-R models predict a similar change in lifetime from BLR to SLR for all parts, in agreement with the damage factor. Overall, the WLP144 would survive about 40% more cycles, while the other two parts have a remaining life in SLR of 40% for CVBGA432, respectively 34% for CTBGA208.

We consider SED-R to give the most accurate prediction, being a direct function of the strain energy ratio (or damage) and the characteristic experimental life. Schubert et al. [52] model predicts values within 10% of SED-R. We find the damage factor to be a valuable indicator in system-level reliability assessment, along with the bubble plots, which help visualize the damage occurring in the solder joints.

Besides these comprehensive tools in system-level reliability assessment, the PCB model plays a crucial role. PCB homogenization is acceptable. However, copper distribution influences the creep damage occurring in the solder joints. During the research period, we discussed PCB modeling and calibration in [79], [80], and [84]. While PCB homogenization provides satisfactory results considering the added efficiency, component homogenization would not be suitable for SLR, as the die size, die-attach, and position are relevant in the local CTE mismatch.

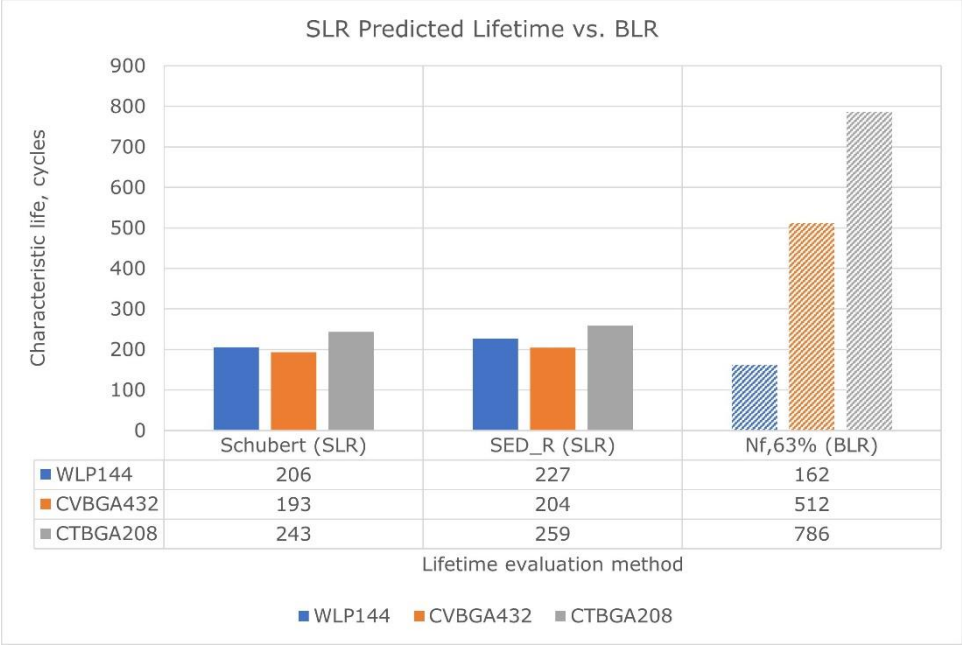


Figure 89 SLR vs. BLR characteristic life evaluation by the different methods considered.

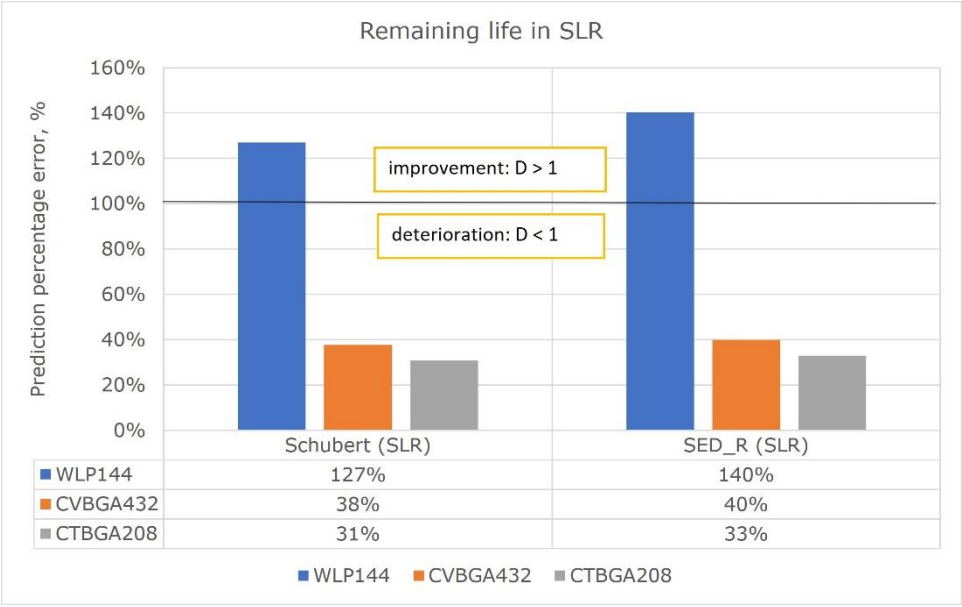


Figure 90 Remaining life in SLR.

3.4 System-Level PCBA Low-Cycle Fatigue Assessment Workflow

The first part of the research program (2017-2020) focused on independent study, networking, testing and review of tools and methods, which resulted in an early proposal of the discussed workflow.

After establishing the research niche, the author reviewed prior work on this topic in the Continental ADAS department. The senior engineers have previously worked on component-related failure analysis with chip suppliers in special workgroups investigating failures such as solder fatigue cracks and via cracks. It then became apparent that the development process required a system-level reliability analysis step. Two main reasons for investing in a simulation process are loss of knowledge due to high employee turnover and the spread of ad-hoc, uncontrollable methods in a growing team of FEA engineers.

The prior work used the SED-R approach. However, more knowledge was needed on electronic components modeling to ensure consistent outputs from one task to another. The author reviewed the relevant literature through independent study and focused on material modeling and life prediction methods. Specialists and experts in different company groups proposed approaches such as the Schubert or Syed models, SED-R or Sherlock. The FEA assessments focused only on the corner joints due to the enormous volume of manual data post-processing. The unavailability of packaging data for accurate modeling leads to multiple assumptions, making models such as Schubert or Syed challenging to use.

The first draft of the simulation workflow used the SED-R approach to determine the remaining life percentage of new packages when assembled in the autonomous mobility sensors. An inconsistent modeling approach, lack of support and training documentation, and insufficient data leads to inconsistent results. Without experimental BLR, the SED-R can determine the lifetime percentage change from BLR to SLR, which is often insufficient to drive improvement measures.

Further, we focused on expanding the internal and external network to create a flow of information for better modeling. With BLR data from suppliers, SED-R could predict the lifetime of the system setup. Further collaboration with suppliers revealed industry-specific methods and techniques, such as the “bubble plot”—automatic data extraction for all solder joints allowed for visually improved outputs and better modeling.

Next, the author improved material modeling and meshing, producing consistent outputs. The last step in defining the workflow was to tailor the simulation output to clearly answer the project requirement. The simulation tasks focused on determining the change in lifetime from BLR to SLR and stating the risk of failure based on the damage value. The results include the bubble plot on which we define the crosscuts in the test analysis. Finally, the solder joint reliability assessment provides two clear outputs with the outcomes described Table 20.

Simulation Output	Outcome
Failure risk of critical parts	The production implements targeted reliability-enhancing methods such as increasing solder volume and pad contact area, using high-reliability solder paste, and considering underfilling.
Cross-section definition	The post-test analysis time is reduced by at least one week.

Table 20 Simulation output and respective outcome.

Besides reducing the test effort overall, simulation helps reduce the DoE test matrices and impacts decision-making across the development chain. Simulation efforts significantly reduced the testing effort in part replacement design changes due to the global part shortage crisis.

Lastly, the work presented in this chapter provides insight in board-level reliability assessment through own experimental measurements, and analytical and numerical analysis. Following the board-level reliability assessment, we attempted an evaluation of the parts' reliability under simplified system-level boundary conditions. In the studied PCBA, changing the PCBA's boundaries impacts its reliability by up to 70%. Pursuing the research presented in this chapter and PCBA modeling studies in the published papers, in Figure 91, we propose a simulation workflow for PCBA low-cycle fatigue assessment.

We focus on low-cycle fatigue rather than reliability because the previous chapters showed how vital a calibration step is in lifetime prediction. The outputs are sensitive to model simplifications, mesh density and quality, which is difficult to control in an environment with multiple engineers with dissimilar experience levels performing the task. The system's integrator also collects data from different suppliers and various sources of questionable reliability.

The system-level analysis showed that even without a cycle prediction, there is valuable information in the analysis. We develop thus a simulation workflow focused on providing the development project team the following:

- Expected relative damage between BLR and SLR, focused on remaining life after assembly.
- Cross – section definition based on the bubble plot of the accumulated creep strain energy density in the solder joints in SLR.
- Safety factor and lifetime prediction when experimental BLR is available for validation and calibration.

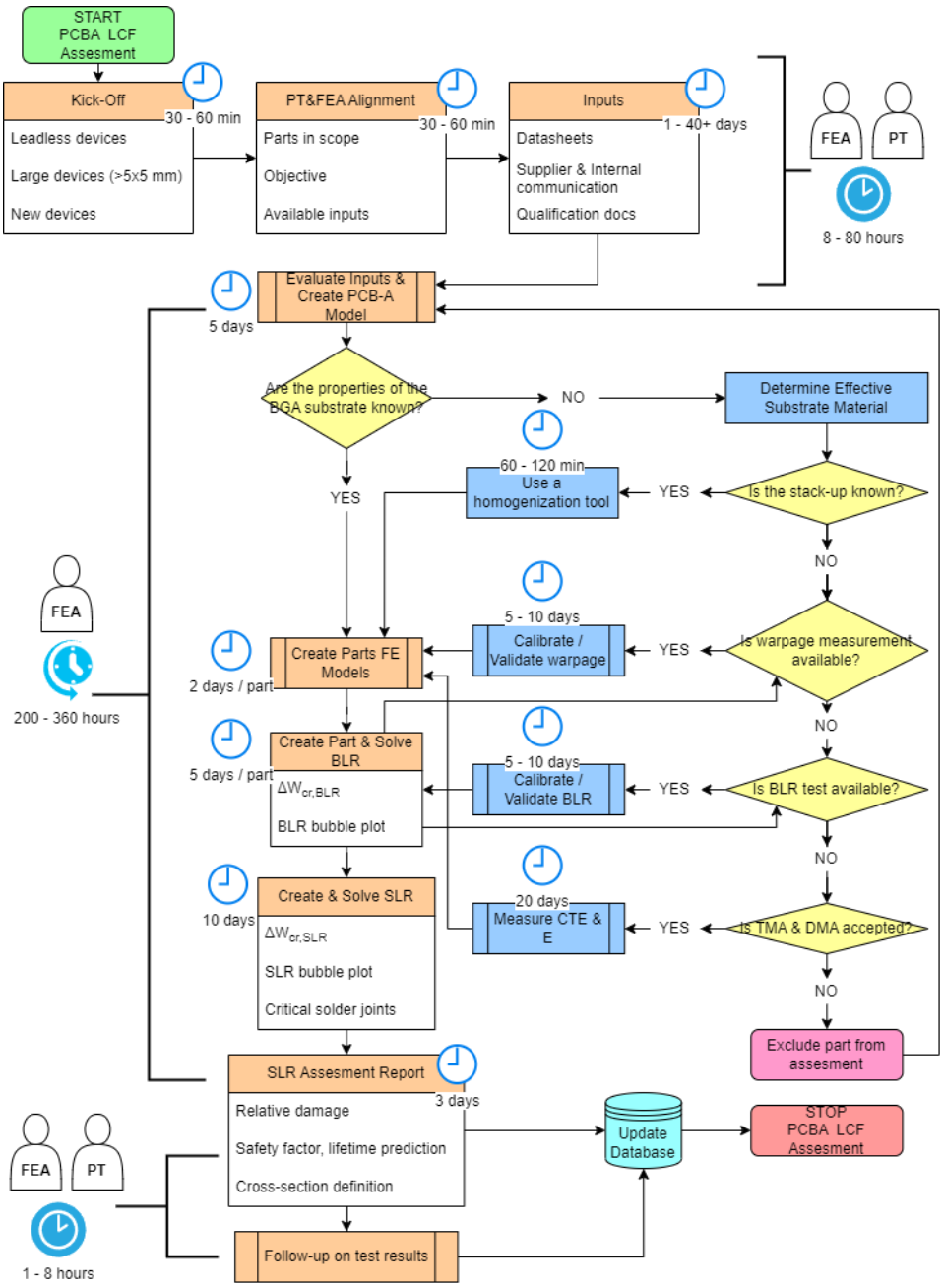


Figure 91 Proposed PCBA low-cycle fatigue assessment workflow showing all necessary steps and resources. Image used courtesy of Continental AG.

The proposed workflow starts with a kick-off section, where the project team (PT) selects the devices which require reliability assessment. As discussed in the literature review chapter, leadless and large devices are more sensitive to low-cycle fatigue. As an FEA engineer picks up the tasks in alignment with the PT, they decide the scope parts, the objective of the analysis and already available inputs.

The research period showed that gathering the inputs is the central blocking point in the workflow. The system integrator needs direct access to all the required information to model the parts. Different disciplines, such as hardware engineers, component engineers, supplier quality managers, and material engineers, have to work together to gather as much data as possible.

In [80] we discussed different approaches for PCBA reliability assessments. We concluded that section homogenization, suffices, although, for in-detail investigations, the engineers should have the means and skill to introduce traces in the model.

The FEA engineer evaluates the inputs and follows up on missing or incorrect data. Usually, the qualification documents, datasheets and direct communication with the supplier provide sufficient data. However, we determined that the characterization of BGA substrates is complex because they are multilayer PCB themselves. Often the engineer receives truncated or no information. In this case, whenever the engineer knows the stack-up and material properties of the substrate, he can create a homogenous material for the PCB.

The following approach would be calibrating on warpage measurements when available. In [84] we discussed more sophisticated calibration procedures based on inexpensive experimental measurements. Unfortunately, experimental determination of the part properties through TMA and DMA or its board-level reliability as the experimental work presented in 3.2.1 remains as last resort due to the prohibitive cost.

With all the necessary data, the engineer can create the BLR finite element model of the parts, as discussed in 3.2.2.3. Usually, the BLR model is a single part on a small PCB to simulate the standard reliability test [10]. The engineer should validate the FE model if experimental data such as warpage analysis or board-level reliability test results are available.

Following the BLR analysis, the parts should be integrated into the PCBA as in Figure 62 by creating a cut in the large PCB and introducing the BLR model.

The report should include the relative damage from BLR to SLR and cross-section definition for all parts. When BLR test results are available, the engineer should use the SED-R approach to predict the expected lifetime in SLR and the safety factor relative to the test requirement.

The FEA engineers return to the project team with the report and follows-up with the future qualification test results. The engineer closes the task once he updates the internal database.

The process has three significant steps:

- The initial phase requires communication and alignment between the project team. Depending on the availability of inputs, it takes 1 to 10 days that can spread across a more extended period, depending on the availability and difficulty getting parts data.

- When all inputs are available, the FEA process lasts about 25 days for one part and adds 5 days for each additional part. Additional calibrations or measurements will add 20 days more whenever data is missing.

- Finally, the post-processing takes about three days due to the large amount of data and inefficient APDL scripts that take much time to access result files.

3.4.1 Workflow Implementation, Standardization, and Validation

The implementation of the proposed workflow spanned three years in distinct stages:

- Build knowledge and competence through corporate worldwide solder joint reliability learning sessions (2020) with 67 participants from ten departments, corporate technical hours (2021), cross-department one-to-one training and support on tools and methods (2021-2022), and regular user group meetings (2022-2023).

- Coordinate and lead solder fatigue simulations in a global team of ten structural analysis engineers, one-to-one training, and support (2020-2023).

- Implementing the workflow on more than 70 parts on 17 product designs, focusing on providing clear outputs, such as the risk of failing the design validation test and cross-section definition (2020-2023).

The standardization phase took place in late 2022 as in the form of a predictive reliability assessment process, including process training, step-by-step tutorials, supervision of ongoing tasks and predictive reliability assessment technical hour for non-specialized audiences.

The process training introduces the topic, focusing on the solder joints and the fatigue failure mode due to creep deformation and further explaining the simulation approach. The process training defines the possible simulation tasks, the outputs and respective applicability as in Table 21. The simulation task will always be a comparison between different components, thermal conditions, PCB designs or mechanical designs. Stand-alone life prediction requires a BLR test result to be available. Within the FEA team, the process requires the engineers to follow the guidelines and tutorial materials to ensure consistent outputs. They discuss and review ongoing tasks in a dedicated meeting. Finally, technical talks with non-specialized audiences aim to reach the project teams, inform them about the topic and offer support.

Simulation	Result	Applicability
Components	Damage assessment	PCB design
Thermal conditions	Life prediction (when experimental BLR is available)	I/O function check
PCB stack-ups	Cross-section definition	Sourcing
Designs		Mechanical design
		Post-test analysis

Table 21 Simulation comparison tasks, outputs and applicability.

In the validation phase we gathered data from 17 projects. Out of 70 parts, we could correlate 21 parts with the physical test outcome in Figure 92. We created a grading system, as in Table 22, to compare the simulation outputs to the test outcomes. The fatigue analysis correctly identified the failure risk for 17 parts, underestimated the risk for two flip-chip BGAs, one lead frame BGA and did not include one BGA.

Simulation Criteria	Test Criteria	Grade
Low (D<3 or SF>1.5)	minor crack <25% or pass	1
Medium (3≤D≤5 or 1≤SF≤1.5)	large crack 25-95% or pass	2
High (D>5 or SF<1)	full crack >95% or fail	3

Table 22 Grading system for simulation vs. test comparison. D stands for relative damage and SF for safety factor.

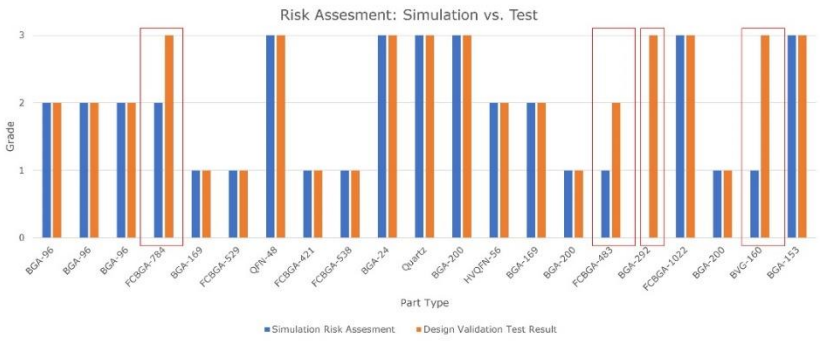


Figure 92 Validation of the proposed workflow: simulation vs. test risk assessment. Image used courtesy of Continental AG.

4 DISCUSSION

To answer the first research question, "How can virtual prototyping be used to improve the reliability of electronics?" the research findings indicate that predictive board-level analysis can be employed to compare different components, designs and materials.

Although not as precise as numerical methods, analytical methods can show the relationship between specific parameters, such as mechanical properties and shear strain developed in the solder joint. Similarly, one could customize geometries such as pad size and solder volume. Additionally, life prediction models can provide valuable insights into the future reliability of the electronic product when adequately calibrated. By considering factors such as material properties, operating conditions, and stress distribution, these models can estimate the lifespan of the electronics and identify potential failure mechanisms. This information allows engineers to make informed decisions regarding design modifications or material choices to improve the reliability and durability of the product. In particular, finite element analysis (FEA) based predictions offer advantages over analytical methods, as they can account for both local and global CTE mismatches, complex boundary conditions, and nonlinear behavior of materials. FEA models simulate the behavior of the electronics under various operating conditions, considering the complex interactions between different components. This comprehensive numerical analysis helps identify potential failure points and provides a more accurate assessment of the system's reliability than simplified analytical methods.

In the analytical approach, we could not achieve an acceptable correlation to experimental data. Although we are not pursuing life prediction as the primary goal, the analytical methods prove their worth in fast assessment of sensitivity of parameters. The FEA results were particularly good. The remaining drawback in the FEA analysis is not identifying the correct failure interface for one of the parts. We consider this result to be the outcome of assumptions such as PCB homogenization, interactions between the solder joints and PCB / substrate, chosen pad design or meshing.

Conversely, the system-level analysis helps detect weak points within the electronic system. Engineers can focus on these areas during the design and manufacturing processes by identifying critical solder joints prone to failure and taking necessary measures to enhance their reliability. Engineers can adjust designs, select appropriate materials, and improve manufacturing techniques for critical solder joints, enhancing overall reliability. Furthermore, the analysis aids in prioritizing testing and inspection efforts. By identifying the exact locations for inspection crosscuts, engineers can perform targeted inspections on solder joints most likely to experience damage or failure, leading to efficient quality control. By quantifying relative damage, engineers can estimate the product's lifespan and reliability under different operating conditions, facilitating proactive maintenance strategies and minimizing unplanned failures.

In evaluating the stress state in solder joints at the system level, we chose to directly integrate a detailed board-level reliability (BLR) model into the printed circuit board assembly (PCBA) within the system model. This method ensures consistency

over time and across different users, as demonstrated in the system-level reliability assessment conducted in our study. Focusing on the desired outcome is essential when choosing the appropriate simplifications for the system-level reliability assessment. Common simplifications include:

- homogenizing the PCB and substrates,
- disregarding intricate designs of parts such as wireframes, and
- removing non-essential components that do not significantly impact PCBA deformation.

By integrating a complex part model into the PCBA and simulating its deformation during temperature excursions, we can obtain valuable outputs for the system-level reliability assessment. One such output is identifying critical solder joints that may require redesigning input/output (I/O) functions.

Additionally, we can further evaluate the system's reliability by plotting the dissipated creep energy in the solder joints. This analysis allows engineers to determine if certain parts are prone to early failure and implement strategies to enhance reliability. Based on the analysis outputs, engineers can consider reliability-enhancing measures such as increasing solder volume, redesigning pads, or implementing underfilling techniques.

These actions aim to improve the strength and durability of the solder joints, reducing the likelihood of failure. Although this approach has limitations, it has proven applicable and effective in our system-level reliability assessment. By integrating detailed models and considering numerous factors, we can gain insights into the stress state of solder joints and make informed decisions to enhance the system's overall reliability.

Our research culminated in developing a simulation workflow for system-level reliability assessment, the foundation for a company-wide simulation process. While statistical validation of the outputs was not part of the research program, we conducted validation by applying the methods discussed in this thesis to over 70 parts across 17 different product designs. The results demonstrated a favorable outcome in terms of risk assessment when compared to test results.

However, despite the numerous benefits of system-level reliability (SLR) assessment and our efforts to establish an efficient methodology by combining commercial software, standardized techniques, and the latest research findings, the process has drawbacks. One prominent drawback is the availability of high-quality inputs. Acquiring the necessary data to perform simulations is often costly and confidential, making it challenging to obtain from third parties. Additionally, engineers need help with handling intricate designs and large simulation models. FEA engineers must specialize in constructing parts from drawings and schematics while navigating many documents to obtain the required inputs.

Furthermore, handling models with millions of nodes necessitates expensive computing power. Post-processing the results can also be challenging, as the developed scripts may be slow, and extracting results from large arrays may take longer than solving the model itself. The engineer involved in the process must

possess a deep understanding of the field and the ability to teach others, as system-level reliability assessment is rare for hardware or mechanical engineers. While each simulation saves time by eliminating trial-and-error engineering tests, the cost remains significant.

As devices become increasingly intricate and the new generation of heterogeneous integration reaches mass production, there is a growing need for higher automation in the proposed workflow. Future advancements should focus on automating the process to reduce the manual effort required. Nonetheless, the current workflow is a solid foundation for future system-level predictive reliability assessment endeavors. In summary, our research has led to the developing of a simulation workflow for system-level reliability assessment. While the process has demonstrated favorable outcomes in risk assessment, it also presents challenges such as limited input availability, managing complex designs and large models, and requiring extensive expertise. Despite these challenges, the proposed workflow serves as a crucial starting point for the future advancement and automation of system-level reliability assessment in the face of increasingly complex devices and heterogeneous integration.

In conclusion, our research has shown the potential of virtual prototyping and system-level reliability assessment in improving the reliability of electronics. Through board-level analysis and life prediction models, we can optimize specific aspects such as material properties, geometries, and operating conditions to enhance reliability and durability. Additionally, integrating detailed board-level models into the system-level analysis allows for identifying critical solder joints and prioritizing testing and inspection efforts, leading to more efficient quality control. These analyses provide valuable insights into the future reliability of electronic products and enable engineers to make informed decisions to enhance reliability.

However, further challenges need addressing. The cost of measurements and limited data availability from third parties need improving in acquiring high-quality simulation inputs. Managing intricate designs, large models, and the computational resources required also represent obstacles in the analysis process. Furthermore, system-level reliability assessment requires expertise and a thorough understanding of the field, which may be rare among hardware or mechanical engineers. Further research in automating the workflow and developing standardized techniques can streamline the process, reduce manual effort, and improve efficiency. Improvements in data accessibility, sharing, and confidentiality can also facilitate more accurate simulations. Additionally, advancements in computational resources and post-processing techniques can enhance the speed and reliability of the analysis.

Despite its limitations and challenges, the proposed simulation workflow is a solid foundation for future endeavors in system-level reliability assessment. With continued research and development, virtual prototyping and system-level analysis can significantly improve the reliability of electronics and contribute to advancing the field.

5 CONCLUSION

The significance of the research lies in addressing the need for a continuous quality improvement strategy in electronics development, particularly in the automotive industry, to prevent costly testing iterations and misidentification of failures resulting in costly recalls, field failures, and safety risks. The research can reduce testing costs, increase the ability to design better products, win customers, help manufacturers collaborate with suppliers, and improve the reliability of the final product. The proposed methodology addresses the problem by highlighting industry-level applications, identifying the limits of applicability of current research, and investigating the challenges of system-level modeling and analysis. It can advance the field by providing a standardized approach to system-level simulations, creating a solid foundation for complex investigations and failure analysis, and improving the reliability of electronic devices. The potential consequences of not addressing the problem include costly testing, recalls, field failures, safety risks, losing potential customers, and struggling to keep up with the industry's innovation pace. The economic aspects of the research are significant, particularly in the context of European manufacturing, where expensive workforces, energy prices, and chip shortage crises are present.

5.1 Research Contributions

5.1.1 Literature review

The main contributions of the literature review conducted for the thesis and published papers contributions are:

- Solder material models and corresponding FEA-based life prediction models in Table 2, Table 3, Table 4, Table 5, and Table 6.
- Analytical life prediction models in [43].
- BLR experimental data and related part characterization in [43].
- PCB material models in [79], [84], and [80].

5.1.2 PCB Modeling

The research papers [79], [84], and [80] contributed to PCB modeling.

Reference [79] evaluates seven popular methods of modeling the PCB considering various levels of homogenization: whole section homogenization, layer by layer homogenization or mesh element-based homogenization. The aim is to predict the static and dynamic behavior of the board and determine the influence of material parameters. This work was the first step in addressing the PCB modeling for further reliability analysis. The work concludes that considering the complete board made of FR4 or layers of FR4 and copper is a gross assumptions that does not reflect the correct stiffness of the board. Considering the copper percentages in the layers, a homogenized board predicts the reaction force response between 10-30%, depending

on the homogenization tool used. The more intricate models provided satisfactory results for a bare board but proved too stiff for the assembled board.

The work in [79] required building a 3-point bending test setup, which was further used for the experimental measurements in [84] and remains to be used in future PCB characterization activities. In [84] we generated a new set of experimental data, including strain measurements. One goal is to analyze the response of the PCB under five modeling approaches: homogenized orthotropic, homogenized transverse isotropic, homogenized isotropic, complete circuit model including the copper artwork and a mesh-based homogenized model. Another aim is to calibrate a homogenized orthotropic section through sensitivity analysis and parameter optimization. Results concluded that a homogenized, transverse orthotropic PCB model is accurate and cost-efficient. However, it does require careful characterization of each layer prior to homogenization to obtain a response within 10% of experimental results. Although we calibrated the material for static and dynamic responses, the results indicate that calibrating on either the static or dynamic response suffices. Material characterization through calibration is more expensive, but desirable for applications requiring unique materials, such as RADAR devices. Another outcome of the research was that for analysis where the PCB plays a secondary role, such as a dynamic analysis focused on the design of a fixation bracket, the engineer could consider a material model available in literature instead of a sophisticated PCB material model.

Further, reference [80] focuses on the impact of PCB modeling in reliability assessment. We evaluated the mode shape results and acceleration response as a first step in a future low-cycle fatigue reliability assessment. Further, we evaluated the elastic strain and warpage in the PCB for low-cycle fatigue reliability assessment and the creep response in the solder joint. The PCB models were the homogenous calibrated model in [84], a complex trace model including the copper artwork, and a mapped mesh-based homogenized model. All models predicted the first natural frequency within 5% and the acceleration response within 10%. The strain response under 3-point bending was within 15%. The research shows that including the copper artwork leads to 25% less warpage and up to 40% less creep work accumulated in the solder joint. Given the complex nature of the models, they present a challenging further research. Lastly, the paper also discussed the material assumptions in the general population of the PCB.

Considering the outcome of the PCB modeling research conducted, we considered a homogenous transverse isotropic PCB model for the work presented in this thesis. The calculated in-plane elastic modulus was within 3% of the DMA measurement and the calculated CTE within 13%.

Overall, the PCB modeling related research contributions include an evaluation of PCB modeling possibilities, a test flow for cost efficient PCB response assessment, and a PCB material calibration procedure. The research is the ground stone for subsequent ongoing efforts in developing a PCB and component modeling workflow for strain analysis.

5.1.3 System-Level Modeling

In [67] and [78], the research focused on system-level modeling by integrating detailed board-level models into the system model to analyze the

reliability of the entire electronic system. By considering the interactions between different components and their impact on reliability, these studies help understand system-level effects on reliability.

Research paper [67] discusses the prediction models such proposed by Schubert et al. [52] and Syed [46] [47], as well as Sherlock's thermomechanical analysis capability and the use of SED-R combined with experimental BLR. The research focused on two flip-chip BGA parts. The Schubert model predicted the characteristic life of one of the BGAs with a 3% error, while the Syed [47] model had a 58% error. However, the two literature models in system-level analysis were very conservative, with SED-R providing a more realistic result. We appreciated Sherlock as a valuable pre-processing tool. Overall, the paper outlined the importance of SLR in the context of reliability drop due to PCB constraints and the need for experimental BLR to correctly assess both SLR reliability and the impact of different thermal cycling conditions between BLR and SLR.

In [78], the focus was on FE modeling to address the challenge of model management in SLR. The SED-R approach simplifies the model because the results are not linked to specific empirical parameters, as for literature prediction models.

The system-level modeling contribution of [67] and [78] is evaluating system-level reliability assessment under different methodologies. They show that different approaches lead to different results and outline the need for BLR experimental data availability for trustworthy SLR life predictions. They also showed the applicability of the SED-R approach and Sherlock as a pre-processor.

5.1.4 Experimental Data, Analytical Calculations, Numerical Simulations

The thesis and [43] publish experimental data for three BGA parts, analytical calculations, and numerical simulations.

The thesis contributes with a detailed BLR analysis using FEA using three FEA-based prediction models and two analytical approaches. Chapter 3.2.1 and the journal paper [43] include BLR experimental data, geometry and material parameters for further study. Besides the experimental data in the thesis, the article collects data from literature. The article focuses on analytical methods and discusses the intricacies and parameters considered.

5.1.5 System-Level Approach, Workflow, Proposed Tools & Methods

The thesis proposed a system-level approach to reliability assessment and developed a comprehensive workflow. It introduced tools and methods to streamline the analysis process, ensuring consistency and efficiency in reliability evaluations. These contributions provided a structured framework for conducting system-level reliability assessments. The workflow allows for accurate task planning and defines the responsibilities within the development team. This workflow comprises three significant phases:

- Initial Phase: Involves communication and alignment within the project team and lasts 1 to 10 days, depending on input availability, which may extend over a more extended period.
- FEA Process: Takes approximately 25 days for one part, with an additional 5 days for each extra part. Additional calibrations or measurements can extend this period by 20 days if data is missing.
- Post-Processing: Requires around three days, due to the large volume of data and inefficient APDL scripts for accessing result files.

The proposed workflow for reliability assessment of electronic devices begins with a kick-off phase in which the project team (PT) identifies the devices requiring assessment. The literature review has highlighted the sensitivity of leadless and large devices to low-cycle fatigue. An FEA engineer then collaborates with the PT to define the scope, analysis objectives, and available inputs.

The workflow's central challenge is gathering necessary inputs. System integrators require access to comprehensive information to model the parts effectively. This necessitates collaboration among various disciplines such as hardware engineers, component engineers, supplier quality managers, and material engineers. Their collective effort aims to collect as much data as possible.

The FEA engineer then evaluates the inputs, addressing missing or erroneous data. Qualification documents, datasheets, and direct communication with suppliers provide the necessary information.

Once all necessary data is acquired, the FEA engineer constructs the BLR finite element model of the parts, typically as a single part on a small PCB, to simulate standard reliability tests. Validation is crucial, especially when experimental data like warpage analysis or board-level reliability test results are accessible.

Following BLR analysis, the parts are integrated into the PCBA, creating a cut in the large PCB and introducing the BLR model. The report should encompass relative damage assessments between BLR and SLR and cross-section definitions for all parts. In cases where BLR test results are available, the SED-R approach is employed to predict expected SLR lifetimes and safety factors relative to test requirements.

The FEA engineers return to the project team with the report and monitor future qualification test results. The task is considered complete once the internal database is updated.

In summary, this proposed workflow involves meticulous data collection, finite element analysis, and integration into the PCBA to assess electronic device reliability, with considerations for calibration and validation. The process duration varies based on data availability and complexity, with considerable time dedicated to post-processing tasks.

5.1.6 Proving the Influence of System-Level Effects on Part Reliability

The research in the thesis and papers [67] and [78] demonstrated the impact of system-level effects on part reliability. Considering the interactions and dependencies between components, the research shows that system-level factors can significantly reduce the reliability of individual parts. This finding emphasized the importance of system-level analysis in improving overall reliability.

5.1.7 Competence Building and Knowledge Sharing

The research aimed to build competence through coaching, dissemination, work groups, and company-wide implementation. By creating awareness and facilitating knowledge sharing, the research contributed to the development of expertise in the field of reliability assessment. This effort is aligned with the heterogenous integration roadmap and aims to demystify thermomechanical analysis and electronics design in product development.

In support of the proposed workflow, the author created unpublished step-by-step tutorials for each phase, from data gathering to results post-processing.

5.1.8 Simulation Process and Automatization Scripts

The research developed a simulation process and unpublished automatization scripts to streamline reliability assessments. These contributions improved the efficiency of the analysis process, reducing manual effort and increasing productivity.

5.2 Conclusions

In summary, the research contributions encompass PCB modeling, system-level modeling, the influence of system-level effects on part reliability, competence building, and simulation process development. These contributions advanced the understanding and application of reliability assessment in the field of electronics, with a focus on practical implementation and knowledge sharing within the industry.

The research addressed a practical problem in the automotive parts manufacturing industry by providing practical guidelines for predictive reliability assessment. The findings have real-world applications in selecting materials and components, optimizing mechanical designs, implementing redundancy, defining cross-section analysis, and proposing reliability enhancement measures. These guidelines serve as valuable tools for automotive manufacturers to enhance the reliability of their products, ensuring better performance and reducing the risk of failures in critical components.

The research outlook focuses on several critical areas for further exploration and development. These include automatizing processes through Python scripting for component creation and post-processing. Building a comprehensive database for materials and components is also an important aspect. Potential experimental areas for improvement are X-ray laminography for non-destructive failure identification and

high-reliability solder characterization. Additionally, the areas of interest are simulating exceptionally large arrays and using design of experiments (DoE) to determine system-level effects. The outlook also suggests using virtual build simulations to predict the lifespan of electronic products based on measured strain during testing. These directions highlight opportunities for future research to enhance the reliability assessment process and improve the understanding and prediction of the lifespan of electronic components.

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