SWITCHED CAPACITOR BASED MULTILEVEL INVERTER STRUCTURES WITH MINIMUM DEVICE COUNT

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Abstract: *This research work presents two novel switched capacitor multilevel inverter (SCMLI) structures. Both the proposed structures possess self-voltage balance capability. Further, a general structure of proposed SCMLI has been developed. An extensive comparative study has been performed with recently developed multilevel inverters in different aspects. Proposed topologies require lesser components like switching devices, capacitors, diodes, power supplies as compared to recently developed multilevel inverter structures to generate specific output voltage levels. Half-height fundamental frequency switching scheme is employed for the investigation. Different losses and procedure for selecting the switched capacitor have been discussed. The effectiveness and merits of the proposed topologies have been verified by extensive simulation study in MATLAB/Simulink of a 17-level inverter structure with four basic switched capacitor units. Further, a laboratory prototype of the same has been developed and experimentally verified for R-L, L and sudden load change conditions*.

Key words: *Capacitor Voltage, Half-Height, Multilevel Inverter, Switched Capacitor, Voltage Boosting*

1. Introduction

In recent years, one of the major challenges for the mankind is to prevent the climate change. It is widely known that one of the main contributors to the climate change is the generation of power from conventional energy sources like coal, oil, natural gas. The power plants based on these fossil fuels are producing maximum amount of greenhouse gases like CO_2, SO_2, NO_2 and are the leading cause of world pollution and global warming issues. One of the better solutions to prevent climate change is to harness power from renewable energy sources like solar, wind, fuel cell [1]. But most of the renewable energy resources generate DC energy. Thus, it is essential to find out an efficient energy conversion system that can be interfaced to the AC grid or a standalone load [2].

Multilevel inverter (MLI) is the key element for an efficient conversion system. It converts the generated DC voltage to an AC voltage. The classic MLI topologies are Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge (CHB). Although classic MLIs have proven their effectiveness in different industrial applications, but, failed to generate high quality output waveforms due to the requirement of large component count like switching devices, clamping diodes, capacitors, isolated DC sources. This further enhances the cost, complexity and size of the conversion systems [2-6]. In addition, the classic topologies do not have the capability to boost the input voltage. Although, by incorporating a front-end converter system, voltage boosting may be possible, but this reduces the overall efficiency of the conversion system. It should be noted that as the generated voltage level for most of the renewable sources are low, the inherent voltage boosting capability of MLI structure is a desirable characteristic for renewable energy conversion systems [9, 12].

To overcome these limitations of classic MLI topologies, numerous innovative MLI structures has been introduced in the literature in recent years [9-25]. Authors of [10] introduced a new topology for cascaded multilevel converter based on sub-multilevel converter units and full-bridge converters. The presence of full bridge circuit across each module of the presented topology increases the component count, thereby increasing its cost and size. Researchers of [11] strived to propose a new single-phase cascaded multilevel inverter based on novel H-bridge units. For producing all voltage levels (even and odd) at the output, nine different algorithms are proposed to determine the magnitudes of DC voltage sources. This inverter topology needs four number of switches and two DC voltage sources across each module, which directly affects the size, cost and complexity of the structure. In [12], switched capacitor (SC) based hybrid MLI structures of two types are proposed. These topologies require large number of switched capacitors and

switching devices for producing higher output voltage levels with symmetrical DC voltage sources. As a result, the cost and losses will be increased and its industrial applications will be limited. Authors of [13] proposed a new MLI topology, which is generalized using the series connection of the fundamental blocks. Fundamental block used in this paper needs six unidirectional switches, four diodes and two input DC supplies for producing specific output voltage levels, which makes it costly, bulky and complicated. MLI presented in [14] has been obtained from series blocks of sub-multilevel inverter. The proposed sub-multilevel inverter utilizes two unidirectional switches, one bidirectional switch and two DC sources, making the structure disadvantageous for higher voltage levels. In [15], a SC based cascaded MLI is presented for high frequency AC power distribution. The topology is constructed by SC front-end and H-bridge back-end. It can be extended to several modules, but each module needs an H-bridge which enhances the number of switching devices in the inverter structure. Paper [16] presented a family of cascaded multilevel inverters (CMLIs), in which each stage is composed of two floating capacitors, one embedded DC voltage source and three power switches. In addition to the presence of large number of components in each stage, this topology requires more components in its current path as compared to other mentioned topologies. Researchers of paper [17] have presented a new capacitor diode structure for H-bridge based MLI structure. The proposed switched capacitor converter (SCC) requires large number of unidirectional and bidirectional switches, capacitors to accomplish high output voltage levels. In [18], an envelope type module based MLI is proposed. In this structure, each module requires different values of DC sources. In symmetrical mode, it requires large number of switching devices and DC power supplies to generate particular output voltage levels.

Thus, with the above literature survey, it can be said that the reduction of component count is one of the major research interest among researchers on inverter systems. In this paper, two switched capacitor based MLI structures have been proposed. Further, general structure of proposed topologies has been developed. The presented topologies are symmetric and modular in nature. Different quantities have been derived. An extensive comparison study with other topologies have been presented. The presented topologies have self voltage balancing capabilities. Half-height fundamental frequency switching scheme is employed for switching the proposed inverters. Extensive simulation and experimental results have been presented for 17 level proposed topology.

2. Basic Unit (BU)

Fig.1 (a) provides the basic circuit used in the proposed SCMLI. This circuit utilizes one DC voltage supply (V_{DC}), one passive diode (D), one floating capacitor (C) and two power semiconductor switches (S_1, S_2). This circuit is well known as series/parallel basic unit for SCMLI [12]. Photovoltaic (PV) cells, batteries and fuel cells can be used as supply voltage. The charging and discharging operations of the capacitor take place by connecting it in parallel and series with the input supply respectively as shown in Fig.1 (b) and (c).

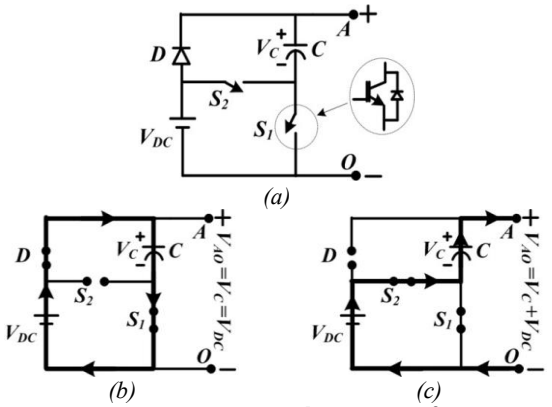


Fig. 1. Circuit presents (a) basic unit for proposed topology, (b) equivalent charging circuit, (c) equivalent discharging circuit

Table-1 gives the states of the switches and capacitor present in the circuit. When the switch S_1 becomes ON, the diode, D gets forward biased and charging operation of the capacitor takes place. In this state, capacitor stores energy from the supply and output voltage of the circuit (V_{AO}) is equal to V_{DC}. When switch, S_2 becomes ON, D gets reversed biased and the capacitor voltage (V_C) is connected in series with V_{DC}. Thus, V_{AO} becomes the summation of V_C and V_{DC} which is equal to $2V_{DC}$. Further, during this mode C discharges its stored energy towards the load. It can be assessed that simultaneous operation of S_1 and S_2 is avoided in order to prevent the short circuit across input supply. It can be noted that the basic unit can boost up the input voltage twice at its output terminals. Furthermore, one of the important merits of the circuit is the absence of extra complex charge balancing control circuit for capacitor voltage.

Table 1. Switch and capacitor states for Basic Unit

Circuit Condition	Switches S_1	S_2	D	V_{AO}	C state
1.	1	0	1	V_{DC}	Charging
2.	0	1	0	$2V_{DC}$	Dis-charging

3. Proposed SCMLI

In this section, two topologies based on switched capacitor *BU*s are introduced. These topologies are symmetrical in nature, thus, have equal magnitude of input DC supplies. Further, the topologies are based on

developed H-bridge structure and bidirectional switches. The developed H-bridge consists of six number of unidirectional switches. Like H-bridge structure, the developed H-bridge is used to act as polarity generation circuit. But the stress across the switches are lesser than that for H-bridge switches. The proposed two structures are described in the following sub-sections.

3.1. First Proposed Topology

The first proposed SCMLI is shown in Fig.2 (a). It consists of *n* number of modules connected in series. Each module is developed by using four *BU*s. For module-1, the basic units are BU_{11}, BU_{12}, BU_{13} and BU_{14}. It can be observed that BU_{11} and BU_{12} are in the same direction of polarity (in upper direction) whereas the polarity for BU_{13} and BU_{14} are in the same direction (in lower direction). Further, each module contains developed H-bridge and bidirectional switches (*BD*). Bidirectional switches are used in between the *BU*s to clamp the midpoint of the *BU*s to the output terminals of the modules. For module-1, the bidirectional switches are BD_{11} and BD_{12}. BD_{11} clamps the midpoint of BU_{11} and BU_{12} at the output terminal A_1 of module-1, whereas BD_{12} clamps the midpoint of BU_{13} and BU_{14} at the output terminal B_1 of the module-1. Similarly, the other modules are developed. The unidirectional switches for developed H-bridge for module-1 are S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{1e}, S_{1f}. The switches are used for the generation of different positive and negative voltage levels across A_1 and B_1. It is observed that each *BU* produces two voltage levels (V_{DC} and $2V_{DC}$), thus the maximum voltage level generated by each module is $8V_{DC}$. Therefore, each module can generate 17 voltage levels at its output terminals A_1 and B_1.

Table 2. General expressions for different parameters of first and second proposed topologies

Parameter	First topology	Second topology
N_{level}	$16n+1$	$8n+1$
N_{sw}	$14n$	$4n+6$
N_{BD}	$2n$	$2n-2$
N_{dc}	$2n$	$2n$
N_{cap}	$4n$	$2n$
N_{diode}	$4n$	$4n$
$V_{O\max}$	$8nV_{DC}$	$4nV_{DC}$
V_{stress}	$36\left(\sum_{k=1}^{n} k\right)V_{DC}$	$\left[4\sum_{k=1}^{n} k+8(n+1)\right]V_{DC}$

Similarly, the other modules can generate 17 voltage levels at their output terminals. This proposed structure is in modular form. Further, the total standing voltage (*TSV*) of all the modules is same. This facilitates the interchange ability among the different modules. Hence, if any module gets damaged, it is easily replaceable. In addition to that, if any module becomes faulty, by proper switching, the inverter can be run at lower voltage levels to supply the load. Further, the topology requires less power supplies because capacitors act as the alternative power supplies. Also, it does not require any complex charge balancing algorithms for maintaining the capacitor voltages, which is one of the major merits of the proposed topology.

3.2. Second Proposed Topology

The second proposed topology is shown in Fig.2 (b). This topology can be considered as the extended version of one module of first proposed topology. It comprises of *2n* number of *BU*s, of which *n BU*s are connected in series in one side and rest *n BU*s are connected on the other side of the structure. The polarities for BU_{11} to BU_{1n} are in same direction (upper direction) where $BU_{1(n+1)}$ to BU_{2n} are in same direction (lower direction) as shown in Fig.2 (b). In this inverter structure, one bidirectional switch is utilized between two consecutive *BU*s so that the mid-point of the *BU*s can be clamped to the output terminal and all the voltage levels can be generated across the output. A developed H-bridge is used to change the polarity of the output voltage levels. This topology utilizes lesser switching devices to generate same voltage levels at the output terminals as compared to first topology. Nevertheless, the blocking voltage of the switches of developed H-bridge is higher compared to that for first topology. Thus, in low and medium voltage applications, second topology is more suitable as compared to the first topology. Further, the gate driver requirement for second topology is lower than that for first topology.

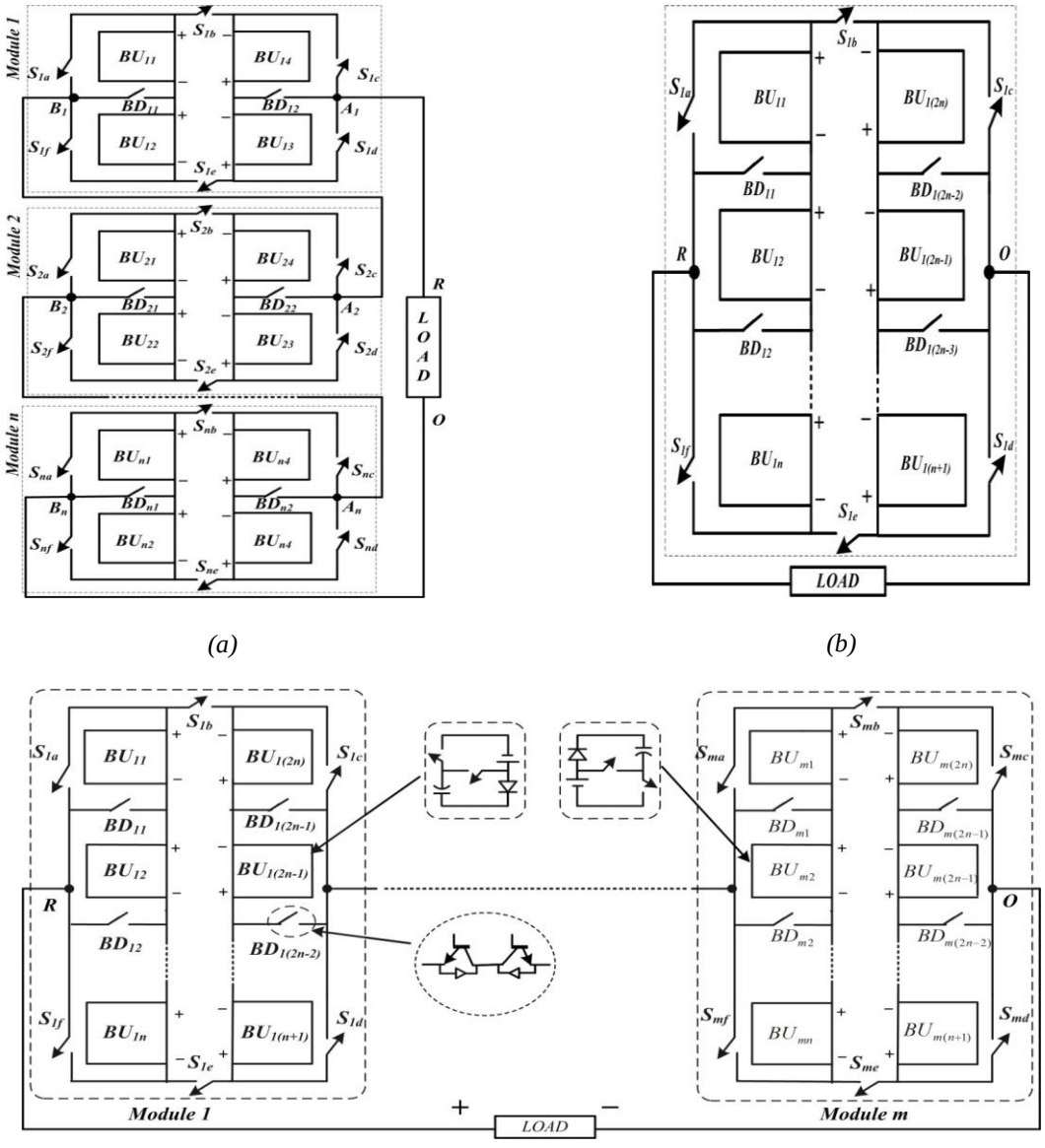
An extensive comparison study of proposed topologies with other MLI topologies is presented in section 8. The general expressions for the various parameters of the first and second topologies are shown in Table-2. Where *n* represents the number of modules in first topology and the number of *BU*s connected in series on one side of the second topology. N_{level} represents the generated output voltage levels.

The required unidirectional switches, bidirectional switches, DC supplies, capacitors and diodes are represented as N_{sw}, N_{BD}, N_{dc}, N_{cap}, N_{diode} respectively. V_{Omax} and V_{stress} represent the maximum output generated by the proposed topologies and the total standing voltage of the proposed inverter structures respectively.

4. General Structure of Proposed SCMLI

The general structure of proposed SCMLI is formed by connecting *m* units of the second topology in series configuration, which is shown in Fig.2 (c). As shown in Fig.2 (c), each module comprises of six unidirectional power switches, (*2n-2*) bidirectional switches and *2n* number of *BU*s in series arrangement. By properly switching the different modules, different voltage levels can be generated between terminals *R* and *O*. As discussed earlier, each *BU* can generate two voltage

levels. So, one module of the general structure with *2n BU*s can produce voltage levels of (*8n+1*), which is same as that of the second topology. The series connection of two modules of the general structure can provide (*2×8×n+1*) i.e. (*16n+1*) voltage level. In the similar fashion, the general structure with *m* number of



(a) *(b)*

(c)

Fig. 2. Proposed Inverter Structures (a) First Topology, (b) Second Topology, (c) General Structure

modules can produce voltage levels of (*8mn+1*) at the output terminals *RO*. The first topology can be achieved from the general structure by considering *n=2*. The derived first topology will consist *m* number of modules. General expressions of several parameters such as number of voltage levels ($N_{level(G)}$), number of unidirectional switches ($N_{sw(G)}$) number of bidirectional switches ($N_{BD(G)}$), number of input DC supplies ($N_{dc(G)}$), number of capacitors ($N_{cap(G)}$), number of power diodes ($N_{diode(G)}$), maximum output voltage ($V_{Omax(G)}$) and total stress voltage ($V_{stress(G)}$) are provided below:

$$N_{level(G)} = (8mn) + 1 \tag{1}$$

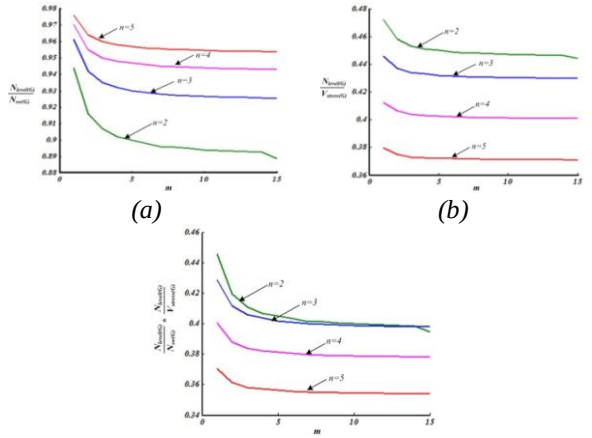
$$N_{sw(G)} = (4n + 6)m \tag{2}$$

$$N_{BD(G)} = (2n - 2)m \tag{3}$$

$$N_{dc(G)} = N_{cap(G)} = N_{diode(G)} = 2nm \tag{4}$$

$$V_{stress(G)} = \left[4\sum_{k=1}^{n} k + 8(n+1) \right] mV_{DC} \quad (5)$$

Here, *n* denotes the number of *BUs* connected in one side of each module and *m* represents the total number of modules connected in series configuration in the proposed general structure. The variation of ratio of number of voltage levels to number of required power semiconductor switches i.e. $N_{levels(G)} / N_{sw(G)}$ and the ratio of number of voltage levels to total standing voltage of the inverter i.e. $N_{levels(G)} / N_{stress(G)}$ with *m* for different values of *n* are illustrated in Fig.3 (a) and (b). As it can be clearly observed from Fig.3 (a), with increasing values of *m*, $N_{levels(G)} / N_{sw(G)}$ decreases for all values of *n* . Further, for a constant *m*, $N_{levels(G)} / N_{sw(G)}$ increases for the increasing values of *n*. The higher value of $N_{levels(G)} / N_{sw(G)}$ is desired for an efficient converter system. Thus in respect of $N_{levels(G)} / N_{sw(G)}$, the proposed topology should contain higher value of *BU*s in the structure which indicates the appropriateness of second proposed topology. From Fig.3 (b), it can vividly seen that with the increment of *m* , $N_{levels(G)} / V_{stress(G)}$ declines with all values of *n*. Further, for a constant *m*, $N_{levels(G)} / V_{stress(G)}$ is higher for decreasing values of *n*. It is desirable for an inverter structure that $N_{levels(G)} / V_{stress(G)}$ should be as high as possible. Thus in respect of $N_{levels(G)} / V_{stress(G)}$, the proposed topology should contain minimum number of *BU*s in the structure.



(a) *(b)* *(c)*

Fig. 3. Figures present the variation of (a) $N_{levels(G)} / N_{sw(G)}$, (b) $N_{levels(G)} / V_{stress(G)}$, (c) $(N_{levels(G)} / N_{sw(G)})(N_{levels(G)} / V_{stress(G)})$ w.r.t number of modules, *m* of proposed general structure.

So, first topology is preferable compared to second topology. Fig.3 (c) represents the variation of $(N_{levels(G)} / N_{sw(G)})(N_{levels(G)} / V_{stress(G)})$ w.r.t. *m* for different values of *n*. It can be observed that for lower values of *m* and *n* the proposed topology is more efficient.

5. Operating principle of Proposed SCMLI

The operating principle of the proposed inverter structure has been discussed in this section considering only four *BU*s in second topology or only considering module-1 in first topology. Fig.4 depicts the inverter structure with four *BU*s (BU_{11}, BU_{12}, BU_{13}, BU_{14}) two bidirectional switches (BD_{11}, BD_{12}) and six unidirectional switches (S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{1e}, S_{1f}). It can produce 17-level output voltage with a maximum value of $+8V_{DC}$ and minimum value of $-8V_{DC}$. Table-3 provides the switching states for generating different voltage levels across the output terminals *RO*. Where '*1*' denotes the ON state and '*0*' represents the OFF state of the switches present in the proposed inverter structure. Further, the capacitor states are presented in Table-3. '+' indicates the charging state of the capacitors and '-' denotes the discharging state condition of the capacitors. From the proposed topology as shown in Fig.4, it is evident that there have a number of redundancies to produce the different voltage levels at its output terminals. It is beyond the scope of this research work to find out the appropriate switching scheme such that minimum switching loss or optimal capacitor sizing can be found out due to the page limit. Thus, by employing switching as tabulated in Table-3, the different voltage levels at the output terminal have been produced.

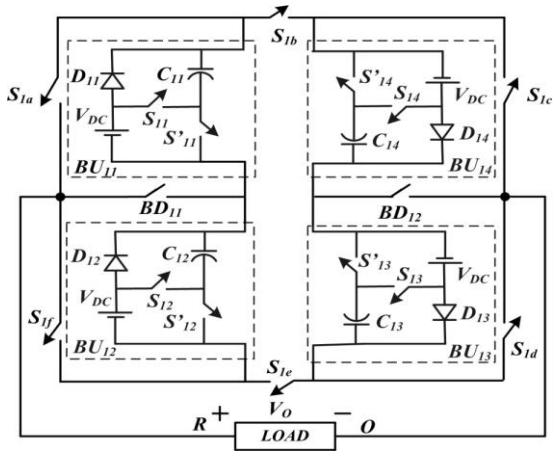


Fig. 4. Proposed 17 level SCMLI

The operating principle with this switching of proposed inverter is explained below:

- Zero voltage across the output terminals *R* and *O* is generated switching ON either S_{1a}, S_{1b}, S_{1c} or S_{1f}, S_{1e}, S_{1d}. In this circuit condition, all the *BU*s are in either not connected (NC) condition or charging state condition. In Table III, the zero output voltage with charging state condition of all *BU*s is shown considering only one switching state.
- $+V_{DC}$ will appear across *R* and *O* by maintaining charging state either BU_{12} or BU_{13}. In this circuit condition, BU_{11} and BU_{14} are in either NC or charging state condition. In this circuit state, either BD_{11} or BD_{12} is in ON state condition.

- Similarly the other voltage levels can be generated by appropriate switching of the different *BU*s.

6. Switching Scheme

Modulation strategies can be high frequency or low frequency. Due to low switching loss, low frequency modulation strategy is preferable for multilevel inverters. Half-height fundamental frequency switching modulation scheme is employed for analyzing the proposed topology. In Half-Height modulation technique, the transition or switching points can be found out when the modulating signal increases to the half height of the level [26**]**. For an M level MLI, the transition points can be found out as follows-

$$t_i = \frac{1}{2\pi f_{ref}} Sin^{-1}\left[\left(i-\frac{1}{2}\right)\frac{2}{M-1}\right] \quad (6)$$

where $i = 1,2,3,.....,(M-1)/2$

7. Selection procedure for switched capacitors

For the selection of capacitors, the largest discharging time (LDT) of the capacitor in a fundamental cycle is required to find out. It is evident that during the discharging state condition of capacitors, the stored energy of capacitors is transferred to the load side. Thus, during LDT, the capacitor current is same as the load current.

Table 3. Switching states of different components present in proposed inverter structure

V_{RO}	BU_{11}	BU_{12}	BU_{13}	BU_{14}	Unidirectional Switches						BD Switches		Capacitor States			
	S_{11}	S_{12}	S_{13}	S_{14}	S_{1a}	S_{1b}	S_{1c}	S_{1d}	S_{1e}	S_{1f}	BD_{11}	BD_{12}	C_{11}	C_{12}	C_{13}	C_{14}
$+8V_{DC}$	1	1	1	1	1	0	1	0	1	0	0	0	-	-	-	-
$+7V_{DC}$	1	1	1	0	1	0	1	0	1	0	0	0	-	-	-	+
$+6V_{DC}$	1	1	1	0	1	0	0	0	1	0	0	1	-	-	-	+
$+5V_{DC}$	0	1	1	0	1	0	0	0	1	0	0	1	+	-	-	+
$+4V_{DC}$	0	1	1	0	0	0	0	0	1	0	1	1	+	-	-	+
$+3V_{DC}$	0	1	0	0	0	0	0	0	1	0	1	1	+	-	+	+
$+2V_{DC}$	0	1	0	0	0	0	0	1	1	0	1	0	+	-	+	+
$+V_{DC}$	0	0	0	0	0	0	0	1	1	0	1	0	+	+	+	+
0	0	0	0	0	1	1	1	0	0	0	0	0	+	+	+	+
$-V_{DC}$	0	0	0	0	1	1	0	0	0	0	0	1	+	+	+	+
$-2V_{DC}$	0	0	0	1	1	1	0	0	0	0	0	1	+	+	+	-
$-3V_{DC}$	0	0	0	1	0	1	0	0	0	0	1	1	+	+	+	-
$-4V_{DC}$	1	0	0	1	0	1	0	0	0	0	1	1	-	+	+	-
$-5V_{DC}$	1	0	0	1	0	1	0	1	0	0	1	0	-	+	+	-
$-6V_{DC}$	1	0	1	1	0	1	0	1	0	0	1	0	-	+	+	-
$-7V_{DC}$	1	0	1	1	0	1	0	1	0	1	0	0	-	+	-	-
$-8V_{DC}$	1	1	1	1	0	1	0	1	0	1	0	0	-	-	-	-

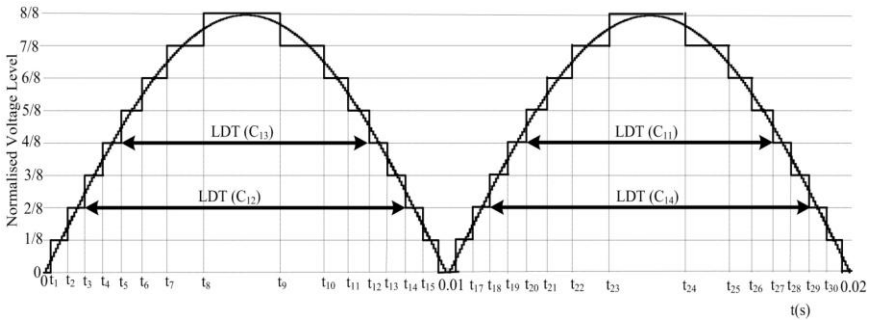


Fig. 5. Half-height switching scheme and large discharge time (LDT) for capacitors.

In Fig.5, the LDT for C_{11}, C_{12}, C_{13} and C_{14} are shown as per the switching states presented in Table-3. It can be observed that LDT for C_{11} and C_{13} are same whereas LDT for C_{12} and C_{14} are same. Thus, the maximum voltage ripple of the capacitors is proportional to the maximum amount of stored charge transferred to the

load side. During LDT, the capacitor discharges maximum amount of charge. The maximum amount of charge discharged by C_{11}, C_{12}, C_{13} and C_{14} during LDT are presented as follows:

$$Q_{C_{11}} = Q_{C_{13}} = \int_{t_3}^{\frac{T}{2}-t_5=t_{12}} I_{out} Sin(2\pi ft - \varphi)dt = \int_{t_{20}}^{2T-t_{20}=t_{27}} I_{out} Sin(2\pi ft - \varphi)dt \quad (7)$$

$$Q_{C12} = Q_{C14} = \int_{t_3}^{\frac{T}{2}-t_3=t_{14}} I_{out} Sin(2\pi ft - \varphi)dt = \int_{t_{18}}^{2T-t_{18}=t_{29}} I_{out} Sin(2\pi ft - \varphi)dt \quad (8)$$

where T, I_{out}, f and φ are time period of one cycle, peak magnitude of load current, frequency of the output voltage, and angle between output voltage and load current respectively. Considering kV_{DC} as highest allowable voltage ripple, optimum values of the capacitors can be given by

$$C_{opt,11} = C_{opt,13} \geq \frac{Q_{C_{11}} or\ Q_{C_{13}}}{kV_{DC}} \quad (9)$$

$$C_{opt,12} = C_{opt,14} \geq \frac{Q_{C_{12}} or\ Q_{C_{14}}}{kV_{DC}} \quad (10)$$

The same procedure for selecting switched capacitors can be extended for higher level inverter structure.

8. Power Loss Analysis

The main power losses of SCMLI are switching loss, conduction loss and loss due to capacitor voltage ripple. In this section, the calculation of different losses are discussed for fundamental frequency switching scheme.

8.1. Switching loss calculation

In this sub-section, switching loss of a switch, S_i is calculated. During transition condition of S_i i.e. when S_i changes from OFF state to ON state and ON state to OFF state, the parasitic capacitors associated with S_i is in charging and discharging state conditions respectively. Thus, during these transition conditions, the energy consumed by the parasitic capacitors can be represented as the switching energy loss of S_i. By finding the total number of transitions over a fundamental cycle, the switching power loss of S_i can be evaluated. If C_p is the equivalent parasitic capacitor of S_i, V_{DC} is the input DC supply, f_{ref} is the fundamental frequency and N_{si} is the total number of transitions over the fundamental cycle. Then, the switching loss of S_i can be expressed by

$$P_{swsi} = \frac{1}{2} C_p {V_{DC}}^2 f_{ref} N_{si} \quad (11)$$

For 17 level proposed topology as shown in Fig. 4., the overall switching loss can be evaluated as follows

$$P_{sw} = \sum_{i=1}^{18} \frac{1}{2} C_p {V_{DC}}^2 f_{ref} N_{si} \quad (12)$$

8.2. Conduction loss calculation

Conduction loss of switching device occurs due to ohmic loss in its on state resistance. Let R_{on} be on state resistance of switching device. Further, S_i remains ON during (t_{i+1} -t_i) in a fundamental cycle. Then, conduction loss over the fundamental cycle for S_i can be expressed as follows-

$$P_{S_i} = \frac{1}{T} \int_{t_i}^{t_{i+1}} ({i_{S_i}}^2 R_{on}) dt \quad (13)$$

where i_{Si} is current through S_i during ON condition. The conduction loss of switch S_{11} of proposed 17 level inverter structure can be evaluated as per Table III and Fig. 5 as follows

$$P_{S_{11}} = \frac{1}{T} \left[\int_{t_7}^{t_{10}} ({i_{S_{11}}}^2 R_{on}) dt + \int_{t_{19}}^{t_{28}} ({i_{S_{11}}}^2 R_{on}) dt \right] \quad (14)$$

Similarly, the conduction loss of other switches can be evaluated. The overall conduction loss of the inverter is the summation of that for individual switches.

8.3. Capacitor voltage ripple loss calculation

When the capacitors are connected in parallel for charging, at that time there is some difference between the input voltage and the capacitor voltage, which is accountable for the capacitor voltage ripple loss. For finding capacitor voltage ripple, maximum discharging time duration of capacitor needs to be found out. Maximum discharging time durations of all SCs are shown in Fig.5. Loss due to capacitor voltage ripple can be expressed by following equation

$$P_{rip} = \frac{1}{2} \sum_{j=1}^{k} C_j (\Delta V_j)^2 f_{ref} \quad (15)$$

where ΔV_j is maximum voltage ripple corresponding to SC, C_j.

9. Comparison Study

To exhibit the benefits of proposed inverter structure in contradiction to various recently developed topologies [10-18], an extensive comparison in the reasonable situation and from various viewpoints has been presented in this section. Comparisons are subsumed considering only the symmetrical form of other topologies as the presented topology is symmetrical in nature. Further, all the selected topologies are modular in nature. Table-4 shows the general expressions for relevant parameters of different MLI topologies and the proposed single phase structure, where n indicates the number of modules.

Fig.6 depicts the comparison of various parameters of the proposed single phase structures with other developed topologies. Fig.6 (a) shows the relative variation of number of required switches versus different output voltage levels. As can be clearly observed, for producing a particular voltage level, proposed topologies utilize less switching devices compared to other topologies. Notably, minimum switch count can aid to an appreciable reduction in the overall cost. The variation

of number of drivers required for producing different output voltage levels are given in Fig.6 (b). It is observed that the proposed topologies along with topology presented in [17**]** require the minimum driver circuits for producing a specific output voltage level.

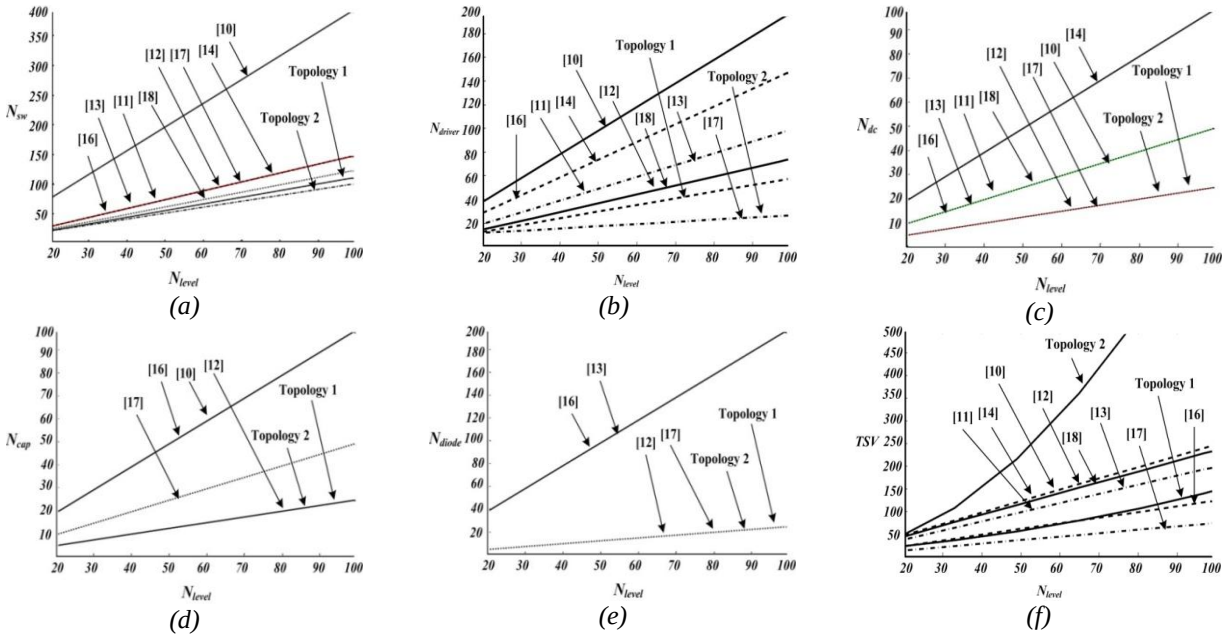
As shown in Fig.6 (c), proposed inverter along with the presented topologies in [12,17] decrease the requirement of isolated DC power supplies consequently making its size smaller as compared to other topologies. Fig.6 (d) gives comparison of capacitors required w.r.t. output voltage levels. According to this figure, proposed topologies and topology presented in [12] require less capacitor in comparison with others to yield higher voltage levels. The proposed topologies alongwith [12, 17] needs less quantity of diodes than topologies presented in [13, 16], which can be observed from Fig.6 (e).

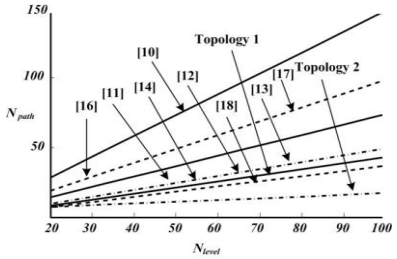
Table 4. General equations of different parameters of proposed topology and other topologies

Topology presented in	N_{level}	N_{sw}	N_{diode}	N_{cap}	N_{dc}	$V_{O\max}$
[10], 2012	$2n+1$	$8n$	–	–	n	nV_{DC}
[14], 2014	$2n+1$	$3n$	–	–	$2n$	$2nV_{DC}$
[15], 2014	$4n+1$	$6n$	n	n	n	$2nV_{DC}$
[12], 2014	$4n+1$	$6n$	n	n	n	$2nV_{DC}$
[11], 2014	$4n+1$	$6n$	$8n$	–	$2n$	$2nV_{DC}$
[13], 2014	$4n+1$	$6n$	–	–	$2n$	$2nV_{DC}$
[16], 2016	$2n+1$	$3n$	$4n$	$2n$	n	nV_{DC}
[17], 2016	$4n+1$	$6n$	n	$2n$	n	$2nV_{DC}$
[18], 2016	$8n+1$	$10n$	–	–	$4n$	$4nV_{DC}$
Proposed Topology 1	$16n+1$	$18n$	$4n$	$4n$	$4n$	$8nV_{DC}$
Proposed Topology 2	$8n+1$	$8n+2$	$2n$	$2n$	$2n$	$4nV_{DC}$

Although, topology presented in [12] require same number of DC supplies, diodes and capacitors as compared to the proposed topologies, but the presence of large number of switches makes it disadvantageous. Some of the aforementioned topologies do not require any diodes or capacitors, but they need large amount of power semiconductor switches and input DC supplies as compared to proposed topologies increasing their cost and complexity.

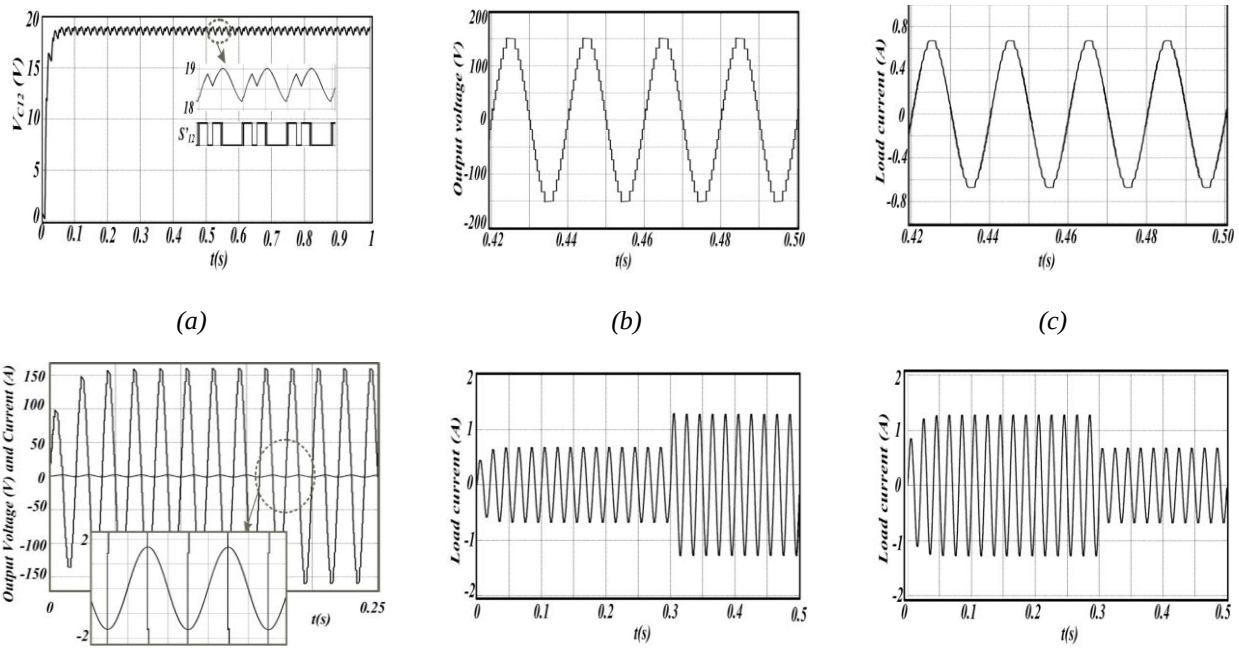
Fig.6 (f) provides the graph of total standing voltage w.r.t. number of output voltage levels for the proposed topologies as well as other recent topologies. It can be observed that first proposed topology has lesser *TSV* as compared to second proposed topology. Number of power switches in the current path for producing highest output voltage level is shown in Fig.6 (g). Second proposed topology requires minimum power semiconductor switches in the conduction path.





(g)

Fig. 6. Comparative study (a) required switches vs. generated voltage levels, (b) required drivers vs. generated voltage levels, (c) required DC supplies vs. generated voltage levels, (d) required capacitors vs. generated voltage levels, (f) required diodes vs. generated voltage levels, (f) total standing voltage of inverter vs. generated voltage levels, (g) Number of switches in conduction path vs. generated voltage levels



(a) *(b)* *(c)*

(d) *(e)* *(f)*

Fig.7. Simulated result for (a) switched capacitor voltage, V_{C12}, (b) output voltage, V_{RO} for *R-L* load condition, (c) output or load current I_O for *R-L* load condition, (d) output voltage and current under *L* load condition, (e) Load current under sudden decrement of load, (f) Load current under sudden increment of load

10. Simulation Study

In order to authenticate the performance of the 17-level proposed inverter structure, simulation study in MATLAB/Simulink platform has been carried out with the following specifications:

Table 5. Specifications

Parameters	Values
Input Supply (V_{DC})	*20V*
Switched capacitors (C_{11}=C_{12}=C_{13}=C_{14})	*5000μF*
R-L Load	*R=224Ω , L=50mH*
L Load	*L=300mH*
Reference Frequency	*50Hz*

Further, the simulation study has been done considering MOSFET switching device with on state resistance (R_{on}) 0.85Ω and diode with forward voltage drop *0.7V*. Fig.7 (a) presents voltage across capacitor C_{12}. It can be observed that the capacitor voltage is around *18.5V* with a ripple of less than *1V*. Other capacitor voltages obtained are also of same value. Fig.7 (b) and (c) show the output voltage and the corresponding output current with *R-L* load. It can be seen that a voltage waveform of 17-level with a maximum magnitude of *+150V* and minimum magnitude of -150V is obtained. Similarly, near sinusoidal current waveform with peak current magnitude 0.69A is obtained. The simulated output voltage and current under inductive load condition is shown in Fig.7 (d). It can be observed that the load current is 90^o lagging with respect to output voltage. The output current for sudden decrement and increment load conditions are shown in Fig.7 (e) and (f) respectively.

11. Experimental Study

For experimental verification of the proposed MLI topology, a 17-level output voltage structure has been

practically implemented and several waveforms are investigated under different load conditions. The hardware set-up and experimental specification are shown in Fig.8 and Table-6 respectively. Input to each *BU* is same and is equal to near about *19.5V*. Fig.9 (a) and (b) show the output voltage and current for *R-L* and *L* load conditions respectively. The output voltage has 17 levels with a maximum value of *150 V* and the output current is sinusoidal in nature with peak value of *0.7A* for *R-L* load condition. Similarly, for L load condition, the current is 90^{o} lagging w.r.t. output voltage and peak output voltage and current are *151 V* and *1.4 A* respectively. It can be observed that the experimental output voltage and current are well obeyed the simulation results. The different switched capacitor voltages are shown in Fig.9 (c). It is observed that with the proposed switching scheme, the capacitors are easily charged and discharged. In addition, capacitors voltages are near about V_{DC} and steady. Output voltages of BU_{11}, BU_{12}, BU_{13} and BU_{14} are shown in Fig.9 (d). It can be observed that output of all the BUs have two voltage levels. The magnitudes of voltage level for output of BUs are indicated in Fig.9 (d). The stress voltage for S_{1c} and BD_{11} are shown in Fig.9 (e) and (f) respectively. The effect of sudden load change on output current and capacitor voltage (V_{C13}) are shown in Fig.9 (g) and (h). It can be accessed from Fig.9 (g) that when there is sudden decrease in load, capacitor voltage decreases immediately. The capacitor voltage changes from *18 V* to *15 V*. Further, reduction in load leads to immediate rise in the output current. Output current varies from *0.7 A* to *1 A*. Similarly, with the sudden increment of load, the capacitor voltage increases and the load current decreases as shown in Fig.9 (h).

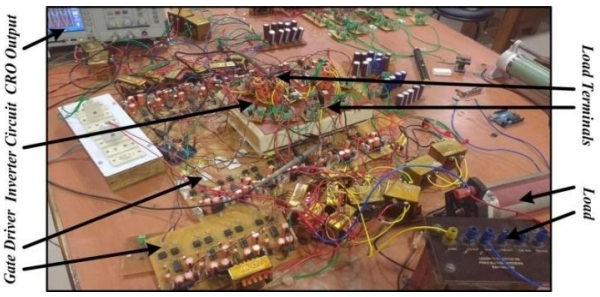
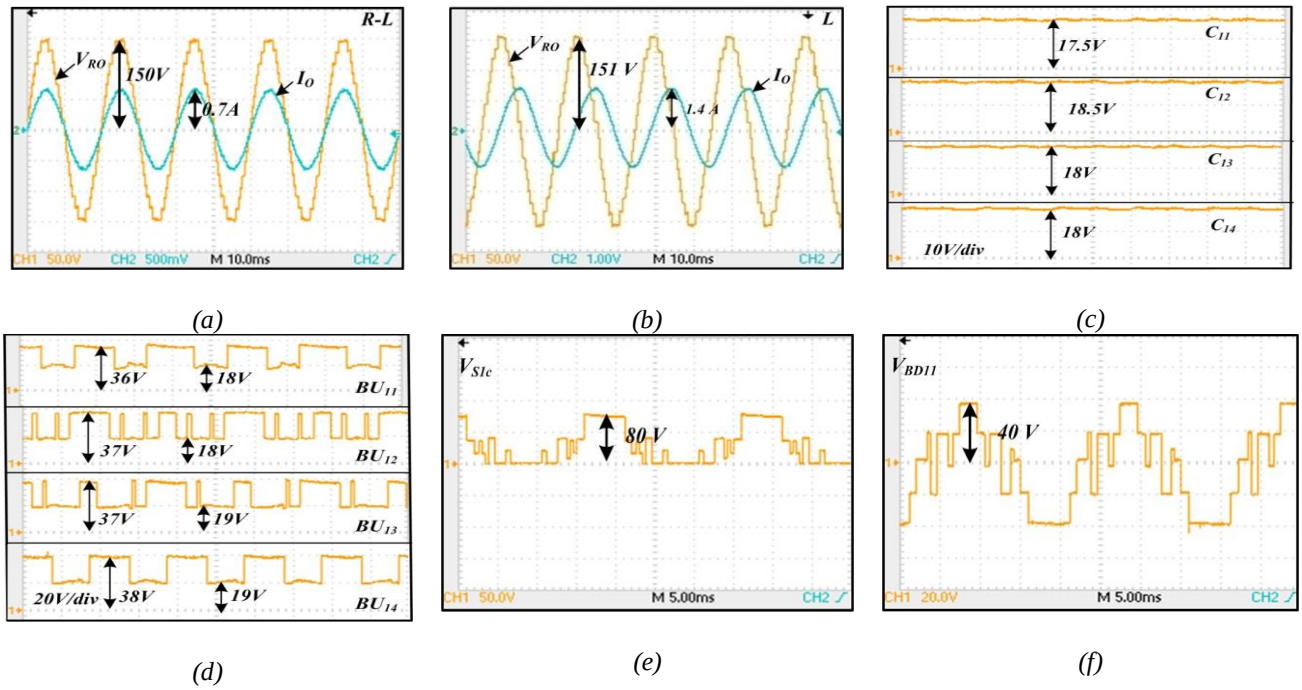


Fig. 8. Experimental Set-up

Table 6. Experimental set-up specifications

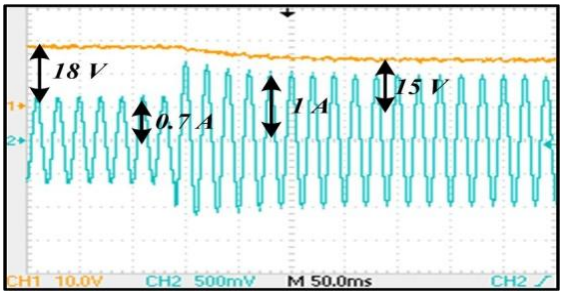
Components and parameters	Values
MOSFET	*IRF840*
Driver IC	*IR2110*
Microcontroller	*Atmega328*
Input voltage (V_{DC})	*19.5V*
Switched capacitors	*5000μF, 50V*
R-L Load	*R=223ohm, L=50mH*

FFT analysis of output voltage and current for *R-L* load condition are shown in Fig.10 (a) and (b) respectively. From Fig.10 (a), the peak fundamental and THD of output voltage are *147V* and *5.66%* respectively. Similarly, peak fundamental and THD of output current are *0.6374A* and *3.7%* respectively. The maximum total standing voltage of the inverter is *735V*. The output power of the inverter is around 48Watt. The power loss in the inverter is *2.04W*. The efficiency of the proposed inverter is *95.9%*.

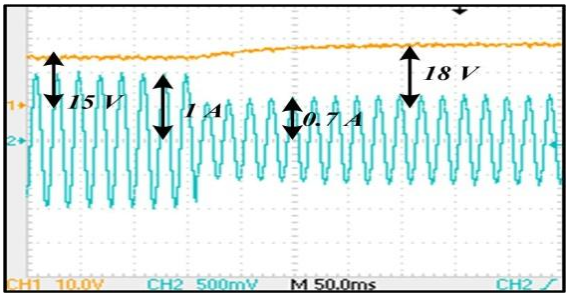


(a) *(b)* *(c)*

(d) *(e)* *(f)*

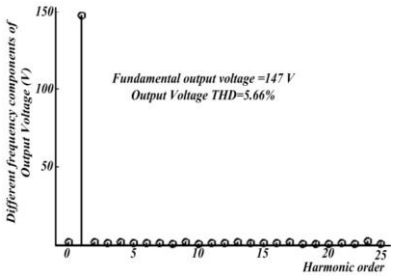


(g)

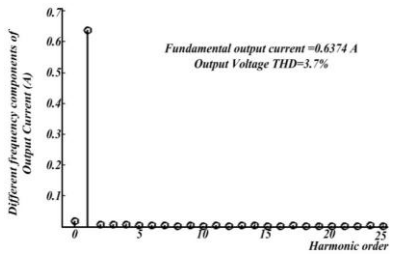


(h)

Fig. 9. Experimental results for (a) capacitor voltages, (b) load voltage and current under *R-L* load condition, (c) load voltage and current under *L* load condition, (d) output voltages of different BUs, (e) stess voltage for switch, S_{1C}, (f) stress voltage for BD_{11}, (g) capacitor voltage (V_{C13}) and load current under sudden decreament load condition, (h) capacitor voltage (V_{C13}) and load current under under increment load condition.



(a)



(b)

Fig. 10. FFT analysis of (a) output voltage and (b) current on experimental data

12. Conclusion

This paper presented a new cascaded MLI structure based on SC basic unit. It can produce higher output voltage levels with reasonable count of components. Less components results in small size, simple control and reduced cost of the proposed inverter compared to other topologies. Further, absence of complicated capacitor voltage balancing methods makes the proposed circuit very simple. Fundamental frequency switching technique is used for the generation of switching signals. Various losses have been calculated for the proposed inverter. Efficiency of the proposed inverter is about *95.9 %*. Furthermore, to have a fair judgement about the salient features of the proposed inverter structure, a comparative analysis has been provided in detail. The presented topology is modular in nature such that damage of any modules, the topology can supply the load with reduced number of voltage levels. In addition, by employing simple switching strategy, the capacitor voltage balancing can be achieved. The operating principle and the expressions for different parameters of the inverter are presented in detail. General equations for different parameters of proposed topologies have been evaluated and compared with other topologies. Simulation study of the proposed inverter has been performed on a 17 level output voltage MLI structure to prove its feasibility and effectiveness. Moreover, the inverter is practically implemented and different waveforms are verified at *R-L* load L load and sudden load change conditions.

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