POWER LOSS MINIMIZATION IN RADIAL DISTRIBUTION NETWORK CONSIDERING DIFFERENT LOAD LEVELS VIA AGPSO PART–II: USING CAPACITORS AFTER DGs & RECONFIGURATION

G.SRINIVASAN[1*] **S. VISALAKSHI[2]**

[1]Associate Professor, Department of Electrical & Electronics Engineering., Tagore Engineering College, Rathinamangalam, CHENNAI-600 127, INDIA. E-mail: powersystemsengineer@yahoo.in (***Corresponding Author**)

[2]Professor & Head, Dept. of Electronics & Instrumentation Engineering, Valliammai Engineering College, Kattankulathur – 603203, Kancheepuram (Dist.), TAMILNADU, INDIA , Email:svisalakshivenkat@gmail.com

Abstract: *Reactive power injection at the optimal nodes in the Radial Distribution Network (RDN) reduces the power loss which is one of the traditional methods. In the past decade, real power injection (DG) based power loss reduction with NR has been yield more power loss reduction than individual application of DG and NR. Reactive power injection along the DN after real power compensation (after DG allocation with NR) will achieve further power loss reduction. This paper proposes an application of Autonomous Group Particle Swarm Optimization (AGPSO) to solve the optimal capacitor problem in reconfigured DG integrated RDN with an objective to minimize power loss subject to satisfying operating constraints. Further, this paper considers optimal allocation and sizing of capacitors at three and four optimal locations under three different load levels (50%, 100% and 160%) to investigate the performance of the proposed method in gaining additional power loss reduction after optimal allocation of DGs with NR. This developed technique is demonstrated using two test systems (standard IEEE 33 and 69 bus). In the proposed method, considerable volume of additional power loss reduction is achieved and the bus voltage is enriched through the concurrent operation of capacitors in reconfigured DG compensated RDN.*

Key words: *Optimal capacitor allocation, Additional power loss minimization, Radial Distribution Network, AGPSO, Bus voltage profile.*

1. Introduction

Unlike transmission network, the DN has high R/X ratio and also due to the steep growth in power demand, the power loss (I^2R) increases resulting increased energy cost, reduction in the bus voltage profile. As the distance between the buses and substation increases, there is a decrease in bus voltage. The reactive power accounts for a portion of these losses. On the other hand high reactive power flows in a network, results in increased power losses. The reactive power loss will be still more and significant when the network is heavily loaded.

Reactive power support to the RDN can be possible using capacitors. By incorporating capacitors at optimal locations along the RDN, certain amount of reactive powers can be compensated which in turn reflect in power loss reduction due to reactive power flow in the entire RDN **[1]**. Moreover the benefits such as increase in MVA flow, reactive current reduction, improvement in system stability, bus voltage profile and power factor, reduced loading of thermally limited apparatus, decreased payment for the energy, power quality improvement and release congestion in RDN **[2,3]** can be gained if capacitors are optimally allocated with proper sizing along the RDN so that maximum profits can be gained, subject to satisfying all the constraints. Hence necessity investigation has to be done for improvement of RDN efficacy. If capacitors are not optimally placed, the problems such as increase in active power loss, poor power factor and over voltage issues etc. may occur in the RDN and even it cause danger to the whole distribution network operation and control **[4,5,6]**

Optimal placement of capacitors in the DN is a well-known technique has been followed since the last four decades **[2,3,6,7,8,9,10].** These methods were solved using mathematical based non-linear programming methods which may provide only local optimum solution **[11]**. Soft computing technique based search for a global optimal solution have been tried for the past two decades. These methods have capable of finding optimal results with little process efforts; handling complex and challenging task and are generally simple in execution. Among these techniques, Genetic algorithm **[12,13],** Simulated annealing **[3]** and Tabu search **[6]** have been extensively applied past. However these three methods have certain drawbacks **[14].** Recently, optimal placement and sizing of capacitors using optimization techniques such as Plant growth simulation algorithm [**15**], Bacterial foraging algorithm **[16],** Bat Algorithm **[17],** Particle Swarm Optimization **[18],** Harmony Search Algorithm **[19],** Modified ABC algorithm **[20],**

TLBO **[11**], FPOA **[21],** GSO **[22],** G S A **[23]** Clustering based optimization **[24]** and Multi-objective Artificial Bee colony Algorithm **[25]** have been presented.

Optimal placement of capacitors is modelled as a complicated combinatorial, constrained optimisation problem. In determining optimal capacitor placement and sizing, loss minimization and bus voltage improvement etc. in RDN, meta-heuristic optimization techniques were found to be successful. Recent research on OCAP using meta-heuristics indicates the great acceptance of these methods **[26]**. The major drawbacks such as suffering from local optimality, requiring large time for simulation, premature or slow convergence etc. have been found in some of the optimization techniques **[27,28]**. Therefore, there is an urge to introduce a new, simple, effective, fast and efficient population based optimization algorithm to solve optimal allocation and sizing of capacitors in reconfigured DG integrated DN to overcome the above demerits which are crucial. In this study, a new meta-heuristic optimization algorithm of best, durable and proficient algorithm which is a modification of PSO called AGPSO is proposed utilizing the concept of autonomous groups inspired by the diversity of individuals in natural colonies, is selected to solve the objective function. AGPSO **[29]** is powerful in solving wide range of optimization problems that is used in this paper to solve the power loss minimization problem by optimal allocation and capacity determination of capacitors in reconfigured and DG compensated DN. Since the main drawbacks of PSO have been eliminated in AGPSO, finding a global or near-global optimum solution can be achieved

In view of this, the present study is an extension of PART-I, in which AGPSO is employed to determine the optimal allocation and sizing of capacitors considering three and four nodes, to achieve additional power loss reduction under three different load levels in the reconfigured DN with DG; it has been suggested as the next stage of power loss reduction. The bus voltage profile is improved and the distribution network power loss reduction is also improved in addition to PART-I by the proposed method. The method has been tested and demonstrated on standard IEEE 33 and 69 bus test system.

2. Objective Function

The objective function is to achieve additional power loss reduction by optimal allocation and sizing of capacitors in the DG compensated reconfigured RDN while satisfying both system equality and inequality constraints.

$$\textbf{Minimize} \quad \text{Fit} = \left[\frac{\text{TP LOSS (ACI)}}{\text{TP LOSS (BCI)}} \right] \tag{1}$$

Subject to Equality Constraints

$$Q_{MS} - \sum Q_D + \sum_{t=1}^{NC} Q_{C(t)} - TQ_{LOSS} = 0 \tag{2}$$

Inequality Constraints

$$V_{(t)}^{min} \le V_{(t)} \le V_{(t)}^{max} \tag{3}$$

$$\sum_{t=1}^{NC} Q_{C(t)} \le \sum Q_D \tag{4}$$

$$Q_{C(t)}^{min} \le Q_{C(t)} \le Q_{C(t)}^{max} \tag{5}$$

Recursive function and a linked-list data structure designed power flow **[30]** and the same optimization algorithm **[29]** which is used in PART-I is also considered in this work for optimal capacitor problem.

3. Implementation of AGPSO

This section explains the application of AGPSO in optimal allocation and sizing of capacitors in the DG integrated reconfigured RDN to achieve additional real power loss minimization. The steps for the AGPSO algorithm for optimal capacitor placements and sizing are given below:

Step 1: Initialize the particles $\boldsymbol{x}_{iG}$ of PSO randomly within the boundary limits according to **Table 1**. The proposed particles consist of position of tie-switches, optimal DG node, size and optimal capacitor node and size. The symbol for the position of sectionalizing switches is *SW.* Optimal node for DG placement is represented as B_{DG} and its corresponding DG size is represented as S_{DG}. Optimal node for capacitor placement and its corresponding size are represented as B_{Cap} and S_{Cap}. The proposed particles are given as

$$X_{(iG)} = \begin{bmatrix} DG \text{ bus limits} & \text{DG sizing limits} & \text{Tie-switch status} \\ (1,3,5,7) & (2,4,6,8) & (9 \text{ to } 13) \\ \text{Status of opening of sectionalizing switches (14 to 18)} & & \\ B_{Cap,1}, S_{Cap,1}, & B_{Cap,2}, S_{Cap,2} B_{Cap,3}, S_{Cap,3}, & B_{Cap,4}, S_{Cap,4} \end{bmatrix}^{T}_{(26\times1)}$$

$$i=1, 2\ldots G \tag{6}$$

The variable ‘G’ indicates the population size from a set of random distributions. Thus, the number of variables for the simultaneous analysis is equal to twenty six. The values obtained under cases III to VI (discussed in ‘PART-I) occupies first eighteen positions. Two each for optimal node for capacitor allocation and sizing occupies remaining eight (scenario 2). Only the particles that satisfy all the constraints will be considered as the initial population. Table 1 indicates the minimum and maximum values of

capacitors under three load levels.

Step 2 to Step 5: Same as discussed in 'PART-I'

Table 1 Typical value of Agents (Cases VII to X)

Variables	Solution Vectors (SV)
$X^{(14)}$ $X^{(16)}$ $X^{(18)}$	Node No.3 to 33 / 3 to 69 (Nodes 1 to 3) – **Scenario 1**
$X^{(15)}$ $X^{(17)}$ $X^{(19)}$	0.15 MVAr - 0.90 MVAr - 50% load 0.15 MVAr - 1.65 MVAr - 100% load 0.15 MVAr - 2.1 MVAr - 160% load (in discrete steps of 0.15 MVAr)
$X^{(14)}$ $X^{(16)}$ $X^{(18)}$ $X^{(20)}$	Node No.3 to 33 / 3 to 69 (Nodes 1 to 4) – **Scenario 2**
$X^{(15)}$ $X^{(17)}$ $X^{(19)}$ $X^{(21)}$	0.15 MVAr - 0.90 MVAr - 50% load 0.15 MVAr - 1.65 MVAr - 100% load 0.15 MVAr - 2.1 MVAr - 160% load (in discrete steps of 0.15 MVAr)

4. Simulation results and Discussion

To validate the application of the proposed method in achieving additional power loss minimization and improvement in node voltage, the same two test systems discussed in 'PART-I' have been considered for analysing the effectiveness of AGPSO. To get optimal network, optimal node of DG units and the status of tie-switches and position of sectionalizing switches have to be known. The minimum and maximum voltages are set as 0.95 p.u. and 1.05 p.u.

To minimize the real power loss and improvement in node voltages, were discussed in 'PART-I under six different cases for each test case to examine the effectiveness of the proposed method under three different load levels (Cases I to VI - 50%, 100% and 160%). Maximum reactive power injection has been assumed to be less than or equal to the total reactive power demand of the system plus reactive power loss in this proposal.

Case I to Case VI: Refer **'PART-I'** (DG units with NR)**.**

Case VII: The condition is similar to case III; nevertheless capacitors are allocated at the appropriate locations (three and four nodes – Scenarios 1 & 2) to evaluate the additional power loss reduction on the test system.

Case VIII: The condition is similar to case IV, but capacitors are placed at the optimal locations (three nodes and four nodes – Scenarios 1&2) to appraise the impact of capacitors on power loss reduction.

Case IX: The conditions are similar to case V, but to estimate further power loss reduction; capacitors are added at the optimal places (three nodes and four nodes – Scenarios 1 to 2) in the RDN.

Case X: The conditions are similar to case VI; yet, capacitors are allocated at the optimal positions (Three nodes and four nodes – Scenarios 1 & 2) to assess the extra power loss reduction on the test system considered.

4.1 33 Bus test system - Discussion

Tables from 2 to 4 display the location of capacitors to be installed at three / four optimal locations under three different load levels (Light, Medium and Heavy) considering cases VII to X. From Tables 2 to 4, it is seen that an additional power loss reduction after optimal placement of capacitors at three nodes considering cases VII to X is between 13% to 14.6% (Light), 14% to 15.4% (Medium) and 13.8% to 15.3% (Heavy). But optimal placement of capacitors at four nodes is yielded an additional power loss reduction of 13.7% to 14.8% (Light), 15% to 16.5% (Medium) and 14.3% to 16.6% (Heavy). The maximum total power loss reduction after optimal placement of capacitors at three nodes in reconfigured RDN with high penetrated DG units is found to be 96.9262% (Light), 96.5925% (Medium) and 97.7345% (Heavy). However the power loss reduction difference between capacitors at three and four nodes is below 1% only. From Table 2 to 4, it is also understood that, at all load levels, the minimum bus voltage is enhanced remarkably comparing cases III, IV, V and VI with cases VII, VIII, IX and X. Maximum bus Voltage improvement difference of 0.00752 p.u. (capacitors at three nodes) and 0.00894 p.u (capacitors at four nodes) for light load, 0.01442 p.u (capacitors at three nodes) and 0.01741 p.u. (capacitors at four nodes) for medium load and 0.02786 p.u (capacitors at three nodes) and 0.02954 p.u. (capacitors at four nodes) for heavy load is observed by comparing cases III, IV, V and VI with cases VII, VIII, IX and X. The difference between the cases VII to X in power loss minimization and improvement in bus voltage is insignificant.

From the above discussion, it is witnessed that for all the load levels (i) Total maximum real power loss reduction seems to be under case X (ii) The maximum bus voltage observed is above 1 p.u. and (iii) The bus voltage is increasing from case VII to X. Figures 1, 2 and 3 show the bus voltages at 50%, 100% and 160% load respectively under cases VII to X for three and four capacitors.

Table 2 Test Results obtained by the proposed method – 33 Bus system – 50% Load

Case	Capacitor Node & Size (KVAr)	P_{Loss} (KW)	Q_{Loss} (KVAr)	$V_{min.}$ (p.u)	$V_{max.}$ (p.u)	Branch $P_{Loss\ (max)}$ (KW) / (Branch)	Total P_{Loss} reduction	*Additional % P_{Loss} reduction
SCENARIO 1 – Optimal Placement of three Capacitors								
VII	6 (150) 8 (300) 30 (450)	**2.6185**	3.1918	0.99431 (10)	1.0019 (7)	0.63955 KW / (19–20)	**94.633%**	**14.5895**
VIII	30 (450) 8 (300) 6 (150)	**2.2405**	3.04	0.99508 (18)	1.0017 (7)	0.40895 KW / (15 – 14)	**95.408%**	**14.592**
IX	29 (450) 6 (150) 8 (300)	**1.7695**	3.6657	0.99591 (14)	1.0022 (8)	0.37296 KW / (8 – 9)	**96.373%**	**13.7643**
X	15 (300) 24 (150) 30 (300)	**1.4997**	3.1944	0.99717 (13)	1.0023 (15)	0.20107 KW / (24 – 25)	**96.9262%**	**13.1748**
SCENARIO 2 – Optimal Placement of four Capacitors								
VII	15 (150) 8 (150) 6 (150) 30 (450)	**2.5429**	3.0321	0.99638 (10)	1.0019 (7)	0.63928 KW / (19–20)	**94.7881%**	**14.7446**
VIII	30 (450) 8 (150) 6 (150) 15 (150)	**2.1437**	2.863	0.99713 (11)	1.0017 (7)	0.40686 KW / (14–15)	**95.6063%**	**14.7903**
IX	25 (450) 6 (150) 8 (150) 12 (150)	**1.7251**	3.4883	0.99788 (33)	1.0003 (8)	0.37435 KW / (8 – 9)	**96.4642%**	**13.8555**
X	30 (300) 24 (150) 6 (150) 15 (300)	**1.2217**	3.0409	0.99822 (13)	1.0023 (15)	0.20096 KW / (24–25)	**97.496%**	**13.7446**

Table 3 Test Results obtained by the proposed method – 33 Bus system – 100% Load

Case	Capacitor Node & Size (KVAr)	P_{Loss} (KW)	Q_{Loss} (KVAr)	V_{min} (p.u)	V_{max} (p.u)	Branch $P_{Loss\ (max)}$ (KW) / (Branch)	Total P_{Loss} reduction	*Additional % P_{Loss} reduction
SCENARIO 1 – Optimal Placement of three Capacitors								
VII	8 (450) 32 (300) 30 (1050)	**12.646**	17.769	0.98735 (13)	1.0069 (31)	3.2896 KW / (24 – 25)	**94%**	**14.525**
VIII	24 (450) 8 (600) 30 (900)	**8.1393**	10.795	0.98925 (18)	1.0007 (9)	1.32 KW / (24 – 25)	**96.1426%**	**16.09**
IX	24 (300) 8 (600) 30 (900)	**7.6341**	12.534	0.99067 (14)	1.0004 (9)	1.0544 KW / (29 – 30)	**96.382%**	**15.793**
X	6 (300) 30 (900) 8 (600)	**7.19**	16.587	0.99184 (14)	1.0045 (8)	1.1292 KW / (8 – 9)	**96.5925%**	**15.3665**
SCENARIO 2 – Optimal Placement of four Capacitors								
VII	8 (450) 30 (900) 6 (450) 32 (300)	**11.134**	16.666	0.99129 (25)	1.007 (31)	3.1174 KW / (24 – 25)	**94.7233%**	**15.2483**
VIII	30 (900) 8 (600) 6 (300) 24 (300)	**7.3457**	10.296	0.99244 (18)	1.0007 (9)	1.9799 KW / (14 – 15)	**96.5187%**	**16.4657**
IX	30 (900) 8 (600) 6 (300) 24 (300)	**6.7585**	12.038	0.99353 (14)	1.0005 (9)	1.0532 KW / (29 – 30)	**96.797%**	**16.208**
X	8 (450) 6 (300) 30 (1200) 18 (150)	**6.5094**	15.973	0.99411 (14)	1.0045 (8)	1.1059 KW / (21 – 22)	**96.915%**	**15.689**

Table 4 Test Results obtained by the proposed method – 33 Bus system – 160% Load

Case	Capacitor Node & Size (KVAr)	P_{Loss} (KW)	Q_{Loss} (KVAr)	V_{min} (p.u)	$V_{max.}$ (p.u)	Branch $P_{Loss\ (max)}$ (KW) / (Branch)	Total P_{Loss} reduction	*Additional % P_{Loss} reduction
SCENARIO 1 – Optimal Placement of three Capacitors								
VII	30 (1950) 15 (750) 6 (450)	**28.535**	32.895	0.98033 (10)	1.0042 (26)	7.8947 / (19 – 20)	**95.272%**	**15.177**
VIII	15 (750) 30 (1950) 6 (450)	**21.903**	27.052	0.98421 (11)	1.0088 (8)	4.5416 / (15 – 14)	**96.37%**	**15.26**
IX	8 (1050) 6 (450) 30 (1650)	**16.834**	38.204	0.98769 (14)	1.0014 (21)	3.8324 / (8 – 9)	**97.211%**	**15.111**
X	8 (750) 30 (1650) 32 (600)	**13.672**	24.728	0.99081 (13)	1.0052 (7)	2.4591 / (24 – 25)	**97.7345%**	**13.8845**
SCENARIO 2 – Optimal Placement of Four Capacitors								
VII	30 (1650) 15 (750) 6 (450) 24 (600)	**26.965**	31.39	0.98242 (10)	1.003 (26)	7.8932 / (19 – 20)	**95.532%**	**15.437**
VIII	6 (450) 30 (1350) 15 (750) 24 (600)	**20.325**	25.471	0.98627 (11)	1.0052 (8)	4.5411 / (15 – 14)	**96.632%**	**15.522**
IX	6 (450) 30 (1350) 8 (900) 24 (600)	**15.117**	34.892	0.99088 (15)	1.0005 (26)	3.8609 / (8 – 9)	**97.495%**	**15.375**
X	33 (450) 21 (600) 30 (1500) 6 (450)	**10.915**	21.229	0.99249 (14)	1.0065 (8)	2.1662 / (24 – 25)	**98.19%**	**14.34**

Table 5 Test Results obtained by the proposed method – 69 Bus system – 50% Load

Case	Capacitor Node & Size (KVAr)	P_{Loss} (KW)	Q_{Loss} (KVAr)	V_{min} (p.u)	$V_{max.}$ (p.u)	Branch $P_{Loss\ (max)}$ (KW) / (Branch)	Total P_{Loss} reduction	*Additional P_{Loss} reduction
SCENARIO 1 – Optimal Placement of three Capacitors								
VII	64 (150) 12 (150) 61 (600)	**2.3995**	1.8605	0.99275 (64)	1.0019 (61)	0.30318 / (50 – 59)	**95.3493%**	**10.34%**
VIII	66 (150) 11 (300) 61 (450)	**1.9884**	1.5313	0.99386 (65)	1.0013 (66)	0.47706 / (9 – 10)	**96.146%**	**9.384%**
IX	64 (150) 12 (150) 61 (600)	**1.4069**	1.4671	0.99495 (50)	1.0017 (64)	0.26891 / (48 – 49)	**97.273%**	**10.21%**
X	64 (150) 12 (150) 61 (600)	**1.1805**	0.89388	0.99584 (64)	1.000 (1)	0.14318 / (27 – 65)	**97.712%**	**10.313%**
SCENARIO 2 – Optimal Placement of four Capacitors								
VII	64 (150) 12 (150) 49 (300) 61 (600)	**2.2198**	1.4246	0.99476 (64)	1.0034 (66)	0.30213 / (50 – 59)	**95.698%**	**10.688%**
VIII	66 (150) 11 (150) 49 (150) 61 (450)	**1.6559**	1.36413	0.99657 (65)	1.0006 (61)	0.18172 / (50 – 59)	**96.7906%**	**10.0286%**
IX	49 (300) 61 (600) 12 (150) 64 (150)	**1.2048**	1.1741	0.99724 (16)	1.0002 (61)	0.19594 / (48 – 49)	**97.665%**	**10.6%**
X	64 (150) 12 (150) 49 (300) 61 (600)	**0.98715**	0.58123	0.99785 (64)	1.0003 (61)	0.14317 / (27 – 65)	**98.087%**	**10.688%**

Table 6 Test Results obtained by the proposed method – 69 Bus systems – 100% Load

Case	Capacitor Node & Size (KVAr)	P_{Loss} (KW)	Q_{Loss} (KVAr)	V_{min} (p.u)	$V_{max.}$ (p.u)	Branch $P_{Loss\ (max)}$ (KW) / (Branch)	Total P_{Loss} reduction	*Additional P_{Loss} reduction
SCENARIO 1 – Optimal Placement of three Capacitors								
VII	66 (450) 11 (450) 61 (900)	**6.9492**	7.1407	0.99109 (65)	1.0054 (67)	0.99578 / (48 – 49)	**96.911%**	**11.914%**
VIII	64 (300) 11 (450) 61 (900)	**6.2757**	4.5871	0.9918 (64)	1.0005 (17)	0.57719 / (27 – 65)	**97.21%**	**11.354%**
IX	64 (300) 11 (450) 61 (900)	**5.4587**	7.1002	0.99201 (21)	1.000 (1)	1.3247 / (48 – 49)	**97.5733%**	**11.31%**
X	64 (300) 11 (450) 61 (900)	**4.129**	4.2881	0.99294 (21)	1.0002 (11)	0.56016 / (40 – 41)	**98.1645%**	**11.271%**
SCENARIO 2 – Optimal Placement of four Capacitors								
VII	66 (300) 11 (450) 49 (600) 61 (900)	**4.8307**	2.901	0.99461 (65)	1.0034 (67)	0.85545 / (11 – 12)	**97.8525%**	**12.8555%**
VIII	64 (300) 11 (300) 50 (600) 61 (1050)	**4.5263**	2.8738	0.99495 (64)	1.0006 (61)	0.47721 / (27 – 65)	**97.988%**	**12.1316%**
IX	49 (600) 61 (1050) 11(450) 64 (300)	**4.2379**	4.9795	0.99548 (21)	1.0002 (61)	0.7475754 / (48 – 49)	**98.116%**	**11.85%**
X	64 (300) 11 (450) 49 (600) 61 (1050)	**3.4182**	2.6832	0.99604 (21)	1.0003 (61)	0.55764 / (40 – 41)	**98.48%**	**11.586%**

Table 7 Test Results obtained by the proposed method – 69 Bus systems – 160% Load

Case	Capacitor Node & Size (KVAr)	P_{Loss} (KW)	Q_{Loss} (KVAr)	V_{min} (p.u)	$V_{max.}$ (p.u)	Branch $P_{Loss\ (max)}$ (KW) / (Branch)	Total P_{Loss} reduction	*Additional P_{Loss} reduction
SCENARIO 1 – Optimal Placement of three Capacitors								
VII	64 (450) 11 (750) 61 (1500)	**10.929**	16.422	0.99122 (50)	1.0026 (11)	3.7697 / (48 – 49)	**98.3248%**	**11.63%**
VIII	65 (600) 11 (600) 61 (1500)	**10.708**	14.53	0.99158 (50)	1.0024 (64)	3.2788 / (48 – 49)	**98.359%**	**10.9135%**
IX	65 (600) 11 (600) 61 (1500)	**10.486**	15.344	0.9918 (50)	1.000 (1)	3.4971 / (48 – 49)	**98.393%**	**10.842%**
X	65 (600) 11 (600) 61 (1500)	**10.226**	10.105	0.99274 (18)	1.000 (1)	1.482 / (65 – 64)	**98.4325%**	**10.81%**
SCENARIO 2 – Optimal Placement of four Capacitors								
VII	27 (600) 11 (750) 49 (750) 61 (1500)	**8.8811**	11.385	0.99463 (50)	1.0009 (11)	2.4333 / (48 – 49)	**98.639%**	**11.943%**
VIII	65 (600) 11 (600) 50 (900) 61 (1650)	**8.7584**	9.9264	0.99494 (68,69)	1.0024 (64)	1.9254 / (48 – 49)	**98.6575%**	**11.212%**
IX	65 (600) 11 (600) 50 (900) 61(1350)	**8.6377**	11.106	0.99523 (16)	1.000 (1)	2.2637 / (48 – 49)	**98.676%**	**11.125%**
X	65 (600) 11 (600) 49 (900) 61 (1650)	**8.4166**	5.9549	0.99575 (18)	1.0012 (61)	1.4819 / (65 – 64)	**98.71%**	**11.087%**

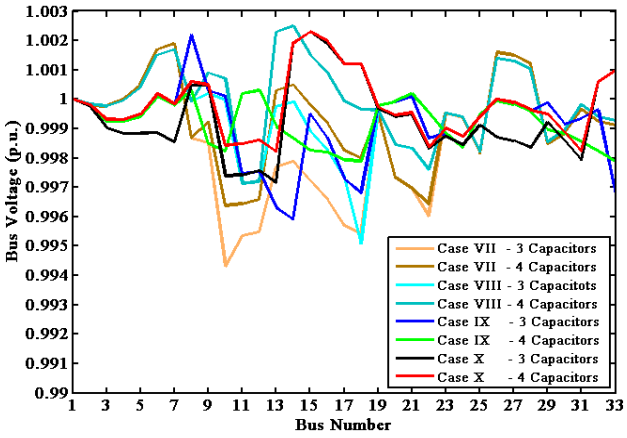

Figure 1 - Bus voltage– 50% Load – 33 Bus

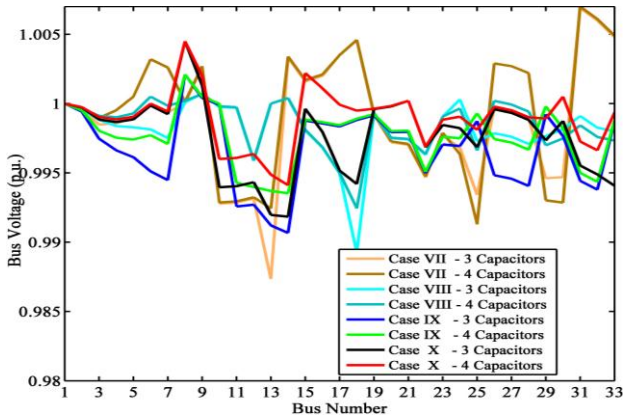

Figure 2 - Bus voltage– 100% Load – 33 Bus

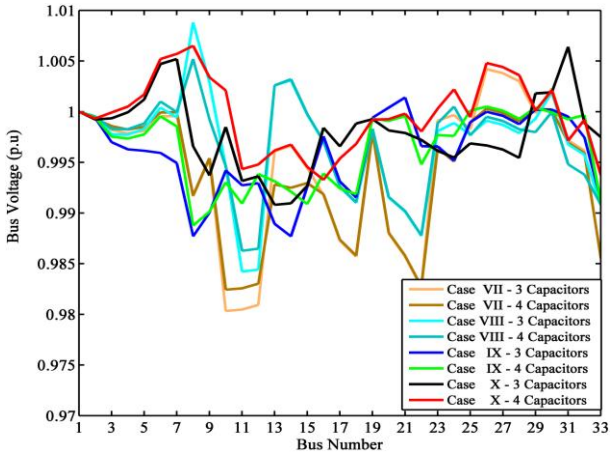

Figure 3 - Bus voltages – 160% Load – 33 Bus

4.2 69 Bus test system - Discussion

From Table 5, it is apparent that, at light load condition an additional power loss reduction of 9.38% to 10.4% (capacitors at three nodes) and 10% to 10.7% (capacitors at four nodes) using cases VII to X compared to cases III to VI (PART-I). Total real power loss reduction after allocation of capacitors at three optimal nodes in DG compensated reconfigured RDN yields, 95.3%, to 97.3% (capacitor at three nodes) and 95.7% to 98.1% (capacitors at four nodes) respectively for cases VII to X compared to B.C. The bus voltages after optimal capacitor placement has improved by 0.003 to 0.005 p.u for three capacitors and 0.005 to 0.0075 p.u for four capacitors considering cases VII to X. Similarly from Table 6, (medium load) it is understood that an additional power loss reduction of 11.2% to 12% (3 capacitors) and 11.5% to 12.9% (4 capacitors) considering cases VII to X is observed. But total power loss reduction after optimal allocation of three and four capacitors in reconfigured DG placed RDN is found to be 96.9% to 98.1% (capacitors at 3 nodes) and 97.8% to 98.5% (capacitors at four nodes). The bus voltage enhancement difference between before and after capacitor placement considering cases VII to X has been found to be 0.008 to 0.01 p.u (capacitors at 3 nodes) and 0.011 to 0.0135 p.u (capacitors at four nodes) Finally from Table 7 considering heavy load, the extra power loss reduction gained by placement of capacitors at three optimal locations is 10.8% to 11.63% (capacitors at three nodes) and 11% to 12% (capacitors at four nodes) compared to cases III to VI (PART-I). Thus the total real power loss reduction achieved varies between 98.3% and 98.4% (capacitors at three nodes) and 98.6% to 98.7% (capacitors at four nodes) compared to B.C. The improvement in bus voltage after optimal allocation of capacitors at three / four nodes in DG allocated reconfigured RDN is found to be between 0.019 to 0.02 p.u (capacitors at three nodes) and 0.022 to 0.0235 p.u (capacitors at four nodes).

It has been substantiated from the above that for all the load levels similar to previous test system this test system is also proved to contribute maximum real power loss reduction under case X. The maximum bus voltage observed is above 1 p.u. and the bus voltage is increasing from case VII to X. Figures 4, 5 and 6 shows the bus voltages at 50%, 100% and 160% load respectively under cases VII to X for three and four capacitors.

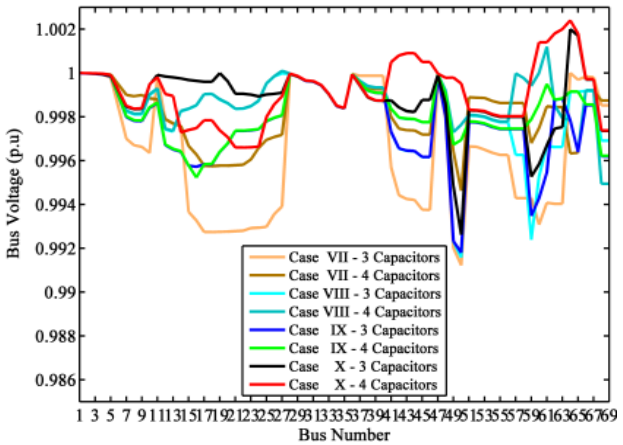

Figure 4- Bus voltages – 50% Load – 69 Bus.

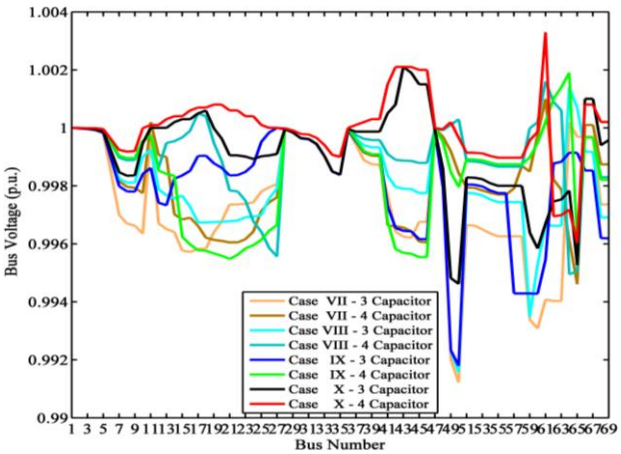

Figure 5 - Bus voltage – 100% Load – 69 Bus

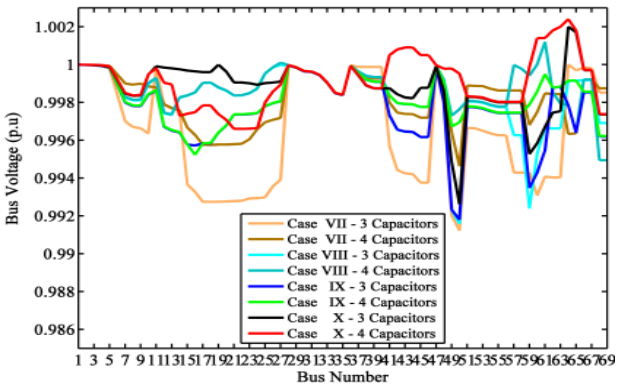

Figure 6 - Bus voltage – 160% Load – 69 Bus

5. Conclusion

In this paper, a complete study has been performed to achieve additional power loss reduction by optimal allocation and sizing of capacitors after optimal allocation and sizing of DG units and NR using the same technique adopted in 'PART-I' (AGPSO) to solve the objective function under three different load levels. The main objective of this paper is to minimize the real power loss before and after capacitor installation. Standard IEEE 33 and 69 bus test systems are used to demonstrate the effectiveness of the proposed method. Though real power loss reduction using high penetrated DGs with NR, achieves above 81% (33 bus), and 87% (69 bus), an attempt has been made to achieve extra power loss reduction by optimal placement and sizing of capacitors (three / four optimal nodes) in the DG allocated reconfigured RDN. It has been proved that after optimal capacitor placement, an additional power loss reduction around 15% for 33 bus system and around 10% for 69 bus test system is achieved after capacitor placement compared to 'PART-I'. Maximum power loss reduction achieved is above 98% for both the test systems compared to B.C. Also from the results it has been witnessed that again case X (optimal placement and sizing of capacitors after case VI) is proved to yield maximum power loss reduction compared to other cases and also maximum bus voltage improved to more than 1 p.u. From the above, it is concluded that greater impacts is noticed after optimal placement of capacitors at four nodes compared to three nodes. However the difference is only meager.

Nomenclature

BCI - Before capacitor Installation
ACI - After Capacitor Installation
TNB - Total No. of Buses
TB - Total No. of branches (TNB-1)
MS - Main Source
NC - No. of nodes for capacitor placement
Q_{MS} - Total reactive power supplied by the Main Source in KVAr
P_{Loss} - Active power loss in a particular branch in KW
Q_{Loss} - Reactive power loss in a particular branch in KVAr
P_D, Q_D - Active and reactive power demand in KW / KVAr respectively
TP_{Loss} - Total active power loss in KW
TQ_{Loss} - Total reactive power loss in KVAr
$Q_{c\,(t)}$ - Capacitance of the Capacitor at t^{th} node
V_t^{min} - Minimum Voltage at t^{th} node (0.95 p.u.)
V_t^{max} - Maximum Voltage at t^{th} node (1.05 p.u.)
V_t - Voltage at t^{th} node

References

[1] Shammah A.A.E, Ahmed M. Azmy, A. Abou El-Ela: "Optimal Sitting and Sizing of Capacitor Banks in Distribution Networks using Heuristic Algorithms", *Journal of Electrical Systems*, Vol.9, No.1, pp. 1-12, 2013

[2] Grainger J.J. and S. H. Lee : "Optimum size and location of shunt capacitors for reduction of losses on distribution feeders", *IEEE Trans. Power App. Syst.*, PAS-100, Issue 3, pp. 1105-18, March,1981

[3] Grainger J.J and S. H. Lee : "Capacity release by shunt capacitor placement on distribution feeders: A new voltage-dependent model," IEEE Trans. Power Apparatus and Systems, Vol. PER-2(5), pp. 1236–1244, June 1982.

[4] Ladjevardi M and M. A. S. Masoum : "Genetically optimized fuzzy placement and sizing of capacitor banks in distorted distribution networks", *IEEE Trans. Power Delivery*, Vol.23, No.1, pp.449-456, 2008

[5] Chiang H : "Optimal capacitor placement in distribution system", *IEEE Trans. Power Deliv*., Vol.4, No.1, pp. 725–34, 1989.

[6] Haque M.H: "Capacitor Placement in Radial Distribution Systems for loss Reduction", *IEE Proceedings - Generation, Transmission and*

Distribution, Vol.146, No.5, pp.501-505, Sep.1999

[7] Bae Y.G. "Analytical method of capacitor allocation on distribution primary feeders", *IEEE Trans. Power Apparatus and Systems, Vol.* 97, No.11, pp.1232–1238, 1978

[8] Baran M E and Wu F F : "Optimal capacitor placement in distribution systems", *IEEE Trans Power Delivery*, Vol. 4, No.1, pp. 725- 734, Jan. 1989.

[9] Baghzouz. Y and Ertem S : "Shunt capacitor sizing for radial distribution feeders with distorted substation voltages", *IEEE Trans Power Delivery*, Vol. 5, pp.650-57, 1990.

[10] Mekhamer S.F, M.E.El-Hawary, S.A. Soliman, MM Mansour :"New Heuristic Strategies for Reactive Power Compensation of Radial Distribution Feeders*", IEEE Transaction on Power Delivery, Vol.17, No.4, pp.1128-1135, 2002*.

[11] Sneha Sultana and Provas Kumar Roy : "Optimal capacitor placement in radial distribution systems using teaching learning based optimization", *Electrical Power and Energy Systems*, Vol.54, pp.387–398, Jan 2014

[12] Boone G and H. D. Chiang :"Optimal capacitor placement in distribution systems by genetic algorithm", *Electrical Power & Energy Systems, Vol.15, No.3, pp.155–162, 1993*

[13] Sundharanjan S, A. Pathwa : "Optimal selection of capacitors for radial distribution systems using a genetic algorithm", *IEEE Trans. on Power Systems*, Vol.9, No.3, pp.1499-1507, 2003.

[14] Carlisle J.C. and A. A. El-Keib : "A Graph Search Algorithm for Optimal Placement of Fixed and Switched capacitors on Radial Distribution Systems", *IEEE Trans. on Power Delivery*, Vol.15, Issue 1, pp.423-28, Jan 2000

[15] Rao, R.S., Narasimham, S.V.L., Ramalingaraju, M : "Optimal capacitor placement in radial distribution system using plant growth simulation algorithm", *Int. J Elect Power Energy System*, Vol.33, No.5, pp.1133-1139.

[16] Devabalaji K.R, Ravi K, Kothari D.P : "Optimal location and sizing of capacitor placement in radial distribution system using bacterial foraging optimization algorithm", *Int. J Electric power and Energy System Vol.*71, pp.383–90, Oct.2015.

[17] Devabalaji K.R, Mohamed Imran A, Yuvaraj T and Ravi K, "Power Loss Minimization in Radial Distribution System", In : *International Conference on Alternative Energy in Developing Countries and Emerging Economies*, Bangkok, Thailand , Vol. 79, Energy Procedia, pp. 917-23, May 2015

[18] Singh S, Rao A : "Optimal allocation of capacitors in distribution systems using particle swarm optimization", *International Journal of Electrical Power and Energy Systems*, Vol.43, No.1, pp.1267-1275, 2012.

[19] Muthukumar K,. Jayalalitha, S, Ramasamy M and Haricharan Cherukuri S : "Optimal Shunt Capacitor Allocation and sizing using Harmony Search Algorithm for power loss minimization in Radial Distribution Networks", *International Journal of Development Research,* Vol.4, No.3, pp.537-545, 2014

[20] Gnanasekaran N, Chandra Mohan S, Sudhakar T.D, and Sathish Kumar P : "Maximum Cost Saving Approach for Optimal Capacitor Placement in Radial Distribution Systems using Modified ABC Algorithm", *International Journal on Electrical Engineering and Informatics*, Vol.7, No.4, pp.665-678, Dec 2015.

[21] Abdelaziz A.Y, Ali E.S. S.M. Abd. Elazim : "Optimal sizing and locations of capacitors in radial distribution systems via flower pollination optimization algorithm and power loss index", Engineering Science and Technology- An International Journal, Vol.19, pp. 610–618, 2016

[22] Mohamed Shuaib Y, Surya Kalavathi M : "Optimal Capacitor Placement in Radial Distribution System using Group Search Optimization Algorithm", *International Journal of Scientific & Engineering Research*, Vol.5, No.4, pp.77-83, 2014

[23] Mohamed Shuaib Y, Surya Kalavathi M, Christober Asir Rajan : "Optimal capacitor placement in radial distribution system using Gravitational Search Algorithm", *Electrical Power and Energy Systems*, Vol.64, pp.384–397, 2015

[24] Jovica Vuletic, Mirko Todorovski : "Optimal capacitor placement in radial distribution systems using clustering based optimization", *Electrical Power and Energy Systems*, Vol.62, pp.229–236, 2014

[25] Attia El-Fergany and A. Y. Abdelaziz. : "Multi-objective Capacitor Allocations in Distribution Networks using Artificial Bee Colony Algorithm", *J Electrical Engg. and Technology,* Vol.9, No.2, pp.441-451, 2014

[26] Silvio Segura, Rubén Romero, Marcos J. Rider : "Efficient heuristic algorithm used for optimal capacitor placement in distribution systems", Electrical Power and Energy Systems, Vol. 32, pp.71-78, 2010.

[27] Abd-Elazim S.M, and E.S. Ali : "A hybrid Particle Swarm Optimization and Bacterial Foraging for optimal Power System Stabilizers design". *Electrical Power and Energy Systems*, Vol.46, pp.334–341, 2013.

[28] Sneha Sultana and Provas Kumar Roy, "Multi-objective quasi-oppositional teaching learning based optimization for optimal location of distributed generator in radial distribution systems", *Electrical Power and Energy System,* Vol.63, pp.34–545, 2014

[29] Seyedali Mirjalili, Andrew Lewis, Ali Safa Sadiq. : "Autonomous Particles Groups for Particle Swarm Optimization", *Computer Engg. & Computer Science, Arabian Journal of Science and Engineering, Vol.*39, pp.4683-97, 2014.

[30] Venkatesh, B., Ranjan, R, "Data structure for radial distribution load flow analysis", *IEE Proceeding in Generation, Transmission and Distribution*, Vol.150, 1, pp.101-6, 2003.