DIGITAL EMI FILTER FOR AN ELECTRIC VEHICLE DRIVE TRAIN STRUCTURE USING XILINX SYSTEM GENERATOR

Yosr BCHIR
Laboratory of Electronics and Microelectronics of the FSM
National Engineering School of Monastir, University of Monastir, Tunisia
Yosr.bchir@hotmail.fr

Soufien GDAIM
Laboratory of Electronics and Microelectronics of the FSM
National Engineering School of Monastir, University of Monastir, Tunisia
sgdaim@yahoo.fr

Hamza DJILALI
Queen's University Kingston,Ontario, Canada
dhamza@ieee.org

Abdellatif MTIBAA
Laboratory of Electronics and Microelectronics of the FSM
National Engineering School of Monastir, University of Monastir, Tunisia
Abdellatif.mtibaa@enim.rnu.tn

Abstract: *Mitigation the Electromagnetic Inferences (EMI) is currently a challenge for scientists and designers in order to cope with CEM compliance in Switching Mode Power Supply (SMPS) and ensure the reliability of the whole system. Standard filtering techniques: passive and active ones present some insufficiency in terms of performances at HF (High frequencies) because analog components would be no more controllable and this is mainly due to their parasitic elements. So developing EMI digital filters is more interesting especially with the embedment of the machines 'control on FPGA (Field Programmable Gate Array) chip.*
In this paper, we present a design of a Digital Active EMI filter (DAF) in a drive train system of an Electric Vehicle (EV). The active filtering process is realized by using Xilinx System Generator (XSG) and its performances are evaluated by simulative results on Simulink/MATLAB.

Keywords: *DAF, drive train system, Conducted EMI noise, XSG*

1. Introduction

Currently, researchers are investigating alternatives to petroleum-fueled internal-combustion-engine vehicles (ICEVs) in transportation. This is mainly due to the facts of climate considerations (decreasing emissions of greenhouse gases and urban air pollutants) and minimizing petroleum consumption. Developing advanced Electric Vehicles (EVs) includes pure battery electric vehicles, hydrogen fuel-cell electric vehicles and plug-in hybrid electric vehicles. EV stimulate a considerable interest but there are many constraints that developers and designers should take into account in order to ensure the reliability and the security of the EV. This paper deals with EMC compliance in the powertrain system.

The powertrain of battery- power vehicles consists of a battery, a power converter that inverts the Direct Current (DC) output of the battery to Alternating Current (AC) and the electric motor. The output of the electric motor is the torque to the wheels that power the vehicle.

The power electronic part is a highly efficient switched-mode three-phase induction motor produces an inherent Common Mode (CM) voltage that drives unwanted currents into the whole system of the drive train. The produced CM currents are considered as a source of EMI, which can not only interfere with other electronic systems of the EV causing intolerable parasitic signals but also damage the motor reliability and shorten its life.

In literature, reducing electromagnetic inferences (EMI) was the aim of many works which discussed the effect of the topology of the inverter on EMI; in fact, in voltage source inverters, reducing the level of the switched voltage step, such as is done in multilevel converters can reduce the noise source in the system [1-3]. The authors of [4] have shown that matrix converter can reduce the noise level by 20 dB due to the varying switched voltage, so that both CM and DM filters can be reduced.

In other works, researchers have highlighted the impact of modulation techniques in attenuating EMI noise. Common Mode Reduction (CMR) techniques was widely used in power inverter to attenuate CM noise [5-7], some authors have exploited modulation techniques

with three-level inverters [8-11] and five-level inverters [12-13].

Therefore, filtering still the conventional technique in reducing EMI noise ; many works was interested in passive filtering because of its simplicity of design and its performance[14-17] , but the disadvantage of high cost and size stimulated in [18-21] to improve its efficiency and deal with its drawbacks. Some authors have considered active filtering as an alternative to passive one [22] But it proves an efficiency ups to 1MHz and this does not cover the range defined by the standard CISPER22 which consider a frequency range of 150 KHz to 30MHz. [23].

In this paper, we propose a design of FPGA-based digital EMI filter in order to overcome conventional filters 'disadvantages in terms of size, weight and cost and to improve the efficiency of the whole system.

This paper is organized as follows: section II contains the principle of the inverter in order to locate the cause of EMI noise, section III is about presenting the design of digital active filter, section IV is devoted to the simulations of the drive system train with and without integrating filtering techniques and discusses the obtained results, finally a conclusion about the paper's contribution is given.

2. The two-level inverter's principle

Voltage source Pulse Width Modulation (PWM) inverters have been widely used in variable speed motor drive systems because of their various advantages such as low THD of output waveforms, high efficiency, high power factor, etc.

The scheme of two-level inverter is illustrated by Figure 1.

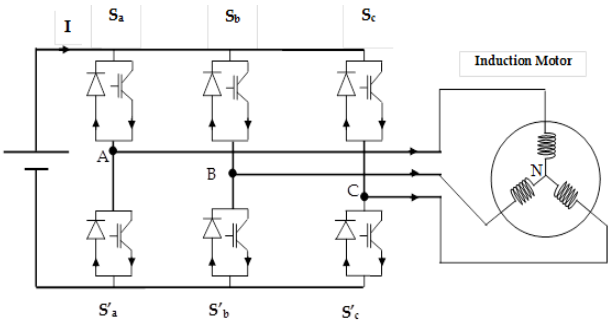

Fig.1 The scheme of a two-level inverter

The common problem with power inverters is the generation of common mode voltage (CMV) that is due to the combination of switching states as shown in equation (1):

$$V_{CM} = \frac{1}{3}(V_{AN} + V_{BN} + V_{CN}) \quad (1)$$

The CMV leads to leakage current which circulates through stray capacitors and the ground producing conducted and radiated EMI to electronic equipment through power lines [24]. This current may cause bearing failure of the induction motor [25] and even produce mechanical vibration [26]. These negative impacts are more significant with the increase of switching frequency and power of electronic elements.

The purpose of the presented work is to attenuate the undesirable EMI conducted noise caused by the power inverter of the an EV's drive train.

3. The design of the ADF (Active Digital Filter)

3.1. An overview on active analog EMI filters

Active noise cancellation technique is realized by using active devices that generate and inject the EMI noise which is the opposite of the EMI system noise. But the switching speeds of these active components are unable to cover the whole frequency range (from 150 KHz to 30MHz); in fact, their reliability is up to 3 MHz. So, in higher frequencies, passive components are needed to increase the filter's efficiency [27]. The disadvantages of analog filter are mainly the parasitic components of analog devices which are more considerable in high frequencies, their volume and cost. Compared to analog filters discrete ones are characterized by their independency on frequency. Besides there are no particular volume devoted to them since they are integrated with the system's control algorithm in the FPGA chip.

The next part is devoted to present the ADF; its principle of attenuating the EMI noise developed using Xilinx System Generator (XSG) and the whole system of the drive train integrating the ADF.

3.2. The principle of ADF

An ADF principle is developed in [28], [29] and it is based on three steps:

- Sensing part: This stage is devoted to sense the noise signal. The used circuit is a RC high-pass filter with a cutoff frequency of 150 KHz.
- Control part: The role of this part is to generate a 180 ° degree shift signal.
- Injection part: This step is about injecting with high fidelity the produced opposed shift noise signal in the order of the nullification of the EMI noise signal .The used circuit at this stage is a RC low-pass filter with a cutoff frequency of 30MHz.

The chosen cutoff frequencies aim to localize the frequency spectrum at the range frequency range of interest (from 150 KHz to 30MHz).

4. The design of the ADF using XSG

Compared to microcontrollers and DSP (Digital Signal Processing), FPGA has the best performances that make it superior to other processors: its programmable hardware structure, the ability of parallel processing and the real time implementation are considered as the main features of FPGA board layout. For the control of IM (Induction Motor) FPGA are widely used and this make the digital filtering technique of conducted EMI noise

interesting since it is embedded with the controller of the IM ; therefore the ADF allows to save size and cost compared to conventional analog filtering techniques.

For prototyping the ADF in the FPGA, knowledge of the required hardware description language VHDL is required which complicate the intended task. XSG is a toolbox developed for MATLAB/Simulink which enables a generation of a synthesizable VHDL code to be directly used for Xilinx FPGA chip. XSG make the co-simulation the hardware with the graphical environment of Simulink (Mathworks models based-Simulink) possible in order to validate the proposed designs. The FPGA implementation flow of the ADF is given in Fig.2.

The scheme of the ADF is developed using XSG as illustrated in Fig.3. Its design is based on the previous model of different described stages is realized by using black boxes and the predefined Xilinx block sets.

The embedded design is created with the different blocks in the Xilinx block sets and it is based on the principle of active filtering technique as detailed in the previous paragraph. It consists mainly of three stages:

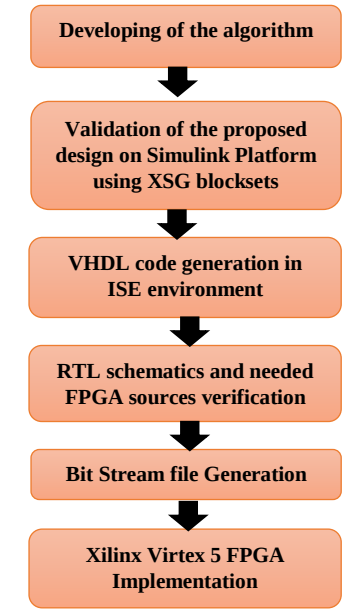

Fig.1 FPGA Implementation flow using XSG

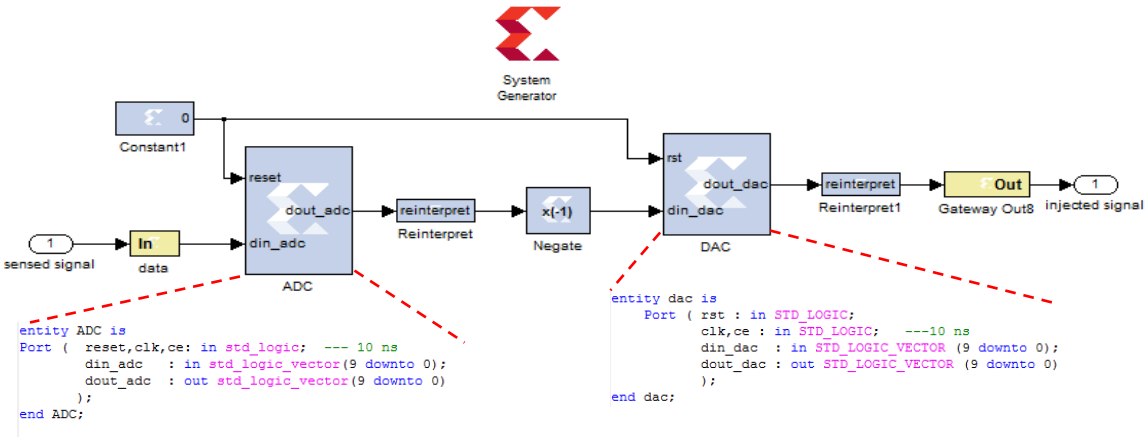

Fig.2. The design of the ADF with Xilinx blocks

- The Analog to Digital Converter (ADC): AD9071 is the used for high-performance signal path. The frequency of the ADC must be higher than twice the upper limit of the frequency spectrum to fulfill Nyquist criterion. . The selected ADC operates at 100MSPS and it is characterized by a resolution of 10 bits. This ADC is designed to convert the analog signal (the sensed noise signal) to digital one.
- The Inversion process: The sampled signal issued from the ADC is conducted to be processed into a phase reversal algorithm.
- The Digital to Analog Conversion (DAC): the used device is a THS6551. It is a 10 bit high speed converter with a sampling rate of 100MSPS. Its role consists on the conversion of the digital inverted signal to an analog one in order to be injected into the circuit to nullify the sensed noise.

5. The model of the drive train integration an ADF

The LISN (Line Impedance Stability Network) is used in EMI measurement step at the frequency range of interest (from 150 KHz to 30MHz). The whole system of the EV ‘s drive train including the battery, the LISN, the inverter, the induction motor and sensing and injecting ports is simulated using PSpice and the scheme is illustrated in fig.4.

The input conducted EMI noise is received by a sensing circuit and digitized by an ADC unit. The acquired data is processed using a reverse data algorithm, then converted to the analog form using the DAC and injected into the system via an injecting circuit.

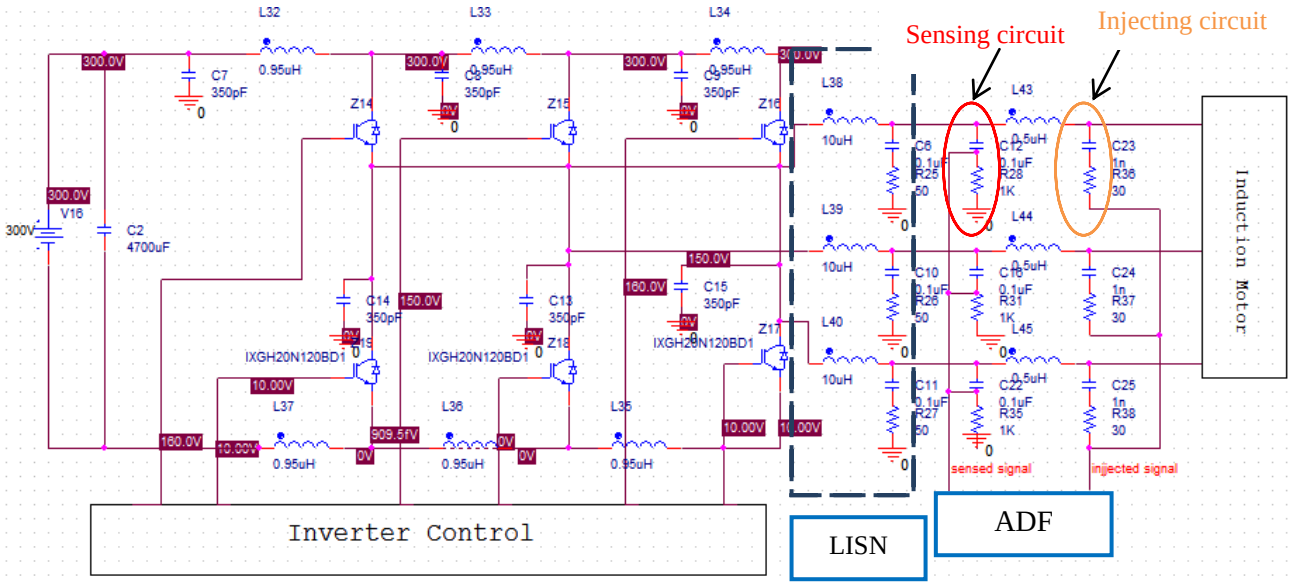

Figure 3 PSpice Schematic of the drive train system with integrating an ADF

In order to validate the scheme of the proposed DAF, the drive train system of the EV is extracted to Simulink using SLPS interface. PSpice SLPS interface is a tool developed by Mathworks that enables the co-simulation between PSpice and MATLAB/Simulink. So the drive train scheme is included in Simulink system simulator allowing a single prototype to co-simulate both the established drive train system and the developed ADF using XSG. The scheme of the EV's drive train's system including the ADF is presented in the following figure:

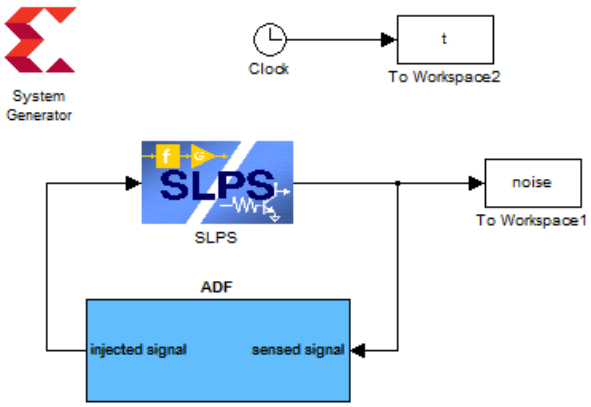

Fig 4. the drive train system and the ADF design on Simulink/MATLAB

Fig.5 illustrate a co-simulation between PSpice/Simulink englobing the two schemes of Fig. 3 and 4. Simulation results and interpretations are detailed in the following paragraph.

6. Simulation results and interpretation

The conducted noise is visualized in frequency spectrum by using the FFT (Fast Fourrier Transform) to compare drive system performances with/without ADF.

Fig.6 and Fig.7 illustrate respectively the frequency spectrum of EMI CM conducted noise without and with integrating ADF.

The first simulation is performed without integrating the EMI filter. As illustrated in Fig.6 , we can note that the first range of frequency is from (150KHz to 2MHZ) in this interval the CM Conducted EMI noise is attenuating: its variation is from 136.4 dBµV to 82.71dBµV, the second range of frequency is from 2MHz to 10MHz and its characterized by several high peaks of unwanted EMI noise such as the points : (2.27MHz,93.71 dBµV),(3.8MHz,99.6 dBµV), (7.55MHz,83.79dBµV), and the third interval of frequency range which is from 10MHz to 30MHz is characterized by an average peak of 55 dBµV of conducted EMI noise.

The second simulation is performed with integrating the ADF filter. We can note that the frequency spectrum is attenuating in the frequency range [150KHz,30MHz], the higher values of CM conducted noise are depicted in a range of [150KHz, 200KHz] with an average value of 104 dBµV. Generally, an attenuation of about 30dBµV is achieved in a frequency range varying from 150 KHz to 8MHz and the peaks of CM conducted noise established in Fig.6 are completely filtered.

The performance of the ADF in terms of attenuating CM conducted noise is proved by the last simulation results.

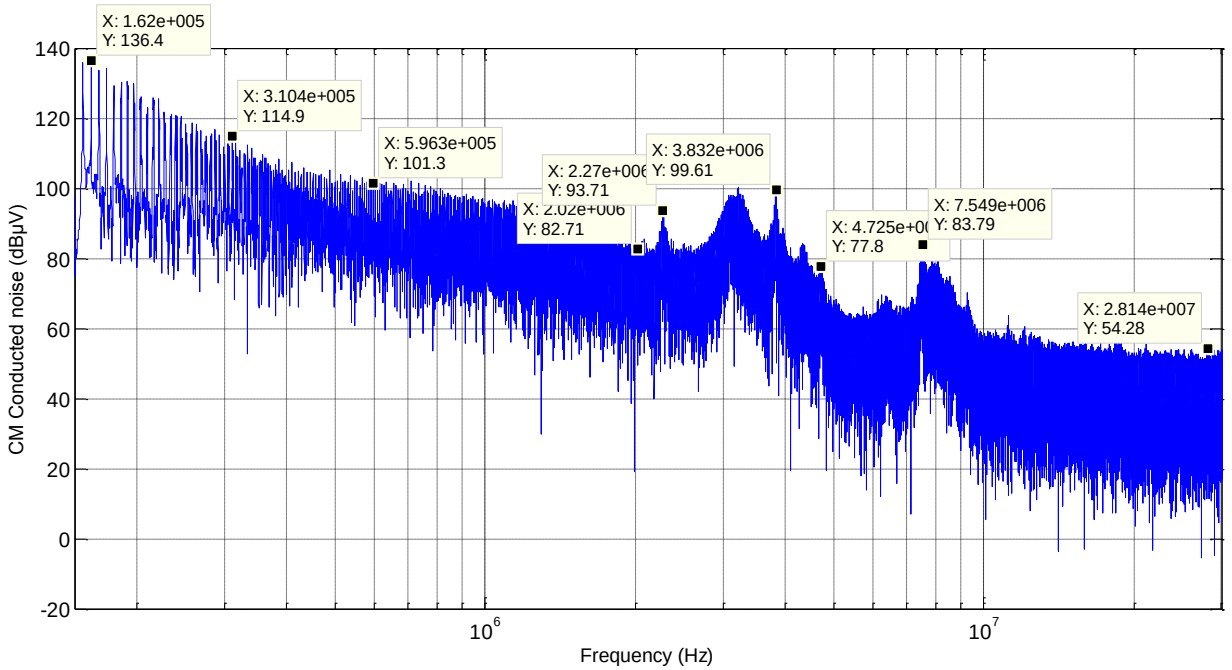

Fig.5 CM EMI Conducted noise without ADF filter

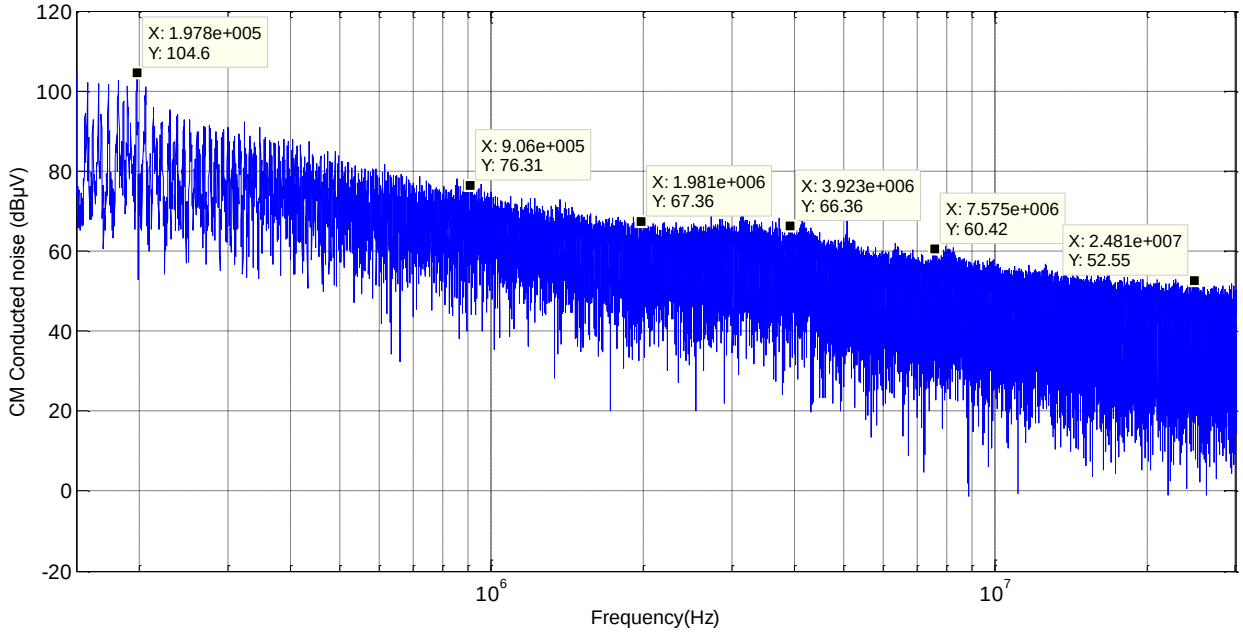

Fig. 6 CM EMI Conducted noise with integrating an ADF

7. FPGA implementation of the ADF

Hardware block of the ADF established in XSG can be synthesized and downloaded into the target FPGA chip. The complete design was verified for area utilization, timing and power consumption using Xilinx ISE. Fig.8 illustrates the RTL schematic implementation result made by Xilinx ISE and table.1 show the implementation results for ADF ressources utilization of the implementation on Viretex-5.

Table. 1 ADF resources utilization Table

Resources	Available	Utilization
Number of Slice registers	44 800	1%
Number of Slice LUTs	44 800	1%
Number OF bonded IOBs	640	3%
Number of BUFG/BUFGCTRLs	32	3%

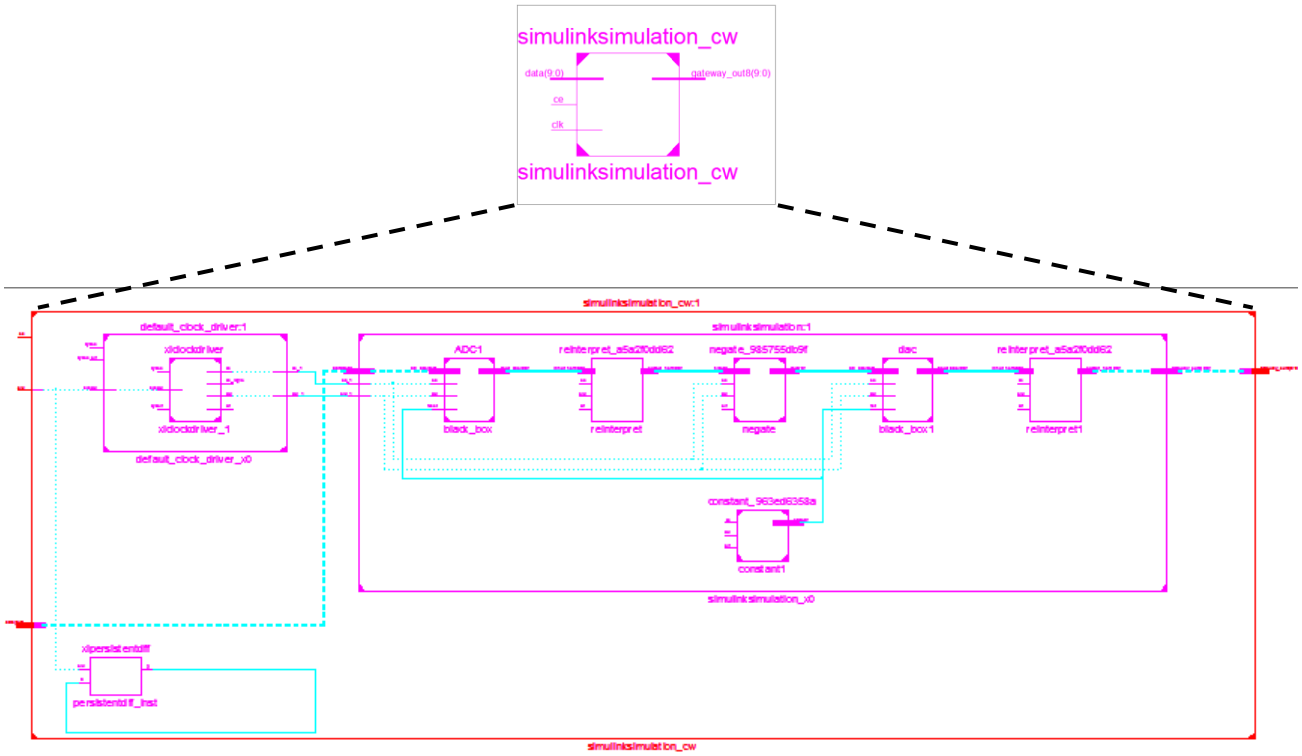

Figure 7 RTL schematic of the ADF design implementation on FPGA

8. Conclusion

In this paper, a DAF is presented. Its concept is based in measuring the EMI behavior and injecting its opposed at the determined injecting point in order to eliminate the conducted CM EMI disturbance. The performance of the proposed method is evaluated by simulative results with and without integrating the digital EMI filter;. The realization of the proposed process is done using XSG and the DAF is embedded in the FPGA chip with the controller system of the used inverter. The novel filtering technique proves its efficiency in terms of cost, size and conducted EMI noise attenuation.

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