INVESTIGATION OF BRIDGELESS POWER FACTOR CORRECTION IN SEPIC BASED ZERO VOLTAGE TRANSITION IN REDUCED RIPPLE FACTOR

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Abstract

In this paper, proffered an ultramodern bridgeless single-phase AC–DC PFC rectifier depends on SEPIC topology and it resort to a bidirectional switch and fast diodes. In the primary stage, AC voltage is indoctrinated into an uncontrolled DC voltage by means of diode rectifiers which is plunged with the second stage of isolated DC-DC converters adopting HF transformer for isolation. These two-stage AC-DC converters have the obstacles of power quality in provisions of injected harmonic currents at AC mains evoked voltage distortion, degraded power factor and large size of DC capacitor filter at first stage. Subsequently the solid-state switch mode AC-DC converters having high-frequency transformer isolation are mellowed in buck, boost and buck-boost configurations by improved power quality in conditions of reduced THD of input current, PFC at AC mains and correctly regulated and isolated DC output voltage feeding to loads starting few Watts to more than a few kW. Their realization of the proposed model is taking measured with the voltage and current stresses on the active switch and diodes, currents uninterrupted inductors and efficiency are juxtaposed to the available quadratic converters. The authority of the new hybrid converters is predominantly on notorious to saving in the range and rate of the inductors and less current stresses in the switching elements premier to smaller conduction losses. Enduringly the simulation results in like manner comparative performance are manifested and conversed for the majority of the proposed topologies.

Keywords: *Power Factor Correction (PFC), Total Harmonic Distortion (THD), Single-Ended Primary Inductance Converter (SEPIC)*

1. Introduction

In recent years, the demand for improving power quality of the ac system has become a great concern due to the rapidly increased numbers of electronic equipment [1]. To reduce harmonic contamination in power lines and improve the transmission efficiency, power factor correction (PFC) research became an active topic in power electronics, and significant efforts have been made on the developments of the PFC converters [2]. As a matter of fact, the PFC circuits are becoming mandatory on single-phase power supplies as more stringent power quality regulations and strict limits on the total harmonic distortion (THD) of input current are imposed [3]. The preferable type of PFC is active PFC since it makes the load behave like a pure resistor, leading to near-unity load power factor and generating negligible harmonics in the input line current. Most active PFC circuits as well as switched mode power supplies in the market today comprise a front-end bridge rectifier, followed by a high-frequency dc–dc converter such as a boost, a buck–boost, a Cuk, and a flyback converter [4-6]. Most of the PFC rectifiers utilize boost converter at their front end. Boost converter provides many advantages such as natural power factor correction capability and simple control. However, low voltage applications such as telecommunication or computer industry an additional converter or an isolation transformer is required to step down the voltage.

Among numerous kinds of electronic utensils, the power supplies through active Power Factor Correction (PFC) procedure is considered as essential for to convene harmonic rules [7]. On the other hand, the effectiveness is diminished in lowest input voltage for complete input voltage application and the awful function condition is measured in the power converter design process [8]. According to the consideration of most awful function position into the thermal design and heatsinks size, the enhancement of effectiveness is significant at minor line voltage [9]. Moreover, the flyback transformer is mainly executed in one quadrant and the magnetic core is not completely exploited. The leakage inductance of transformer necessitates appropriate clamp or snubber circuit for to bind the voltage stress through the switch. Consequently, it is not a high power effectiveness or compactness explanation [10] [11].

A SEPIC converter is generally encompassed the finest power feature rectification presentation, but the effectiveness is not equivalent to the further explanation. A flyback converter is not containing a transformer and the related leakage ring consequence [12]. Also, it is premeditated for a broad variety of output and input proportion. In DCM, the input inductor current is maintained the input voltage through lesser ripple current when contrasted by the flyback and boost converters [13]. Here, the isolated SEPIC converter employs a transformer for to restore the second inductor [14]. The two magnetic elements actually augment the expenditure among one magnetic core. The symmetrical and asymmetrical half-bridge converters are employs for standard power applications [15]. These converters are generally included enhanced power feature and enhanced effectiveness among two switches. Besides, the transformer is executed in two quadrants through the additional exploitation of core and lesser size of magnetic elements for both the transformer and output inductor [16] [17]. The foremost benefit of SEPIC converter is that it encompassing a low input current ripple. On the other hand, a mass inductor is employed to diminish the current ripple [18]. Input current ripple is considered as a significant necessity for the broad employ of low voltage resources like batteries, supercapacitors, and fuel cells [19] [20]. Additionally, the large ripple current is lessening the duration of input resources. The significant aspect of the converter is to maintain the PFC, which is analyzed with the proposed converter and combined with the existing converter design. The detailed analysis of the proposed method is described in the section 3 and the literature review is presented in the section 2. The performance analysis of the proposed and existing models is analyzed and implemented in MATLAB/Simulink platform presented in the section 4. The conclusion part is presented in the section 5.

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2. Recent Research Works: A Brief Review

In literature, several related works already exist for the voltage ripple investigation with the help of SEPIC converter. Some of the works are specified as below.

Lee *et al*. [21] have offered an isolated SEPIC DC-DC converter among ripple complimentary input current and lossless snubber. The anticipated converter was generally derived from a predictable isolated SEPIC converter which is used to facilitate electrical segregation and high voltage gain by means of a coupled inductor. The input current ripple was considerably diminished by means of exploiting a supplementary circuit in a lossless snubber circuit among a supplementary diode. Additionally, the greatest switch voltage stress was fastening a low voltage through the snubber circuit. So, a low voltage evaluation MOSFET is containing low RDS (on) which is exploited as a major switch device. Therefore, the overall power effectiveness was enhanced.

Kanimozhi *et al*. [22] have examined a DC-DC type double boost converter which is incorporated by means of SEPIC converter. The incorporated converter encompasses the attributes of predictable boost and SEPIC converters like continuous input current, low input current ripple among unmitigated competence. The converter includes seven active components and a small signal of the converter. Position space averaging procedure was employed to obtain the diminutive signal representation. The responsibility of ratio control with output voltage transfer function was determined.

Rosas-Caro *et al*. [23] have offered a dc-dc SEPIC which is used to accomplish high voltage gain through uniting the converter among a diode-capacitor voltage multiplier and their applications to PEMFC systems. The constant input current and high voltage gain were sufficient for the power circumstance in fuel cell systems. Here, the voltage gain was synchronized by means of PWM which is augmenting the diode-capacitor multiplier arrangement. The foremost uniqueness of converter is constant input current, high-voltage gain, to evade the employ of severe responsibility sequences and transformers, and low voltage stresses in the power switches. Moreover, the converter topology utilizes a control switch and two inductors which permit a comparatively uncomplicated execution.

Al-Saffar *et al*. [24] have offered an enhanced edition of Single-Ended Primary Inductor Converter (SEPIC). The converter includes predictable SEPIC converter with a supplementary high-frequency transformer and diode which is used to preserve an unrestrictive method of DC inductor currents for the period of a switch on condition. The voltage conversion proportion uniqueness, semiconductor device voltage, and current stresses are distinguished. The foremost benefit of the converter is the constant output current, lesser output voltage ripple, and lower semiconductors current stress when contrasted by the predictable SEPIC converter.

Shi *et al*. [25] have offered a Single-Ended Primary Inductor Converter (SEPIC) among coupled inductors because the power features preregulator (PFP) phase for two-stage ac/dc converters. A PFP is generally supplying the initial phase of an active two-stage ac/dc converter in diverse applications such as inductive heating systems, wireless charging systems, and onboard chargers for plug-in electric vehicles. Usually, boost-category PFPs are exploited to normalize the dc-link voltage at a predetermined voltage. On the other hand, a variable dc-link voltage is augmenting the general effectiveness of converters. The converter was premeditated to activate in irregular conduction method for to accomplish soft switching in switches and diodes. The directly coupled inductors are exploited to diminish the quantity of magnetic elements and diminish the input current ripple.

In consequence of small cost and minimalism, diode rectifiers and thyristor rectifiers are used for transmogrify the AC input source to DC bus voltage. Though the focal dilemma is low power factor and high harmonic content of the input current. A family unit of single-stage isolated PFC power supplies is depend on buck and boost PFC cells and an integrated boost fly back PFC converter is voltage spikes facing the switch as it turns off. This converter is enriched by use up a supernumerary winding on the fly back transformer to pare the bulk capacitor voltage. But it uses two active switches and thus its convolution is lofty. The distortion induced via the discontinuity dead zone is relative to output voltage and upturn the overall THD of the buck PFC. It is fortuitous to append additional switches to the buck PFC to resolve dead zone and to improve THD but this overture comes at the cost of lower efficiency and discomfiture the hope of electing the buck PFC more than the boost PFC topology. Someone design challenge of buck PFC on THD specifications is yoked with the discontinuity of input current. As input current converts zero as the diode is conducting, the averaged input current swerve from an ideal sine wave impute to additional distortion. The discontinuity of input current too induces redundant Electromagnetic Interference (EMI). Therefore, for the PFC, an enhanced SEPIC is designed and analyzed their power factor and THD values. The following section is analyzed with the enhanced SEPIC modeling and traditional modeling of SEPIC and specified their performances also.

3. Structure of Proposed Bridge less SEPIC Converter

Modern rectifier technology currently coalesce many of the DC to DC converter fundamentals in between the diode bridge configuration and the load to structure the Hybrid converters. The conventional converters grieve from low efficiency at extremely low voltage gains. Solid-state switch mode AC-DC converters having high-frequency transformer isolation are advanced in buck, boost, and buck-boost configurations with improved power quality in conditions of reduced THD of input current, PFC at AC mains and correctly regulated and isolated DC output voltage fatten to loads from few Watts to some kW [29]. The conventional SEPIC PFC converter is pictured in figure 1. There are numbers of international standards to perimeter the harmonic content, incite owing to the line currents of equipment attached to electricity distribution networks. For that reason a reduction in line current harmonics or PFC is vital. This inspiration is the research effort. The intention is to progress the power factor almost unity with minimum THD. There are two types of PFC's as Passive PFC and Active PFC. The PFC converter topology using active techniques is the superior compared to the passive PFC [30]. The deprivation of passive PFC is the sizes of the filters are not felicitous for a compressed system and existing for one condition of load solitary.

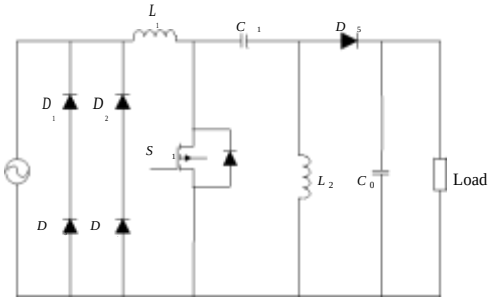
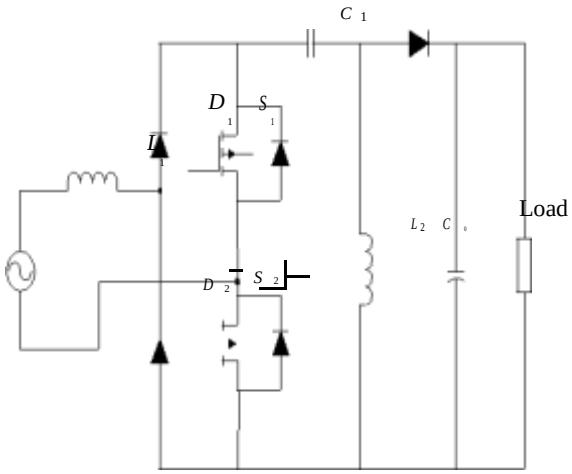


Figure.1 The conventional PFC with SEPIC converter

For this revise small EMI (LC) passive PFC and Boost Converter active PFC are expound with rightful switching control. Contrastive conventional and nonlinear control schemes are rehash for the switching of Boost PFC Converter which is the key to get at power factor virtually to union with fewest percentage of THD. For particular cases the input power factor is practically unity and the line current waveform is espied as sinusoidal with THD percentage is in the sustain limit. In figure 2 (a), the structure of the bridgeless SEPIC converter has been illustrated. The component count is reduced and it shows high efficiency due to the absence of the full-bridge diode. However, in this converter, an input inductor with large inductance should be used in order to reduce the input voltage and current ripple. In addition, the conduction losses on intrinsic body diodes of the switches are caused by using single Pulse Width Modulation (PWM) gate signal. Normally, the buck operation is corral by inlay either $Down_1$ and $Down_3$ structure in a conventional SEPIC converter which is shown in Figure 2 (b, and c). In the circuit $Down_1$, the input capacitor of a SEPIC is gratuitous. In the circuit $Down_3$, the output inductor and diode become needless.



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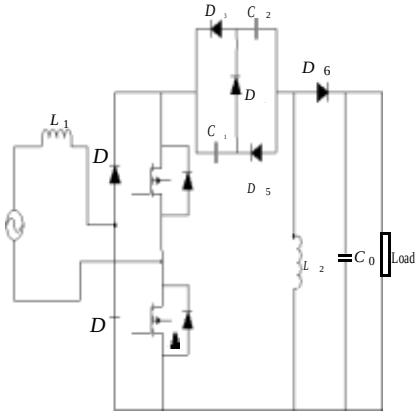

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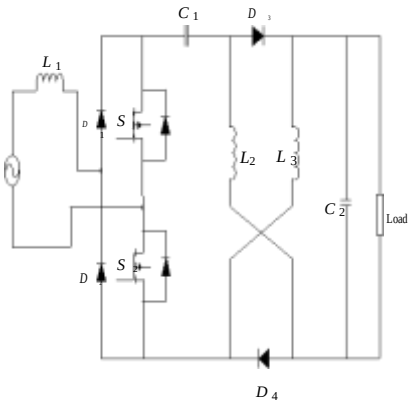

(c)

Figure.2: The Structure of (a) the bridgeless SEPIC converter and the PFC buck operations (b) $Down_1$ and (c) $Down_3$ in SEPIC converter

For the first one, the input to output voltage ratio can be found as (1),

$$V_{out} = \frac{D}{D_1(1+D_1)} V_{in} \quad (1)$$

Explicitly one gets a buck of the line $1+D_1$ times hilly than in a classical SEPIC converter [31]. For the second buck hybrid SEPIC converter, the voltage second proportion on L_{in} and L_1 written for the two switching stages are express as equations (2) and (3),

$$V_{in}D + (V_{in} - V_c - V_{out})(1-D) = 0 \quad (2)$$

$$\frac{1}{2}(V_{out} - V_c)D + V_{out}(1-D) = 0 \quad (3)$$

Then it comes from,

$$V_{out} = \frac{D}{2D_1} V_{in} \quad (4)$$

The buck of the line voltage two times more obvious than in a classical SEPIC converter is hoard.

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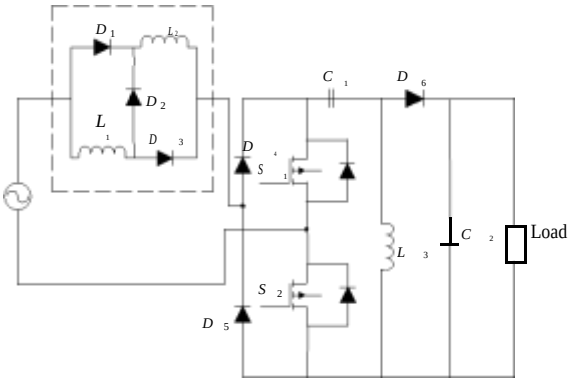


Figure 3. Proposed boost mode Bridgeless PFC-SEPIC Converter

The hybrid SEPIC converter in the boost mode is inheriting by using Up_3 , which is established in figure 3, the input inductor of a classical SEPIC becoming preventable. The first stage is basic single phase rectifier displaced by high frequency customized switched capacitor DC-DC second stage. The value of duty cycle ought to be preferred to reach specific low output voltage from a conventional two stage converter is lesser than that of proposed converter. Adding of the switched capacitor branch used to attain equal output voltage level with relatively high duty cycle. Hence the efficiency of the proposed converter should be more than that of conventional two stage converter for similar voltage gain [32]. The voltage balance on L_1 and L_2 set in an equation (5) and (6),

$$V_{in} D + \frac{1}{2}(V_{in} - V_c - V_{out})(1-D) = 0 \quad (5)$$

$$V_c D + V_{out}(1-D) = 0 \quad (6)$$

That results becomes in (7),

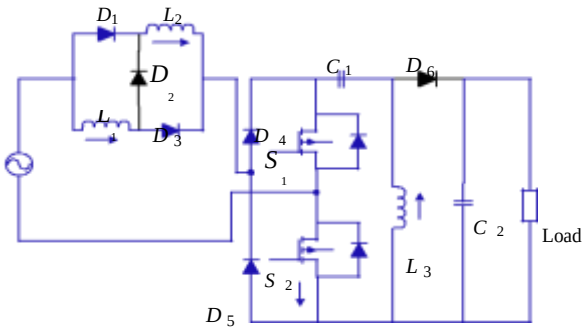
$$= D(1+D) \quad (7)$$

The output voltage is $1+D$ times more DC gain than that lend by a classical SEPIC converter.

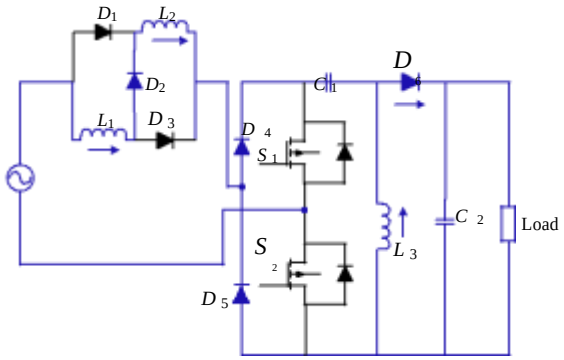
$$V_{out} \quad \frac{}{D1} V_{in}$$

3.1. Principle of Operation

The proposed two stage converter circuits inject three inductors (L_1, L_2 *and* L_o) , two capacitors (C_1 *and* C_o) , eight diodes ($D_1 - D_7$, *and* D_{out}) and one unidirectional switch (S) . L_1, L_2 and L_o are SEPIC inductors. The input filter enclose with inductor and capacitor. R_o and C_o are the load resistance and output filter capacitor of the proposed circuit resultantly. Resistive load has been chosen for this exploration since this kind of load tenders highest harmonic distortion in the input side while output is filtered. Conversely R-L or R-C type of load has built-in filter property to lessen the distortion [33]. Therefore in perform the converters are considered with resistive and inductive load.



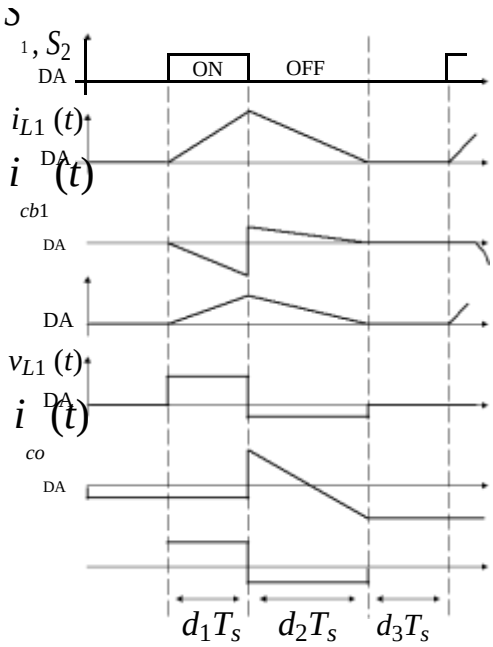
(a)



(b)

Figure 4. The proposed PFC-SEPIC converter model operation in (a) switch ON and (b) switch OFF

In modern converters the high frequency input AC chopping grant chopped input current. A small input filter frame the shape near sinusoidal. So the input current THD reduces. To raise the input power factor proper feedback is impoverish [34]. The operating principle of the proposed converters is expounded below. The proposed two-stage SEPIC topology has two operating steps and made known in figure 4.



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The waveform of currents and voltages in Bridgeless SEPIC Power Factor Correction with Coupled-inductors is open to view in figure 5. Firstly the circuit switch is ON and OFF in that order in positive and negative half cycle of the supply AC voltage. The operation in positive half-line cycle and negative half-line cycle are similar thus the analysis will be contest in positive half-line cycle only [35]. The proposed converter will control in its remuneration as the ability to operate as PFC is inborn, lower component stress, and suitable for low power applications. The rewards are also together with the power switches are turned on at zero current and the output diode is turned off at zero current and near unity power factor.

4. Results and Discussions

In this part, reason about the performance of the bridgeless SEPIC converter and check out the power factor, efficiency, and THD. The proposed system is guesstimate by help out of MATLAB/Simulink platform and the effectiveness is contemplated with other conventional models. Derived from the performance the proposed model is bridgeless and lofty effective. The comparative models and the proposed model are displayed in figure 6, which is wrought with Simulink model. The performance of the bridgeless SEPIC converter is analysis with the 5 variations. These are listed below,

- Conventional SEPIC
- bridgeless
- step down 1
- step down 3
- proposedmodel

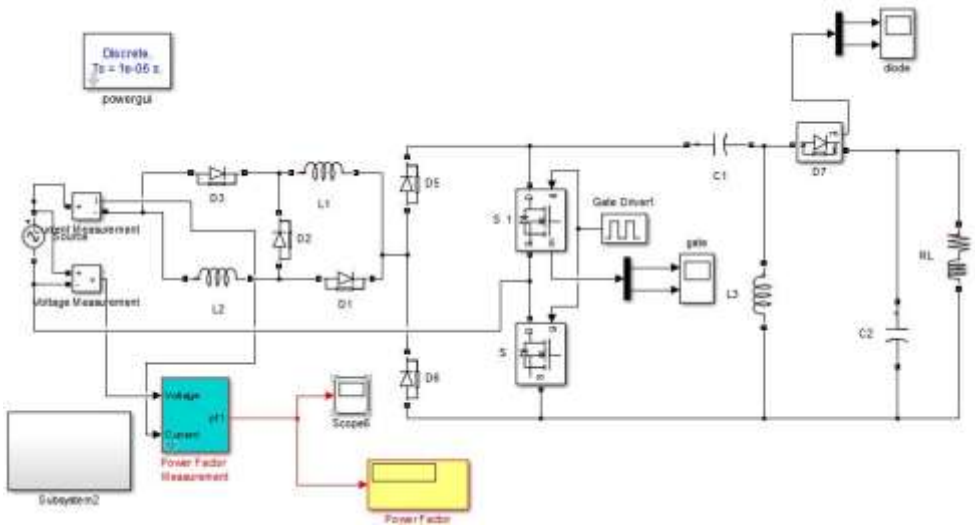


Figure 6. Simulink model for proposed boost Model

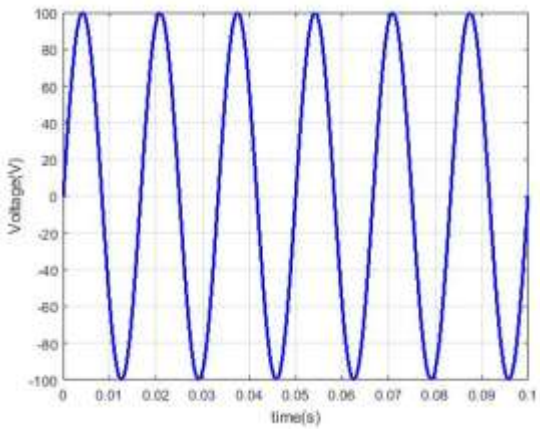
The performance of the converter analysis is presented with the various conditions. Then the THD and power losses are analyzed with the controllers. Initially discussed the base model of the conventional SEPIC model results is analyzed. Table 1 describes the implementation parameters of the proposed model.

Table1. Parameters of proposed method

Description of parameters	**Values**
Peak Amplitude	$100V$
Nominal Frequency	$60\ Hz$
Inductance(L1,L2,L3)	$1\times10^{3}\ H$
Capacitance(C1,C2)	0.03×10^{3}F
Resistance	$300\ \Omega$
Snubber capacitance	0.1×10^{-6}F
Snubber Resistance	$250\ \Omega$

Analysis of Proposed model

The input voltage of the converter is 100V and it is illustrated in figure 7. In the proposed model is used to achieve boost the input voltage of the converter.



Input voltage of the converter

Figure7. Analysis of input voltage in proposed model

Figure 7 shows the voltage across the intermediate capacitors C1 and C2 along with the input voltage and diodes current, the voltage also illustrated. The capacitor and diode are connected to the SEPIC converter. The presented bridgeless topology is implementing a boost-type circuit configuration because of its low cost and its high performance in terms of efficiency, power factor, and simplicity. The proposed model the capacitor voltages are analyzed in figure

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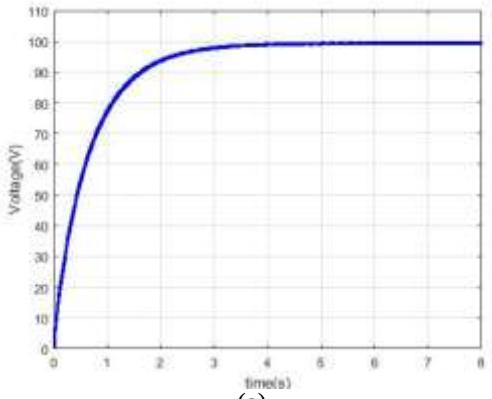
8. The capacitor C1 voltage is 100V and the capacitor C2 voltage is 300V. Initially, the voltage is increased 10v at 0.002s then it increased and it moves on the stable 100V at 8s. The same the 300V obtained in the linear variation. Comparing to the proposed model with the bridgeless SEPIC, it has several advantages such as the presence of one or two semiconductors in the current conduction path and reduced voltage stress across the semiconductor devices but it requires an isolated gate-drive on the same time, it has a complexity. So the proposed method is efficient with the boost configuration. The input voltage is 100V; the proposed model increases the voltage level up to 300V and decreases the loss and harmonics of the converter.

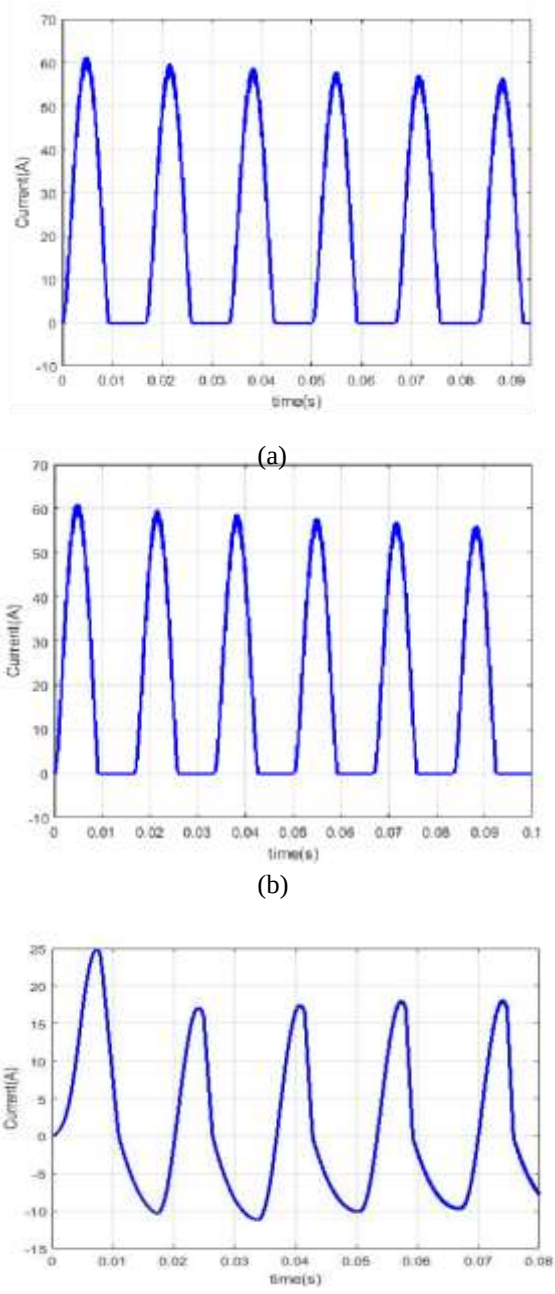


(a)

(b)

Figure 8. Analysis of (a) C1 voltage and (b) C2 voltage

An inductance reflects this dependence on the rate of change of the magnetic field; the proposed model inductance currents are analyzed and represented as pictorial in figure 9. In this stage, the three-inductor currents increase linearly at a rate proportional to the input voltage of the converter. The inductor L1 and L2 are varied linearly and maximum current is 60A, the L3 is varied at continues mode and the maximum current is 25V. Thus, efficiency improvement by using SEPIC based Bridgeless Single Phase AC–DC PFC Rectifiers relies mainly on the switching loss and THD minimization difference between the topologies of bridgeless, step down 3 and step-down 1.



(a)

(b)

(c)

Figure 9. Analysis of inductance current (a) L1, (b) L2 and (c) L3

The measured parameters are prescribed depend on the gate controlling pulse by the help of the PWM. The controlling pulse current and voltage is illustrated in the figure9. The gate current and voltage is linearly increased from the starting time seconds. The 0.7s the gate current is 2A and it is increased to 6A at 2s. Based on this it is linearly increased the current and voltage. In this modulation, there is an only one output pulse per half cycle. The output is changed by the changeable width of the pulses. The gating signals are generated by comparing a rectangular reference with a triangular reference. The frequency of the two signals nearly

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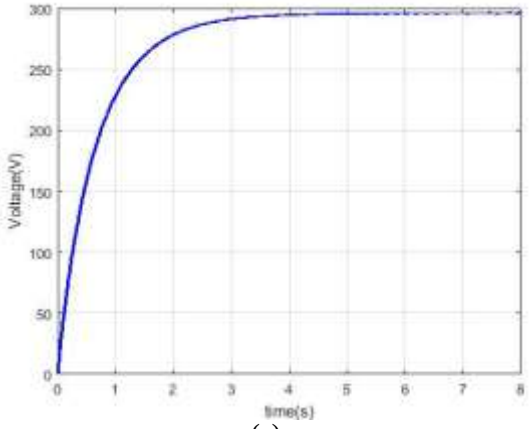
equal. Based on these controlling signals the switching loss and THD are minimized.



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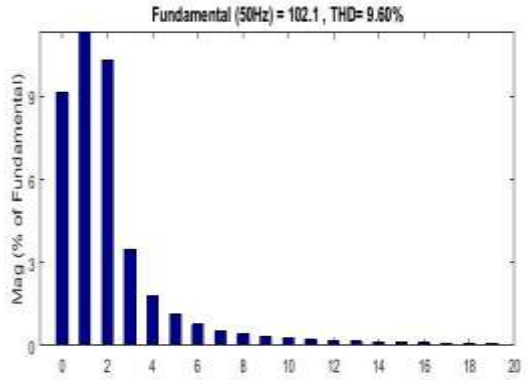


(b)

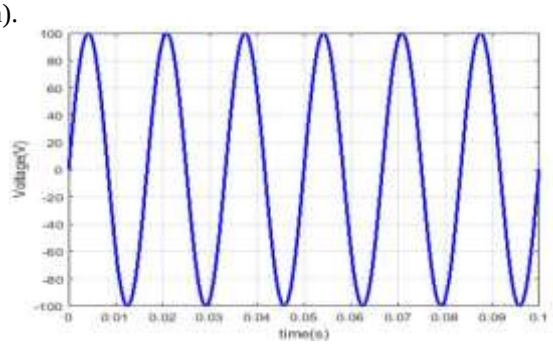
Figure 10. Analysis of (a) output voltage and (b) THD

Output voltage and THD of the proposed model is described in the figure10. The input voltage is a boost in the converter. Actually, the input voltage is 100V in the proposed model, it was improved to 300V. Then comparing to the other methods, it is efficient because it is improved the voltage level optimally with reducing the switching loss and THD minimization. In the same, the THD ratio also determined, the 9.60% THD present in the proposed model.

Analysis of Conventional SEPIC

In figure 11, the performance analysis of the input voltage and output voltage has been illustrated. Here the reference voltage is 100V at 0.1 seconds settling process. The output voltage is taking 130V at settled 0.3 seconds in figure 11 (b) respectively.

(a).



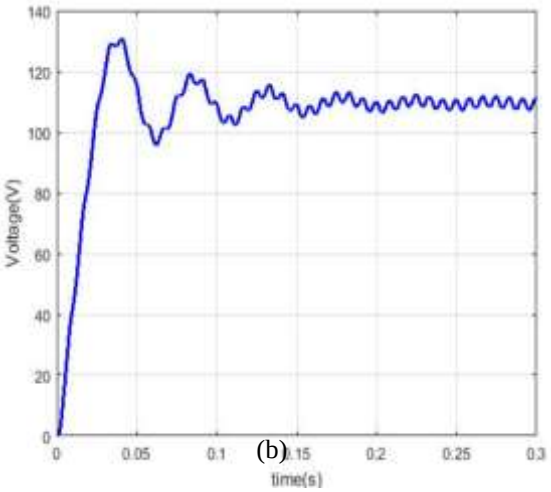


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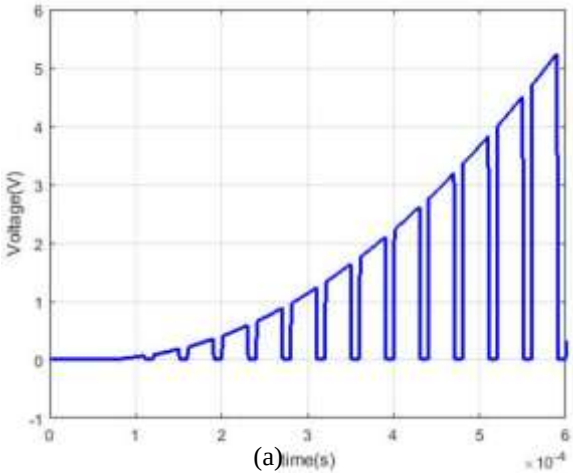
Figure11. Performance analysis of (a) input voltage and (b) output voltage



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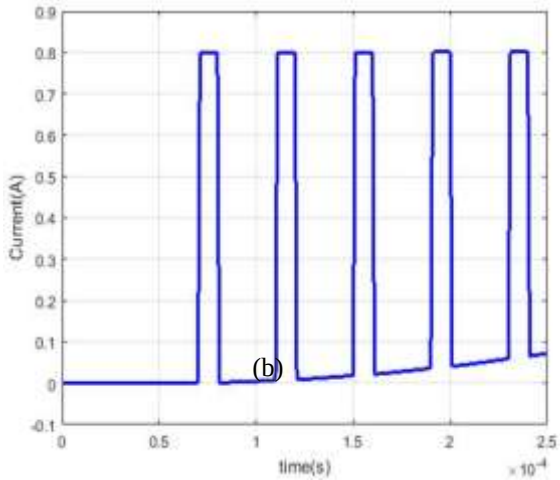

(b)

Figure12. Performance analysis of controlling gate pulse (a) voltage and (b) gate current

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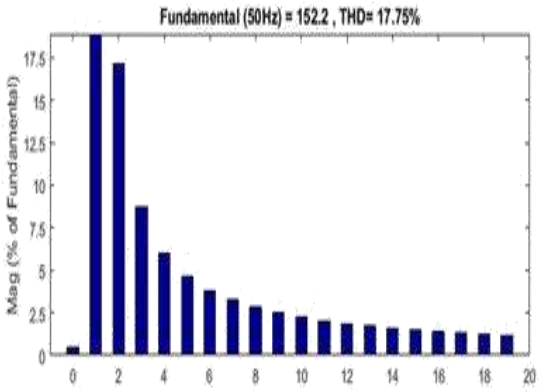
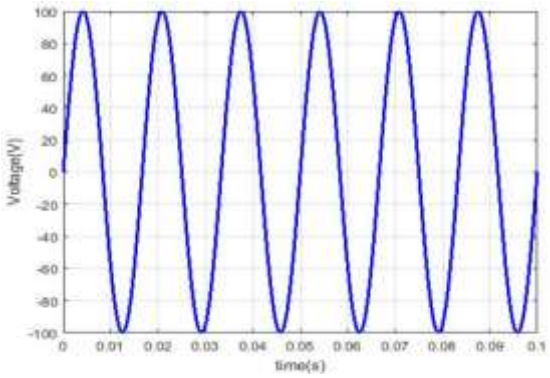


Figure13. Performance analysis of THD

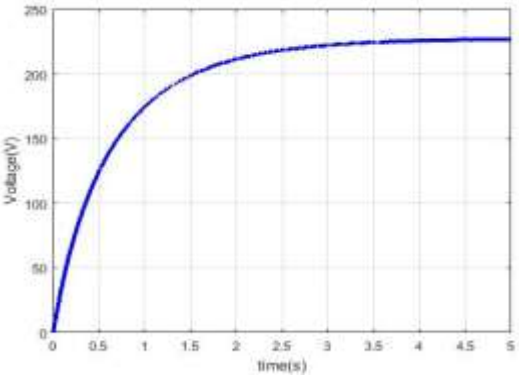
In figure 12, the performance analysis of gate voltage and current has been illustrated. The gate voltage is takes 5.1V and current is 0.8A at 2.5 seconds. From the figure 13 shows that the performance analysis of THD has been evaluated. The case-1 shows that the elimination of harmonic is 17.75% respectively. The performance analysis of case 2 has been described in the following subsection.

Analysis of bridgeless SEPIC

In figure 14 shows that, input voltage for case 2 has been analyzed. The input voltage is 100V at 0.1 seconds settling process respectively. In figure 14 (b), the performance analysis of output voltage in case 2 has been illustrated. The output voltage takes 225V at 3.5 seconds settling process

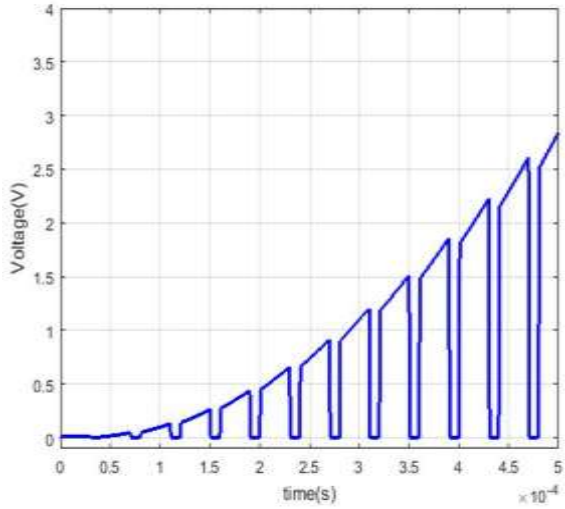


(a)

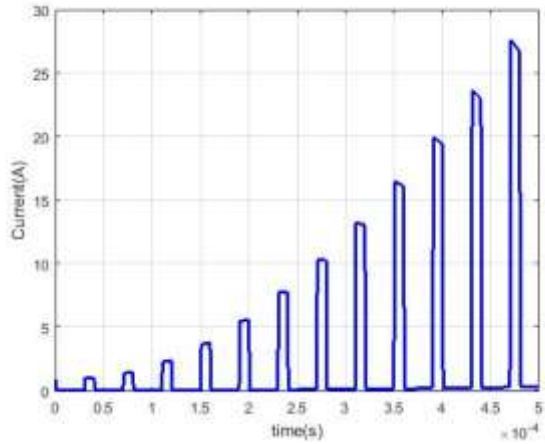


(b)

Figure14. performance analysis of (a) input voltage and (b) output voltage



(a)



(b)

Figure15. Performance analysis of controlling gate pulse (a) voltage and (b) current

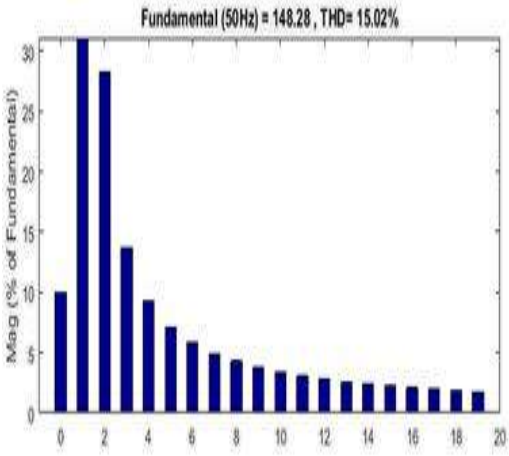


Figure16. Performance analysis of THD

From the figure 15, the performance analysis of the controlling gate pulse voltage and current has been analyzed. The gate pulse output voltage waveform is step by step increasing at 2.75V has been illustrated in figure 15 (a). The controlling gate pulse performance analysis of output current waveform takes 27.5A has been represented in figure 15 (b).

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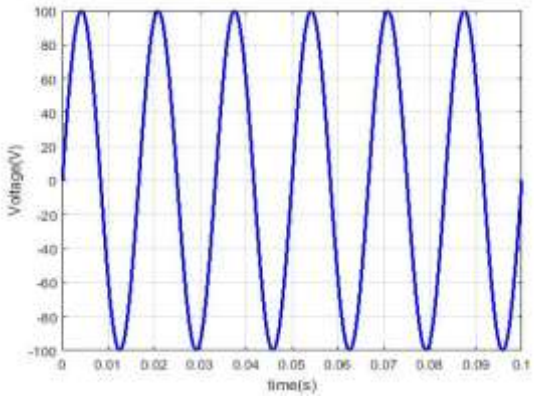
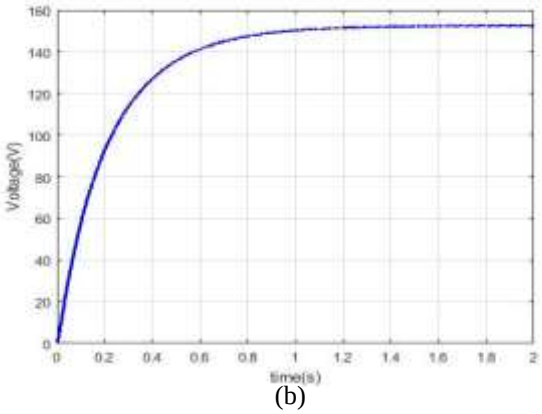
In the figure 16, performance analysis of harmonic distortion has been illustrated. The figure, 15.02% harmonic reduced for using the bridgeless converter. The performance analysis of the step down-1 has been explained in the following section.

Analysis of Step down-1 SEPIC

The input voltage and output voltage are portrayed in figure 17 which is the output voltage is step-up from the input voltage. From the case 3, the input voltage is 100V and the output voltage is 155V respectively.

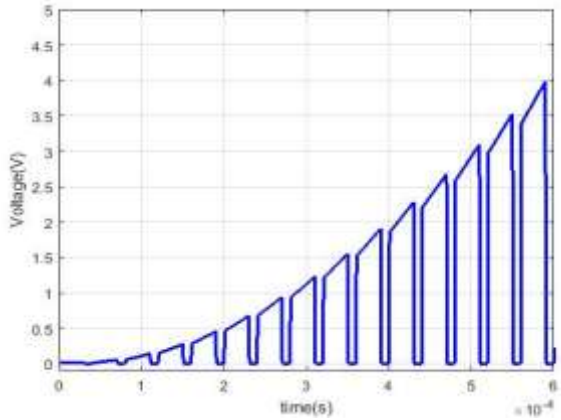


(a)

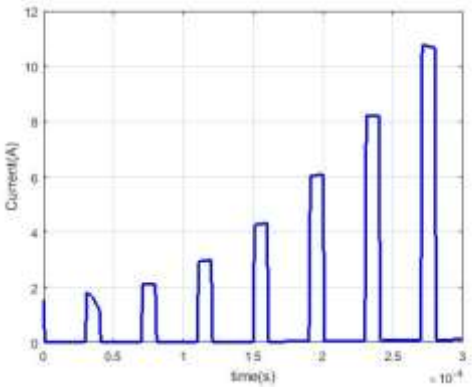


(b)

Figure17. Performance analysis of (a) input voltage and (b) output voltage



(a)



(b)

Figure18. Performance analysis of gate pulse (a) voltage and (b) current

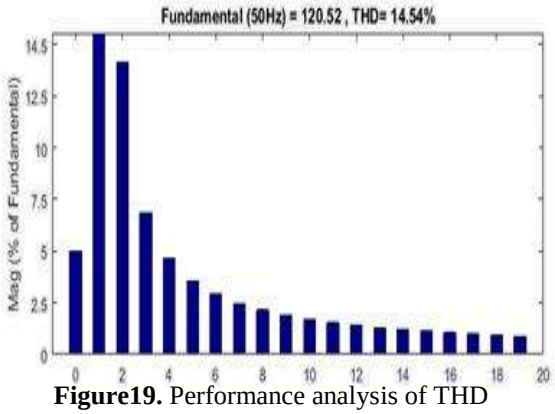
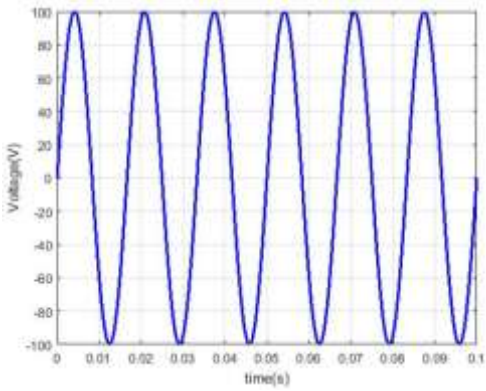


Figure19. Performance analysis of THD

From the figure 18, performance analysis of the waveform of gate pulse voltage and current has been represented. The above figure 19 shows that, the analysis of THD in case-3 has been illustrated. It shows, the case-3 has been minimum THD of step down-1 is 14.54% respectively. The performance analysis of the case 4 has been analyzed in the following section.

Analysis of Step down-3 SEPIC

In figure 20, the performance analysis of the input voltage and output voltage has been illustrated. Here the reference voltage is 100V at 0.1 seconds settling process. The output voltage is taking 120V at settled 4.5 seconds in figure 20 (b) respectively.



(a)

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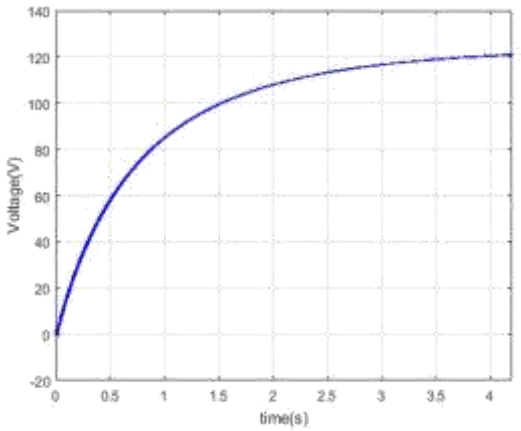
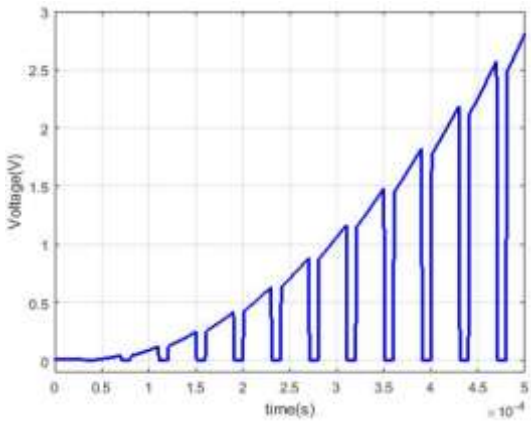
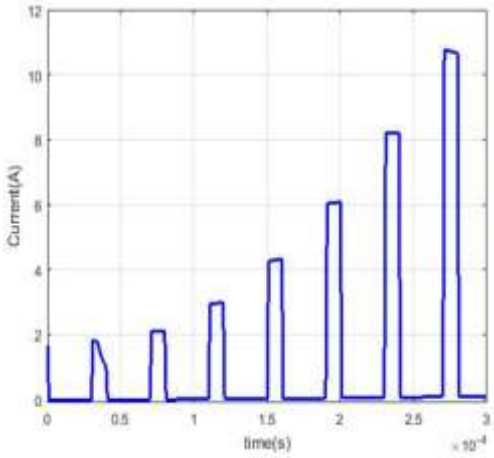


(b)

Figure20. Performance analysis of (a) input voltage and (b) output voltage



(a)



(b)

Figure21. Performance analysis of (a) gate pulse voltage and (b) gate pulse current

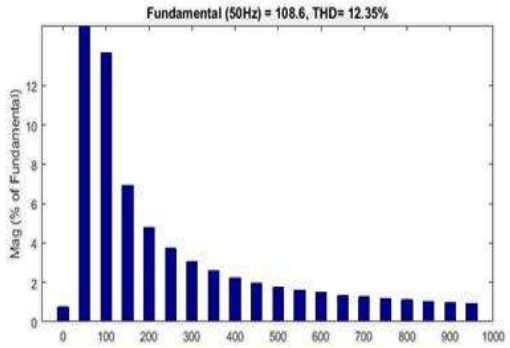


Figure 22. Performance analysis of THD

From the figure 21, the performance analysis of the controlling gate pulse voltage and current has been analyzed. The controlling gate pulse performance analysis of output current waveform takes 11 A has been represented in figure 21 (b). The measured parameters are proscribed depend on the gate controlling pulse by the help of the PWM. In the figure 12, performance analysis of harmonic distortion has been illustrated. The figure, 12.35 % harmonic reduced for using the step down-3 condition.

The comparison analysis of the proposed method with the other methods is briefly described in the below section.

Comparison Analysis

An efficiency comparison between the SEPIC based Bridgeless Single Phase AC–DC PFC Rectifiers with conventional SEPIC, step-down 3, step-down 1, the base model is performed based on simulation results. In this comparison, all methods are assumed to operate with the same operating conditions and parameters. The simulated efficiency presented in Figure 21, includes efficiency, power factor, and THD. In figure 21(a) denotes the comparison analysis of the efficiency proposed method with the other methods. The base model have the efficiency is 35-39 %. Then the step down 3 designs is reducing the switching loss and THD minimization with the efficiency is 38-40%. The same the other structures are have an efficiency is 49-51% and 70-72%. The proposed method is have 92-98% efficiency, comparing to the other methods it has a higher efficiency. The proposed method is analyzed with the power factor and THD. The power factor analysis, the base model, step-down 3, step-down 1, Bridgeless, proposed are 0.95, 0.96, 0.96, 0.97 and 0.99. Based on this analysis, the proposed model is having a higher value and higher efficiency.

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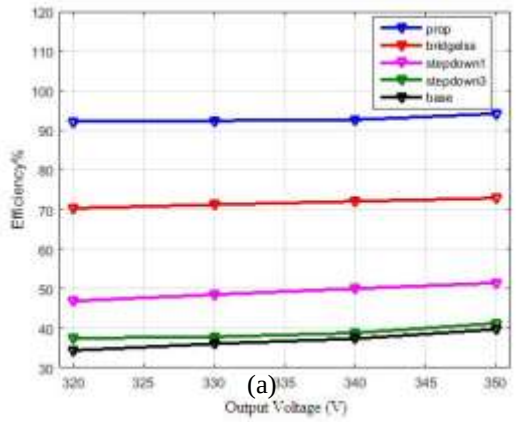
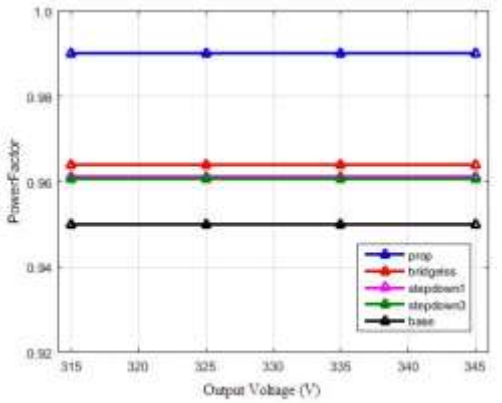
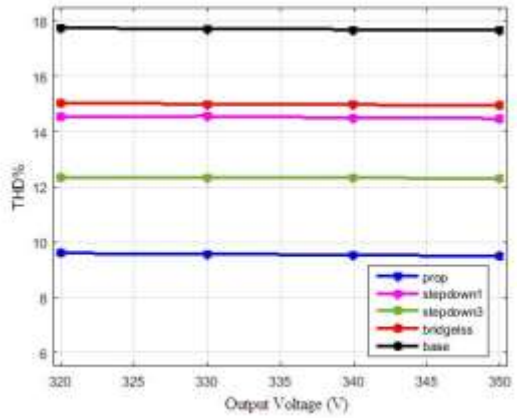


(a)



(b)



(c)

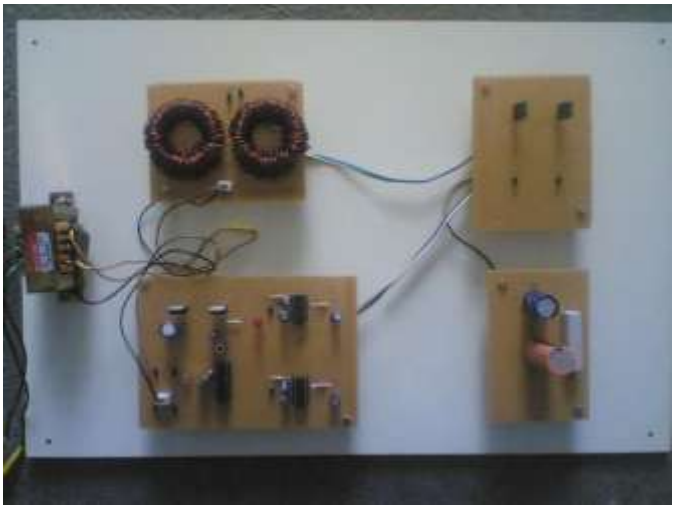
Figure23. Comparison Analysis of (a) Efficiency (b) Power factor and (c) THD

Figure 23 (c) shows the THD comparison with the other methods. The other methods are having a higher THD ratio comparing to the proposed model.

Table2. Comparison of efficiency, THD and Power factor

	Methods				
Performance	**Base**	**Bridgeless**	**Step-down 3**	**Step-down 1**	**proposed**
Power factor	0.95	0.965	0.96	0.96	0.99
THD in %	17.95	15	12.5	14.25	9
Efficiency	42	72	40	50	95

In conclusion in table 2 explicate the value of THD, Power factor and efficiency of four conditions. From the performance analysis, the proposed boost model is improved than the other bridgeless SEPIC converter models.



(a)

(b)

Figure 24 .(a) prototype model of boost converter (b)corresponding input and output voltage

Figure 24(a) shows the fabricated proto type model of the proposed boost mode sepic converter. This circuit includes three inductors, two capacitors, eight diodes and one unidirectional switch. Resistive load has been selected for this operation because this type presents highest harmonic distortion in the input side. Initially the circuit switch is ON and OFF respectively during positive and negative cycle of the supply.

Figure 24 (b) shows corresponding prototype model Input voltage which is 100v at 0.6 secs settling time and output voltage is shown as 120 v at settled 4.5 secs indicating the operation of effective boost mode of operation.

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5. Conclusion

Hence the PFC and voltage regulation of the proposed bridge less single phase AC-DC SEPIC converter was hold out and the performance analysis similar to PF, efficiency and THD was scrutinized and correlated. The conventional double-stage converter is customized to design the topology. The proposed converter shows indicative perfection in the conversion efficiency at extremely low voltage gains. The THD of the input current is set aside low but the input power factor to be very low. Consequently suitable feedback control is endorsed to recuperate the input power factor. An amalgamated method for developing hybrid converters by a high step-down/up conversion voltage ratio was spitball. The new hybrid converters prompt a reciprocal multiplicity with applicable quadratic converters, related voltage stresses on the transistors and diodes, and comparable conversion ratio as the quadratic converters for a few values of the duty cycle, some of the quadratic converters have the edge for other values and the new hybrid converters have a steeper step T down/up dc voltage ratio. Experimental results long-established that the proposed topology percolate with input sinusoidal currents, with no current sensors or a control loop strategy for this intention, foremost to a cost reduction, simplicity and robustness and it comes from the use of a simple control loop to regulate the output voltage as confirmed from the simulation results.

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