AN OPTIMIZED TWO INVERTER TRI STATE - LEVEL SENSITIVE SCAN DESIGN

[1]V. Suresh Kumar and Dr. R. Manimegalai[2]

[1]Assistant Professor, [2]Professor,
[1]Department of Electronics and Instrumentation Engineering,
[2]Department of Information Technology,
[1]Valliammai Engineering College, Chennai, Tamilnadu, India
[2]PSG College of Technology, Coimbatore, Tamilnadu, India
[1]sureshkumarv.eie@valliammai.co.in, [2]drrm.it@psgtech.ac.in

Abstract*—Scan design provides controllability and observability of internal state variables for the circuit under test and also converts a sequential circuit problem into a combinational one by partitioning the circuit in testing process. Scan design with multiple latches and multiple clocks emerge as a solution for clock skew, jitter issues in contemporary design. Later single-clock, single-latch Level Sensitive Scan Design (LSSD) emerge as the scannable cell for latches, in low power and high performance designs. Recently Tri-state LSSD (TLSSD) emerges with less number of transistors and offers less power consumption than original LSSD. In this paper, an LSSD scan cell which consumes less power and area compared with original single latch LSSD and Tri-state LSSD (TLSSD) is proposed. The proposed LSSD extension of TLSSD has better trade-offs between number of transistors, area and power of less than 28 % compared to the existing TLSSD.*

***Keywords*—** *Scan Design, DFT, LSSD, SRL*

I. INTRODUCTION

Scan based design serves as the foundation for Design For Testability (DFT). The fundamental Shift Register Latch (SRL) introduced four decades ago by the Level Sensitive Scan Design (LSSD) survived in its original form over the years. Several other scan designs such as random access scan and test generation techniques have been proposed. Usage of multiple latches and multiple clocks are the common design aspect in all the proposed designs. Later the single-clock, single-latch LSSD [4-7] comes to existence. Later it is replaced by TLSSD (Tri-state LSSD) [1] which consumes less power and area compared with single latch LSSD [2-3], becomes the popular scan design nowadays. The aim of this paper is to design an LSSD scan cell, which consumes less power and area compared with original single latch LSSD and TLSSD. DFT is an approach which makes subsequent testing easier. Embedded system testing problems are multitude and unique in nature where no single methodology provides the solution. Same is the case with DFT, in providing solution to all kinds of circuits. There are two broad approaches pertaining to DFT techniques – ad-hoc techniques and structural techniques. Scan design provides controllability and observability of internal state variables for circuit testing. A sequential circuit problem gets converted to a combinational one with the help of a scan design with full controllability and observability. Scan based approach helps in partitioning huge circuits into simpler ones. Appropriate design rules and test structure needs to be the major factor in scan design. Test control pins are provided in the place where the primary inputs are applied. It requires availability of at least one primary input pin for testing. The primary input pins also control the clock pins of the flip flop. There are no gated clocks as it is necessary for flip flops to act as scan register. Flip flop, in most of the verified designs, are not of the usual type, rather are scan flip flops (SFF). During testing, SFF act as a shift register with known input being fed and the output easily checked. SCANIN and SCANOUT denote the two flip flops respectively connected to input pin and the output pin. D type master slave Flip flops are employed forming a chain making them work as shift register. All clock inputs to flip-flops must be controlled from primary inputs (PIs). The design is prone to Race condition if Clocks feed data inputs [8-10]. MUXed Scan, Scan-Hold Flip Flop, Scan set, Scan path, Serial scan, Level Sensitive Scan Design (LSSD), Random access scan are some of the variations of scan based approach. Two latch, three clock based faster and

simplified hardware based SSD approach eliminates races and hazards. Rise time, fall time, and delay remain ineffective in SSD based approach. The superiority comes in handy only when certain design rules are followed like insensitivity of steady state response to in-circuit delays. The order of input change should not affect the response. There is a slack time which does not compute the combinational delay during transparent state. Latches save time by borrowing time from the previous and later stages of pipelining resulting in minimum clock period. Flip flop poses restrictions in using borrowed time to make up for the delay, hence latch based design results in lesser power consumption [3]. Replacing flip flops with level sensitive latches becomes a straight away option. The latch based design goes with certain constraints, the system designed with such an approach results in level sensitive logic subsystem [2]. A pair of low active and a high active latches make up for the single flip flop without changing the functionality of the circuit. The pair of latches, placed one after the other, is driven by the same clock. This is referred to as the single phase latches scheme [4].The time borrowing nature of the latches and its immune to clock skew makes it an ideal choice to improve the performance of the logic blocks and to work at higher clock frequency [5].

The rest of the paper has organized as follows. Section II deals with the different single latch LSSD. The mathematical model of two inverter LSSD disused by using CMOS logic is detailed given in Section III. In section IV, the simulation results of the proposed TLSSD clearly displayed with valid result shown. Finally, the conclusion has been made from the simulation result.

II. SINGLE LATCH LSSD (ORIGINAL LSSD)

A level sensitive logic circuit has to ensure certain conditions to be referred to as level sensitive logic system. The steady state response – response of the circuit when all the input activities are ceased – is independent of the in-circuit delays and is immune to the order in which the inputs are changing when more than one inputs are involved. Only allowed input changes ensure the level sensitive operation. Fig. 1 shows the Shift Register Latch (SRL) based Single latch LSSD proposed by Eichelberger and Williams [2], Here C and D specifies the functional input pins while A, B and I are the test input pins. There are two modes of operation – functional mode and test mode. During the functional mode, output Latch L1 registers the data from D when the input C is high. The test mode takes place in two steps. Latch L1 gets the data registered from I in the first step and A must be high during this step. Latch L2 gets the data from L1 copied during the second step and B must be high during this step, characterizing a master-slave behavior.

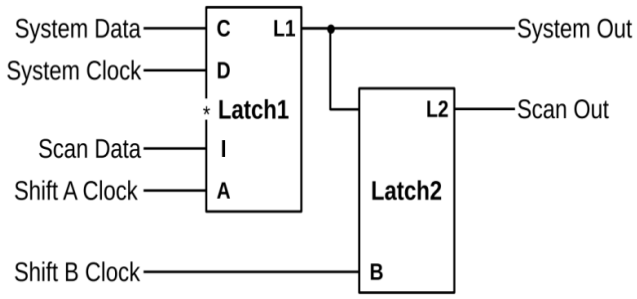

Fig. 1Single Latch LSSD Using Shift Register Latch

a) LSSD based Scan Chain Organization

The LSSD scan cell is used to test the lager combinational logic circuits. LSSD were fixed in the various places of combinational logic to check whether the combinational circuit is working based on the functionality.

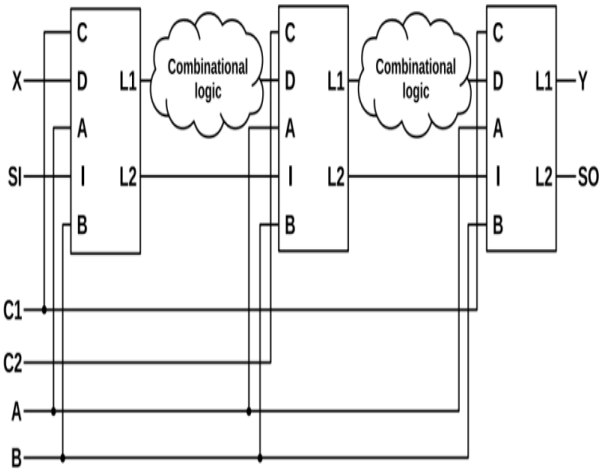

Fig. 2 Latch Based Scan Chain Organization

Fig. 2 illustrates LSSD working as standard latch and as master-slave during the functional mode and test mode respectively. LSSD cells forms a scan chain here, as L2 is connected to I of the next register. Here L1 is used as functional output.

b) Gate level schematic of LSSD

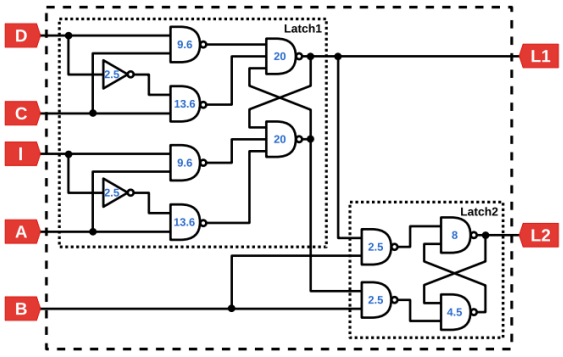

Fig. 3 Gate Level Schematic of Original LSSD

LSSD [2] is shown in Fig. 3. A total of 48 transistors is needed for 2 inverters, 8 two-input NANDs, 2 three-input NANDs to make up the LSSD. The cross-coupled

NANDs employed causes problems pertaining to transistors sizing and electrical cell characterization. As few logical nodes feed 3 nodes and 2 nodes – 3 inputs NAND connected to L1 and 2 inputs NAND to L2 respectively – there arises complexity due to cross coupled NANDs in the logical effort calculation owing to high input capacitance. Transistor size and the consequent cell area increases due to high input capacitance. Also the cross couple NANDs create problems like cross wire routing and difficulties in defining hold and set up time due to feedback delay.

Table. 1 Truth table of Original LSSD

D	C	I	A	B	LATCH 1	LATCH 2
X	0	X	0	0	-	-
0	1	X	0	0	0	-
1	1	X	0	0	1	-
X	0	0	1	0	0	-
X	0	0	1	0	0	-
X	0	1	1	0	1	-
X	0	X	0	1	-	L1

c) Tri-State LSSD

The existing LSSD proposed by Leonardo Rezende Juracy et al.,[1] is based on inverters and Tri-state inverters, hence it is also known as TLSSD. Fig. 4 shows the high speed and most energy efficient topology of the Tri-State Inverter Logic (TLSSD) cell. The TLSSD uses 12 transistors less compared to that of original single latch LSSD, which uses 48 transistors. Four transistors used at each tristate inverter, two transistors at each inverter, six transistors at the tristate inverter with the specific function logical OR between C and A make the total number of transistors as 36. The TLSSD (0.97075 μm^2) occupies just half of the total area occupied by the original LSSD (1.97375 μm^2).

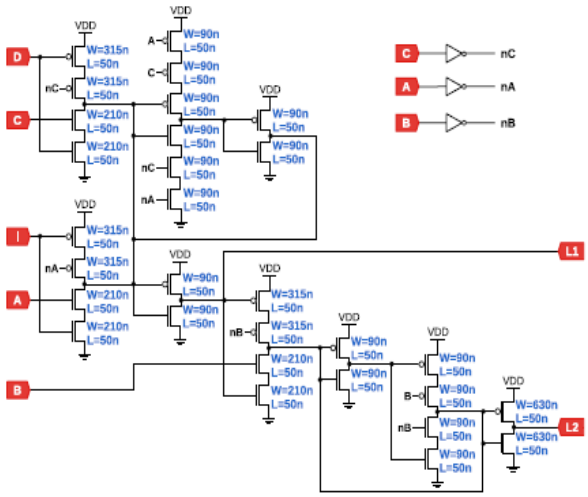

Fig. 4 LSSD Using Tri-State Inverter Logic

TSLLD has many features worth mentioning. The set up and hold times are easily measured due to absence of unpredictable transitions in the array making the electrical characterization simpler. Also the absence of cross coupled NANDs makes the transistor sizing simplified and transistor area smaller. One third of the transistors in TLSSD are present in the feedback loop. The transistors in the feedback loop do not drive loads rather only store data, thus making them minimum sized. This makes the TLSSD to consume lesser power and occupy minimum area. This strategy is seen in the design of cells of conventional libraries. Even though the transistors are minimum sized, problems due to static noise are lesser pronounced. Transistors sizing at the output and the input are carefully carried out. The one that drives the output is designed to handle the strength to drive the output load. The one that is present in the input are designed as an amplifier to recover the signal from noise. For designing the series of transistors, logical effort techniques are employed. When there is a cross coupling, as in LSSD, the design is no longer simpler. TLSSD employs logical effort approach as there is no cross coupling in the configuration. Exhaustive simulations are also used sometimes to size the transistors.

III. PROPOSED SYSTEM – TWO INVERTER LSSD USING CMOS LOGIC

Two Inverter LSSD logic attempts to reduce the size by reducing the number of transistors to implement a given logic function.

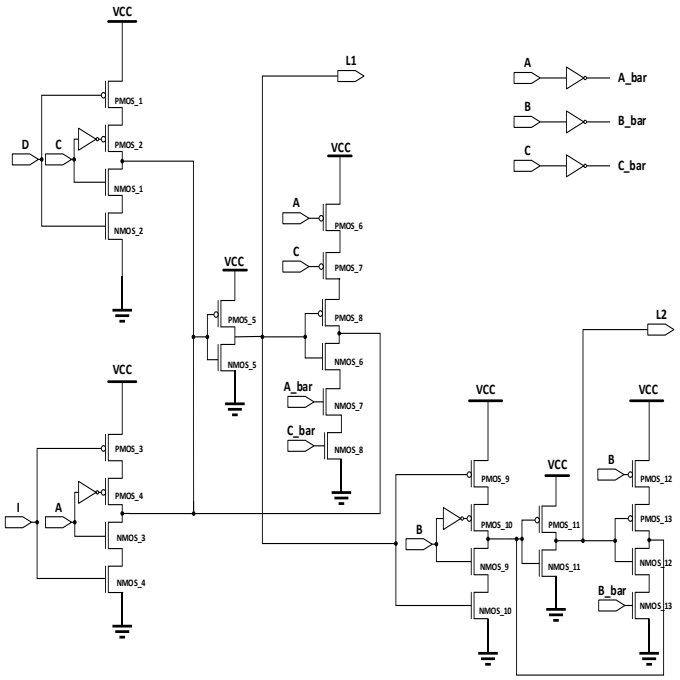

Fig. 5 Proposed Two inverter LSSD

Fig. 5 shows the proposed LSSD design using two inverters. Transistor PMOS 1 to 8 and NMOS 1 to 8 form the two inputs Latch. The input D and I are controlled by the clock C and A respectively. The clock C and A are non-overlapping clock. Clock C sample the regular input and clock A samples the Test input. When C=1, Transistor PMOS 2 and NMOS 1 are turned ON and based on the D input, either PMOS 1 or NMOS 2

turns ON. Similarly in test input circuit, clock A and input I are used to pass the testing input. In the proposed two inverter based LSSD, 20 transistors are used to construct first Latch (L1) whereas in TLSSD proposed in 2017 [1] uses 22 transistors. This reduction of two transistors is achieved by rearranging the inverter used in existing TLSSD design, without altering the functionality of first LSSD. In the existing TLSSD, the output of first stage (L1) is taken after two inverter stages. But in the proposed design, the inverter is eliminated by the rearrangement of feedback circuit which results in reduction of two transistors. The second latch (L2) is used to forward the regular input or testing input to the next stage and it is controlled by clock B. The tristate buffer in the second stage is used to form the feedback circuit. To deliver the second stage output (L2) the existing TLSSD design uses 14 transistors whereas the proposed design of two inverter LSSD uses only 12 transistors. Two transistors are reduced in the second stage by eliminating one inverter. Hence the proposed design of LSSD uses only 32 transistors which is four transistors less, compared to the existing TLSSD using Tri-State Inverter Logic. Due to reduction of four transistors the area, power and delay of LSSD design is reduced to considerable level.

IV. RESULT AND DISCUSSION

This chapter deals with comparison of original LSSD [2], the existing TLSSD [1] and the proposed optimized two inverter based LSSD. All these LSSD designs are implemented using Tanner tool in FREEPDK-45nm technology. Design metrics such as area and power are also calculated for 45 nm technology. The area consumed by the circuit is calculated using layout design in glade tool.

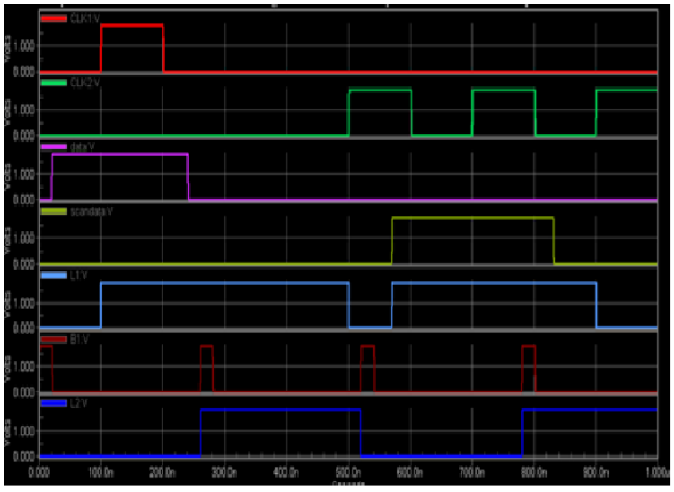

Fig. 6 Simulation result of two inverter LSSD

The functionality of circuit is verified by simulating the circuit and the result is shown in Fig. 6, which shows that the circuit is working properly. Here A is shift A clock, B is shift B clock, C is system Data, D is system clock, I is scan Data and all these parameters are input to the LSSD scan cell. L1 and L2 are the Latch 1 and Latch 2 outputs respectively. The Fig. 7 shows the propagation delay involved in the proposed two inverter based LSSD.

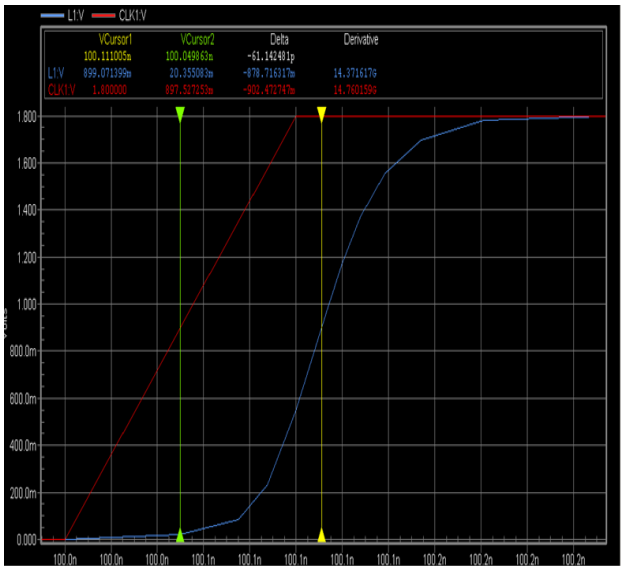

Fig. 7 Result of delay calculation

By using this layout, the area consumed by the circuit is calculated. The area consumed by the proposed LSSD is 0.5980 µm2.

Table 2 Comparison based on Area, Power and Delay

Description/Type	LSSD [2]	TLSSD [1]	TILSSD
Number of transistors	48	36	32
Area in μm^2	1.9735	.97075	0.5980
Power (uW)	0.1750	0.1334	0.12698
Delay (ps)	-	-	61.142
ADP	-	-	7.78×10^{-18}

Table 1 provides the number of Transistors, Area and Power consumption of original single latch LSSD [2], TLSSD [1] and proposed Two Inverter LSSD. From the table it is evident that the proposed LSSD design requires only 32 transistors which are 22% lesser than TLSSD and 33% lesser than original LSSD design. This reduction of number of Transistor reduces the Area, Power consumption and Delay. The Fig. 8 shows the comparison chart of power consumption of various LSSD design. The graph shows that, the proposed LSSD design consume 28 % lesser power than original single latch LSSD and 4 % lesser power than the Tri-state inverter based TLSSD. The Fig. 9 shows the comparison of the area occupied by the various LSSD design. It is evident from the graph that the proposed design consumes 36 % lesser chip area than the TLSSD [1] design proposed in 2017 and 70 % lesser chip area than that of original LSSD [2].

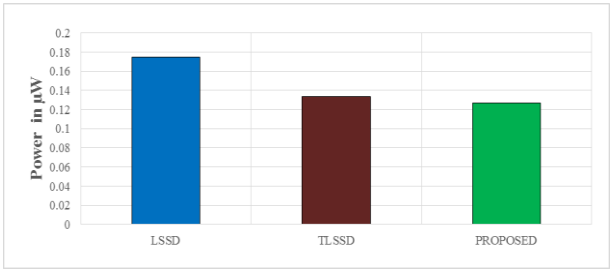

Fig. 8 Comparison based on Power Consumption using Various Design Methodologies

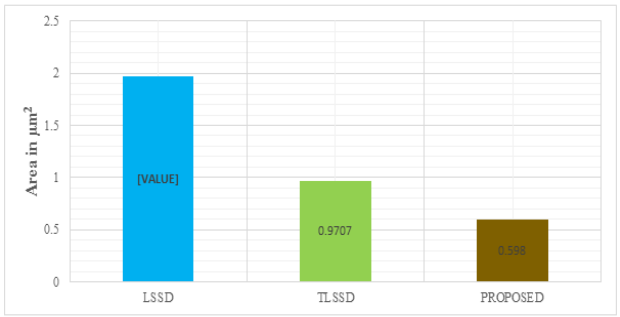

Fig. 9 Comparison based on Area Occupied by Various Design Methodologies

V. CONCLUSION

The proposed two inverter based LSSD design uses 32 transistors compared to 36 transistors in TLSSD, resulting in 22 % reduction in no of transistors. The TLSSD Scan cell spans 0.97075 µm2 area where as the proposed LSSD spans 0.5980 µm2 area, resulting in 36% less silicon area. Also the proposed design consumes 0.1268 µw power compared to 0.1334 µw powers in TLSSD which comes to 28% less power. Hence the proposed, Two inverter based LSSD design is more efficient in terms of number of transistors, Area and Power. The future work will be based on implementation of LSSD scan chain using efficient LSSD Scan Cell.

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