APPLICATIONS OF ZIGBEE SoC WITH LOW POWER BASED ON FULL SWING GATE DIFFUSION INPUT

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Abstract- *ZigBee system-on-chip (SoC) is an essential module in all advanced wireless communication devices and it is the alternating advanced technology over the conventional Bluetooth technology. System on chip (SoC) is to develop complex network products fastly, easily and reliably which enable the end-users. A new implementation technique of efficient Xnor delay based encoder using full swing Gate-Diffusion-Input (GDI) technique is presented. Xnor circuit is the most energy efficient and very suited to low voltage application designs. This full swing GDI based encoder design allows reducing power and delay of the circuit, while maintaining low complexity of logic design. It minimizes the number of bit "1"s in modulated bit stream without losing information combined with full swing GDI logic style. Performance analysis is based on delay and power dissipation, advantages and drawbacks of full swing GDI encoder.*

Keywords: *Gate-Diffusion-Input (GDI), encoder, power dissipation, ZigBee SoC, circuit delay.*

I. INTRODUCTION

In short range wireless communication systems have turned out to be prevalent in our day to day life. To name a few, Wi-Fi ZigBee, Bluetooth, RFID, UWB etc. have worked wonders in several domains including security, medical care, vehicular communication and consumer applications. ZigBee standard was particularly developed for cost effective functions of minimize the rate of data in wireless networks with consuming low power. The ZigBee is used to reduce the cost of implementation. The minimum demands to meet ZigBee specifications are compared to other standards such as IEEE 802.11 (Wi-Fi) and Bluetooth. This reduces the complexity and implementing cost of ZigBee compliant transceivers. This feature of ZigBee enhances the application in wireless sensor network for gathering details from various sensors such as temperature, humidity, pressure and other physical parameters. ZigBee is the only standards-based technology that addresses the unique needs of most remote monitoring and control sensory network applications. These technologies employ various physical layer protocols for encoding the information bits. Different standards support different encoding mechanisms present in wireless technology. These include Manchester encoding, Differential Manchester encoding and FM0 encoding. Manchester encoding have another name called phase encoding (PE), which encoding process of the each bit is either low and then high or high and then low. PE has no DC component so electrical connections are galvanically isolated. Differential Manchester encoding is also a line code, data and clock signals are combined to synchronizing data stream. In this encoding scheme does not consider logical 1 or 0 is received, but it is only based on the polarity is same or different. FM0 encoding technique is also known as Bi-phase space encoding, it must demonstrate a transition between before half cycle of the clock and later half cycle of the clock.

SHORT RANGE COMMUNICATION (SRC) CODING AND MODULATION TECHNIQUES

In SRC system, the modulated data is transmitted between the transmitter and receiver. In order to increasing the efficiency of the system, the data is encoded before being modulated. In general, the Manchester and Miller codes can be applied to telecommunication sector and are often used in the SRC system. Figure 1 shows block diagram of a SRC system contains the following blocks such as cyclic redundancy check (CRC), encoder, and modulator. The control circuit is used to monitor the above block and antenna is used to receive various signals and then transmitted through SRC system.

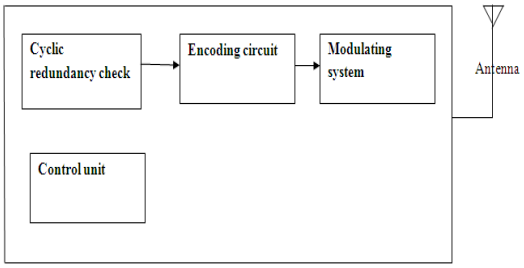

Figure.1 Structure of SRC system

The logical values '1' and '0' in a binary system can be coded in various forms. The SRC system commonly uses one of the following encoding methods: Non-Return-to-Zero code (NRZ), Manchester code, FMO, and Miller code. NRZ is a binary code, one represents a positive voltage and zero represents negative voltage of the signals but it does not go to neutral or rest condition. Manchester code figure 2 shows that the transition started at the middle of each bit period and transmissions are started at the start of the period, but it is done by depending on the information to be transmitted. The transition of middle bit direction is denoted as the data. In that transitions at the particular boundaries have not any information.

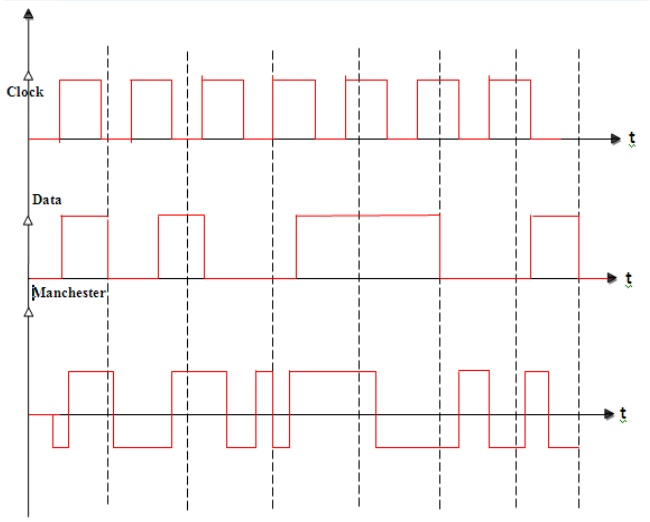

Figure.2 Manchester encoding scheme

The modulation methods are present in SRC systems are amplitude shift keying (ASK), phase shift keying (PSK), on-off key (OOK) and orthogonal frequency division multiplexing (OFDM). Generally, the transmitted signal waveform is expected to have zero mean for strength problem in when using ASK and less number of ones for transmission power reduced consumption when using OOK modulation. OOK is mainly popular in battery-operated portable and control applications, it can save on transmit power and also low implementation costs.

In OOK modulation, the transmitter is sending bit "1"s maximum power is mostly consumed. We proposed XNOR-Delay based encoder decreases the number of bit "1"s in transmitted sequence without losing information based on above strategy. After transmission of data, the encoded bit-stream can be recovered easily using an XNOR-Delay decoder at the receiver. XNOR delay based encoder system clock synchronization between the transmitter and the receiver can be reached using an FSK-OOK modulation which can be transmitted asynchronous UWB signals. Figure.3 shows, when logic zero the transmitter goes to idle state, which helps to conserving battery power in OOK modulation.

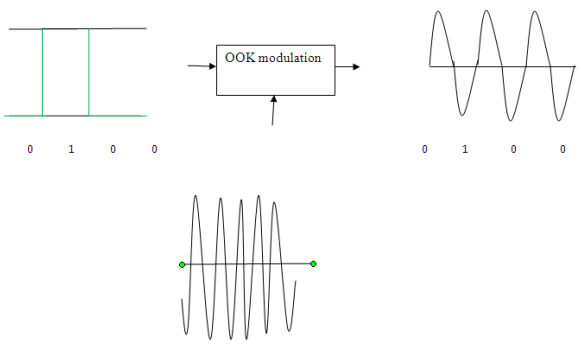

Figure.3 On-Off Key modulation scheme

In section II contains the various information about encoder design and gate diffusion input related different project strategies. In section III shows that GDI based encoder design can be implemented stage by stage. In section IV have details about comparison between various physical parameters for proposed project and other related information. In section V have the overall project details and further development information about the proposed work.

II. RELATED WORK

Soumya Roy [1] et al proposed a ZigBee communication based short range health monitoring system is analyzed. ZigBee technology has great challenge for its acceptance in short range applications due to some important features like reliability, low latency, high security, low power, interoperability and inexpensive implementation technique. MSP430 microcontroller based wireless ECG monitoring system is indicated which is used as wireless receiver like Telegesis ETRX1 ZigBee module. In this paper, structure of ZigBee module single packet transmission contains synchronous byte, packet serial number, compressed data bytes, error checking byte. **N. Javaid [2] et al** proposed, using ZigBee communication systems monitoring and controlling power. ZigBee is an important role in diagnosing and load controlling for efficient power utilization. It occupies suitable area is needed for communication and it operates only on low data rate of 20$Kbps$ to 250$Kbps$ with minimum power consumption. This paper describes the user friendly home application control, power on/off through the internet, PDA using Graphical User Interface (GUI) and through GSM cellular mobile phone. In this paper contains the power utilization, power organizing and power controlling architecture for power saving purpose. **Marcos Tomio Kakitani [3] et al** proposed an energy efficiency of forward and an amplify repetition codeing in short range communication systems. In short range transmission in a wireless sensor network are typically powered by batteries, so that they are limited energy. In addition, battery's capacity presents a latest growth if compared to the capacity and wireless throughput gains obtained in the previous decades. Thus, the energy consumption is important role in wireless sensor networks. In this paper, various sensors are being processed based on energy efficiency in short rage communication systems. These sensors can operate under cooperative decode-and forward with repetition coding (RC) or parallel coding (PC), and cooperative amplify-and-forward (AF) protocols. AF offers best efficiency because relay is very close to destination. The single hop transmission can perform the cooperative techniques for high spectral efficiency values, and also when the target outage constraint values assumes become high. **A. Karagounis [5] et al** proposed a Manchester code generator with CMOS switches range at 90nm and running frequency at 2.4GHz and 5GHz. In this code generator NMOS switches are presented. In this generator 26 transistors are being used. The main advantage of this project is use of clock signals are operating at same frequency. This output results will change from raising edge of the clock and falling edge of the clock. The circuit has similar behavior as fixed D flip-flop but it does not need of resetting the starting stage. In this paper, the proposed stage is Manchester encoder principle and then analyzes the transistor characteristics. This code generator has 26 transistors and 6 NMOS switches running frequency at 2.4 GHz and 5 GHz without changing the size of transistors. According to this paper simulation results a correct behavior up to 5 Gbit/s data rate is achieved. This result showing the correct operation of the switches and the high wideband function of the specific encoder. The transistors are being proper

identified and dimension also to be predicted for better propagation time and duty cycle above 5 GHz. **P. Benabes [4] et al** proposed 1 GHz operating frequency running of a Manchester code generator. 32 transistors are being used in this generator and also it has same complexity used in optical communication systems. In this system clock frequency is operating at same. The behavior of system is up to 1 Gbit/s data rate with a 0.35 micro CMOS technology. In data transmission, magnetic recording, and fiber optic data links modulation codes are widely used. In this paper, encoder is composed with an inverting latch and also non inverting latch in parallel combination and also it have three state buffers. This paper delivers the information about behavior of edge-triggered D flip-flop, except the output is being inverted. In optical communication systems, the cell is being implemented and will be part of a chip conditioning.

Yu-Cherng Hung [6] et al proposed a Manchester ad miller encoder used to design for high speed CMOS chip manufacture. It can operate only in high frequency and data throughput will be improved. In hardware design the number and size of the transistor being reduced. Average power consumption of the circuit under the room temperature is 549 microwatts. In radio frequency applications this circuit can be easily manufactured. In this paper contains the following operations like parallel operation and hardware sharing mechanisms. This paper gives the information about modified Manchester and Miller CMOS encoder scheme. **M Ayoub Khan** [**7] el al** proposed based on Manchester encoder for tag emulator to design for a finite state machine (FSM). The behavior of tag emulator is imitating the UHF RFID (radio frequency identification system) tag emulator. It acts as a general purpose data transport devices for different RFID systems. FSM and RTL implementation encoder is motivated by RFID. The FSM synthesis design is efficient because it can occupy less area and high speed. It operates at a high frequency of 256.54 MHz. RFID is used to capture the data systems and these captured datas are being stored on silicon chips which are tagged with the target. In this paper the whole circuit is designed using verilog hardware description language. The stages of this project are over sampling technique, detection and analysis. **Satoshi Shigematsu [9] et al** proposed **a** power-down application circuits used a 1-v high speed MTCMOS (multithreshold-voltage CMOS) circuit scheme. It is mainly concentrate on speed, ultra low power large scale integrators for battery driven portable component. It achieves a low threshold voltage and a smaller leakage current. It has a feature like MOS transistors have both high and low voltage on single chip. The major advantage of this project is a small, fast, low-power balloon circuit for preserving data. It is very efficient circuit for high performance applications. **Lawrence T. Clark [10] et al** proposed to reduce circuit and control complexity using low standby power flip-flop. In the semiconductor manufacturing the battery performance is not being improved. In this circuit have a master-slave flip-flop which is used to reduced power of the entire circuit. Final stage is to reduce the storage latch power supply voltage and it can be used to control the drain to big band to band tunneling leakage component.

Hamid Mahmoodi-Meimand [12] et al proposed to retention of data in flip-flop for power-down applications. Cross coupled invertors is to store a data in flip-flop. In power down mode it can hold the data with various states. In this project 16-bit shift- register is used to retention of data and it can be fabricated and tested in a 0.25 micrometer. It does not need any extra latches, so it can minimize the area, power and delay penalties for data retention. **M Ayoub Khan [8] et al** proposed a finite state machine based FM0 and miller encoder is used form ultra high frequency RFID tag emulator. This technology is used in data capture system automatically. RFID are low frequency range 125 KHz to 123 KHz, high frequency range 3MHz to 30MHz, and ultra high frequency 300MHz to 1GHz used in data capture systems. The tag data in EPC format is generated by tag emulator. In this paper, the implementation result efficiency will be improved. **Victor Zyuban [11] et al** proposed a scan retention mechanism in low power integration. In this paper mainly concentrated

on power and area overhead and also it have various common latch style. They proposed on different power gating techniques are used because reducing leakage during sleep mode. The power and performance are calculated exactly and extracted various layouts built in a state. This scan mechanism is very small and main feature is data retention mechanism. **Gugulothu Saida [13] et al** proposed a low power BCD adder implementing by using gate diffusion input cell. The major important factor in this paper is to reduce power consumption. It deals with low power, full voltage swing addition. The designing of the buffer is to get the full voltage swing that is high level is logic '1' and low level is logic '0'. This method is only concentrated on low power circuits design. It operates on levels of low voltage and speed is very less at the output. **H. Partovi [14] et al** proposed a latch and edge triggered flip-flop flow through hybrid elements. The timing methodology is aimed in this paper such as hybrid latch- flip-flop for reducing latch latency and clock load. There are following logics are used in this paper like static logic, dynamic logic and self resetting logic. **Jiren Yuan [15] et al** proposed to improve the speed and power consumption using new single-clock CMOS latches and flip-flops are used. In the advantages of speed, the new differential flip-flops are being used and also clock loads are minimized. In this paper TSPC flip-flops are used to reducing power and increasing speed of the system. **Arkadiy Morgenshtein [17] et al** proposed a efficient use of power method for digital combinational circuit using gate diffusion input. This technique is used to minimize the power consumption, delay, and area. In this paper various models are being concentrated and to decreasing the power. **Sohan Purohit [16] et al** proposed an implementation on full adder performance based on impact of logic circuits. In this paper dynamic logics are being used and also it has 12 full adder circuits and it is in split path data driven. In this paper, analyze and comparing the circuit performance of various logic functions are being processed.

R. Uma [18] et al proposed a new method for increasing the performance in full adder circuits using modified gate diffusion input technique. In this paper, they consider power utilization and the speed of the system. This design is very complex and tries to minimize the delay and area of the logic circuits because 5 full adder circuits are being used in this system. **V. Foroutan [19] et al** proposed a GDI structure and hybrid CMOS logic style is used to develop the two low power full adder cells. The feature of this system is only providing the low power dissipation and very high speed but also full voltage swing designs. In this paper the various components are being compared such as power, area, delay and power-delay-product (PDP). **A. Morgenshtein [20] et al** proposed a low power CLA adder design for implanting full-swing gate diffusion input logic. In this proposed paper, it has 40 nanometer carry look ahead adder (CLA) is used. This method is used to decrease the leakage current, energy efficiency, advanced design metrics of GDI cells, and to minimize the leakage vector.

III. PROPOSED WORK

In this paper, encoder and decode circuits are to be used based on the logic like XNOR Delay circuits. XNOR delay based Encoders and decoders are represented in Fig.6. In encoder part have a feed forward structure and decoder part have a feedback structure. The feedback and feed forward structure performance are evaluated in cascade form. Feed forward controller predicts direct and takes an accurate control action and also it eliminates its effect on the process output. Figure.4 indicates the feed forward configuration. It is rarely used in industrial applications and the process flow streams are contain of liquid, gases, powders or melts. It does not error-based adjustment of control variable. It is used to solve a problem like to avoid the slowness of the feedback control. Feedback controller detects a signal and it deviates in the value of the controlled output from its updated set of point. Figure.5 shows that the representation of feedback structure configuration. Feedback control is based on PID control algorithms and it also widely used. It gives a value in the progress and react to change in the value is measured.

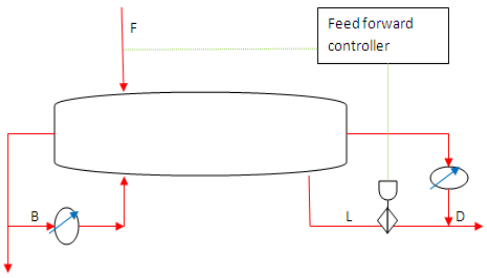

Fig.4 Feed forward structure configuration

Feed forward controller can be designed by using following equation,

$$G_{ff}(s) = -G_d(s) / G_p(s) \text{ ---------- (1)}$$

Where, the feed forward controller is represented by $G_{ff}(s)$, disturbance is indicated by $G_d(s)$ and the individual process is denoted as $G_p(s)$.

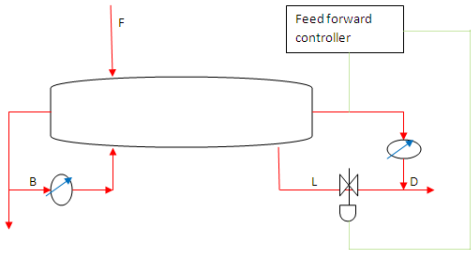

Fig.5 Feedback structure configuration

The proportional integral derivative (PID) control system is used in feedback control system. A PID controller equation is given by,

$$u = K_p(e) + K_i \int edt + K_d\left(\frac{de}{dt}\right) \text{ ---------- (2)}$$

It is used to monitor and the production process and also it will improve the efficiency of the system. Where $K_p(e)$ represented as proportional stage, $K_i \int edt$ denoted by integral part of the function and $\int K_d\left(\frac{de}{dt}\right)$ indicated as derivative stage of the system. In encoder and decoder circuits, the delay is presented in the unit of z-1 as a D Flip-Flop implemented with gate diffusion input. The D flip-flop analyzes the various inputs and it makes the transitions with match those of the input D. The output Q taken from the input at the rising edge of the clock or when the clock input is low it occurs falling edge of the clock. The delay is predicted in D flip-flop by its one clock count.

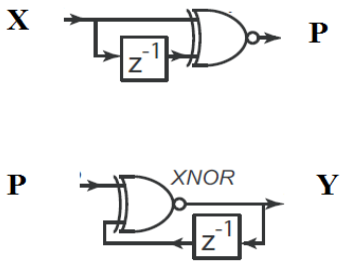

Fig.6 Encoder and decoder circuit

In the encoder and decoder circuit we have the following equations,

$$P(n) = \overline{x(n) \oplus x(n-1)} \text{ ---------- (3)}$$

$$y(n) = \overline{p(n) \oplus y(n-1)} \text{ ---------- (4)}$$

Where x (n) is the nth bit of the input bit-stream value and x (n - 1) indicates the value of the past bit in the bit-stream x {n}. Similarly, p {n} is the output of the encoder value bit stream, and y{n} is the decoder output value of the bit-stream. Each bit has a "1" or "0" digital value, ^ denotes XOR operation and ^' denotes XNOR operation. The ultimate aim of XNOR-Delay encoder is applied for minimizing the number of bits "1"s in the transmitted. Consider the OOK modulation; the transmitted consume a power is directly related to the average percentage of bit "1"s in the bit-stream. The average duty-cycling of the bit stream can be evaluated by using the above percentage. XNOR based delay encoder can save power in the transmitter part. In OOK modulations, it requires to meet ultra low power consumption. In short range communication the OOK modulation is being used and it can be used as power efficiency. Figure.7 shows that the calculation and probability density function of OOK modulation technique. It is used to calculate the performance of transmitter power.

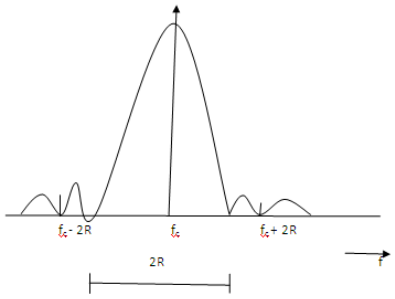

Fig.7 OOK modulation PDF

Gate Diffusion Input (GDI) LOGIC

In our proposed encoder consist of D flip-flop and XNOR gate equipment. To reducing the transistor count and delay complexity D flip-flop and XNOR gate is designed using GDI logic. It is an efficient implementation technique used in this paper. It is used to reduce the power delay product and area of the circuit. Various logic circuits were investigated and presented in the literature [12][13][14][15], targeting to reach an optimal design in terms of delay, power and area. Some efficient techniques were improved and adopted by designers for a various kinds of technologies [1]. Gate-Diffusion-Input (GDI) design technique that was recently established and presented in [15], proposes an efficient alternate method for logic design in standard CMOS and SOI technologies. The basic GDI cell is shown in Fig. 8 it looks like a conventional CMOS inverter the source/drain diffusion input of both PMOS and NMOS transistor is different. In conventional inverter circuit, source and drain diffusion input of PMOS and NMOS transistors are always connected at VDD and GND potential, respectively. The diffusion terminal turns as an external input in the GDI cell. It supports in the realization of various Boolean functions such as AND, OR, MUX, INVERTER, F1 and F2, as listed in Table1.

N	P	G	Out	F
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

Table.1 Different logic implementation using GDI

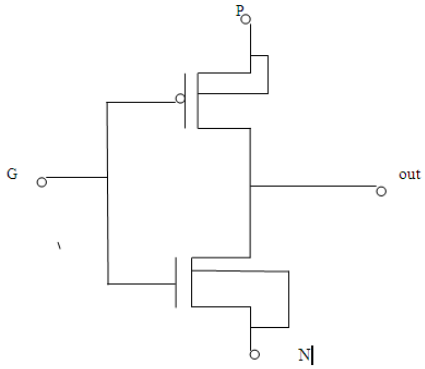

Fig.8 Basic GDI cell

The swing problem present in low, it is the most effect of this system. The output value is **A=0, B=0** in this case the functionality is PMOS pass transistor state and its voltage is threshold level. When **A=0, B=V_{DD}** in this case CMOS inverter functionality is used and the voltage level is high. When **A=V_{DD}, B=0** in this case NMOS pass transistor is used and the voltage is below threshold level. In the GDI cell, when **A=V_{DD}, B=V_{DD}** in this case the CMOS inverter functionality is used and the voltage level become low. The implementation of any logic function using GDI cell standard is very suitable one. This logic function is expansion by Shannon equation. The algorithm is based on the Shannon expansion and it is implementation of any function F by GDI cells. The algorithm steps are following below,

1) Given a function 'F' with variable is represented by n.
2) Check the function, if it is not equal to 1, 0 or not inverted variable as single.
3) If the function is equal, it does not need additional hardware.

4) Using the Shannon expansion function for a given equation.
5) Using GDI cell for function implementation purpose.
6) Repeat to step 2.

This algorithm is used to evaluate the number of transistors needed for n- input implementation function. This is evaluated by,

$$\mathbf{M=2 \times 2^{n-1} = 2 \times N = 2^n} \text{ ---------- (5)}$$

Where M is maximum number of transistors used in this implementation, N is the maximum count of GDI cells and n is the number of variables in that given function. In this design the number of transistors is used to design six XNOR gate. XNOR operation using gate diffusion gate input (GDI) is represented by figure.9.

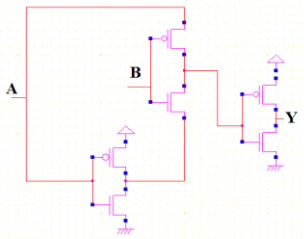

Fig.9 XNOR using gate diffusion input (GDI)

GDI D flip-flop is depends on the Master-Slave connection of 2 GDI D-latches. Four basic GDI cells are presented in each latch as a result of simple eight transistor structure. The equipments of the circuit are divided into two categories: 1) Body gates: using the clock signal these gates are controlled. It has two paths such as one is transparent stage and then holding stage. 2) Inverters: it is used to maintain the complementary values of internal signals and output of the circuits. The performance of this circuit is evaluated by varying the size of the transistors and to obtain reducing power delay product. The structure of the proposed system is to improve the performance of the system. D flip-flop contain eighteen transistors and it is obtain low area and the high performance. Figure.10 indicates D flip-flop logic functions using gate diffusion input (GDI). Using the variety of implementation GDI D flip-flop has 71% reduces of gate area and also reducing 40% power delay product.

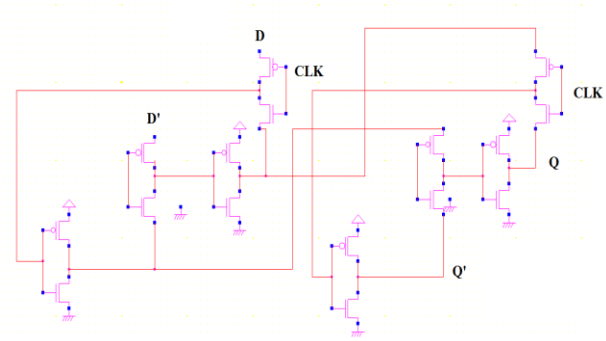

Fig.10 D flip-flop using GDI

ZigBee applications in low power mode

ZigBee is used for low power application mode but it is not suitable for radio frequency power mode. In sleep mode, it is specifically designed to occupied battery powered devices. ZigBee devices are very cheap because it consume power very low and it offers a battery life is long days. Now a day, ZigBee act as a major role in wireless sensor network because data rate must vary depending on the frequency bands. In low power design of ZigBee is an important role in wireless networks because it has a sleep mechanisms and sleep methods for nodes. The data will send to its parent node after complete data acquisition by sensor node. The data sent successfully the nodes are fall sleep. The next round will start of data acquisition and transmission when the sleep time after completion. Figure.11 shows that data transmission process of terminal node in low power mode. Zigbee system realizes the nodes sleep and sensor data acquisition of terminal nodes are should be combined.

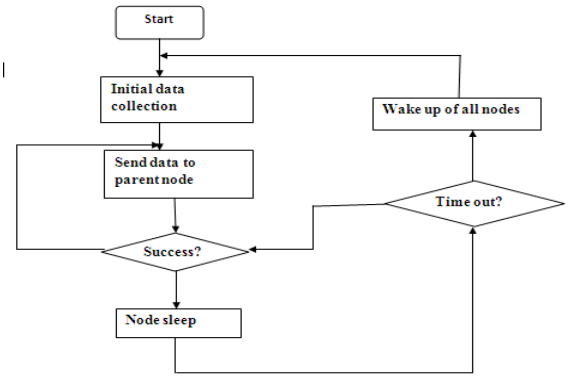

Fig.11 Low power data transmission process

In the low power ZigBee applications, the energy and power will be calculated by following equations. The energy will calculated by total power consumed added with duty

cycling mechanisms. Energy will indicated as W [J], power is represented as P, t is time taken by the system. So the energy consumed by the system is,

$$\mathbf{W\ [J] = (P + 13 \times 10^{-3}) \cdot t} \text{ ---------- (6)}$$

$$\mathbf{W\ [J] = P_{am} \cdot t_{am} + P_{sm} \cdot t_{sm}} \text{ ---------- (7)}$$

$$\mathbf{W\ [J] = P_{am} \cdot \left(\frac{operation\ time}{data\ transmission\ interval}\right)} \text{ ----- (8)}$$

The power is giver by,

$$\mathbf{P = W\ [J] \cdot \left(\frac{data\ transmission\ interval}{operation\ time}\right)} \text{ ------ (9)}$$

Where, $\mathbf{P_{am}}$ indicated as active mode of power, $\mathbf{t_{am}}$ is time active mode, $\mathbf{P_{sm}}$ is power sleep mode, $\mathbf{t_{sm}}$ is time sleep mode. The power is calculated by product of energy in terms of joules with the data transmission interval to operation time. Power is indicated by Watts.

IV. SIMULATION AND RESULT

Our proposed GDI XNOR delay encoder designed and simulated results using analog design tool. The output values are tabulated in table 2 and various components like CMOS and TG are to be compared. In the above table, CMOS have 12 XNOR gates and 24 D flip-flops; transmission gate has 8 XNOR gates and 12 D flip-flops; our proposed system has 6 XNOR gates and 18 D flip-flops [21]. Figure.14 shows that delay occurs in CMOS is 4.772 ps, gate diffusion input delay is 13.4 ps and XNOR delay based system with full swing GDI is 1.947 ps are represented in existing systems. Our proposed method is full swing GDI XNOR delay based encoder and existing method is GDI encoding scheme.

	CMOS	TG	Proposed
XNOR	12	8	6
DFF	24	12	18

.

Table.2 Comparison of output details for devices

	GDI	CMOS	XNOR based delay encoder with full swing GDI
Delay (ps)	13.4	42.2	8.5
Power (nW)	35.9	78.7	5.29
Energy consumption (J)	4.7	5.2	1.9
EDP (J sec 10^{-24})	8.2	16.5	2.85

Table.3 Comparison of output details for existing methodology

Figure.15 represents the power analyses of various components like CMOS, GDI and proposed model. In the CMOS circuit the power consumption is 39.17 nano watts, power consumption present in gate diffusion input is 31.01 nano watts and GDI XNOR delay encoder consumed 2.5 nano watts power. So our proposed model consumed less amount of power compared with other circuit designs.

	GDI	CMOS	XNOR based delay encoder with full swing GDI
Delay (ps)	4.772	26.57	1.947
Power (nW)	31.01	39.17	2.5
Energy consumption (J)	2.12	4.57	0.54
EDP (J sec 10^{-}	6.2	9.14	0.45

^{24})			

Table.4 Comparison of output details for proposed methodology

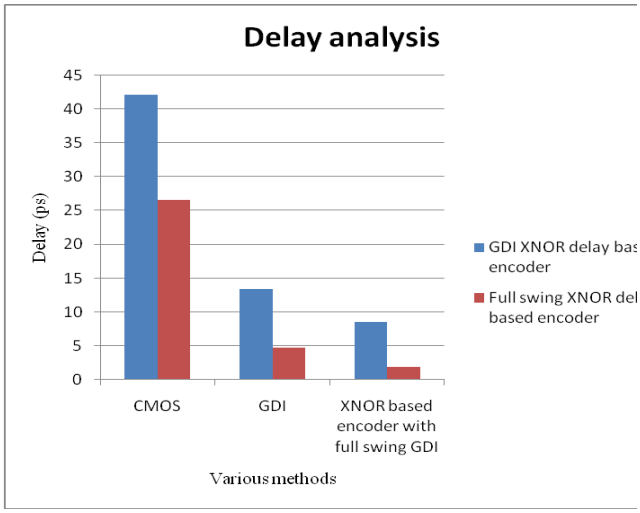

Fig.14 Delay analysis

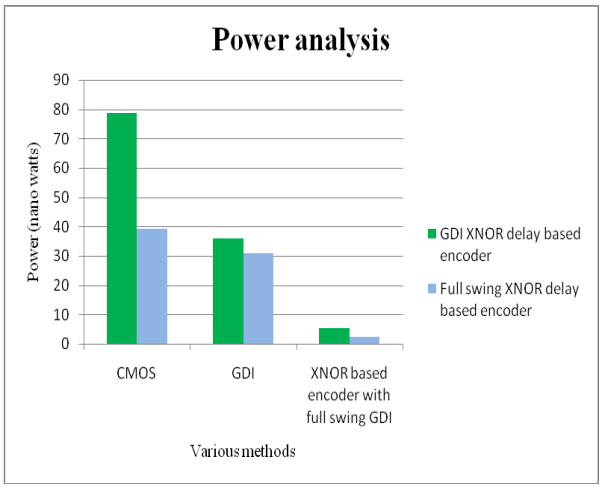

Fig.15 Power analysis

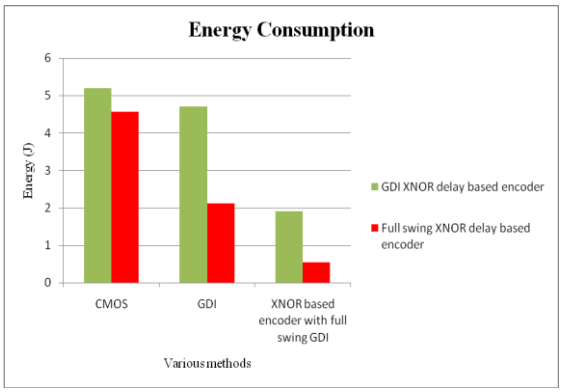

Fig.16 Energy consumption analysis

In figure.16 denotes the various components are compared like CMOS, EDR that is energy delay product of existing and proposed system. In CMOS system has 9.14 sec 10^{-24} are present, 6.2 J sec 10^{-24} are present in gate diffusion input and our XNOR based system with full swing GDI have 0.45 J sec 10^{-24}. Power dissipation is nothing but the electrical power should be converted into energy in the form of heat. The energy consumption will be calculated based on the power analysis. In figure.17 shows, various components are being compared with energy consumption. In CMOS design 4.57 J energy will be consumed. The gate diffusion input consumes 6.2 J and XNOR delay based system 0.54 J will be consumed.

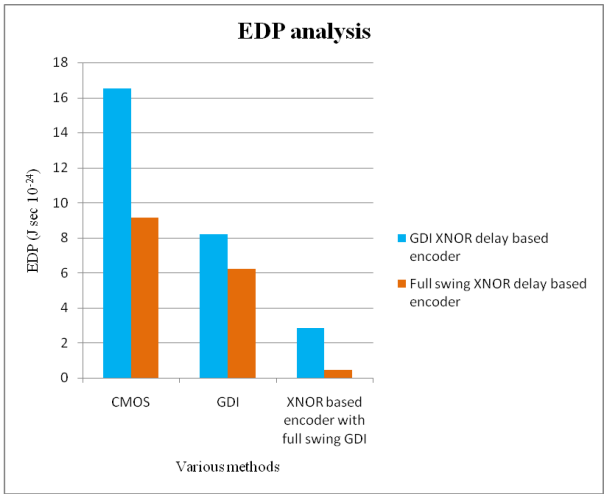

Fig.17 EDP analysis

V. CONCLUSION

A new technique of high-performance XNOR based encoder using full swing Gate-Diffusion-Input (GDI) technique was presented. In the XNOR delay based encoder using full swing gate diffusion input (GDI) is applied to low power ZigBee applications. In this technique helps to reducing power and delay from the circuit while maintain low complexity of logic design. The simulation results show that our proposed GDI XNOR-Delay encoder with full swing gate diffusion input is suitable for low power mode with minimized power,

delay complexity and minimized energy consumption.

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