Efficient RF-to-DC Energy Harvesting for Portable Applications using TFET

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Abstract *–This paper proposes a method for RF-to – DC energy harvesting with high efficiency using TFET, sensitive low load resistance and increased dynamic range for low power devices. It measures peak power conversion for more power efficiency at low input power. The Proposed TFET rectifier takes the advantages of a forward bias technique to control the selective transistor to rectify the conduction. The tunnel devices are used for specific characteristics to increase the strength of weak input signals. In this paper it is proposed to have a design performance related with peak power conversion efficiency for power and amplitude, our design fabricated starts to operate -18dBm input. The operation of rectifier circuit with tested frequency GSM 900 band includes other frequency band such as 2.4 GHz with normal impedance matching. The efficiency of the measured peak power conversion for the implemented TFET is 87% and -19.2dBm (13µW) sensitivity and this is the best rectifier utilization for energy harvesting applications and Internet of things.*

Keywords: Energy harvesting, RF-to-DC conversion, PCM, Dickson charge pump, rectifier, Tunneling FET

I. INTRODUCTION

Nowadays most arrival of Internet of Things (IoT) and low powered devices are the challenges in battery life so that the need to charge the power or energy harvesting, in RF energy harvesting devices has been the goal for many researchers [1] with respect to the discovery of electricity and transmission of energy through wireless [2]. The independence of wireless energy transmission included less weight, huge backup and easy to access in par with enhanced wireless energy transfer technique and improves the efficiency of IC [4]. The wireless electronic devices are low power with reality [5].

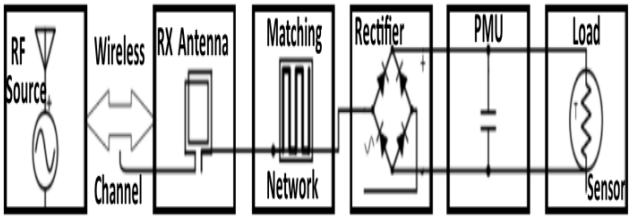


Figure 1: Block diagram for RF- DC Energy Harvesting

The basic block diagram of RF energy harvesting system is shown in Figure 1. The existing RF energy harvesting system consists of micro strip antenna, matching network and RF to DC converter [3]. The surrounding RF waves are converted into electrical energy signal in the rectifier to proper impedance matching to transfer the power for low power electronic devices for charging.

We propose a TFET design and analysis of the detailed operation limit of TFET based rectifier with respect to input signal voltage level and input power. The specific purpose for tuning the rectifier methods in TFET function is to control the reverse current for the extension of the power range of TFET rectifier.

II. ANALYSIS AND OPERATION FOR TFET RECTIFIER

A. Circuit design

The well known 2-T passive rectifier is shown in Figure 2. It operates in two regions respectively region I and region II. In region I the transistor P1 is ON and N1 is OFF, then the supply current is transferred to the output load RL. In region II transistor P1 is OFF and N1 is ON to the supply VIN then no current flows through P1, the direct current output voltage is produced.

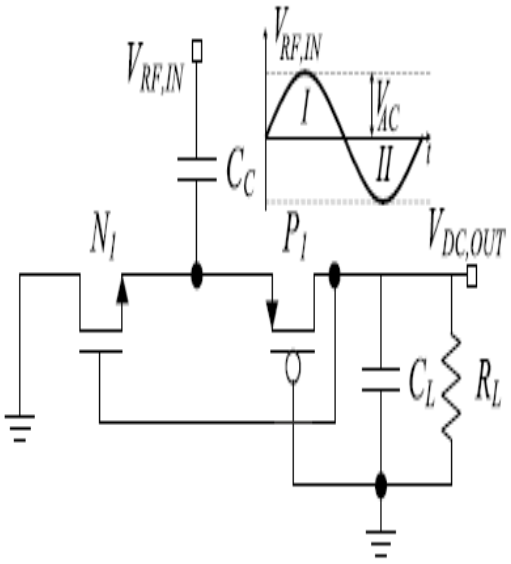


Figure 2:P Well Known 2-T Passive Rectifier

The two different voltage inputs levels 0.05 V peak and 0.01 V peaks are reviewed for single cell and a single stage circuits respectively. The expected output for the above cases at 50 ns time for transient is shown in Figure 3, if the output is low for excitation 0.05V and the condition for the transistor do not turn ON in two cases. If we want to increase the output voltage, in this process we can expect the clear output voltage of a single stage cell with dual transistor is higher and 1V input voltage closer when compared to the cell unit.

The proper cascaded multi stages achieved a high output voltage. If we have added a basic unit into the cascaded stage using a capacitor provide a basic voltage for corresponding N1 of the below stages during the negative half cycle. The corresponding transistor is turned on to the charging path. The process continues through all stages in RF input and then rectified with low ripple into proper steady state output DC voltage, the output is multiplied for N for N/2 stages for configured to multi-stage division.

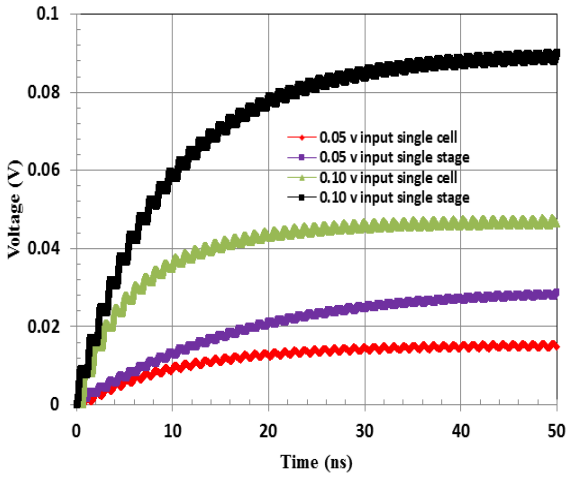
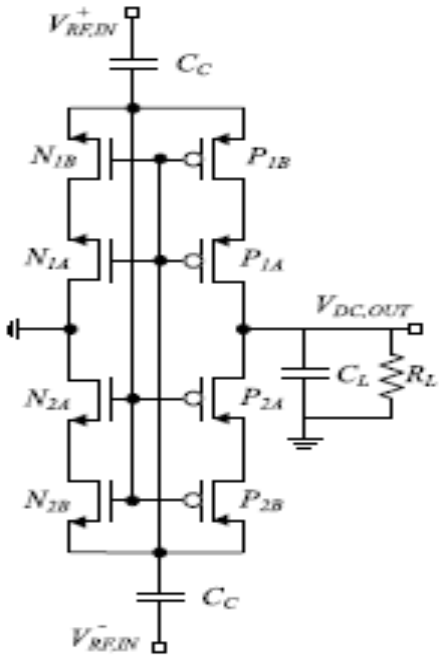


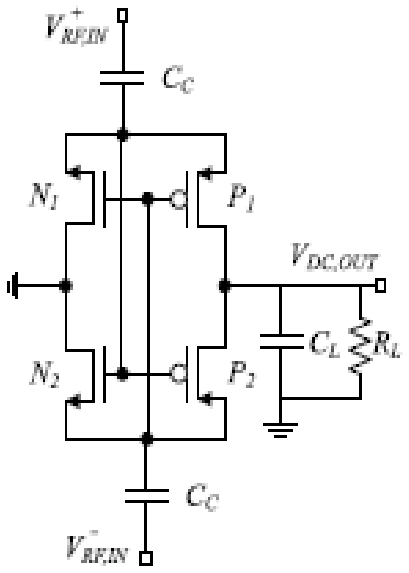
Figure 3: Output Voltage of Single Cell and well known 2-T Passive Rectifier

$$V_A=2V_R-V_{TH} \quad (1)$$

$$V_{out}=2(V_R-V_{TH}) \quad (2)$$



(a)



(b)

Figure 4: Schematic Design of Gate Cross – coupled TFET(a)&(b)

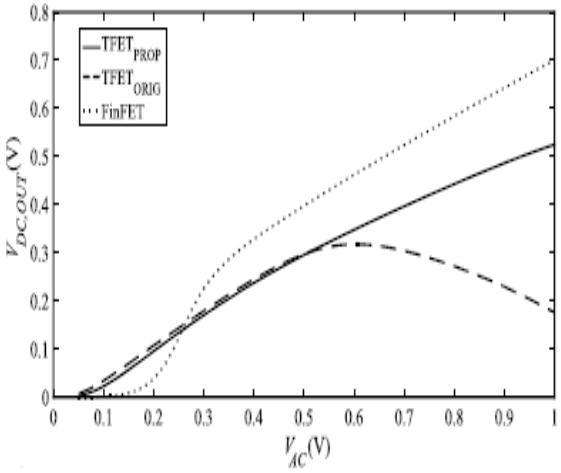


Figure 5: Performance of Cross coupled TFET

B. Performance and analysis

The gate cross coupled TFET topology is designed for specifications with R_L=1 MΩ and R_L=100 KΩ. In the first step the transistors are resized as in 2-T design and the performance is shown in Figure 5. After examination, we identified the analysis - the different signal that is V_{in}^{-} and V_{in}^{+} from the section II. The PCE results for R_L=100 KΩ transistor size is large have been used to develop the peak PCE of the original design.

C. Modeling circuit

For the proposed architecture, the mathematical model has been derived and explained. They are two different categories of rectifier stages which are divided in to two cells. Each individual cell is used for averaging the above threshold voltage level of RF signal. But the proposed design is based on the cross coupled configuration to perform continuously in high sensitivity features. The performance of TFET Rectifier with different load is shown in Figure 6.

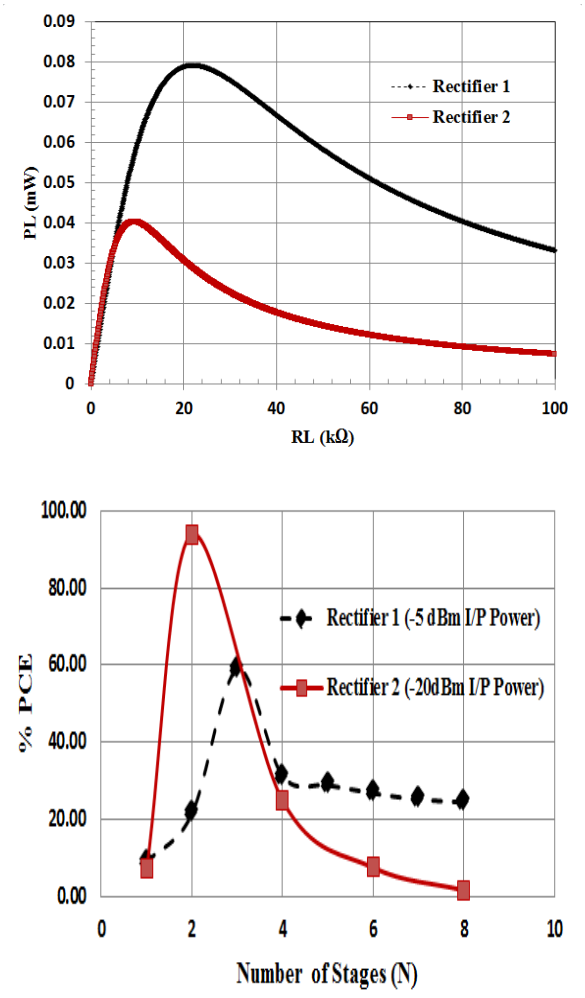


Figure 6: Output Power of Rectifier with different loads

III. DISCUSSION AND MEASUREMENTS

The preferred designs are plotted in a 0.19-μm standard TFET technology, die microphotographs of the preferred designs are given in Figure 4 and the performance is shown in Figure 5. The FX and self-biased designs are also manufactured on the same die for a fair comparison.

The active area of the proposed single-sided design is 8400 μm2 and for the double-sided design 8800 μm2, compared to 5000 μm2 for the FX design and 16 900 μm2 for the self biased design.

The measurement setup has a vector network analyzer (VNA) (Agilent N5225A), a digital multimeter (Keysight 34420A), and a programmable variable load resistor. The test is achieved by getting the input RF power, the load, and the operating frequency, and recording the corresponding output voltage and the S-parameters. The S-parameters are measured using on-chip probing via GSGSG differential probes with the reference plane set to be the on-chip pads of the rectifier input.

$$P\text{in}\ (\text{dBm}) = P\text{source}\ (\text{dBm}) - L\text{cable}\ (\text{dB}) - 10 \log |S11\text{rec}|2 \quad (3)$$

In general, the preferred single-sided and double-sided designs provide peak PCE for a larger range of input power. Figure 5 shows the measurement results for the PCE versus the RF input power for different architectures, operating with a 100-k_ load at the industrial, scientific, and medical (ISM) bands (433 MHz) [Fig. 10(a)] and the UHF 900-MHz band .

The preferred topologies uses the strengths the FX and the self-biased architectures by governing an effective results by considering both low and high input powers. In addition, when operating frequency at the ISM and UHF bands, the preferred double-sided design provides the highest peak PCE of 82% and 66% respectively.

Basically both the single-sided and double-sided architectures are able to produce the best sensitivity and higher output voltage for a higher range of RF power. In general sensitivity is known as the lowest radio frequency power needed to produce a voltage of 1V at the load. In the preferred double-sided topology improves the sensitivity higher than 1.9 dB demonstrates the dependence of the proposed architectures on the load. This is achieved by fixing the operating frequency, varying the load resistance, and measuring both the peak PCE and the sensitivity.

The single-sided architectures and double-sided architectures give steady peak PCE when operating frequency is 433-MHz with negligible dependence on the loading value. The highest value of PCE for the double-sided architecture varies by lesser than 15% when operating frequency is 900 MHz. The results for the single-sided architecture are good with only 2% dissimilarity.

IV. CONCLUSION

In this paper, we proposed a RF to DC energy harvesting for portable applications using TFET with high sensitivity. The RF rectifier designs for RF power system, uses the tunnel devices which are used for implementation of typical topologies to remove the degradation of their performance by the forward biasing P-i-N diodes. Our design has superior margins and performance except for read delay than CMOS due to the low drive current. The measured peak power conversion efficiency of the implemented TFET is 87% and -19.2dBm (13µW).

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