A HIGH STEP-UP QUADRATIC BOOST CONVERTER INTEGRATED WITH VOLTAGE MULTIPLIER

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Abstract: *An interleaved quadratic boost converter integrated with capacitive voltage multiplier is proposed in this paper. Two quadratic boost switching cells are interleaved to minimize the current ripples in input side. Its output is coupled to a voltage multiplier to incr`*

ease the static gain, resulting in a higher output voltage with moderate duty cycle. Compared with the conventional boost converter and quadratic boost converter, the proposed converter has reduced voltage stress in the switches and diodes. The detailed analysis of the converter is presented for both continuous. A prototype is simulated and implemented in the laboratory. The results validate the theoretical analysis and confirm the viability and significant performance of the converter. The maximum efficiency of the proposed converter is 91.5 % under full load.

Key words: *DC-DC power converters, distributed power generation, fuel cells, photovoltaic systems, switching converters.*

1. Introduction.

A large and sustainable economic growth in India is to develop a great demand for energy resources. There is a risk of increasing in import of oil, creating serious problems for energy security in the future of India. In India, a large proportion of people still live without access to electricity and other forms of commercial energy. More than 50% of the population in India has little or no energy for life and living.

The power generation through photovoltaic panels, and through the fuel cells bring advantages like diversification of energy sources, increased distributed generation and also in services to isolated areas [1,2]. Various applications such as uninterrupted power supply and motor drives, often need to raise a low level of input voltage from batteries, solar panels, fuel cells, small wind generators, and others, to voltage values between 300V and 400V, constituting a DC bus power required for its voltage inverters [3].

The cascading of N conventional boost converters is a practical solution to obtain a high voltage gain with increased power losses. The voltage gain is increased by number of converter stages [4-7]. However, cascaded topologies are not suitable for high gain applications, because the voltage stress across the power switch and diodes are high which will reduce the efficiency of the converter. In [8,9] the conventional boost converter is combined with multiple switched capacitor cells to obtain a high conversion ratio. Topologies with coupled inductors [10-12] can provide high voltage gain with reduced voltage stress. However, the leakage inductance in the coupled inductors cause high voltage spikes on the switches. In [13-15], the coupled inductors and voltage multiplier cells are integrated with conventional boost converters to obtain large gain. However, the added stage increases the parts count and complexity of the design as well as introducing extra losses related to the multiplier cell. The conventional boost converters are interleaved with a voltage multiplier cell can extend the voltage gain, minimize the input current ripple [16,17]. Thus, an interleaved converter improves the performance, but at the expense of increased size, cost, and control complexity.

This work is a contribution to a new DC-DC converter topology without the use of high-performance switching devices or sophisticated control strategies while preserving a high voltage gain and compatible switching efforts with commercially available components. The proposed converter is obtained by integrating interleaved two quadratic boost cells and voltage multipliers. The principle of operation and analysis of the proposed converter is explained in Section 2 and Section 3. Section 4 gives the design methodology for the proposed converter. Simulated and experimental results are presented in Section 5 and some concluding remarks in Section 6.

2. Interleaved Quadratic Boost Converter Integrated with Voltage Multiplier

The conventional quadratic boost converter with a single active switch, two-phase interleaved boost converter and the voltage multiplier are shown in Figs. 1(a), (b) and (c) respectively.

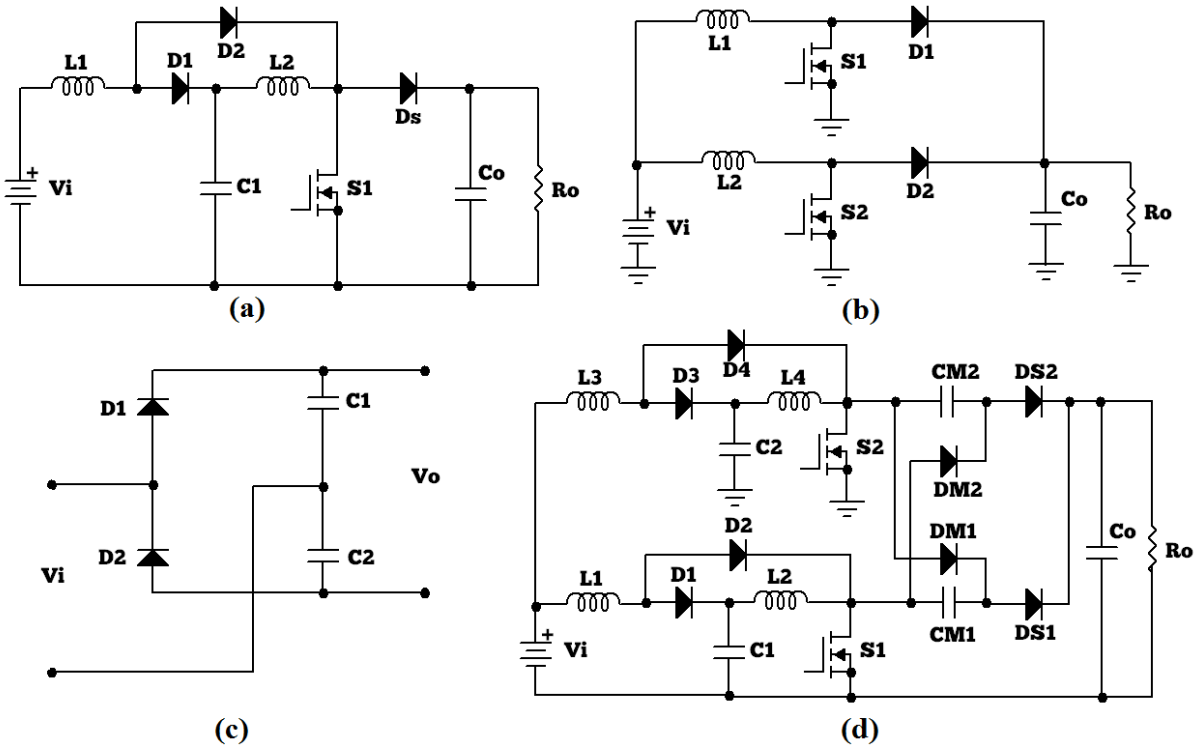

Fig. 1. Topology derivation of proposed converter. (a) Quadratic boost converter (b) Interleaved converter (c) Voltage multiplier (d) Interleaved Quadratic Boost Converter integrated with voltage multiplier

They are integrated to obtain the topology of the proposed converter and it is shown in Fig. 1(d). The proposed topology consists of two quadratic converters, the first being formed by S_1, L_1, L_2, D_1 and D_2 and the second by S_2, L_3, L_4, D_3 and D_4. Both converters are interleaved and its output is connected to the load (R_O) through the voltage multiplier cell (D_{M1}, D_{M2}, C_{M1}, C_{M2}, D_{S1} and D_{S2}) and the filter capacitor (C_O).

The analysis is divided into two stages, the converter operating with duty cycle D > 0.5 and D < 0.5. The following characteristics are considered to make the analysis simple. All the MOSFETS and Diodes are ideal at this stage. The capacitor C_O is large enough so that the voltage ripples is minimum. The number of stages in parallel is equal to 2. The number of voltage multiplier stages is 1 (k = 1).

2.1. Analysis of Proposed Converter for D > 0.5.

This is the operating region where the converter is generally used, being the one which allows higher static voltage gains. The circuit has four operating modes as shown in Fig. 2, that will be qualitatively analyzed.

Mode I (D > 0.5): (t0 – t1)

In the first operating mode, shown in Fig. 2(a), the switches S_1 and S_2 are in ON state. The input currents are interleaved, circulating through the inductors, L_1 and L_3 and the energy is stored in it. All diodes are in OFF state except D_2 and D_4. In this mode the average voltage in inductors L_1, L_2, L_3 and L_4 are defined by (1) to (4).

$$V_{L1avg} = -Vi\,DT_{on} \quad (1)$$

$$V_{L2avg} = -V_{C1}\,DT_{on} \quad (2)$$

$$V_{L3avg} = -V_i\,DT_{on} \quad (3)$$

$$V_{L4avg} = -V_{C2}\,DT_{on} \quad (4)$$

Mode II (D > 0.5): (t1 – t2)

In the second operating mode, as shown in Fig. 2(b), the switch S_2 is switched OFF. In this mode, the energy stored in inductor L_4 in the previous mode is transferred to the output capacitor C_O via the diode D_{S2} and also to the multiplier capacitor C_{M1} through the diode D_{M1}. It can be seen that the multiplier capacitors C_{M1} and C_{M2} are connected in series through the diode D_{M1}, and connected in parallel with the output capacitor C_O through the diode D_{S2}. Therefore, the output voltage will be equal to twice the voltage of the multiplier capacitor. If the voltage of the multiplier capacitors C_{M1} and C_{M2} are V_M, then

$$V_O = 2V_M \quad (5)$$

In general, the equation of output voltage for the proposed topology would be

$$V_O = V_M\,(k+1) \quad (6)$$

The maximum voltage at the terminals of the switch S_2 is equal to the voltage on the multiplier capacitor C_{M1} (V_M) and the maximum voltage at the terminals of the diode D_{S1} is equal to the multiplier capacitor C_{M2} voltage (V_M). However, the maximum voltage across the diodes D_{M2} is always equal to twice the multiplier

capacitor voltage (V_{CM1} + V_{CM2}). In this mode, the average voltages in inductors, L_1 and L_2 are same as in the previous mode and in L_3 and L_4 are given in (7) and (8).

$$V_{L3avg} = (V_i - V_{C2})(1-D)T_{on} \quad (7)$$

$$V_{L4avg} = (V_{C2} - V_M)(1-D)T_{on} \quad (8)$$

Mode III (D > 0.5): (t2 – t3)

The third mode of operation is shown in Fig. 2(c). The switch S_1 is switched to the conduction state. At this mode, the inductors will store energy as in the Mode I.

Mode IV (D > 0.5): (t3 – t4)

The fourth mode of operation is shown in Fig. 2(d). The switch S_1 is turned OFF. The energy stored in the inductor L_2 is transferred to the output capacitor C_O and the multiplying capacitor C_{M2}. As the multiplier capacitor C_{M1} was charged in the Mode II, the output diode D_{S1} will start conducting and it allows current which was greater than the multiplier diode D_{M2} current, but both have the same average value. In the fourth mode of operation, average voltage of the inductors L_3 and L_4 are same as in the Mode III and average voltages of the inductors L_1 and L_2 are

$$V_{L1avg} = (V_i - V_{C1})(1-D)T_{on} \quad (9)$$

$$V_{L2avg} = (V_{C1} - V_M)(1-D)T_{on} \quad (10)$$

For calculating the static gain, it is considered that the average current in the inductors (L_1 to L_4) are zero. It is observed that the voltage on the multiplier capacitor (V_M) is equal to the output voltage of the Quadratic Boost Converter, so we have:

$$G = \frac{V_M}{V_i} = \left(\frac{1}{1-D}\right)^2 \quad (11)$$

As already shown, the output voltage across the capacitor C_O is the sum of the voltages of the multiplier capacitors C_{M1} and C_{M2}. Substituting (6) in (11) yields (12).

$$G = \frac{V_O}{V_i} = (k+1)\left(\frac{1}{1-D}\right)^2 \quad (12)$$

For the proposed converter, we have k = 1. Hence the static gain of the proposed converter is given by

$$G = \frac{V_O}{V_i} = 2\left(\frac{1}{1-D}\right)^2 \quad (13)$$

Expressions (11), (12) and (13) are analogous to equations of a basic quadratic converter. The waveforms of the converter for operating condition D > 0.5 is as shown Fig. 3.

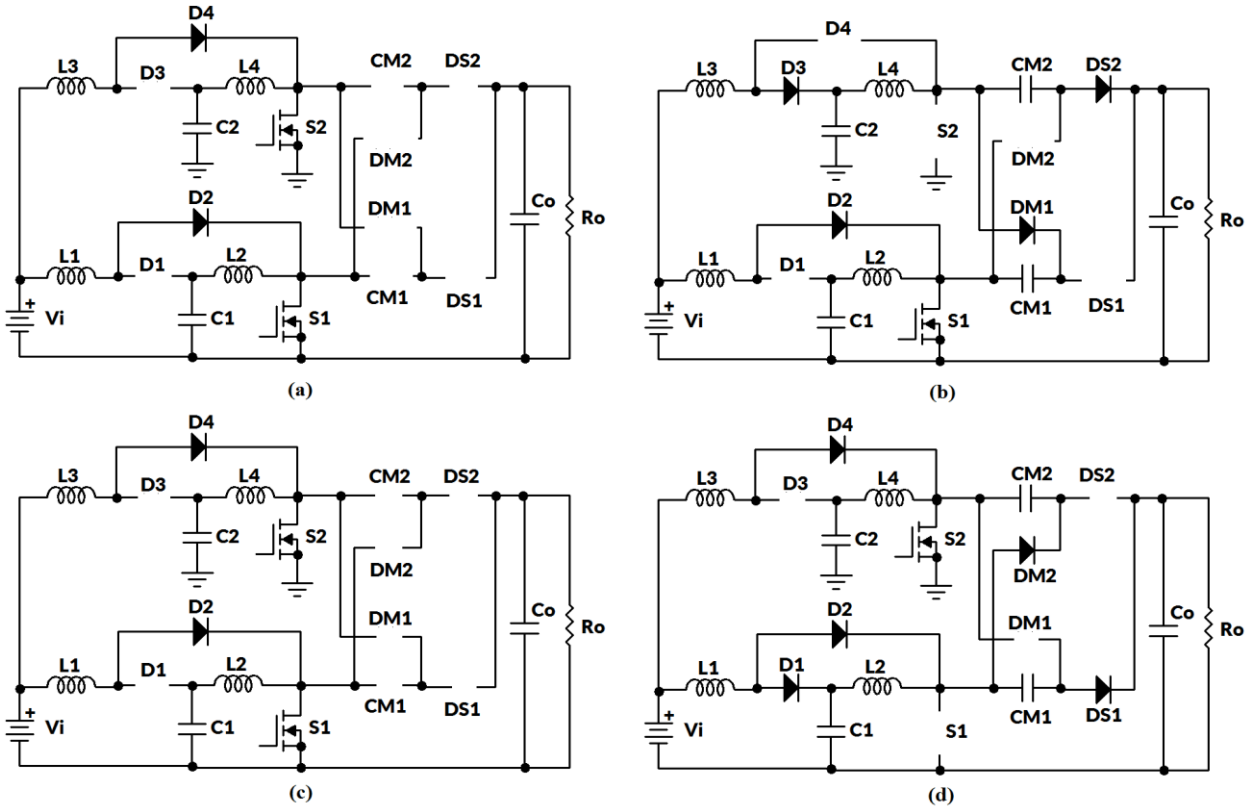

Fig. 2. Operating Modes of Proposed Converter for D>0.5. (a) Mode I: (t0 – t1) (b) Mode II: (t1 – t2) (c) Mode III: (t2 – t3) (d) Mode IV: (t3 – t4)

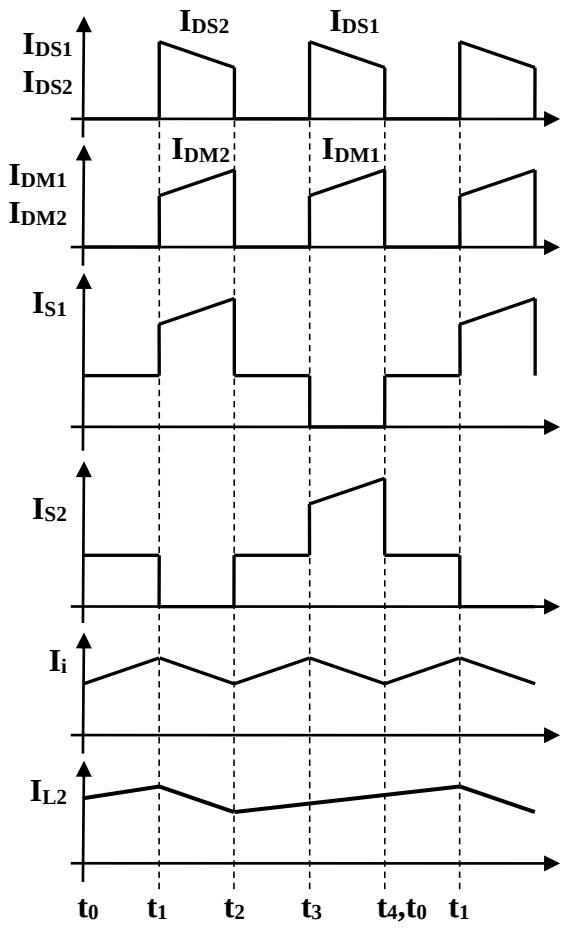

Fig. 3. Waveforms of proposed converter for (D > 0.5)

The operating region with less than 50 % duty cycle is not the primary mode of operation of the converter, whose purpose is to operate at high gain. Table I summarizes the voltage step-up ratio, the voltage stresses across switch and diodes for the interleaved quadratic boost converter integrated with voltage multiplier as well as the quadratic boost converter, boost converter and the converter proposed in [18,19]. Compared to other converters, the voltage stresses of the switch S_1, diodes D_1, D_2 and D_{S1} are less in the proposed topology. Those allow using lower voltage rated diodes and switch, hence the conduction loss and switching loss could be reduced leading to efficiency improvement [20].

4. Converter Design Methodology

The design values of the proposed converter are given in (14) to (17).

$$V_i = 24V \quad (14)$$

$$V_O = 300V \quad (15)$$

$$P = 400W \quad (16)$$

$$f = 100kHz \quad (17)$$

The input voltage value of 24 V has chosen because it represents values typically available in photovoltaic cells or micro wind turbine. The output voltage was chosen as a typical value of DC bus of DC / AC inverters for standalone power systems or grid-tied systems. The operating frequency is a compromise between reduction in size of the passive components and losses in the switches.

The same operating frequency value is being used in other topologies by other researcher groups, which will allow a more realistic comparison on performance between the topologies in future. The duty cycle, D of the PWM pulses applied to the MOSFETS is the primary control aspect of the drive. Considering the input and output voltage values of the prototype converter, the desired duty cycle is calculated by using (13). The calculated values are G = 12.5 and D = 0.6. The inductor values are calculated by using (18).

$$\Delta I = \frac{V_i}{L} T_{on} \quad (18)$$

Let the maximum permitted ripple current in inductors be 3.5 %. The calculated inductance values of the inductors are $L_1 = L_3 = 350$ µH and $L_2 = L_4 = 761$ µH.

The intermediate capacitors C_1 and C_2 are calculated by using (19).

$$\Delta V_C = I \frac{T_{on}}{C} \quad (19)$$

The ΔV_C variable is the voltage variation across the capacitor during charge and discharge cycles. Let the maximum permitted ripple voltage in capacitors be 0.5 %. The calculated capacitance values of the capacitors are $C_1 = C_2 = 78$ µF. The output capacitor, C_O should be calculated according to the desired output voltage ripple. In interleaved converters, the output ripple frequency is twice the switching frequency of each stage, thus C_O can be calculated by using (20).

$$C_O > \frac{DI_O}{2\Delta V_C f} \quad (20)$$

For 0.5 % output voltage ripple, considering the duty cycle, output current and operating frequency, the calculated value is $C_O > 3$ µF. The values of C_{M1} and C_{M2} are calculated by using (21).

$$C_{M1} = C_{M2} > \frac{P_{in}}{f \cdot \left(V_O^2 - V_{\min}^2\right)} \quad (21)$$

By considering the voltage ripples in the multiplier capacitor as 0.5 %, the minimum output voltage, V_{min} will be 298.5 V and the $C_{M1} = C_{M2} > 4.7$ µF.

5. Analysis of Simulation and Experimental Results

The complete circuit of the proposed converter with component values is as shown in Fig. 4 and its prototype is shown in Fig. 5.

Table 1
Comparison of voltage stress

Converter Parameters	Proposed Topology	Converter of [19]	Converter of [18]	Quadratic Boost Converter	Boost Converter
Voltage step-up ratio	$\frac{2}{(1-D)^2}$	$\frac{(1+n_1D)(1+n_2D)}{(1-D)^2}$	$\frac{(1-D)}{(1-2D)}$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)}$
$V_{S\text{-stress}}$ (V)	$\frac{V_O}{2}$	$V_O\left[1-\left(\frac{n_2D}{1+n_2D}\right)\right]$	$(1+D)V_o$	V_o	V_o
$V_{D1\text{-stress}}$ (V)	$\frac{(1-D)V_o}{2}$	$\frac{V_i(1+2n_1D)}{1-D}$	$\frac{V_o(1-2D)}{(1-D)}$	$(1-D)V_o$	–
$V_{D2\text{-stress}}$ (V)	$\frac{DV_O}{2}$	$V_O\left[1-\left(\frac{n_2D}{1+n_2D}\right)\right]$ $-V_{C1}-\frac{V_in_1D}{1-D}$	$\frac{2DV_o}{(1-D)}$	DV_o	–
$V_{DS1\text{-stress}}$ (V)	$\frac{V_O}{2}$	$V_O\left[1+\left(\frac{n_2D}{1+n_2D}\right)\right]$	$\frac{V_o}{(1-D)}$	V_o	V_o

The driver and control circuits are not shown. The proposed converter is designed and simulated using PSIM software. And it is necessary to implement a prototype model in order to prove the theoretical analysis.

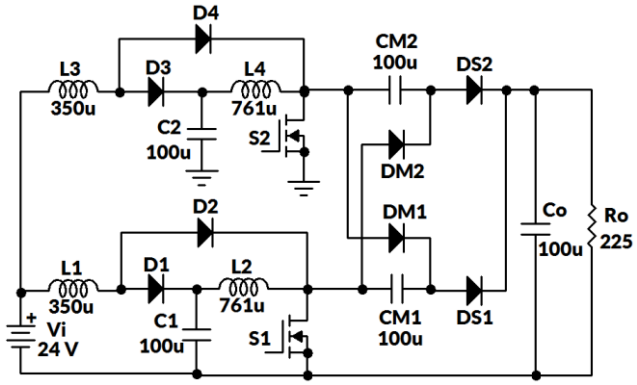

Fig. 4. Complete circuit of the proposed converter

Table 2 presents the components used in simulation and prototype. Fig. 6 shows the gate drive pulses of the switches S_1 and S_2. The Channel 1 represents the gating signal of switch S_1 and Channel 2 represents gating signal of switch S_2. Its frequency and amplitude are constant, but the pulse width can vary significantly according to the operating conditions. The amplitude is low about 3.6 V, because of the digital circuit used to generate the gate dive pulses.

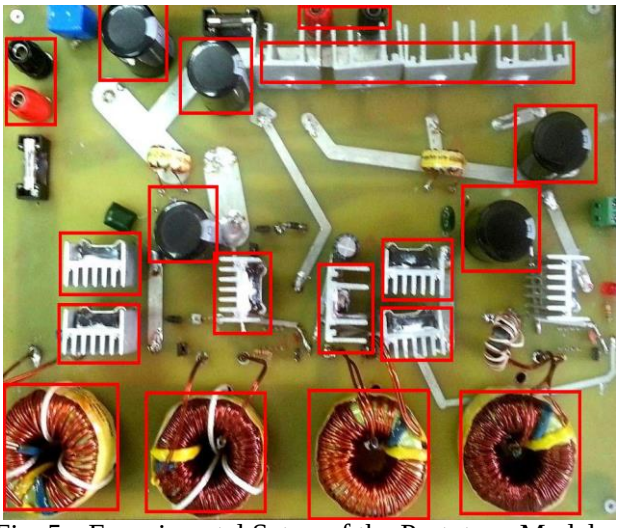

Fig. 5. Experimental Setup of the Prototype Model

Table 2
Components used in simulation and prototype

Component	Simulation	Prototype
MOSFETs (S_1, S_2)	Ideal	IRFP260 N
Diodes (D_1 – D_4)	Ideal	HFA15PB60
Multiplier Diodes (D_{M1}, D_{M2})	Ideal	MUR880EG
Output Diodes (D_{S1}, D_{S2})	Ideal	MUR880EG
MOSFET Drivers	-	TC 4432
Inductors (L_1, L_3)	350 µH	
Inductors (L_2, L_4)	761 µH	
Capacitors(C_1, C_2, C_{M1}, C_{M2}, C_O)	100 µF (electrolytic)	

Fig. 7 shows the simulated waveforms of the voltages in the input, capacitor C_1 and load. In Fig. 8, the experimental results of the input voltage (Ch1), the voltage in the capacitor C_1 (Ch2) and the load voltage (Ch4) are shown to prove the step-up operation of the proposed converter. The behavior of the quadratic converter and the multiplier stage can be checked from this Fig. 10. For the calculated gain, G = 12.5, the voltage across the capacitor C_1 must be equal to V_{C1} = 60 V. At rated load condition, it confirms the capacitor, C_1 and load voltages are within the predicted values in the theoretical analysis.

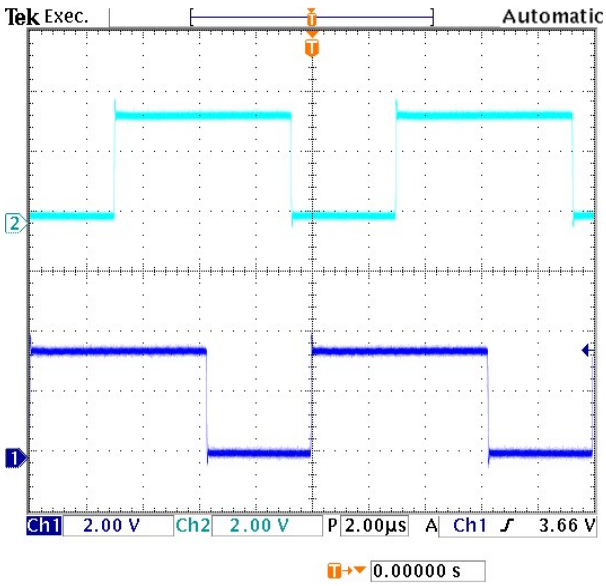

Fig. 6. Gating pulses of Switches S_1, S_2

One of the advantages of interleaving effect in converters is to increase the frequency of current ripple and voltage at input and output of the converter. This increased frequency implies the lower values of passive components, which is used to build filters to eliminate electromagnetic interference and noise. Fig. 9 shows the simulation results of the currents in the input inductors and the supply current. Fig. 10 shows the currents in input inductors I_{L1} sampled at Ch1 and I_{L3} sampled at Ch2. Due to interleaving effect, the input current, sampled in Ch3 has less ripple.

Fig. 11 depicts the current on the switch S_1, I_{S1} sampled at Ch1 and on the diodes I_{DS2} sampled at Ch2 and I_{DM2} sampled at Ch3. In certain stages of the converter, the elements store energy and it will be discharged on subsidiary elements. Necessary steps have to be done that the increased voltage will not damage the components in the converter.

It can be seen in Fig. 11, that the current in the switch S_1 is similar to the waveform obtained in theoretical analysis. Since the two quadratic arms are symmetrical in nature, the current through switch S_2 will be similar to the current through switch S_1.

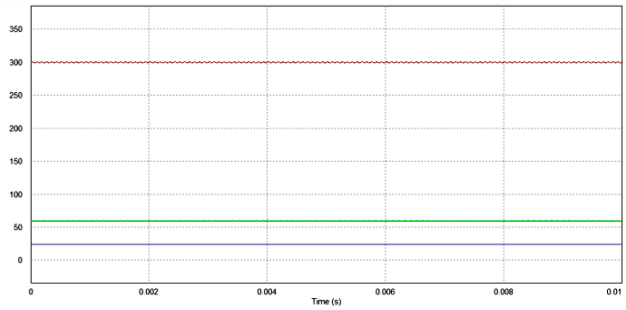

Fig. 7. Simulated waveforms of V_i, V_{C1} and V_O

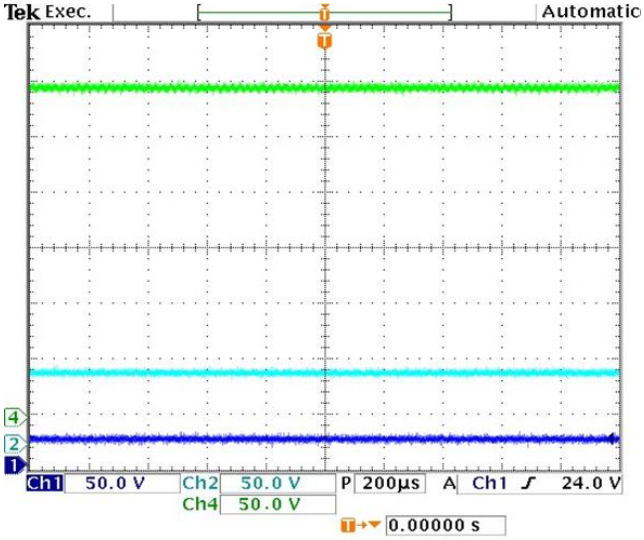

Fig. 8. Experimental waveforms of V_i (Ch1), V_{C1} (Ch2) and V_O (Ch4)

The proposed converter is tested in the power range of 150 W to 500 W. The input power and output power is measured by using general purpose watt meters available in the laboratory. Fig. 12 shows the converter efficiency values for the various output power. Considering a region of 360 W to 440 W, which corresponds to the – 10% to + 10 % of the nominal power, the obtained efficiency is 90 % to 91.5 %.

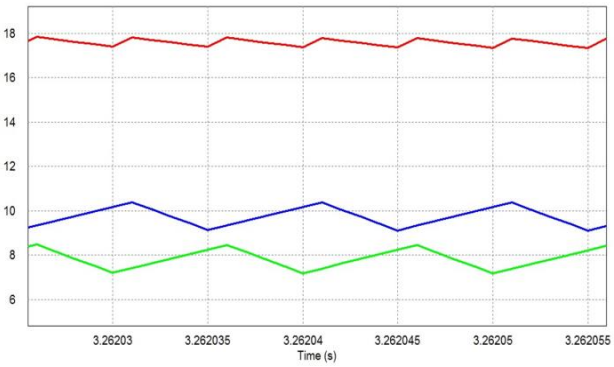

Fig. 9. Simulated waveforms of I_{L1}, I_{L3} and I_i

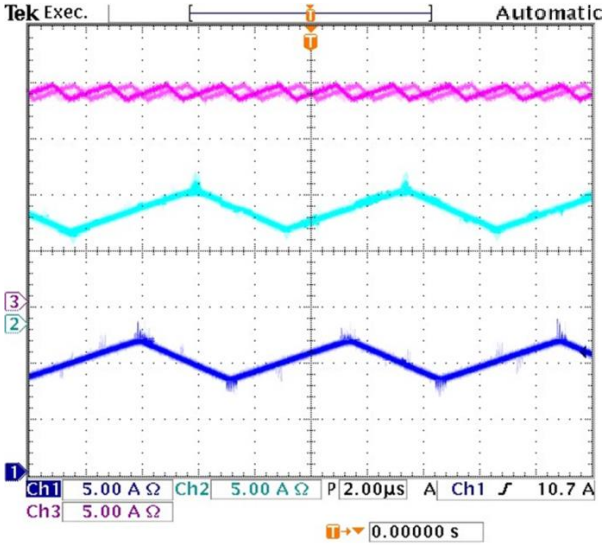

Fig. 10. Experimental waveforms of I_{L1} (Ch1), I_{L3} (Ch2) and I_i (Ch3)

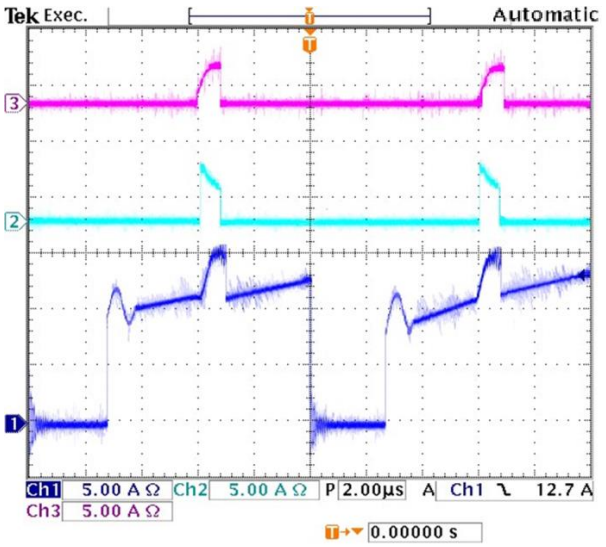

Fig. 11. Experimental waveforms of current I_{S1} (Ch1), I_{DS2} (Ch2) and I_{DM2} (Ch3)

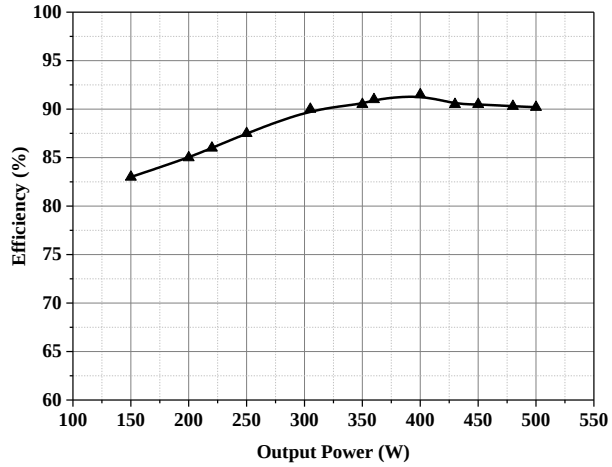

Fig. 12. Converter efficiency

6. Conclusion

The design and performance of an interleaved quadratic boost converter with voltage multiplier is described in this paper. The use of interleaving technique shows an improvement in the reduction of current ripple and consequent conduction losses in the switches, maintaining a low ripple of the input current, resulting in higher conversion efficiency compared to non-interleaved quadratic converters. A method for combining interleaved quadratic converters and voltage multiplier to elevate the voltage gain with low ripple amplitudes has been successfully demonstrated in this paper, which makes it suitable for applications where high step-up gain is required. Compared with the other high gain converters, the proposed converter has the highest voltage gain and the lowest switch voltage stress. The experiment results verify the theoretical analysis and effectiveness of the proposed converter. The main drawback of the converter is low efficiency; however, it can be improved with the adoption of regenerative or dissipative snubbers.

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