

Improved Response of Closed Loop Controlled Three Phase CBBC Fed SLI System Using FOPID Controller

R.Umamageswari¹, C.R.Balamurugan², T.A.Ragavendiran³

Research Scholar, Department of Electrical and Electronics Engineering, Anna University, Chennai.
Professor, Department of Electrical and Electronics Engineering, Karpagam College of engineering, Coimbatore.

Research Supervisor, Department of Electrical and Electronics Engineering, Anna University, Chennai.
umaravi2527@gmail.com

Abstract—As of late, fell buck-help converter with a multilevel inverter is an elective framework between DC source and engine. DC from PV framework is helped to utilize Buck-Lift Converter (BBC). The yield of BBC is modified utilizing Seven Level Inverter (SLI). The yield of SLI is utilized to drive a three stage enlistment engine. This paper completely explores shut circle effect of fell buck support converter multilevel inverter structure together with PI and FOPID controllers. The major objective of this proposed converter is to effectively carry out the speed of the acceptance engine drive in a quick manner. In order to carry out the research in a proper manner, simulink models are constructively generated for the effective functioning of PI and FOPID controlled BBCSLI frameworks. With the aim of demonstrating the working and its effectiveness, Matlab is employed for formulating an enhanced dynamic execution through the utilization of FOPID controller. It must be observed that the equipment for BBCSLI is formulated and effectively tested its working on several circumstances. The formulated equipment shows its effectiveness in almost all the circumstances and its effect in the overall output seems to very convincing. All the results are effectively carried out with utmost care and its results are recorded and shown in the simulation results. The simulation result proves the effectiveness of the proposed framework.

Keywords—New Topology of MLI, Fundamental Switching Frequency, PWM, THD,

I. INTRODUCTION

Inverter is an electrical device, which is used to transform direct current (DC) effectively to alternate current (AC). Its application ranges from emergency backup power to some aircraft systems for the purpose of transforming DC power to AC.

At present, a lot of industrial applications have initiated to use high power. Particular appliances in the industries on the other hand have need of medium or low power for their consistent working. Exploitation of a high power source for entire industrial motors possibly will prove advantageous to certain motors requiring high power, whereas it might destruct the other loads. Quite a lot of medium voltage motor drives and normal applications have requirement of medium voltage. For this purpose, multi-level inverter has been introduced during 1975 as substitute in high power and medium voltage situations. The Multi-level inverter is similar to an inverter and it is purposefully employed for industrial applications as a substitute in high power and medium voltage circumstances.

It must be taken into account that the three-level converters were prominently displayed in the standard of multi-level inverter. A multilevel converter is a kind of power electronic formulation that effectively combines a pinned for the purpose of yielding voltage from a twosome level of dc voltages by way of information sources. It must be observed that with a prolonging number of dc voltage sources, the range of converter yield voltage waveform marches towards a pattern

of sinusoidal wave, despite the fact that using an indispensable repeat trading procedure. The preferred viewpoint of multi-level inverter might be its small amount of yield voltage, which competently responsible for the more yield quality, moreover it effectively diminishes the consonant segment, improved electromagnetic calculability, and considerably lowering the exchanging losses [1, 2]. Despite the fact that a wide range of formulated multi-level inverter topologies at present, only the two common and more effective topologies which are taken into consideration are the fell H-connect inverter together with its derivatives [3] and the Diode-clamped inverter [4]. The principal in good position of the two topologies is to be noted that the assessment of the swap among devices is reduced to a certain extent to the rating of each cell. It must be taken into consideration that they have the obstacle of the vital huge number of swapping devices which squares with $2[k - 1]$, in which k represents the quantity of levels. This quantity is extremely high and possibly will inflate the circuit to several-sided quality, and moreover diminish its unwavering quality and efficiency.

In general, the framework or organization of Fell H-connect inverter is more of a modularized strategy and the major concern of the dc interface voltage unbalancing does not happen, in this way effectively extended to multilevel. Because of these points of interest, fell H-connect inverter are typically attached with the kind of applications like SVC, HVDC, high power engine drives and stabilizers. Furthermore, it is to be observed that Diode-supported inverter requires only a solitary dc-transport and the voltage levels are made by a couple of capacitors in strategies that tract the dc transport voltage into a sequences of capacitor voltages. Moreover, fine-tuning of the capacitors is cluttered all over the place in predominantly number of levels. Besides, it is known fact that three-stage form of this topology is extremely complicated to execute because of the unbiased point regulating complications. It is to be observed that the outcome waveforms of these inverters are in a wandered nature; henceforth they have moderately diminished sound. In order to drop the sounds further, bearer dependent PWM approaches are suggested in the literature [5]. The emerging Topologiessuchasmultilevelinverters (MLI) are capable of generating high quality waveforms of voltage (stepped in nature) with reduced distortion in harmonics (less THD), at low switching frequency, using the IGBTs/MOSFETs devices having low current and voltage ratings and generation of low dv/dt on switches [6-7]. As per IEEE 591 standard the THD of the injected currents should not exceed 5%. To obtain such a fine quality output voltage, the inverter switching frequency is kept at high value [8], [9]. However, high switching frequency causes higher switching losses which results in lower efficiency. The problem is more serious in large scale solar PV plants as the thermal losses could damage the switching devices. Lower switching frequency further reduces the switching losses

which makes the proposed solution to integrate large scale PV system in the grid more attractive.

II. SYSTEM DESCRIPTION

Piece Graph of existing BBCTPSLI framework with PI controller is given in Figure 1. The yield of PV is helped utilizing BBC. The yield of BBC is changed over to three stage utilizing TPSLI which nourishes a three stage acceptance engine. The engine speed of acceptance engine is detected and it is contrasted with the reference speed with create speed blunder. The speed blunder is connected to a PI controller. The yield of PI is given to the beat generator.

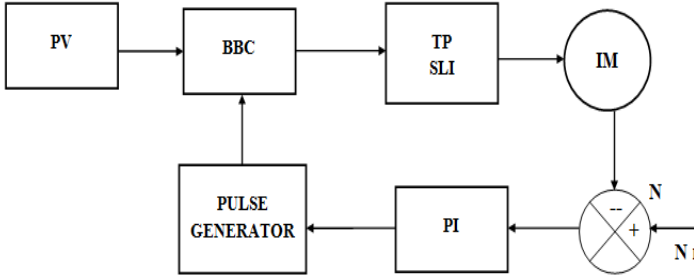


Figure 1: Block Diagram of Existing System

The Piece outline of the proposed BBCTPSLI framework has appeared in Figure 2. The PI controller is supplanted by FOPID controller.

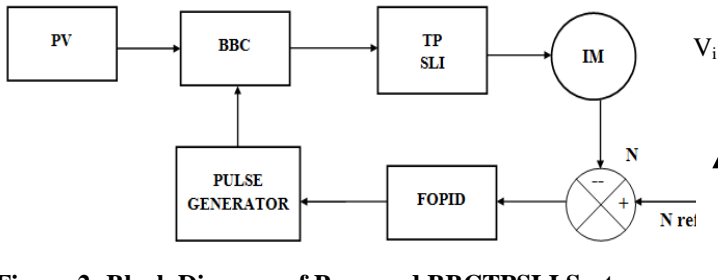


Figure 2: Block Diagram of Proposed BBCTPSLI System

III. RESEARCH GAP

The above writing does not manage FOPID controlled BBCTPSLI framework. The above papers don't report the examination of PI and FOPID controlled BBCTPSLI framework. This work proposes FOPID for the control of shut circle BBCTPSLI framework. This work proposes BBCTPSLI for the control of three phase induction motor.

IV. SIMULATION RESULTS

i. Closed Loop BBCTPSLI system PI controller

Shut circle BBCTPSLI framework with PI controller is appeared in Figure 3.1. The real speed of acceptance engine is contrasted and the reference speed of IM. The speed blunder is connected to a PI controller. The yield of PI is given to three comparators. The beats from comparator are given to the switches of BBC in each Stage. Figure 3.2 displays the info voltage and its esteem is found to be 210 V. Figure 3.3 shows the yield voltage of buck support converter and its esteem is determined to be 400V. Figure 3.4 displays the engine speed and its esteem is found to be 1100 RPM. Figure 3.5 displays the yield voltage of three stage inverter and its pinnacle esteem is determined to be 800 V. It might be noticed that the speed and torque are directed.

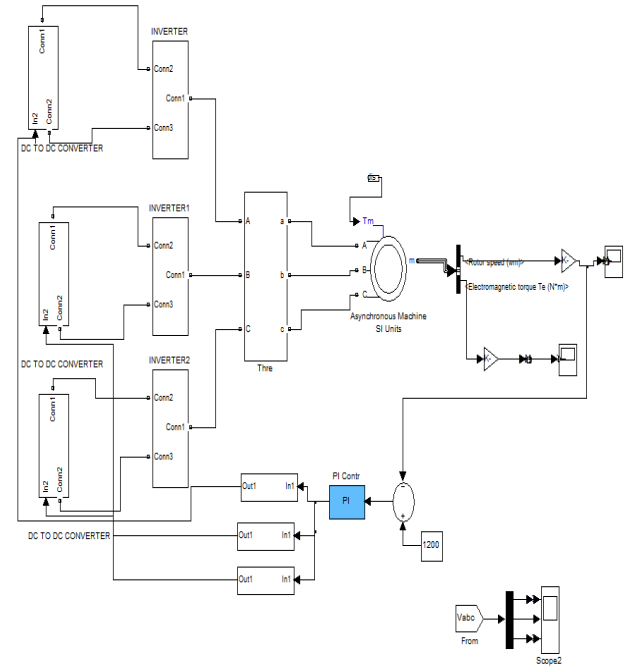


Figure 3.1: Architecture of Closed Loop BBCTPSLI together with PI Controller Module

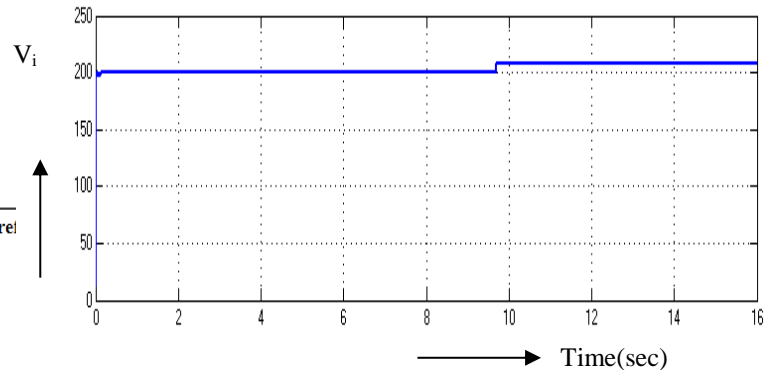


Figure 3.2: Input Voltage of BBCTPSLI System with PI Controller Module

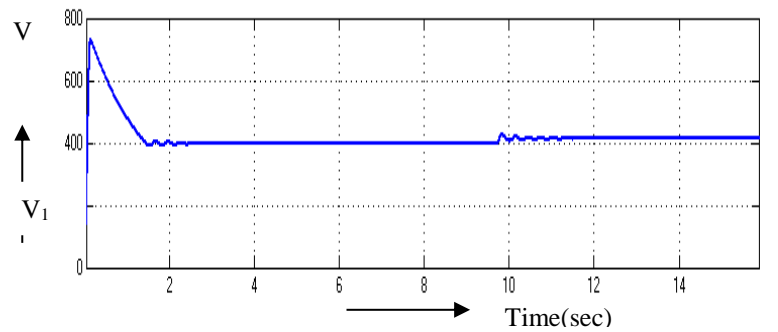


Figure 3.3: Output Voltage of BBCTPSLI System with PI Controller Module

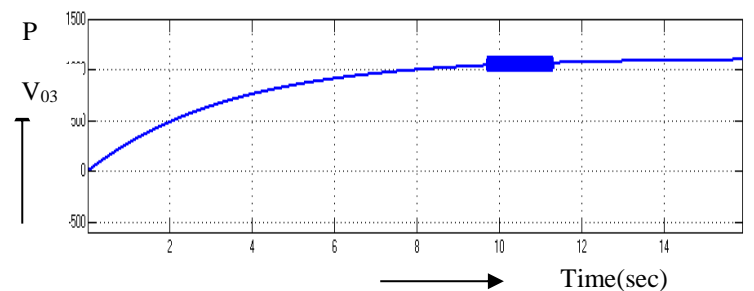


Figure 3.4: Motor Speed of BBCTPSLI System with PI Controller Module

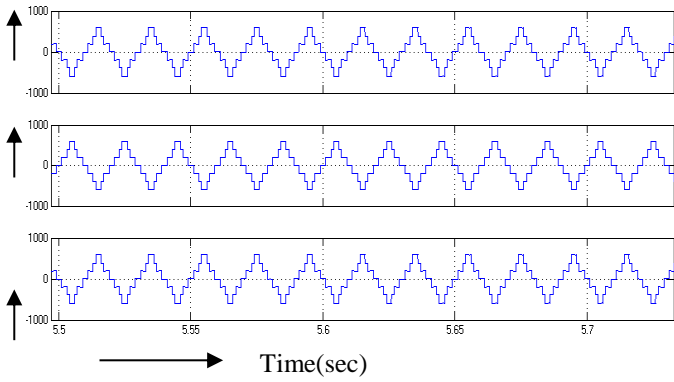


Figure 3.5: Output Voltage of BBCTPSLI System with PI Controller Module

ii. Closed Loop BBCTPSLI System together with FOPID Controller Module

The Shut circle BBCTPSLI framework with FOPID controller is appeared in Figure 4.1. The PI controller is presently supplanted by FOPID controller. The info voltage is appeared in Figure 4.2 and its esteem is 210 V. Figure 4.3 displays the yield voltage of the buck-boost converter and its esteem is determined to be 400V. Figure 4.4 demonstrates the engine speed and its esteem is found to be 1100 RPM. The Yield voltage waveforms of three-stage inverter are appeared in Figure 4.5 and the pinnacle esteem is 800 V. The examination of time space parameter is appeared in Table-1

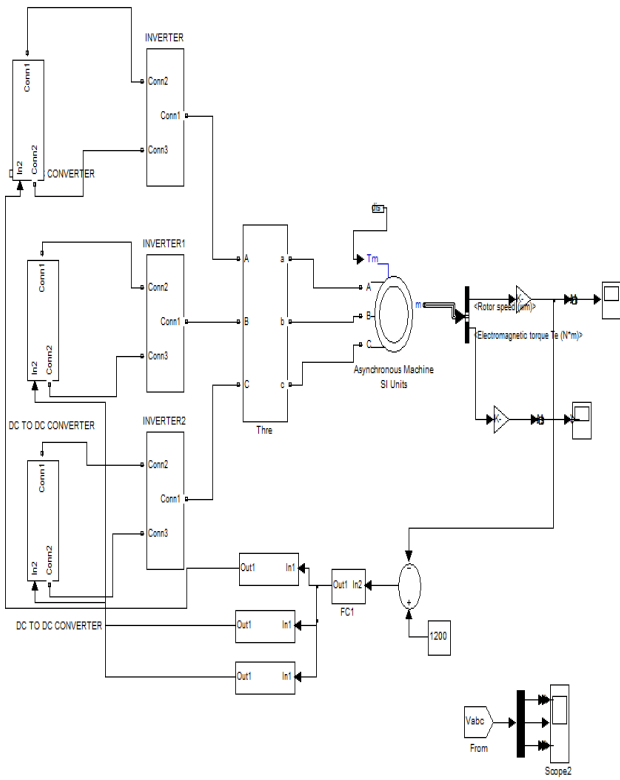


Figure 4.1: Closed loop BBCTPSLI System with FOPID Controller

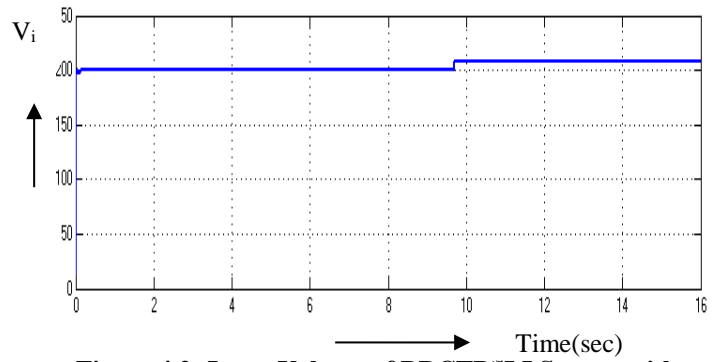


Figure 4.2: Input Voltage of BBCTPSLI System with FOPID Controller

Rise time is decreased from 9.9 to 9.7 sec, Pinnacle time is diminished from 10.3 to 9.9 sec, settling time is lessened from 11.3 to 10.6 sec and enduring state blunder in speed is diminished from 8.2 to 5.8 RPM by supplanting PI with FOPID controller.

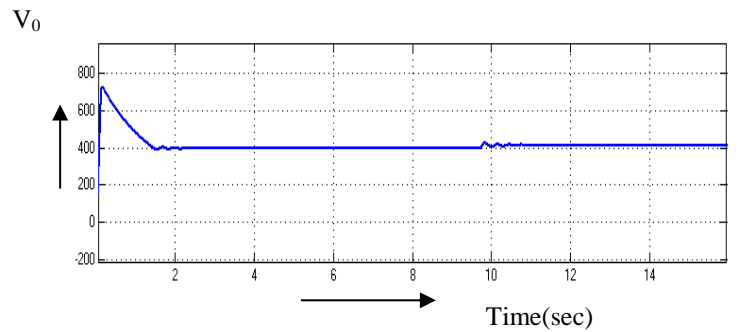


Figure 4.3: Output Voltage of BBCTPSLI System with FOPID Controller

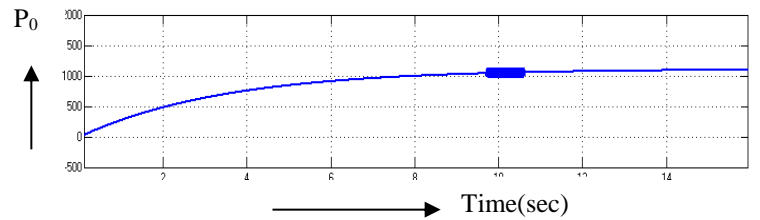


Figure 4.4: Motor Speed of BBCTPSLI System with FOPID Controller

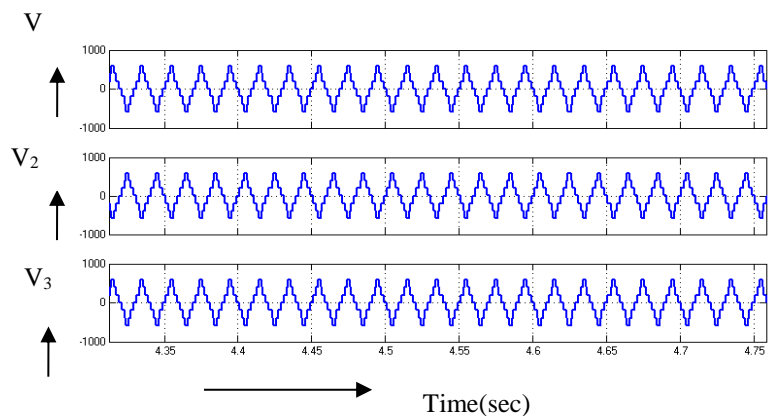


Figure 4.5: Output Voltage Waveform of BBCTPSLI System with FOPID Controller

Table-1
Comparison of Time Domain Parameters

Controller Type	Rise Time (sec)	Peak Time (sec)	Settling Time (sec)	Steady State Error (RPM)
PI	9.9	10.3	11.3	8.2
FOPID	9.7	9.9	10.6	5.8

IV. CONCLUSION

Fell buck-support converter multilevel inverter framework controlled by PI and FLC are displayed and recreated utilizing Simulink. The recreation consequences of open circle framework, shut circle framework with PI and FOPID are completely demonstrated. It is observed from the results that the settling time is considerably lessened to 10.6 sec and relentless state mistake is effectively decreased to 5.8 RPM with the assistance of utilizing FOPID controller. As a result, the complete outcome of FOPID controlled BBPSLI framework is comparatively far better than the PI controlled BBPSLI framework. The major positive aspects of the proposed framework are its low symphonious substance and speedy response. The noteworthy demerits are its very reasonable in case of low power circuits and it involves additional amount of switches.

This work manages the examination of reactions with PI and FOPID controlled BBCTPSLI framework. The correlation amongst FOPID and PR controlled frameworks will be done in future.

REFERENCES

- [1]. J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, IEEE Transactions on Power Electronics, Vol.no. 19, pp- 491, (2004).
- [2]. J. Rodriguez, J.-S. Lai, and F. Zheng, IEEE Transactions on Industrial Electronics, Vol.no. 49, pp- 724, (2002).
- [3]. V. G. Agelidis and M. Calais, Application specific harmonic performance evaluation of multicarrier PWM techniques, Proc. IEEE PESC'98 (1998), Vol. 1, pp. 172–178.
- [4]. K. Corzine and Y. Familant, IEEE Transactions Power Electron., Vol.no.17, pp-125, (2002).
- [5]. X. Yuan and I. Barbi, IEEE Transactions Power Electron. Vol.no. 15, pp-711, 2000.
- [6]. "Modular multilevel converters and other multilevel converter topologies and applications," 2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE), Jun. 2014.
- [7]. J. Rodriguez, J. Pontt, E. Silva, J. Espinoza, and M. Perez, "Topologies for regenerative cascaded multilevel inverters," IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.
- [8]. M. Metry, Y. Liu, R. S. Balog, and H. Abu-Rub, "Model predictive control for maximum power point tracking of quasi-Z-source inverter based grid-tied photovoltaic power system," 2017 IEEE 26th International Symposium on Industrial Electronics (ISIE), Jun. 2017.
- [9]. C.Bharatiraja, R.Latha, S.Jeevananthan, S.Raghu and S.S. Dash, "Design And Validation Of Simple Space Vector PWM Scheme For Three-Level NPC– MLI With Investigation Of DC Link Imbalance Using FPGA -IP Core ", Journal of Electrical Engineering , vol.13, no.1, pp 54-63, March 2013.
- [10]. M. Tolbert and T.G. Habetler, IEEE Trans. Ind. Appl. Vo.no.35, pp- 1098 ,1999.
- [11]. H. S. Patel and R. G. Hoft, IEEE Trans. Ind. Appl. Vol.no.3, pp-310, 1973.
- [12]. J. N. Chiasson, L. M. Tolbert, K. J. Mckenzie and Z. Du, IEEE Transactions Control System Theory, Vol.no. 11, pp-345, 2003.
- [13]. J. Sun and I. Grotstollen, Pulsewidth modulation basedon realtime solution of algebraic harmonic elimination equations, Proceedings 20th Int. Conf. Ind. Electron. Contr. Instrum. IECON (1994), pp. 79–84.
- [14]. J. N. Chiasson, L. M. Tobert, K. J. McKenzie and Z. Du, IEEE Trans. Power Electron. Vol.no. 19, pp- 478, 2004.
- [15]. F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," 2010 Int. Power Electron. Conf: - ECCE Asia -, IPEC 2010, pp. 492–501, 2010.