NEW SELF-BOOST (Z-SOURCE) AND BOOST DC-AC CONVERTER TOPOLOGIES

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PREFACE

In many non-pollutant, enviroment friendly electrical energy generation systems (wind turbines, solar pannels, fuel-cells etc.) the obtained output dc voltage level varies in a large range. Before making this dc voltage grid compatible ac voltage usually we use a DC-DC converter which delivers a constant dc voltage regardless of the fluctuating dc input voltage. Another way to control the dc voltage level is to use a Z-source network in the dc-ac converter's dc-link. Thus two things get solved in one stage: the dc voltage level used in the inverter modulation algorithm is kept under control and the desired ac output voltage is obtained.

The thesis deals with this recently proposed Z-source network as the dc-link circuit in DC-AC converters between the dc voltage source and the single/ three-phase inverter bridge which can boost the input voltage to any desired level without any extra additional switch. The boost is realised with the shortcircuit of all the inverter bridge switches. It proposes three new Z-source inverter topologies with reduced switch count: one single phase and two three-phase Z-source inverter topologies. In the detailed analysis of these Z-source inverter topologies throughout the thesis the reader, besides the voltage and current relationships of the different operating states of these Z-source inverter topologies, can find details regarding the control algorithms and practical implementation issues and solutions as well as simulation and experimental results in open and closed loop. The thesis also proposes a improved control algorithm of the hybrid switched-capacitor DC-AC PWM converters. The proposed improved control is verified through digital simulations and experiments which validate the theory of the proposed improved control.

OUTLINE OF THE THESIS

The thesis comprises five chapters that unfolds as follows:

The first chapter after the brief presentation of the main formulae describing the operation of a Z-source inverter it presents the single-phase Z-source inverters with four switches and after that a new two-switch single-phase Z-source inverter is proposed and analysed in details. Digital simulations and experimental results validate the proposed topology at the end of this chapter.

The second chapter deals with a proposed four-switch three-phase Z-source inverter. The theoretical background, starting from the traditional four-switch three-phase inverter, necessary to understand the operation of the new topology is followed by some details regarding the implementation of the control on a low cost dsp and finally simulation and experimental result are presented.

After the first two chapters, hopefully, the reader has become familiar with the Z-source inverter topologies in order to be able to cope with the delicate issues and control aspects of the Z-source inverters presented in chapter four. This chapter addresses the following main topics: maximum voltage boost, shoot-through state generation (software and hardware implementation), Z-source inductor and capacitor design.

In chapter four the new proposed improved four-switch three-phase Z-source inverter (obtained from the re-arrangement of the Z-source topology elements presented in chapter two) is described and validated through digital simulations.

In the last chapter a improved SVM algorithm, which lowers the inverter bridge voltage stress and optimizes the voltage gain, for switched-capacitor DC-AC converters is presented and validated through simulations and experiments.

Acknowledgement

I wish to thank Prof. Ion Boldea and Prof. Nicolae Muntean for providing academic guidance and an opportunity to perform this research work at Politehnica University of Timisoara and at Aalborg University.
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Timişoara, September 30th, 2010
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Summary,
The thesis deals with the recently proposed Z-source network as the dc-link circuit in DC-AC converters between the dc voltage source and the single/ three-phase inverter bridge which can boost the input voltage to any desired level without any extra additional switch. The boost is realised with the shortcircuit of all the inverter bridge switches. It proposes three new Z-source inverter topologies with reduced switch count: one single phase and two three-phase Z-source inverter topologies. The thesis also proposes a improved control algorithm for the hybrid switched-capacitor Cuk and Sepic derived DC-AC PWM converters.

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OBJECTIVES OF THE THESIS

The objectives of the thesis can be summed up as follows

- Comprehensive study and presentation of the Z-source network based converters
- Design of new Z-source network based single and three-phase inverter topologies with reduced number of switches
- Analytical description of the new topologies
- Validation of the new proposed topologies through digital simulations and experiments
- Study of the switched-capacitor hybrid DC-AC PWM converters with high voltage gain
- Development of a improved SVM algorithm, in terms of reduced voltage stress of the inverter bridge and optimal voltage gain, of the switched-capacitor hybrid DC-AC Cuk and Sepic derived topologies.
- Validation of the proposed improved SVM algorithm through digital simulations and experiments

CHAPTER 1 SINGLE-PHASE Z-SOURCE INVERTERS

1.1 Introduction

One of the major problems in single-phase voltage source inverters, having in the input stage batteries, photovoltaic, and fuel cells or a diode rectifier fed by the 230 V ac line, is the dc-link voltage level, which could be smaller than the desired level, imposed by the application. Single-phase voltage source inverters are used in photovoltaic or fuel cell grid-connected inverter systems as well as in inverter based motor drive systems. A growing interest is also shown in the field of hybrid electric vehicles.

Some of the solutions to boost the dc-link voltage are transformer-less boost circuits or circuits with high frequency transformers which are introduced between the dc voltage source and the inverter [1]-[3]. The well-known half-bridge inverter's [4] peak ac output voltage is limited to half the dc voltage. In [2][3] this limited peak output voltage is exploited.

A great amount of the produced electrical energy is consumed in heating, air conditioning and ventilation systems. The use of variable-speed drives in these application increases the cost of the system even though they make them energy efficient. For the above mentioned consumers the use of fixed-step drives is also suitable and less expensive.

The cost reduction of fixed step-drives can be approached from two directions: optimization of the static converter and optimization of the motor. The optimization of the converter can be done by reduction of the number of switches [7][8] and the optimization of the motor by the use of cheaper (cheaper to produce) single-phase motors instead of three-phase ones [9]-[11].

The passive Z-source network as a filter and self-boost network was proposed by F. Z. Peng in 2003 [1]. Up to today several studies have been carried out on Z-source network inverters with fuel cells, photovoltaic panels, ultracapacitors, wind turbines or combinations of these [6][13]-[16][19][21][26]. All these studies are related to the field of renewable energy or hybrid vehicles. In the aforementioned studies the Z-source network is in the main power flow path from the input to the output but it can be also used for voltage sag/swell compensation [25] or even for electronic loads [28].

The majority of the studied topologies are for three-phase output voltage and just a few for single phase [15][22]-[24]. The single-phase Z-source inverter for uninterruptable power supplies (UPS) proposed in [22] pointed out the competitive effeciency compared to traditional UPS topologies.

New topologies [5][18][27] were derived from the Z-source network proposed by Peng.

Details regarding the voltage control in the Z-source network based on PI and hysteresis controller can be found in [12][17].

The main reasons why the Z-source network seems to be a good choice for the intermediate circuit between the dc-link voltage and the inverter are the following:

- it provides a greater voltage than the dc link voltage if it is necessary
- it makes the inverter immune to short circuits produced by the conduction of both transistors on the same phase leg (caused by EMI or bugs in the control software of the transistors)
- it forms a second order filter and handles the undesirable voltage sags of the dc voltage source [1]-[7].

1.2 Four-Switch Single-Phase Z-Source Inverter

Figure 1.1. presents the electrical circuit of the Z-source network connected to a single-phase full bridge inverter. The diode D at the front end of the Z-source network makes the circuit unidirectional. The electrical energy flows from the DC voltage source to the load.

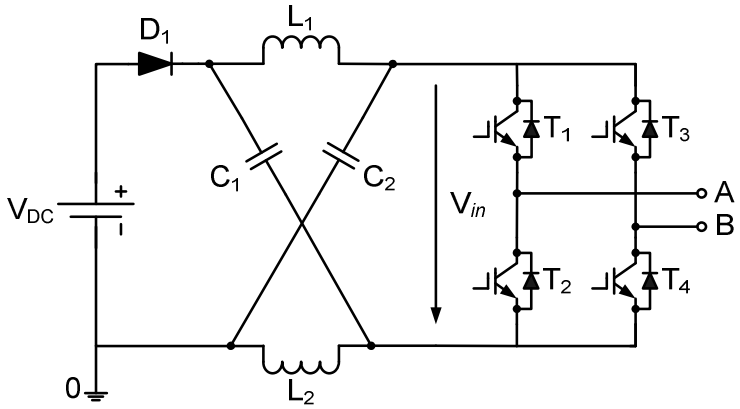


Figure 1.1 Four-switch single-phase Z-source inverter

1.2.1 Principle of Operation. Voltage Gain

The four-switch single-phase Z-source inverter has two main operating states: one active state (also called the non-shoot through state) charactarized by the modulation of the dc-link voltage V_i by the four switches T_1-T_4 to obtain a desired voltage waveform and frequency at the A and B output terminals and one shoot-through state charactarized by the conduction of at least both transistors in one phase leg to boost the average dc-link voltage V_i. The two equivalent circuits corresponding to the two operating states of the single-phase Z-source inverter are shown in Figure 1.2.

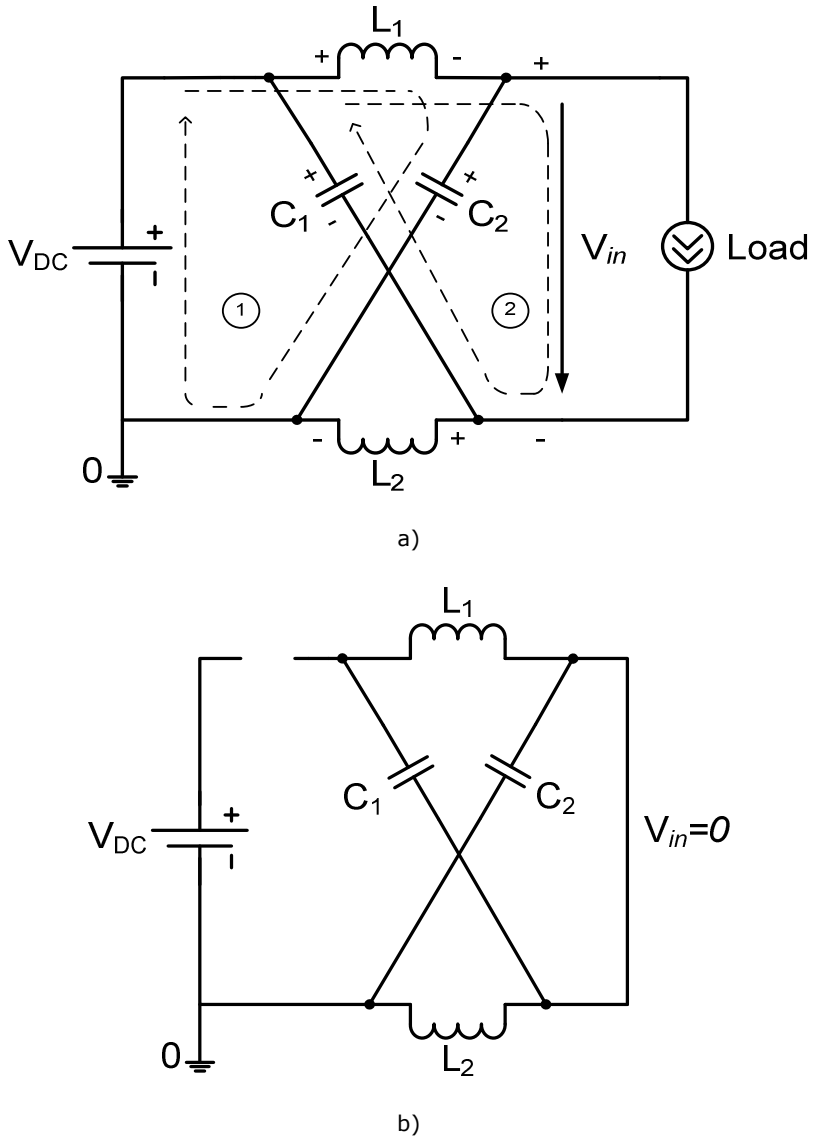


Figure 1.2 Equivalent schemes of the four-switch single-phase Z-source inverter in (a) active state (non-shoot through state) and (b) shoot-through state.

In the active state the load is simbolized by a current source. Now assume that the load is large enough and the average current of the load goes through the diode D which was substituted with a wire. We will see later that for a lighter load the converter has a third state the pseudo-active state. In this state the desired output voltage waveform and voltage frequency can be obtained by applying one of the well-known PWM modulation techniques: unipolar pulse width modulation or bipolar pulse width modulation. During this state in steady-state operation mode the average V_{in} voltage is equal with the average voltage across capacitors C_1 and C_2.

Assuming $C_1=C_2=C$ and $L_1=L_2=L$ ($v_{C1}=V_{C1}=V_C$ and $V_{L1}=V_{L2}=V_L$) in the equivalent schemes and applying Kirchhoff's voltage law in Figure 1.2a on the voltage loops 1 and 2 (drawn with dotted line) we get

$$v_L = V_{DC} - \overline{v_C} \tag{1.1}$$

$$v_{IN} = \overline{v_C} - v_L \tag{1.2}$$

Substituting the expression of v_L from (1.1) into (1.2) the dc-link voltage will be

$$v_{IN} = \overline{v_C} - \left(V_{DC} - \overline{v_C}\right) = 2\overline{v_C} - V_{DC} \tag{1.3}$$

In the shoot-through state in Figure 1.2b the Z-source network voltages across the inductors are equal with the voltages across the capacitors

$$v_L = \overline{v_C} \tag{1.4}$$

A line appearing over a term indicates the average value of that term, terms written with small letters and capital subscript indicate instantaneous values of that term and terms written with capital letters and capital subscript indicate that we are dealing with continuous terms.

Both states of the four-switch single-phase Z-source inverter are present during one switching period. Now, with t_{ST} being the time duration of the shoot-through state and T_s-t_{ST} the time duration of the active state the average voltage across the inductors during one switching period T_s can be expressed as

$$\overline{v_L} = \frac{(T_s - t_{ST})\left(V_{DC} - \overline{v_C}\right) + t_{ST}\overline{v_C}}{T_s} \tag{1.5}$$

Knowing that in steady state the average voltage across the inductors is zero

$$\overline{v_L} = 0 \tag{1.6}$$

with the duty ratio of the shoot-through state

$$D_{ST} = \frac{t_{ST}}{T_s} \tag{1.7}$$

from equation (1.5) we get the relationship between the average voltage on the capacitors $\overline{v_C}$ and the input dc voltage V_{DC} and the shoot-through time t_{ST}

$$\begin{aligned} \overline{v_C} &= \frac{1 - D_{ST}}{1 - 2D_{ST}} V_{DC} \\ D_{ST} &= \frac{\frac{\overline{v_C}}{V_{DC}} - 1}{2\frac{\overline{v_C}}{V_{DC}} - 1} \end{aligned} \tag{1.8}$$

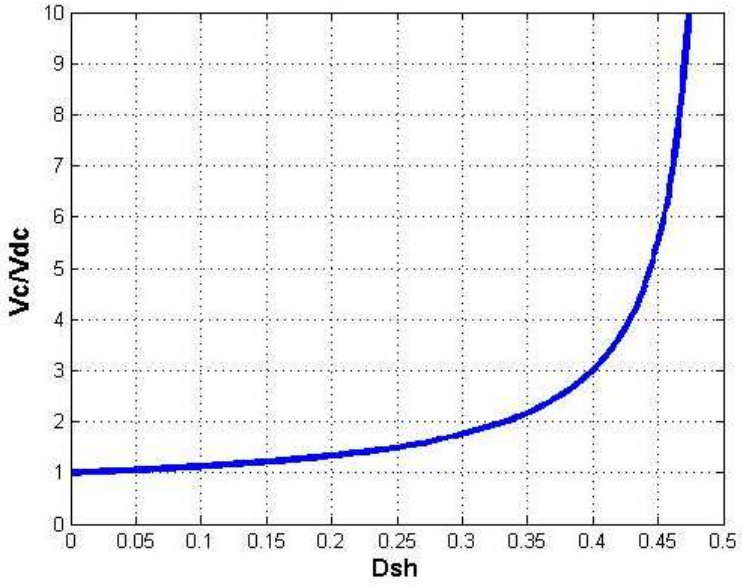


Figure 1.3 Relationship between capacitor voltages $\overline{v_C}$ /dc input voltage V_{DC} and shoot-through time duty ratio D_{ST}

Figure 1.3 and (1.8) clearly show that at a 0.5 shoot-through duty ratio the voltage across the capacitors is infinit, theoretically. In practice measures should be taken to avoide excesive increas of the shoot-through time.

In Figure 1.2b the front-end diode D does not conduct due to the series connection of the inductors which are in parallel with the capacitors thus the diode is inversely polarized. To illustrate this situation better we will redraw the shoot-through state from Figure 1.2b.

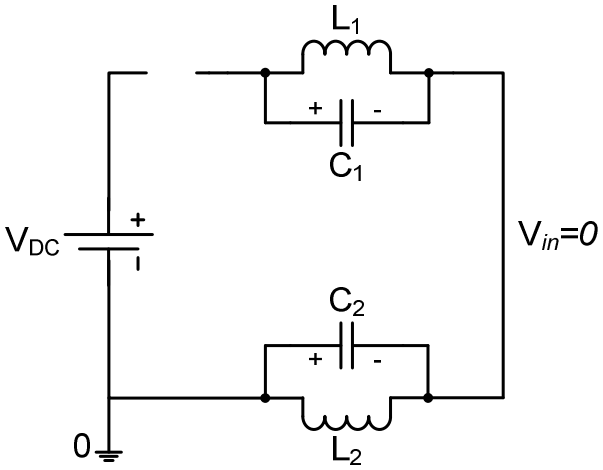


Figure 1.4 Redrawn shoot-through state

Eq. (1.8) shows that the average voltage across the capacitors increases as the shoot-through duty ratio increases but on the other hand the average dc-link voltage $\overline{v_{IN}}$ decreases in the first few switching periods as the duty ratio increases because during the shoot-through time the dc-link voltage is zero. So the average dc-link voltage over one switching period is

$$\overline{v_{IN}} = (1 - D_{ST})(2\overline{v_C} - V_{DC}) \tag{1.9}$$

From (1.9) is obvious that the maximum voltage stress of the four-switch bridge is equal with $2\overline{v_C} - V_{DC}$. Now to reduce the current stress of the inverter bridge the first step would be to drive all the switches simultaneously in the transistor full bridge during the shoot-through time. That is why throughout the whole thesis only this shoot-through state will be considered and any shoot-through state involving only two switches in one or a number less than the total phase legs in the used transistor bridge will be neglected!

For a given shoot-through duty ratio the maximum modulation index is

$$M_{max} = 1 - D_{ST} \tag{1.10}$$

Therefore the maximum average dc-link voltage can be expressed as

$$\overline{v_{IN}} = (1 - D_{ST})^2 (2\overline{v_C} - V_{DC}) \tag{1.11}$$

The peak dc-link voltage across the inverter bridge can be written as (see Figure 1.2a)

$$\hat{v}_{IN} = \overline{v_C} - v_L = 2\overline{v_C} - V_{DC} \tag{1.12}$$

Substituting (1.8) into (1.12) the peak dc-link voltage can be rewritten as

$$\hat{v}_{IN} = \frac{1}{1 - 2D_{ST}} V_{DC} = BV_{DC} \tag{1.13}$$

where

$$B = \frac{1}{1 - 2D_{ST}} \geq 1 \text{ and } 0 \leq D_{ST} \leq \frac{1}{2} \tag{1.14}$$

is the boost factor resulting from the shoot-through zero state. Further, the output peak load voltage from the inverter can be expressed as

$$\hat{v}_{ac} = M \frac{\hat{v}_{IN}}{2} \tag{1.15}$$

where M is the modulation index. Using (1.13) and (1.15) the load peak voltage will be

$$\hat{v}_{ac} = BM \frac{V_{DC}}{2} \tag{1.16}$$

where the product BM is the buck-boost factor. By choosing an appropriate buck-boost factor BM the output voltage can be stepped up or down.

1.3 Proposed Two-Switch Single-Phase Inverter

A new two-switch Z-source network is proposed in order to reduce the number of switches in a single-phase inverter, from four switches in a full-bridge inverter, to only two switches, as well as to maintain the desired average voltage level in the dc-link.The proposed modified Z-source network is presented in Figure 1.5. In many electrical circuits instead of a high voltage rated electrolytic capacitor series smaller voltage rated capacitors are used thus one load terminal can be connected at the common node of two series capacitors. It can be noticed that this change in the Z-source network reduces the number of switches in the inverter bridge. The load is connected between the common node of the two series capacitors and the common node of the two switches. We have to mention here that the load terminal which is connected to the common node of capacitors C_2 and C_3 could be as well connected to the midpoint of two capacitors connected in series replacing capacitor C_1.

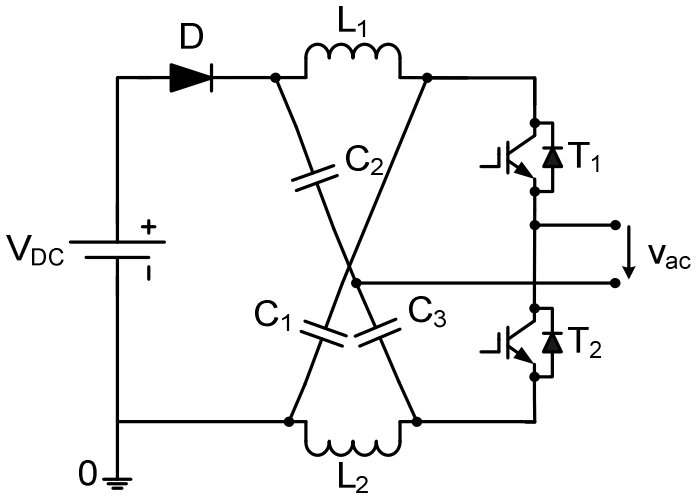


Figure 1.5 Proposed two-switch single-phase inverter

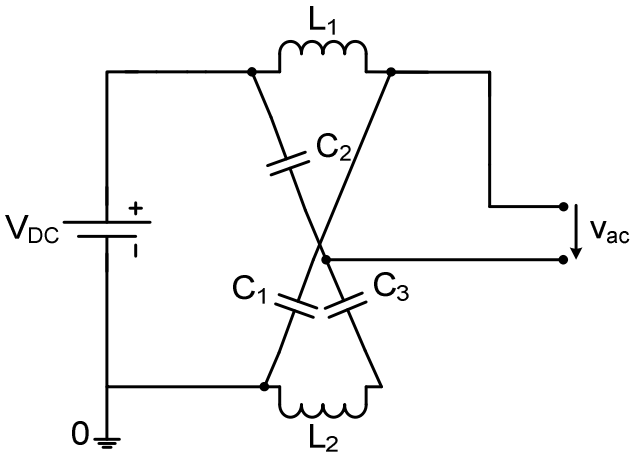
For the above circuit we make the following asumptions:

$$C_1 = C_2 = C_3 = C; L_1 = L_2 = L \text{ and } \overline{v_{C1}} = \overline{v_C}; \overline{v_{C2}} = \overline{v_{C3}} = \frac{\overline{v_C}}{2} \qquad (1.17)$$

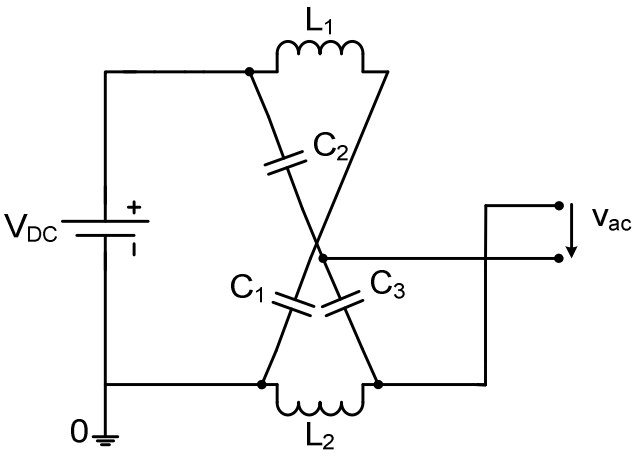
If we write the equation for the voltage across one inductor during one switching period which in steady state is equal with zero one could obtain the same relationship between the input dc voltage and the output voltage as in (1.8). So the voltage gain of the traditional Z-source network with four-switch bridge is also valid for this new single-phase topology.

1.3.1 Principle of Operation

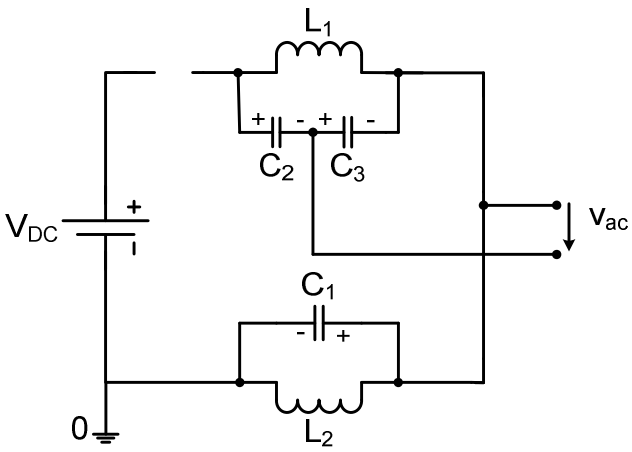
The proposed two switch single-phase Z-source inverter has three different operating states, two active states and one shoot-through state. The three equivalent circuits for the three states are illustrated in Figure 1.6



a)



b)



c)

Figure 1.6 Equivalent circuits of proposed Z-source single-phase inverter for active state 1 b) active state 2 (c) state 3 shoot-through state

Notice that we assumed that during the active states the diode D is always conducting and during the shoot-through state it is blocked. With light loads diode D gets blocked during the active states and the voltage boost relationship between the input voltage V_{DC} and the average capacitor voltages is no more valid. Next the three operating states will be discussed.

[State 1] The converter is in one of the two active states when only the upper transistor T_1 is on. The load voltage v_{ac} can be expressed as

$$v_{ac} = \frac{\overline{v_C}}{2} - v_L \text{ but } v_L = V_{DC} - \overline{v_C} \tag{1.18}$$

thereby the load voltage will be

$$v_{ac} = \frac{3}{2}\overline{v_C} - V_{DC} \tag{1.19}$$

[State 2] The converter is in the other non shoot-through state. The lower transistor T_2 is conducting and the upper transistor T_1 is blocked. The voltage on the load is equal with minus the voltage across capacitor C_2

$$v_{ac} = -\frac{\overline{v_C}}{2} \tag{1.20}$$

[State 3] In this operating state the demanded load voltage boost is realized. Both the upper and the lower switches are conducting, therefore an energy transfer is realized from the capacitors to the inductors. It can be seen that the circuit is asymmetrical (because the load is connected in parallel with the capacitor C_3), so the energy transfer from the capacitors to the inductors is not the same on the upper and on the lower side of the equivalent circuit. In this state the output voltage can be described by

$$v_{ac} = -\frac{\overline{v_C}}{2} \tag{1.21}$$

It is obvious that in the active state 2 and the shoot-through state 3 the instantaneous output voltage is the same. From the expression for the instantaneous output voltages in state 1 and state 2 we see that the instantaneous voltage across the load will not be symmetrical to zero voltage. In other words for different shoot-through duty ratio the proposed single-phase Z-source inverter will not be able to generate the same magnitude peak voltage on the positive and negative side of the output ac voltage for a sinusoidal reference voltage. To overcome this issue in the prescribed output sinusoidal voltage we will inject a continuous component as we will see later on. The amplitude of the injected continuous component will be derived analitically. However with the injected continuous component the output voltage and current at the fundamental output frequency will have no low harmonics.

The average output voltage over one switching period can be described by

$$\overline{v_{ac}} = D_1\overline{v_C} - D_2'\frac{\overline{v_C}}{2} \tag{1.22}$$

where

$$\begin{aligned} &D_2' = D_2 + D_{ST}; \\ &D_1 + D_2' = D_1 + D_2 + D_{ST} = 1; \\ &D_1 = \frac{t_1}{T_s}; D_2 = \frac{t_2}{T_s}; D_{ST} = \frac{t_{ST}}{T_s}; \\ &t_1 + t_2 + t_{ST} = T_s. \end{aligned} \tag{1.23}$$

D_1 - duty cycle of state1

D_2 - duty cycle of state 2

D_2' - duty cycle of state 2 and state3

D_{ST} - duty cycle of the shoot-through state (state 3)

The scope of the control algorithm of the proposed two-switch single-phase inverter is to obtain the two duty ratios of the gating signals of the two switches T_1 and T_2. The two duty ratios can be described by

$$\begin{aligned} D_2' &= \frac{2\left(\overline{v_C} - \overline{v_{ac}^*}\right)}{3\overline{v_C}} \\ D_2 &= D_2' - D_{ST} \\ D_1 &= 1 - D_2 \end{aligned} \tag{1.24}$$

Now in (1.24) we have three equations and four variables. One possible way to solve this issue would be to prescribe not only the output voltage v_{ac} but the average voltage on the capacitors $\overline{v_C}$ also. This would mean to prescribe the capacitor voltages regardless of the prescribed output voltage. The optimum voltage boost could be obtained by somehow corelating the capacitor voltage boost with the prescribed output voltage. In other words to generate as much voltage boost as is

needed to be able to modulate the output voltage with the desired amplitude. The following section will derive the optimum voltage boost.
Using (1.24) the average output voltage will be

$$\overline{v_{ac}} = \overline{v_C} - D_2' \frac{3\overline{v_C}}{2} \tag{1.25}$$

Another form of (1.25), using D_1 instead of D_2' on the right side, looks like

$$\overline{v_{ac}} = D_1 \frac{3\overline{v_C}}{2} - \frac{\overline{v_C}}{2} \tag{1.26}$$

1.3.2 Simulation Results

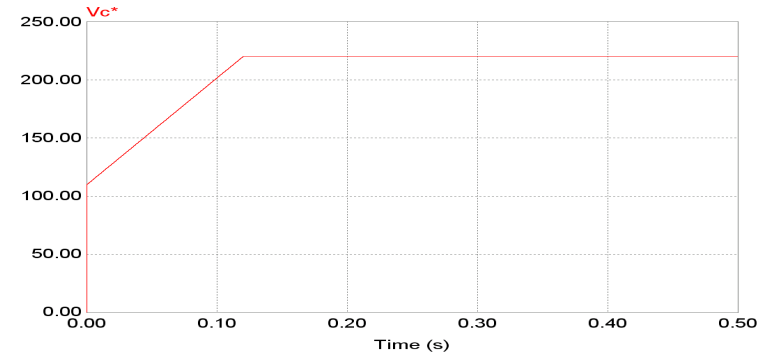


Figure 1.9 Prescribed capacitor voltage waveform across C1

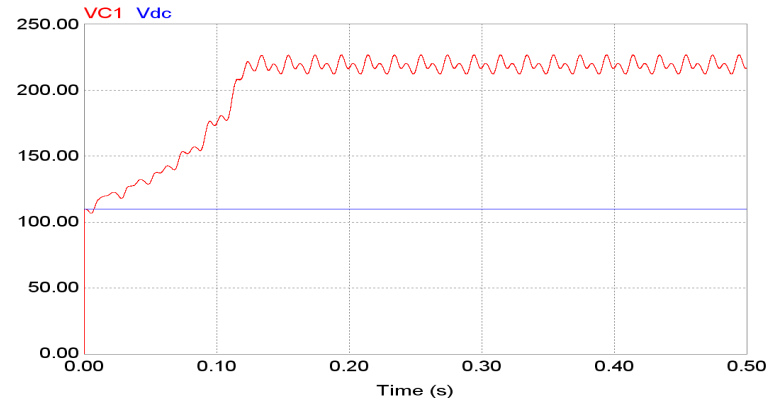


Figure 1.10 Instantaneous voltage waveform across C1 and the input dc voltage

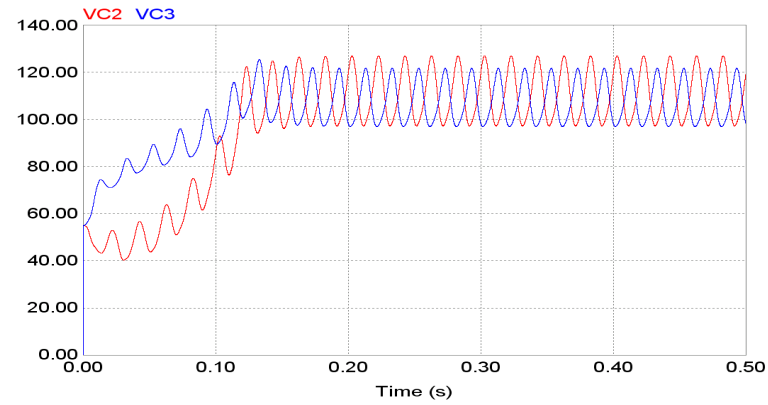


Figure 1.11 Capacitor voltage waveforms across C2 and C3

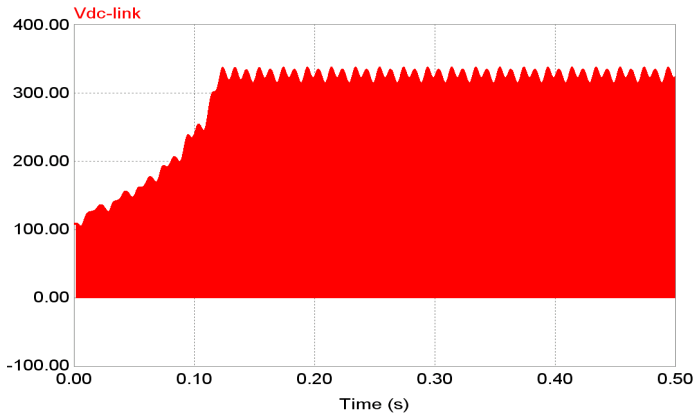


Figure 1.12 Instantaneous voltage waveform across the inverter leg

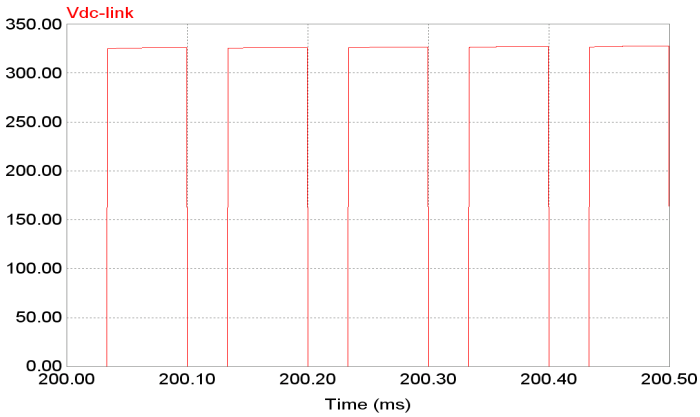


Figure 1.13 Instantaneous voltage waveform across the inverter leg (zoom)

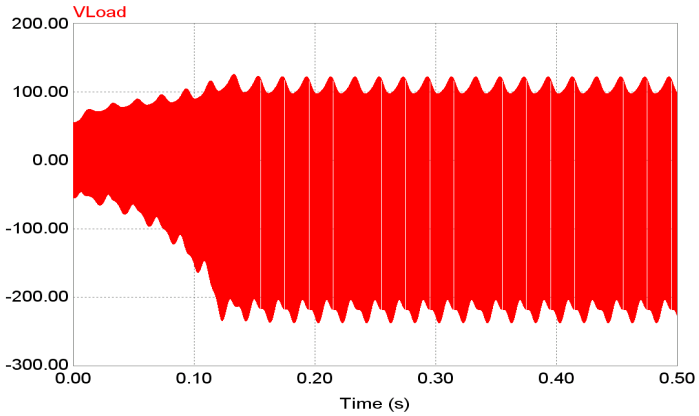


Figure 1.14 Instantaneous load voltage waveform

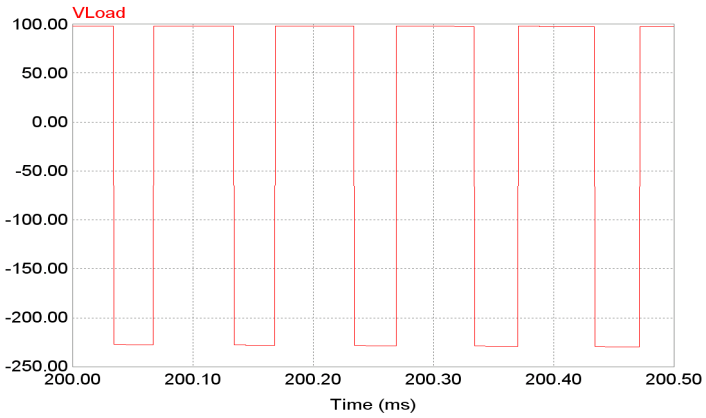


Figure 1.15 Instantaneous load voltage waveform (zoom)

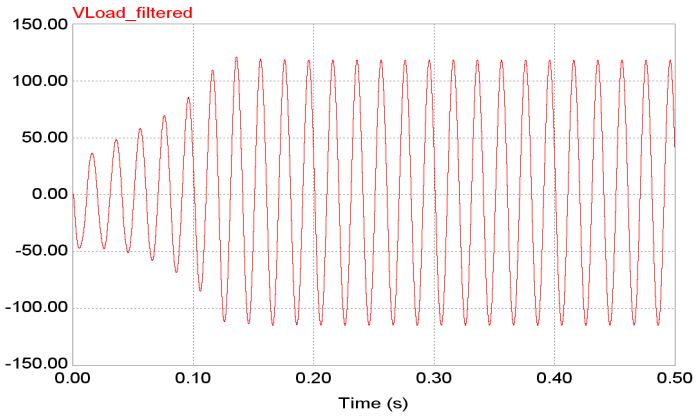


Figure 1.16 Filtered load voltage waveform

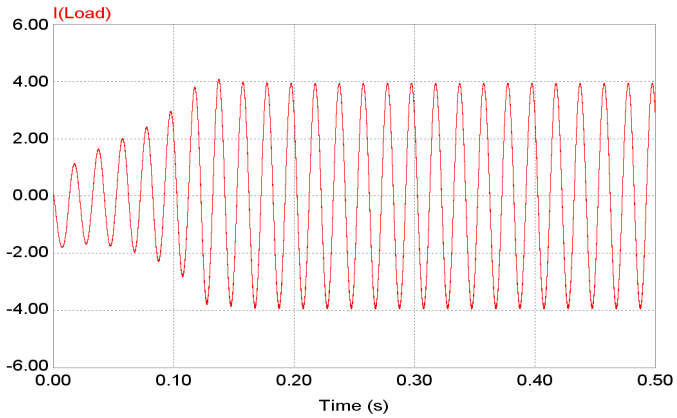


Figure 1.17 Instantaneous load current waveform

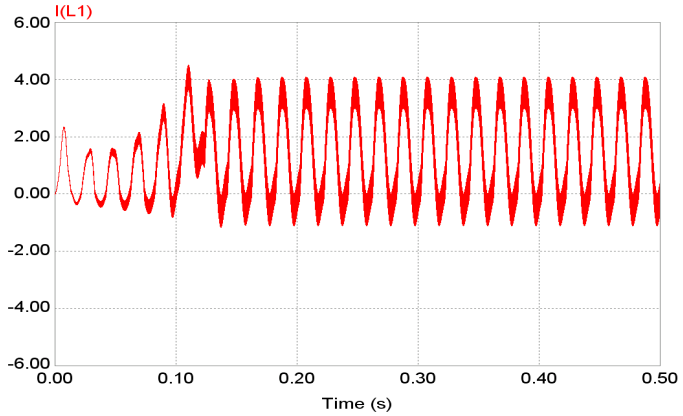


Figure 1.18 Instantaneous current waveform through inductor L1

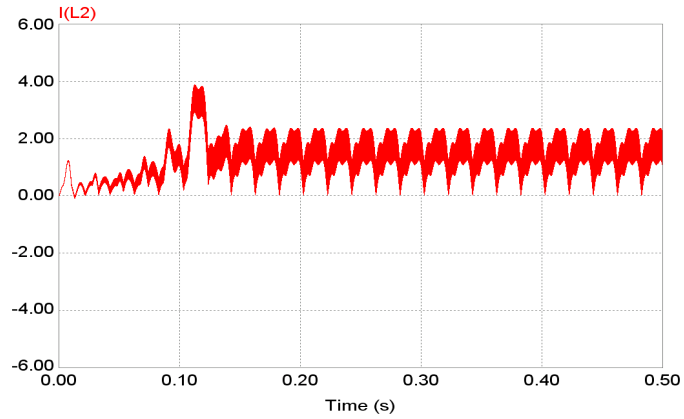


Figure 1.19 Instantaneous current waveform through inductor L2

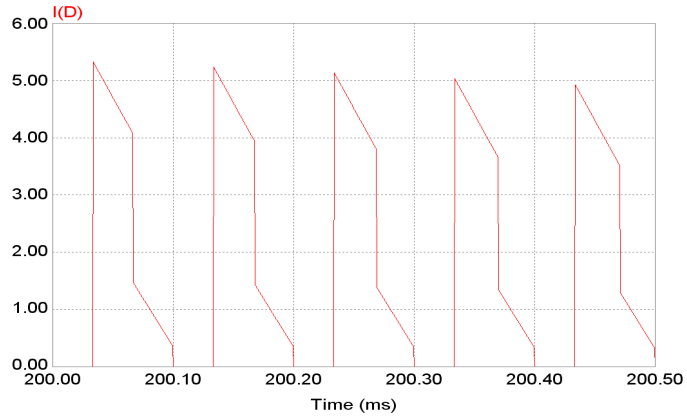


Figure 1.20 Instantaneous current waveform through front-end diode D (zoom)

The used circuit for the simulation is shown in Figure 1.21 The circuit parameters were the following:

- input voltage 110V
- the Z-source network inductors 6.4mH, the capacitors C_1=235μF, C_2=C_3=470μF
- the RL load parameters R_{load}=20Ω, L_{Load}=70mH
- switching frequency 10kHz

The prescribed voltage boost is 2:1 as we can see in Figure 1.9 To avoid the high inrush current the shoot-through duty cycle is increased linearly in 120ms which can be noticed in the increase of the Z-source capacitor voltages in Figure 1.10 and Figure 1.11 We can see that the series Z-source capacitor voltages are half the prescribed voltage. In Figure 1.12 and Figure 1.13 we have the voltages across the inverter leg. Even if the instantaneous load voltage waveform is not symmetrical to 0V in Figure 1.14 and Figure 1.15 we can see in Figure 1.16 the filtered load voltage waveform, at the fundamental frequency, is symmetrical as well as the load current waveform in Figure 1.17. The last three figures Figure 1.18Figure 1.19 and Figure 1.20 illustrate the current waveform of the Z-source network inductors and the current through the front-end diode D.

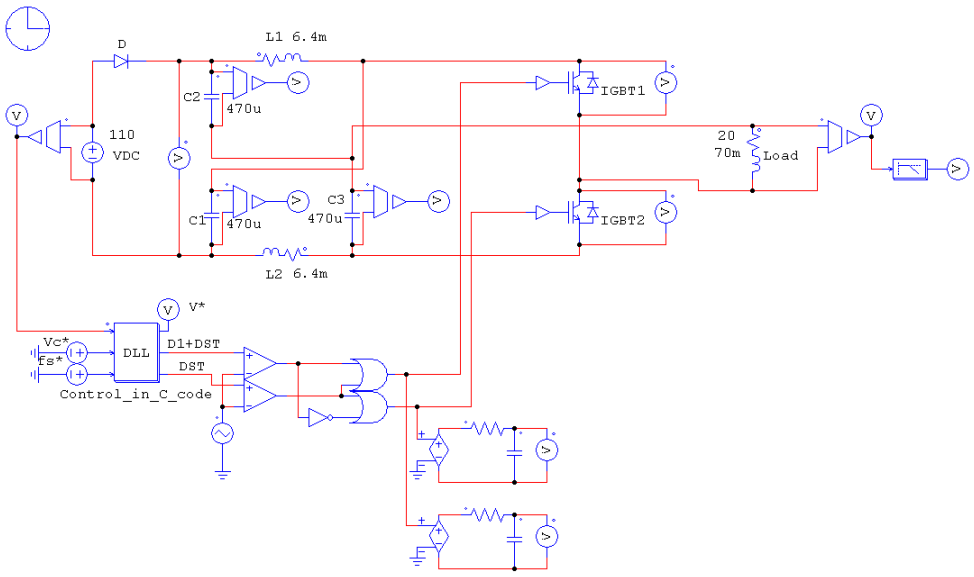


Figure 1.21 The simulated single-phase Z-source inverter with two switches

The following section presents the experimental waveforms of a prototype, built in the laboratory, with the same parameters and the same control as in the simulation.

1.3.3 Experimental Results

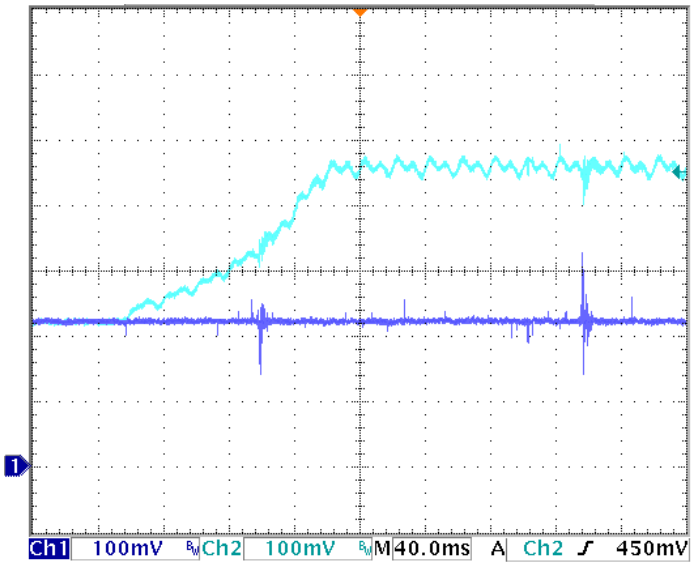


Figure 1.22 The instantaneous voltage across C1 and the input voltage VDC

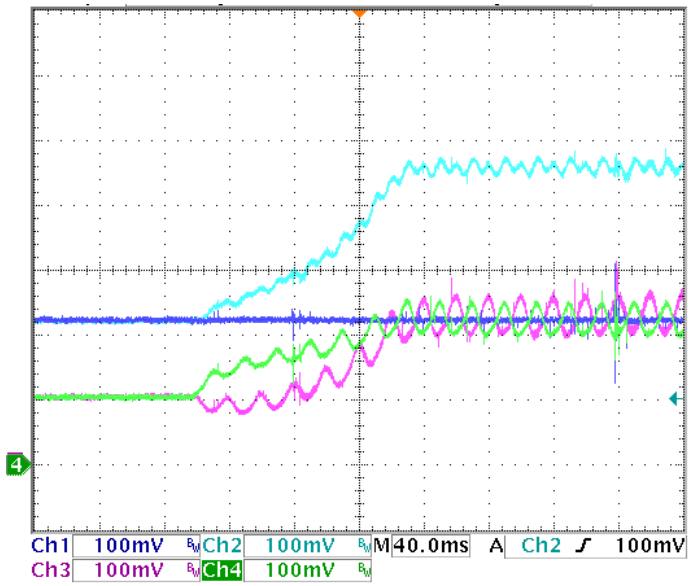


Figure 1.23 The Z-source capacitor (C1,C2,C3) voltages and the input voltage VDC

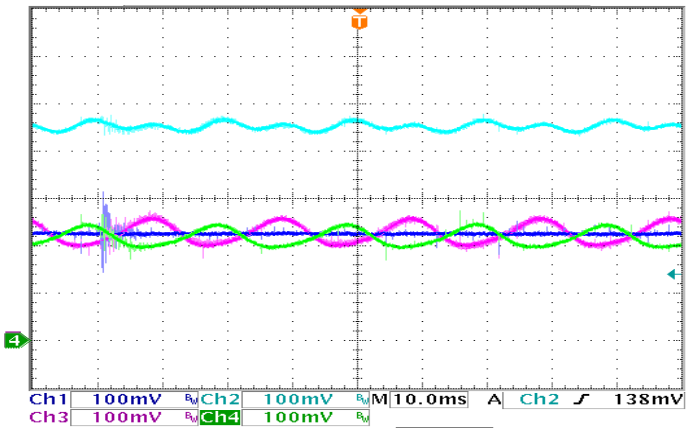


Figure 1.24 The Z-source capacitor voltages (C1,C2,C3) and VDC after start-up

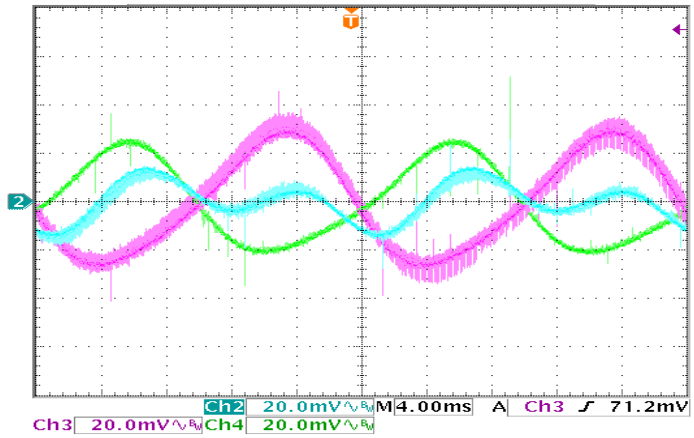


Figure 1.25 The Z-source capacitor voltage ripples after start-up

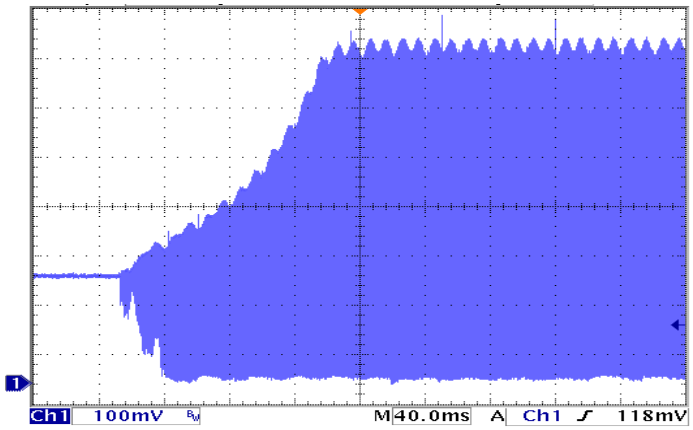


Figure 1.26 The instantaneous dc-link voltage at startup

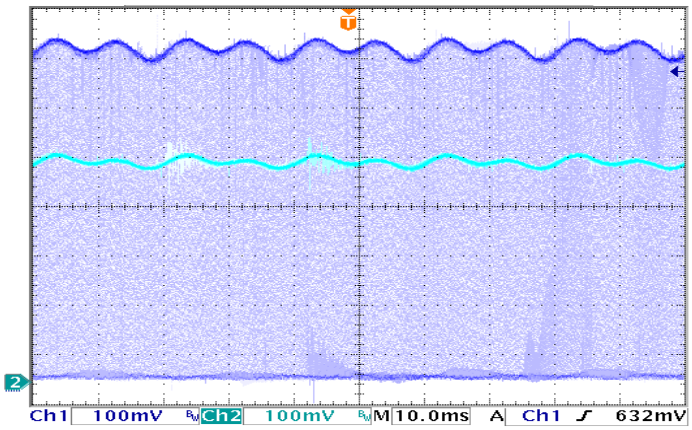


Figure 1.27 The instantaneous dc-link voltage and capacitor C1 voltage after start-up

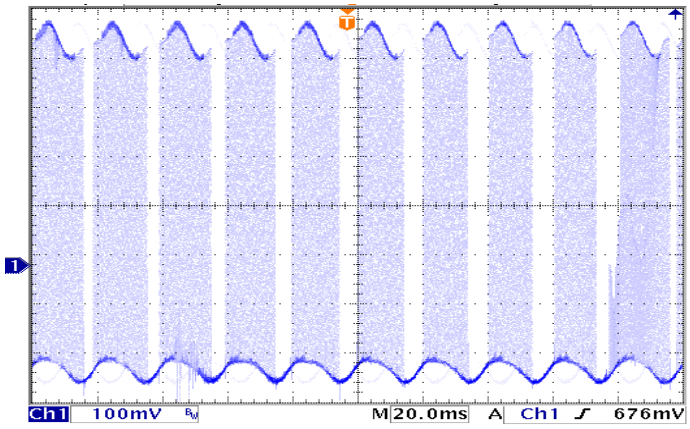


Figure 1.28 Instantaneous load voltage after start-up

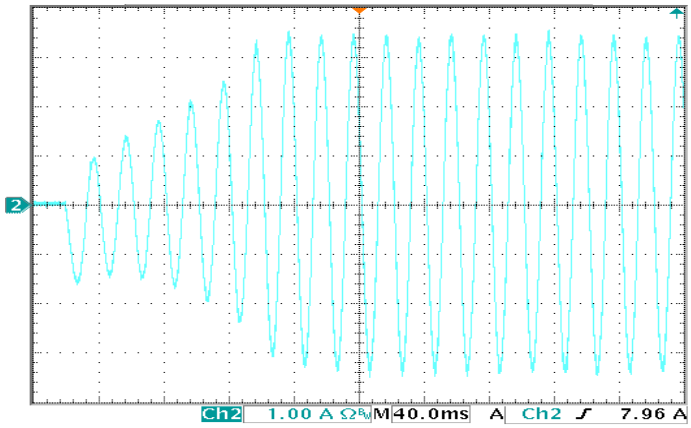


Figure 1.29 Load current at startup

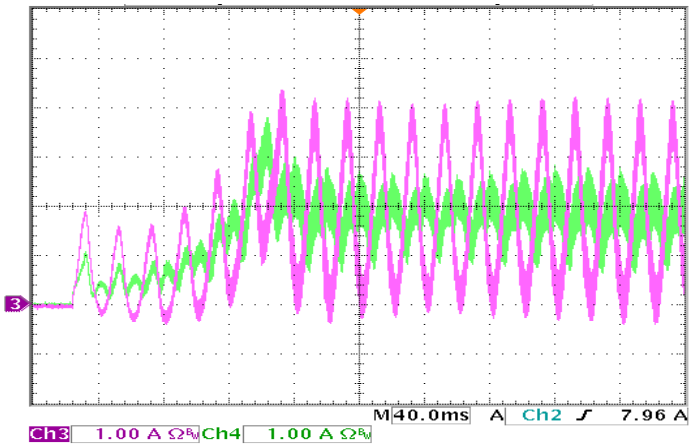


Figure 1.30 The Z-source inductor currents at start-up

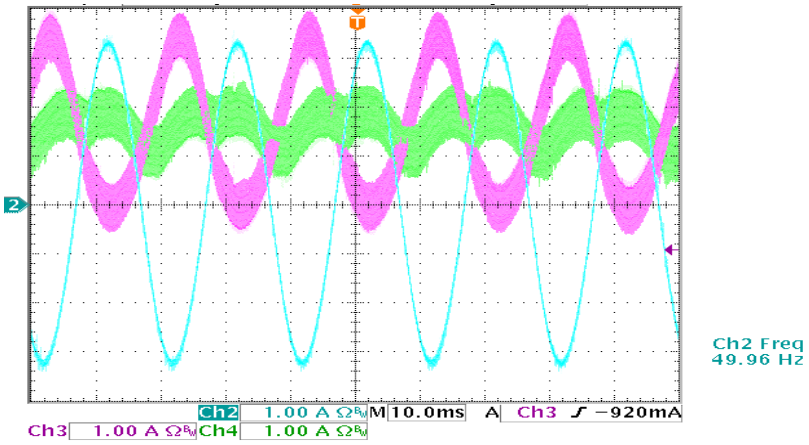


Figure 1.31 The Z-source inductor currents and the load current after start-up

As Figure 1.22-Figure 1.31 show, the experimental voltage and current waveforms are similar to the simulated waveforms. In Figure 1.22-Figure 1.24 the experimental Z-source capacitor voltages have small voltage spikes caused by the voltage source as it can be seen in these figures. Figure 1.27 and Fig. 4.26 point out that the instantaneous dc-link voltage is greater than the voltage across C1 which is considered to be the average dc-link voltage. Figure 1.28 shows the asymmetricall instantaneous load voltage waveform. One could notice in Figure 1.31 the almost 50Hz load current.

The control algorithm based on (1.24) and (1.32) was implemented on the 16-bit dsPIC30F3011 digital signal processor with a clock frequency of 96MHz As an implementation detail of the control algorithm for the dsp we can say that the sine values, needed in the control, only for the first 90 electrical degrees were stored in the dsp. The carrier signal used in the dsp, for the gating signal generation of the two switches, was right aligned and the switching frequency was 10kHz as in the simulation.

Summary

The topology, the capacitors C_1 and C_2 connected in X shape between the two inductors L_1 and L_2 plus the front-end diode, and the operating principle of the Z-source inverters was presented. The voltage gain of the Z-source network was derived.

The new proposed two-switch single-phase Z-source inverter topology was presented with its dual shoot-through state. Detailed analysis based on the equations describing the new topology has been done revealing some delicate issues in the operation of the new topology which has to be taken into account in the control algorithm to properly control the voltages across the series capacitors.

As the first step of the validation process of the proposed topology simulation were made based on the equations describing the inverter.

The control algorithm was implemented on a low cost digital signal processor dsPIC30F3011 in C language. Finally the experiments in the laboratory on a prototype with the parameters and conditions used in the simulation were carried out and the experimental voltage and current waveforms were quite similar to those in the simulation.

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CHAPTER 2 THREE-PHASE Z-SOURCE INVERTERS

2.1 Introduction

The three-phase four-switch inverter presented in [1]-[3] despite his dc-link voltage unbalance which affects the inverter performance is still a good candidate for a reduced cost three-phase inverter. However, it can not deal with voltage sags and has no voltage boost capability in contrast with the Z-source inverters [4][5].

The two six-switch three-phase inverters sharing the same Z-source network [15] can be considered also a reduced element count soution because instead of two Z-source networks it uses only one.

In essence they are self-boosting unidirectional dc-ac converters with only six power switches (unless used in multilevel topologies [9][12][15][19]), which are used with some PWM strategies to short-circuit the z-source and thus produce dc voltage boosting. In between short-circuits the same six power switches produce the required output voltage waveforms.

Making the Z-source inverter bidirectional means to ad an extra switch with its inherent control circuit [16].

The proposed dc-ac topology combines the advantages of a traditional four-switch three-phase inverter with the advantages of the z impedance network (one front-end diode, two inductors and two X connected capacitors). This new topology, besides the self-boost property, has low switch count and it can operate as a buck-boost inverter. In contrast to standard four-switch three-phase inverter which operates at half dc input voltage the proposed four-switch z-source inverter, by self boosting, brings the output voltage at same (or higher) value as in six switch standard three-phase inverter.

The self-boosting attribute of Z converters is "paid for" by some voltage and current over rating [10][11]. The average dc-link voltage is equal with the voltage across the capacitors in the z impedance network but the voltage strees of the inverter bridge is much higher. On the other hand lower count four switch three-phase inverters with split dc-link capacitor are characterized by half dc input voltage used for output voltage PWM and thus a 2/1 current overrating of switches is necessary. To alleviate this situation, while bringing back full dc-link voltage utilization, a novel, four-switch three-phase z-source converter topology is proposed in this chapter. This way the overcurrent rating in comparison with the six-switch three-phase inverter is small, though some notable voltage overrating remains. However this demerit should be justified by the additional voltage buck-boosting attributes that can be indispensable for voltage sags handling in safety critical applications.

Among applications we enumerate here renewable dc-ac interfacing of photovoltaic panels, fuel cells, batteries and electric drive with frequent voltage sags. This proposed novel inverter topology can be also used for small (1...10kW) off-grid wind energy-electrical energy generation systems with permanent magnet synchronous generators.

The chapter is organized as follows: first the equations describing the operation of the inverter are derived, after that the shoot-through time generation

and the gating signals are presented and finally digital simulations and experimental results validate the theory.

2.2 Six-Switch Three-Phase Z-source Inverter

The circuit of the six-switch three-phase Z-source inverter in Fig. 2.1 is similar to the four-switch single-phase Z-source inverter. It has one extra inverter leg. Similar to the single-phase topology it has the same two operating states the non shoot-through state and the shoot-through state thus the equations deduced in Chapter 1 subsection 1.1.1 are valid for this topology also.

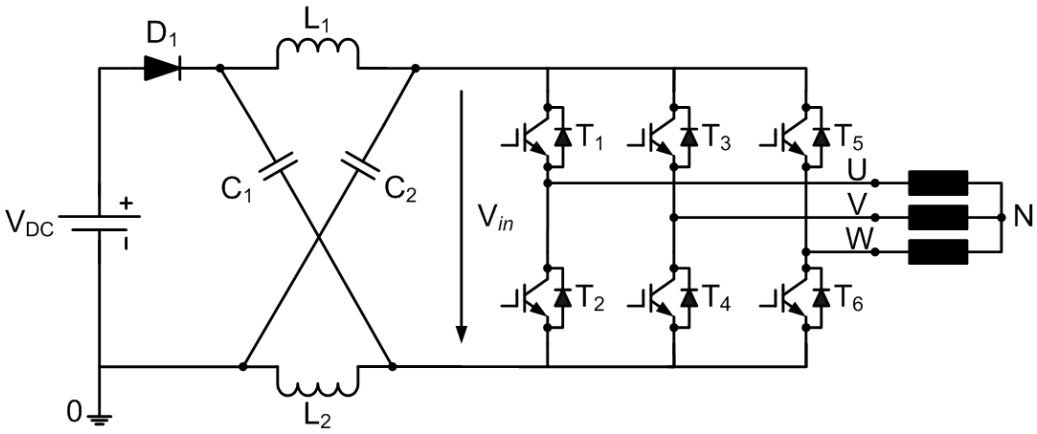

Fig.2.1 Six-switch three-phase z-source inverter

2.3 Four-Switch Three-Phase Voltage-Source Inverters

The today's widely used variable-speed drives for ac motors usually incorporate a six switch inverter bridge. The necessity for further cost reduction of the variable-speed drives can lead to the substitution of the six switch bridge with a four switch bridge illustrated in Fig. 2.2. In case of a three-phase four switch inverter one of the three-phase load terminals is at a fixed potential referenced to the ground of the dc supply.

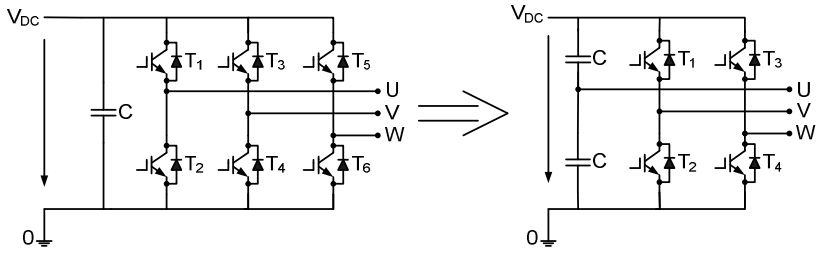

Fig. 2.2 Six IGBT voltage-source inverter versus four IGBT voltage-source inverter

With the reduction of the number of switches the possible switching states of the inverter had been reduced also from eight to only four (see Table 2.1). Thus the four switch inverter permits a fewer number of switching pattern implementations to synthesize the output three-phase ac current from the dc current than a six switch inverter.

	T_1	T_2	T_3	T_4	T_5	T_6
S_1	1	0	0	1	0	1
S_2	1	0	1	0	0	1
S_3	0	1	1	0	0	1
S_4	0	1	1	0	1	0
S_5	0	1	0	1	1	0
S_6	1	0	0	1	1	0
S_7	1	0	1	0	1	0
S_8	0	1	0	1	0	1

	T_1	T_2	T_3	T_4
S_1	0	1	0	1
S_2	1	0	0	1
S_3	1	0	1	0
S_4	0	1	1	0

0 – switch off

1 – switch on

S_x – switching state

Table 2.1 Six IGBT inverter's switching states versus four IGBT switching states

The load phases can be connected in wye configuration or delta configuration Fig. 2.2.

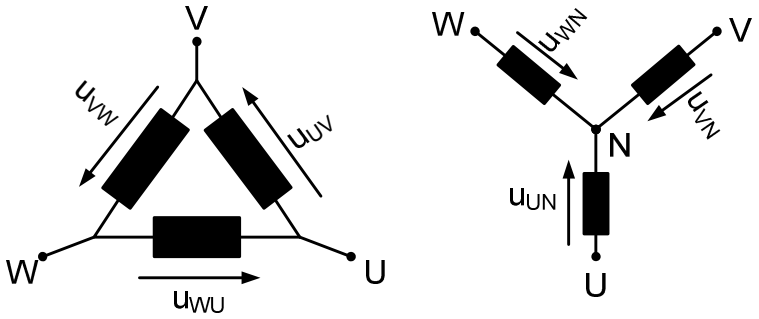

Fig. 2.2 Three-phase load configurations a) delta connection b) wye connection

For a balanced three-phase load we have the following relationships between the phase voltages for delta load connection and wye load connection respectively

$$\begin{aligned} u_{UV}(t) + u_{VW}(t) + u_{WU}(t) &= 0 \\ u_{UN}(t) + u_{VN}(t) + u_{WN}(t) &= 0 \end{aligned} \tag{2.1}$$

Applying Kirchhoff's voltage law on the voltage loops considered in Fig. 2.3. the phase voltages (line to neutral voltages) can be calculated with the following formulae

$$\begin{aligned} u_{UN} &= u_{U0} - u_{N0} = u_{V0} - \frac{1}{3}\left(u_{U0} + u_{V0} + u_{W0} - \left(\underbrace{u_{UN} + u_{VN} + u_{WN}}_{=0} \right) \right) \\ &= \frac{2}{3} u_{U0} - \frac{1}{3}\left(u_{V0} + u_{W0} \right) \\ u_{VN} &= u_{V0} - u_{N0} = \frac{2}{3} u_{V0} - \frac{1}{3}\left(u_{U0} + u_{W0} \right) \\ u_{WN} &= u_{W0} - u_{N0} = \frac{2}{3} u_{W0} - \frac{1}{3}\left(u_{U0} + u_{V0} \right) \end{aligned} \tag{2.2}$$

The expression of the line-to-zero voltage is

$$u_{N0} = \frac{1}{3}\left(u_{U0} + u_{V0} + u_{W0} \right) \tag{2.3}$$

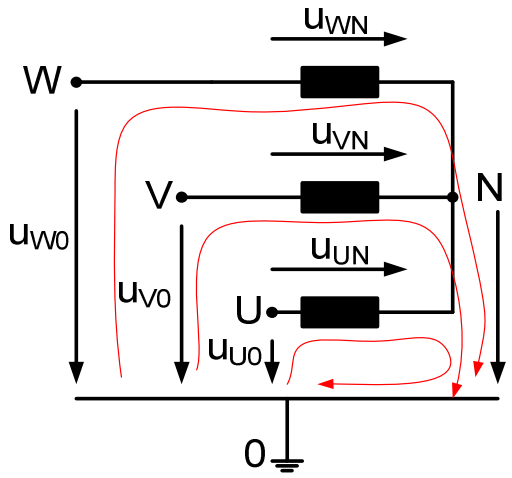

Fig. 2.3 Wye connected three-phase load

The sinusoidal three-phase voltages for simpler manipulation can be represented in the complex plane by the voltage space phasor defined by

$$\begin{aligned} \underline{u_s} &= k\left(u_{UN}(t) + u_{VN}(t) e^{j\frac{2\pi}{3}} + u_{WN}(t) e^{j\frac{4\pi}{3}} \right), k = \left\{ \frac{2}{3}, \sqrt{\frac{2}{3}} \right\} \\ e^{j\frac{2\pi}{3}} &= \cos\left(\frac{2\pi}{3} \right) + j \sin\left(\frac{2\pi}{3} \right) = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \\ e^{j\frac{4\pi}{3}} &= \cos\left(\frac{4\pi}{3} \right) + j \sin\left(\frac{4\pi}{3} \right) = -\frac{1}{2} - j\frac{\sqrt{3}}{2} \end{aligned} \tag{2.4}$$

with the instantaneous phase voltages given by

$$\begin{aligned} u_{UN}(t) &= U_{eff}\sqrt{2}\cos(\omega t) \\ u_{VN}(t) &= U_{eff}\sqrt{2}\cos\left(\omega t - \frac{2\pi}{3}\right) \\ u_{WN}(t) &= U_{eff}\sqrt{2}\cos\left(\omega t - \frac{4\pi}{3}\right) \\ \omega &= 2\pi f = \frac{2\pi}{T} \end{aligned} \tag{2.5}$$

The most common scale coefficients k used for the voltage space phasor are $2/3$ or $\sqrt{2/3}$ .With the former the length of the voltage space phasor is equal with the peak phase voltage with the latter it is equal with the effective phase voltages multiplied by $\sqrt{3}$. Although using one or the other results in different formulae for the complex plane components of a space phasor v_α, v_β and finally the switching time intervals t_1, t_2 , it does not change the desired synthesized output voltage of the inverter.

Using the simple well-known trigonometric formula

$$\cos(a-b) = \cos(a)\cos(b) - \sin(a)\sin(b) \tag{2.6}$$

by substituting the instantaneous phase voltages (2.5) into the definition of the space phasor we get

$$\begin{aligned} \underline{u_S} &= k\left(U_{eff}\sqrt{2}\cos(\omega t) + U_{eff}\sqrt{2}\cos\left(\omega t - \frac{2\pi}{3}\right)e^{j\frac{2\pi}{3}} + U_{eff}\sqrt{2}\cos\left(\omega t - \frac{4\pi}{3}\right)e^{j\frac{4\pi}{3}}\right) \\ &= kU_{eff}\sqrt{2}\left(\cos(\omega t) + \cos\left(\omega t - \frac{2\pi}{3}\right)e^{j\frac{2\pi}{3}} + \cos\left(\omega t - \frac{4\pi}{3}\right)e^{j\frac{4\pi}{3}}\right) \\ &= kU_{eff}\sqrt{2}\left(\begin{array}{l} \cos(\omega t) + \left(\cos(\omega t)\left(-\frac{1}{2}\right) - \sin(\omega t)\left(\frac{\sqrt{3}}{2}\right)\right)\left(-\frac{1}{2} + j\frac{\sqrt{3}}{2}\right) + \\ + \left(\cos(\omega t)\left(-\frac{1}{2}\right) - \sin(\omega t)\left(-\frac{\sqrt{3}}{2}\right)\right)\left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right) \end{array}\right) \\ &= kU_{eff}\sqrt{2}\left(\cos(\omega t)\left(1 + \frac{1}{4} - j\frac{\sqrt{3}}{4} + \frac{1}{4} + j\frac{\sqrt{3}}{4}\right) + \sin(\omega t)\left(\frac{\sqrt{3}}{4} - j\frac{3}{4} - \frac{\sqrt{3}}{4} - j\frac{3}{4}\right)\right) \\ &= kU_{eff}\sqrt{2}\frac{3}{2}\left(\cos(\omega t) + j\sin(\omega t)\right) \end{aligned} \tag{2.7}$$

The space phasor can be represented by its projections on the two axes shown in Fig. 2.4.

$$\underline{u_S} = u_\alpha + ju_\beta = \left|\underline{u_S}\right|\left(\cos(\alpha) + j\sin(\alpha)\right) \tag{2.8}$$

Basically (2.7) and (2.8) are two formulae for the same space phasor therefore

$$\left|\underline{u_s}\right| = kU_{eff}\sqrt{2}\,\frac{3}{2} \tag{2.10}$$

From (2.8) the amplitude of the space phasor can be expressed by

$$\left|\underline{u_s}\right| = \sqrt{u_\alpha{}^2 + u_\beta{}^2} \tag{2.11}$$

For the eight switching states in of the six switch three-phase voltage source inverter in Table 2.1 using the expression of the voltage phasor in (2.4) we get eight phase voltage phasors in the complex plane for a wye connected three-phase load while for the four-switch three phase inverter we get only four phase voltage phasors as we can see in Fig. 2.5.

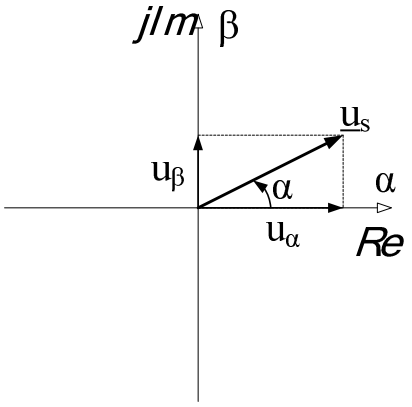

Fig. 2.4 The space phasor in the complex plane

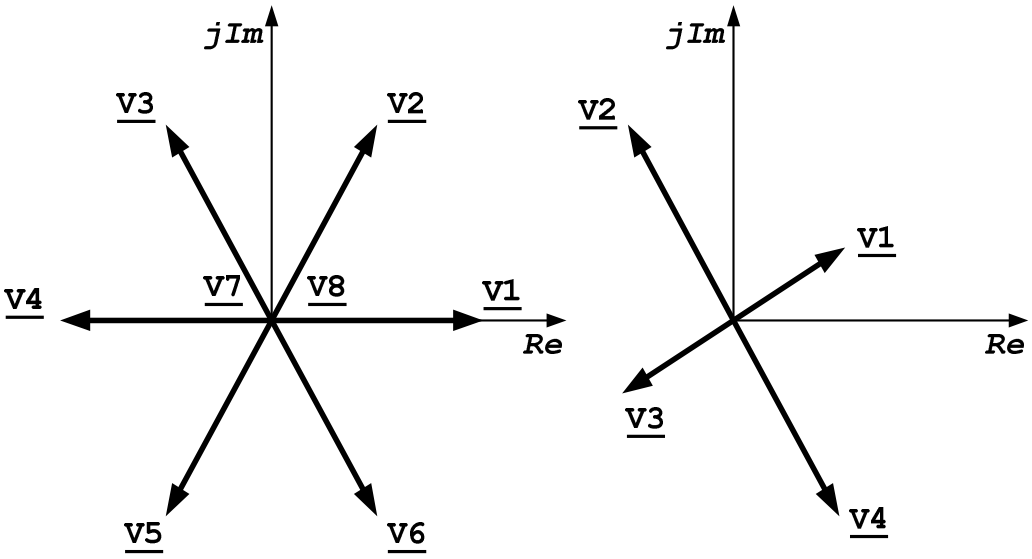

Fig. 2.5 Phase voltage phasors in the complex plane for a six-switch (left)/ four-switch (right) three-phase voltage source inverter with a wye connected load

A well synthetized sinusoidal three-phase load phase voltages can be obtained if the voltage phasor in Fig. 2.4 rotates smoothly.

The reference rotating voltage phasor in Fig. 2.4 in between the voltage phasors generated by the switching states of the two topologies can be obtained by applying two or more voltage phasors for a different definite time duration thus for the average amplitude of the applied voltage phasors during one T_s in Fig. 2.5 we get different lengths and by trigonometrically summing the voltage phasors we get the desired voltage phasor with the desired length and orientation. The last sentence can be mathematically expressed by

$$\begin{aligned} &\underline{u}_s^* T_s = t_1\underline{V}_1 + t_2\underline{V}_2 + t_3\underline{V}_3 + t_4\underline{V}_4 + t_5\underline{V}_5 + t_6\underline{V}_6 + t_7\underline{V}_7 + t_8\underline{V}_8 \\ &t_1 + t_2 + t_3 + t_4 + t_5 + t_6 + t_7 + t_8 = T_s \end{aligned} \tag{2.12}$$

for the six-switch VSI and for the four-switch VSI by

$$\begin{aligned} &\underline{u}_s^* T_s = t_1\underline{V}_1 + t_2\underline{V}_2 + t_3\underline{V}_3 + t_4\underline{V}_4 \\ &t_1 + t_2 + t_3 + t_4 = T_s \end{aligned} \tag{2.13}$$

The number of applied voltage phasors during one switching period, their time duration and their sequence is a matter of control algorithm of the prescribed voltage.

2.4 Proposed Four-Switch Three-Phase Z-Source Inverter

As we could see in case of a z-source inverter with six switches the voltage across the inverter bridge is zero when the voltage boost is applied by short-circuiting at least one of the three inverter legs. So the shoot-through state of the inverter limits the available maximum output voltage of the inverter. Hence to fully utilize the voltage boost and to limit the voltage and current stresses of the inverter bridge without affecting the output voltage, the placing of shoot-through states during the zero voltage vector time intervals (no voltage seen by the load) seems to be a practical solution [8].

2.4.1 Principle of operation

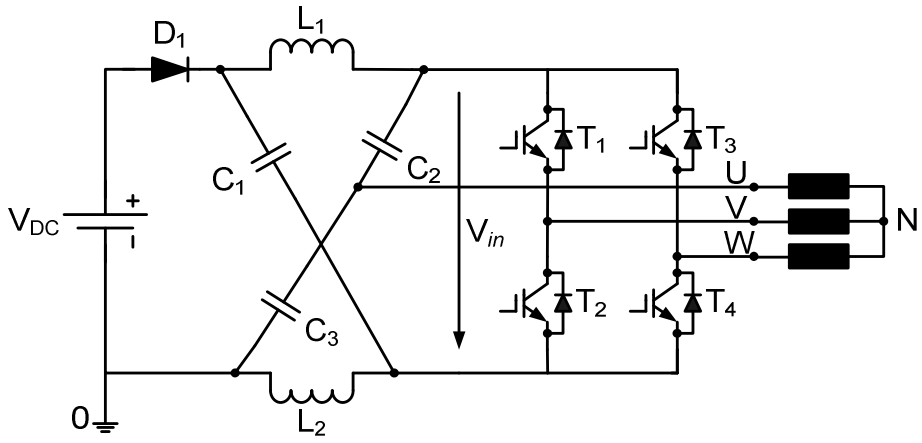

Fig. 2.6 Four-switch z-source three-phase inverter.

The proposed four-switch z-source three-phase inverter is shown in Fig. 2.6. In essence, the novel topology shows that one of the capacitors in the Z network is split into two and the middle point is connected to one phase of the load.

This 50% voltage drawback of conventional four-switch three-phase inverter is eliminated by the proposed four-switch Z-source inverter because the shoot-through state produces not only the voltage boost but it produces also an active voltage vector, thus generating non-zero output voltage Fig 2.7.

The equivalent scheme of the shoot-through state of the proposed inverter (when all four transistor are conducting) in Fig. 2.7 clearly shows that during the shoot-through state the voltage seen by the load is equal with the voltage across capacitor C_2.

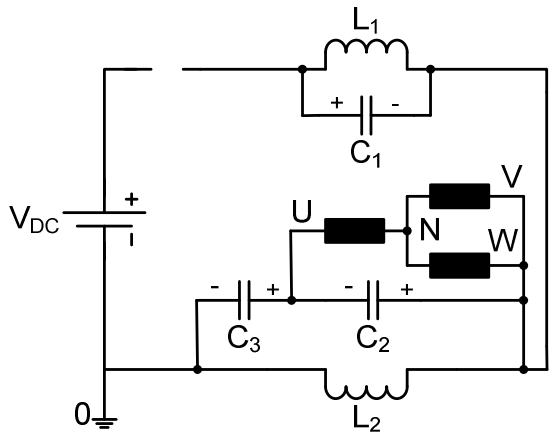

Fig. 2.7 Shoot-through state equivalent circuit of the 4-switch z-source three-phase inverter.

By averaging the voltage across one inductor during one switching period in steady state the same relationship can be obtained between the input dc voltage V_{DC} and the average dc-link voltage V_{in} as in eq. (2.7). The average dc-link voltage is equal with the voltage across C_1 or across C_2 and C_3 as for a three-phase z-source inverter with six switches or for a single phase two or four switch Z-source inverter. Before we step further into the analysis of the proposed topology we make the following assumptions:

- The average voltages across C_2 and C_3 are equal with each other.
- The front-end diode D1 is always conducting when the converter is in the non-shoot through state, thus the pseudo-active state is avoided.

It must be noticed that the new proposed topology does not have zero voltage states and the comprehensive control strategies based on voltage space phasors presented in [9][18][19].

2.4.2 Space Phasor Analysis

For the three-phase load in Fig. 2.6 the voltage space vector can be defined as follows

$$\underline{v_s} = \frac{2}{3}\left(v_{UN} + e^{-j\frac{2\pi}{3}} v_{VN} + e^{-j\frac{4\pi}{3}} v_{WN} \right) \tag{2.14}$$

where v_{UN}, v_{VN} and v_{WN} are the instantaneous phase voltages. With the four switches in Fig. 2.6 five voltage vectors can be obtained, as shown in Table 2.2

Table 2.2 Switching Pattern

	T_1	T_2	T_3	T_4
V_1	0	1	0	1
V_2	1	0	0	1
V_3	1	0	1	0
V_4	0	1	1	0
V_{ST}	1	1	1	1

All voltage vectors are active voltage vectors as we will see in the following section. Although two more shoot-through states can be obtained by turning on T_1 and T_2 or T_3 and T_4 at the same time these states were neglected because the maximum current flowing through the inverter bridge would only flow through one leg of the inverter bridge which would lead to a bigger kVA transistor bridge. The wye connected three-phase load terminal voltages referenced to ground are shown, with respect to the switching pattern in Table 2.2, in Fig. 5.

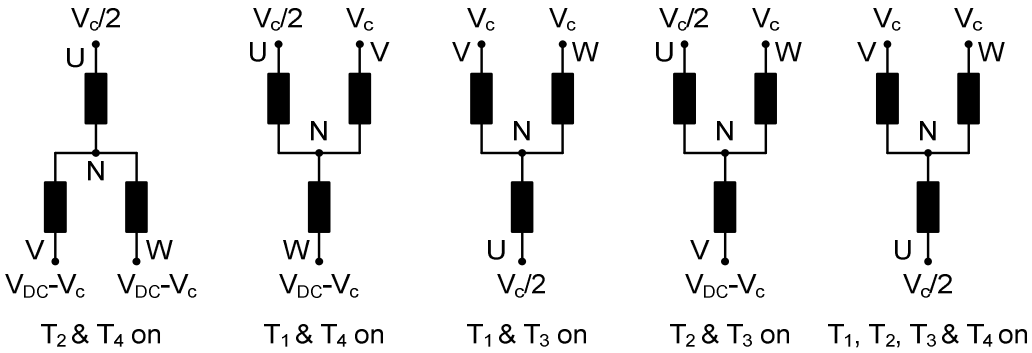

Fig. 2.8 Phase terminal voltages referenced to ground 0.

In order to derive the phase voltages we will consider

$$\overline{V_C} = \overline{V_{C1}}; \overline{V_{C2}} = \overline{V_{C3}} = \frac{\overline{V_C}}{2} \tag{2.15}$$

where $\overline{V_{C1}}$, $\overline{V_{C2}}$ and $\overline{V_{C3}}$ are the average voltages across C_1, C_2 and C_3 capacitors. For a symmetrical balanced wye connected three-phase load (Fig. 2.6) the phase voltages can be written as

$$\begin{aligned} v_{UN} &= \frac{2}{3}v_{U0} - \frac{1}{3}(v_{V0} + v_{W0}) \\ v_{VN} &= \frac{2}{3}v_{V0} - \frac{1}{3}(v_{W0} + v_{U0}) \\ v_{WN} &= \frac{2}{3}v_{W0} - \frac{1}{3}(v_{U0} + v_{V0}) \end{aligned} \tag{2.16}$$

Substituting u_{U0}, u_{V0} and u_{W0}, from Fig. 2.8, into (2.16) and using the expression of the space voltage vector (2.14) the five voltage vectors can be derived as

$$\begin{aligned}
\underline{V_1} &= \overline{V_C} - \frac{2}{3}V_{DC} \\
\underline{V_2} &= \left(\frac{1}{3} + j\frac{2\sqrt{3}}{3}\right)\overline{V_C} + \left(-\frac{1}{3} - j\frac{\sqrt{3}}{3}\right)V_{DC} \\
\underline{V_3} &= -\frac{1}{3}\overline{V_C} \\
\underline{V_4} &= \left(\frac{1}{3} - j\frac{2\sqrt{3}}{3}\right)\overline{V_C} + \left(-\frac{1}{3} + j\frac{\sqrt{3}}{3}\right)V_{DC} \\
\underline{V_{ST}} &= -\frac{1}{3}\overline{V_C}
\end{aligned} \tag{2.17}$$

The relationship between the average capacitor voltage $\overline{V_C}$ and the input dc voltage V_{DC} can be expressed as

$$\overline{V_C} = k \cdot V_{DC} \tag{2.18}$$

$$k = \frac{1 - D_{ST}}{1 - 2D_{ST}}; k > 1 \tag{2.19}$$

Rewriting (2.17) using (2.19) the voltage vectors can be derived as

$$\begin{aligned}
\underline{V_1} &= \left(k - \frac{2}{3}\right)V_{DC} \\
\underline{V_2} &= \left[\frac{1}{3}(k-1) + j\frac{\sqrt{3}}{3}(2k-1)\right]V_{DC} \\
\underline{V_3} &= -\frac{1}{3}kV_{DC} \\
\underline{V_4} &= \left[\frac{1}{3}(k-1) + j\frac{\sqrt{3}}{3}(-2k+1)\right]V_{DC} \\
\underline{V_{ST}} &= -\frac{1}{3}kV_{DC}
\end{aligned} \tag{2.20}$$

Notice that in (2.20) the boost factor k influences the amplitude as well the direction of the six voltage vectors.
For k=2 the six voltage vectors in the complex plane are illustrated in Fig. 2.9.

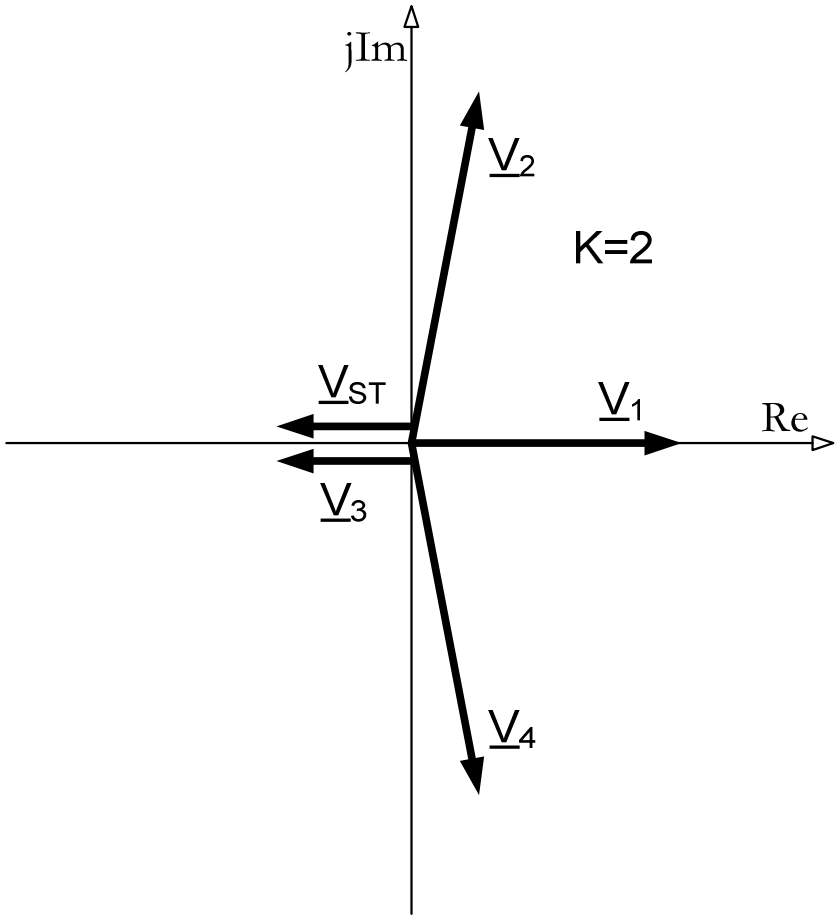

Fig. 2.9 Locations of the voltage vectors in the complex plane.

The voltage vector generated by the shoot-through state V_{ST} has the same amplitude and direction as the V_3 voltage vector.

The voltage space vector expressed in (2.14) can be rewritten in the complex plane as

$$\underline{v_s} = v_{s\alpha} + jv_{s\beta} \tag{2.21}$$

The average voltage space vector over one switching cycle should be equal with the sum of the five average voltage space vectors (V_1…V_4 and V_{ST}) over one switching cycle T_s

$$\overline{\underline{v_s}} = \left(t_1\underline{V_1} + t_2\underline{V_2} + t_3\underline{V_3} + t_4\underline{V_4} + t_{ST}\underline{V_{ST}}\right)/T_s \tag{2.22}$$

where

$$t_1 + t_2 + t_3 + t_4 + t_{ST} = T_s \tag{2.23}$$

To obtain the expressions of $v_{s\alpha}$ and $v_{s\beta}$ (9) the expressions of the five voltage vectors (2.20) are introduced in (2.22)

$$\begin{aligned} v_{s\alpha} &= \frac{V_{DC}}{3T_s}\left[t_1(3k-2)+(t_2+t_4)(k-1)-(t_3+t_{ST})k\right] \\ v_{s\beta} &= \frac{\sqrt{3}V_{DC}}{3T_s}(t_2-t_4)(2k-1) \end{aligned} \tag{2.24}$$

Given (2.14)-(2.24) in this section it is possible to derive several algorithms that can be implemented in a digital signal processor which, for a prescribed input space voltage vector,

$$\underline{v_s^*} = v_{s\alpha}^* + jv_{s\beta}^* \tag{2.25}$$

calculate the duty ratios for the four transistors and generate the four gating pulses.

2.4.3 Hardware Implementation of the Shoot-Through Pulse Generation

One easy way to generate the gating signals for the four transistors is to use three synchronized PWM units in complementary mode of a DSP with some additional circuitry.

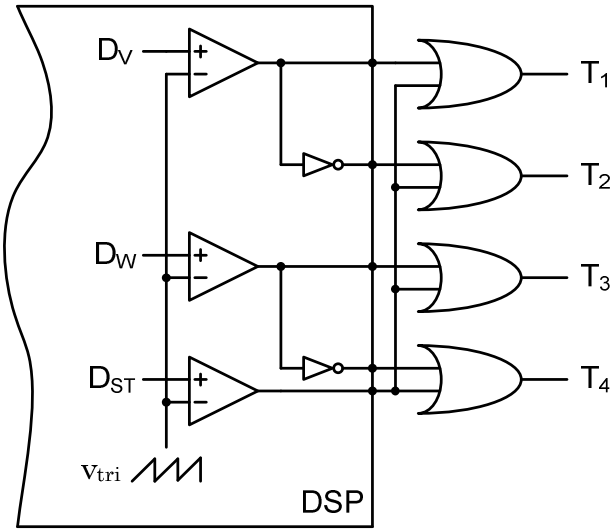

Fig. 2.10 Block diagram of the PWM signal generation implementation.

Two of the three PWM generation units yield the two complementary signals for the two phase legs of the inverter bridge based on the prescribed duty ratios D_V and D_W. The third PWM unit generates the ST signal from D_{ST}. The four outputs from the two units are ORed with the ST signal thus obtaining the PWM signals for $T_1 \ldots T_4$.

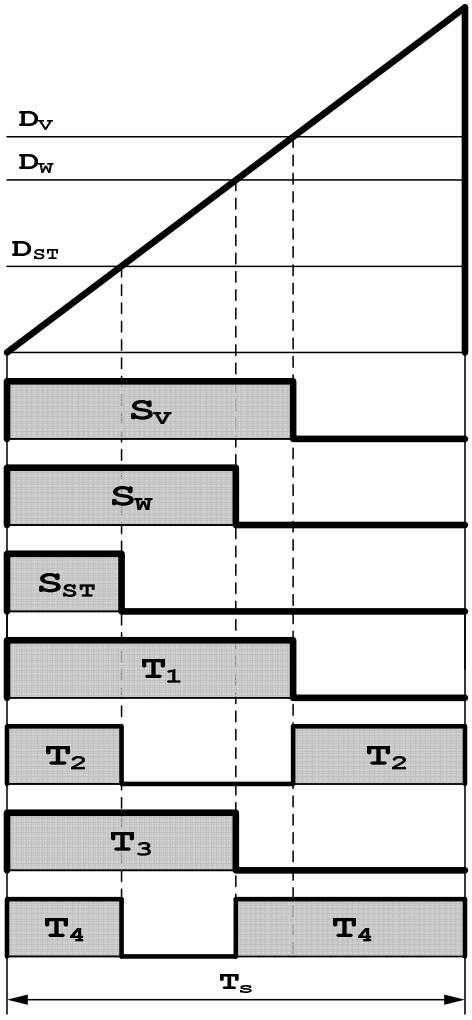

Fig. 2.11 PWM signal waveform generation for T1, T2, T3 & T4.

2.4.4 Open Loop Simulation Results

In the first step of the validation, the proposed four-switch z-source three-phase inverter was simulated in PSIM. The circuit parameters were as follows

$$V_{DC} = 90V; L_1 = L_2 = 6.4mH; C_1 = 235uF;$$
$$C_2 = C_3 = 470\mu F; R_{L1} = R_{L2} = 0.9\Omega$$
$$\left|\underline{v_s^*}\right| = 60V; k^* = 2; f^* = 50Hz$$
$$f_s = 10kHz$$

A three-phase wye connected RL load was used with the following parameters

$$R_U = 10.5\Omega; R_V = 10.6; R_W = 10.2;$$
$$L_U = 20.1mH; L_V = 18.4mH; L_W = 17.7mH$$

Only open loop performance with imposed output voltage vector amplitude, to derive commutation sequences and the required shoot-through time for the dc-link voltage boost, was investigated both in simulations and experiments.

The simulated waveforms are shown in Fig. 2.12-Fig. 2.15.

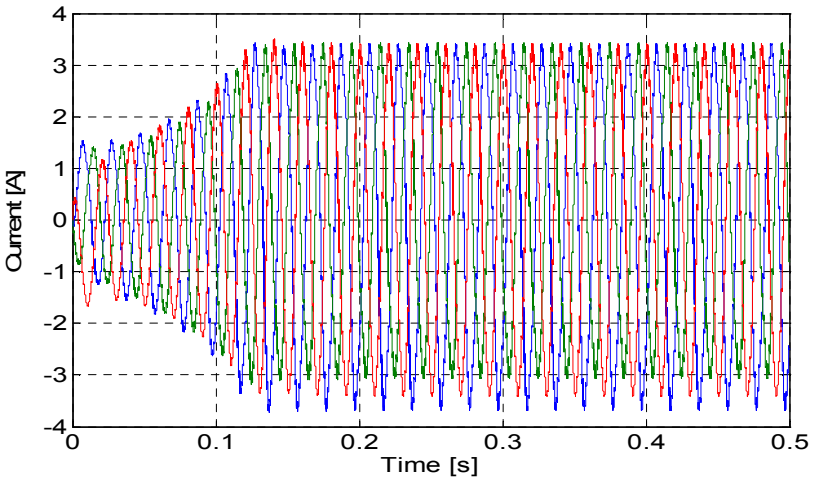

Fig. 2.12 Simulated load currents at start-up

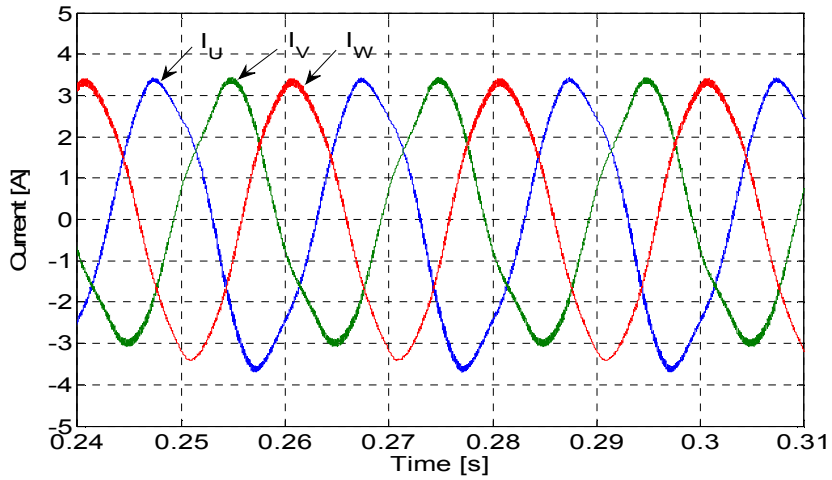

Fig. 2.12 Simulated load currents(zoom)

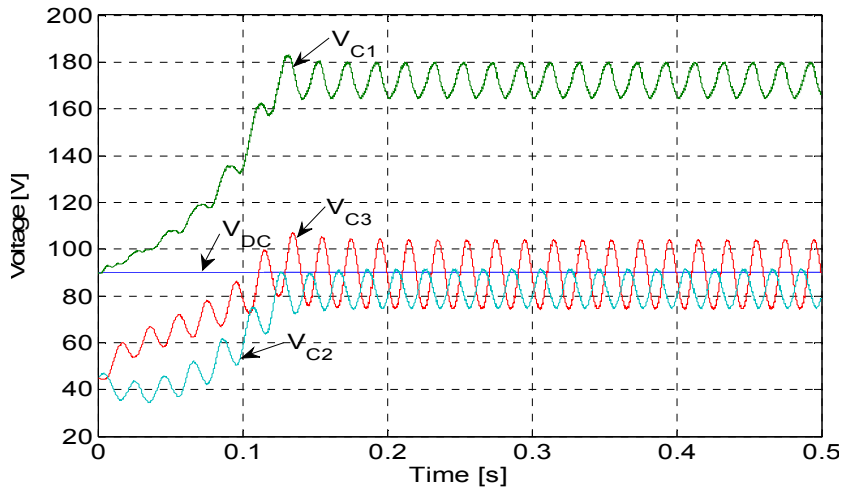

Fig. 2.13 Simulated voltage waveforms across C1, C2, C3 and the input dc voltage at start-up.

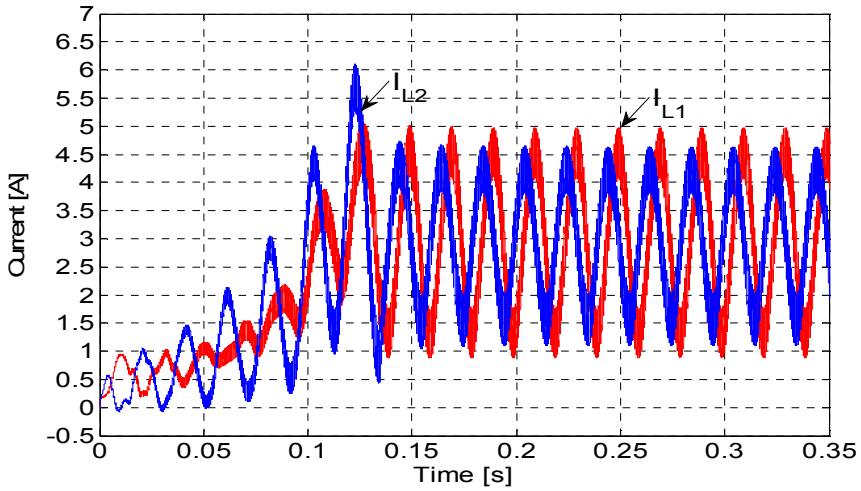

Fig. 2.14 Simulated z-impedance inductor current waveforms IL1 and IL2.

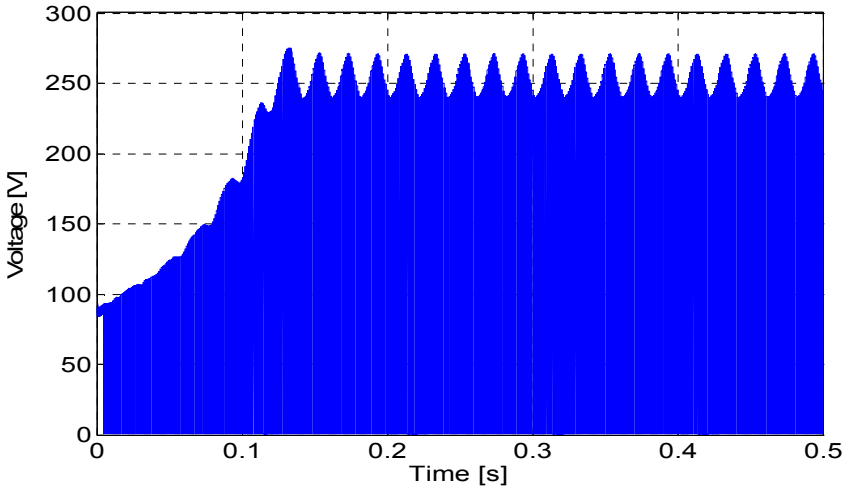

Fig. 2.15 Simulated instantaneous dc-link voltage Vi.

The shoot-through time was linearly increased from 0 to its nominal value in 0.120s to avoid the high inrush current Fig. 2.14. In Fig. 2.12 it can be seen that the load currents are not perfectly symmetrical due to the connection of phase U to the common node of capacitors C_2 and C_3 which causes the voltage potential at this terminal to vary around $\overline{V_C}/2$ Fig. 2.13.

The simulated inductor currents (which flow through both inverter legs during shoot-through states) are shown in Fig. 2.14, and they are less than 150% the peak load currents (Fig. 2.12). The boost dc-link voltage is shown in Fig. 2.15 (input dc voltage is 90V dc).

2.4.5 Open Loop Experimental Results

A laboratory setup was built to experimentally validate the proposed four-switch Z-source three-phase inverter. The control algorithm based on equations (1)-(12) was implemented on a dsPIC30f3010 digital signal processor from Microchip with a clock frequency of 120MHz. The experimental waveforms are shown in. Fig. 2.16-Fig.2.20.

The laboratory setup data are the same as for the digital simulations.

The experimental load currents in Fig. 2.16 are close to those from digital simulations (in Fig. 2.12) though a bit more asymmetric. The inverter starting experimental transients of Fig. 2.17-2.20 are similar to those obtained for same transients by digital simulations in Fig. 2.12, Fig. 2.13 and Fig. 2.14 respectively.

The test and simulation load phase current transients (Fig. 2.16 and Fig. 2.12) fit rather well; the same observation is valid for V_{C2}, V_{C3} which pulsate around the input dc voltage of 90V dc. The dc-link (boosted) voltage V_{C1} in experiments (Fig. 2.17) pulsates around 160V while in simulation it is around 180V dc, while the experimental inductor currents (Fig. 2.20) are smaller than the digital simulations (Fig. 2.14). These discrepancies require further insight.

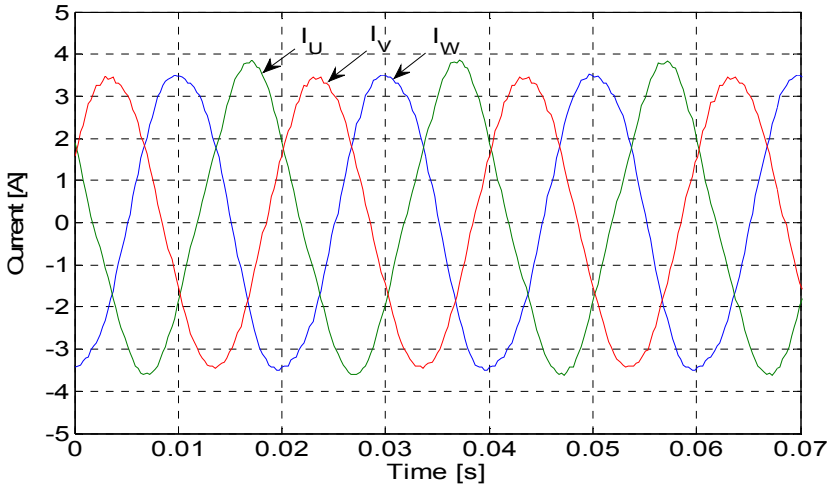

Fig 2.16 Experimental load currents.

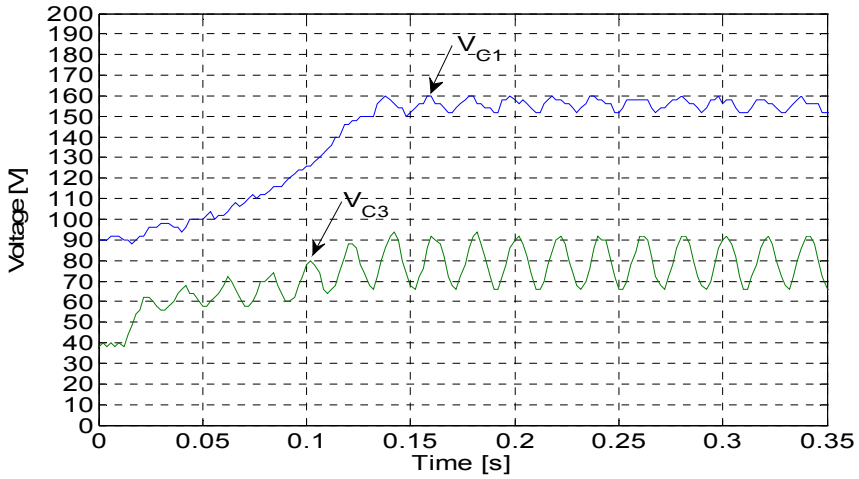

Fig. 2.17 Experimental voltages across C1 and C3 capacitors at start-up.

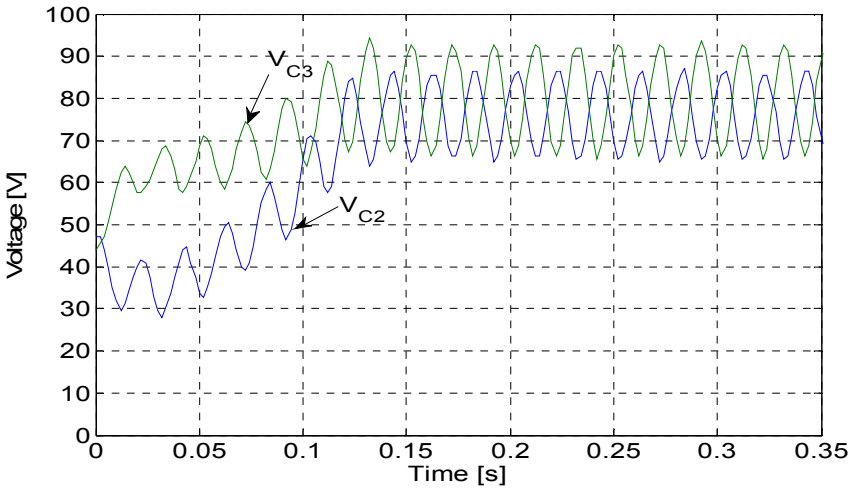

Fig. 2.18 Experimental voltages across C2 and C3 capacitors at start-up.

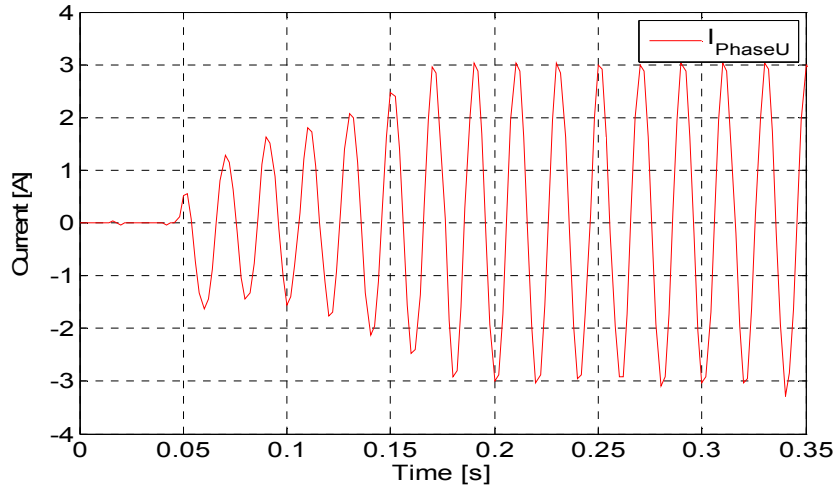

Fig. 2.19 Experimental current waveform through phase U at start-up.

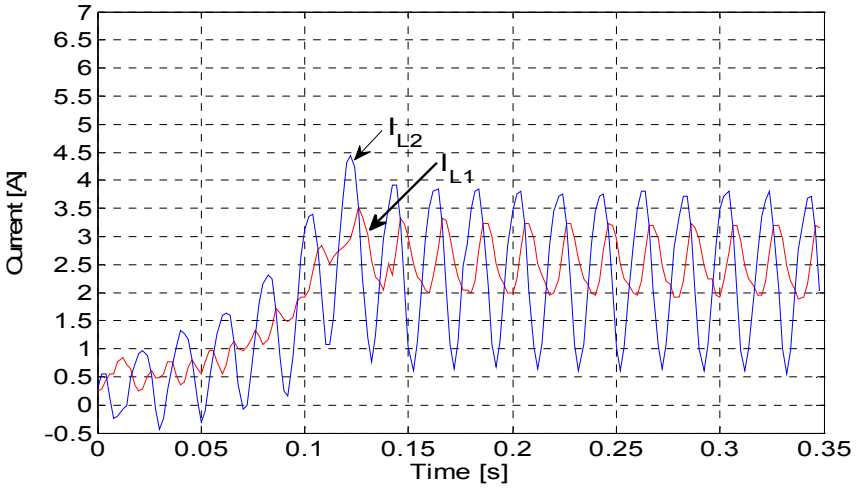

Fig. 2.20 Experimental Z-impedance inductor current waveforms IL1 and IL2.

2.4.6 Closed Loop Simulation Results

Digital simulations in closed loop were carried out with a three-phase wye connected RL load as it can be seen in the simulated circuit in Fig. 2.21. The voltage boost was 2:1. The control algorithm was written in C. Only one PI controller was used to control the shoot-through time interval from the Z-source capacitor voltage error. The PI controller can be seen in Fig. 2.22. The input is the error between the prescribed C_1 capacitor voltage and the measured capacitor voltage and the output is the shoot-through time interval. The PI controller output is shown in Fig. 2.23. We can notice in Fig. 2.24 that the C_1 capacitor voltage smothly raises up to 400V while the C_2 and C_3 capacitor voltages vary around the dc input voltage 200V.

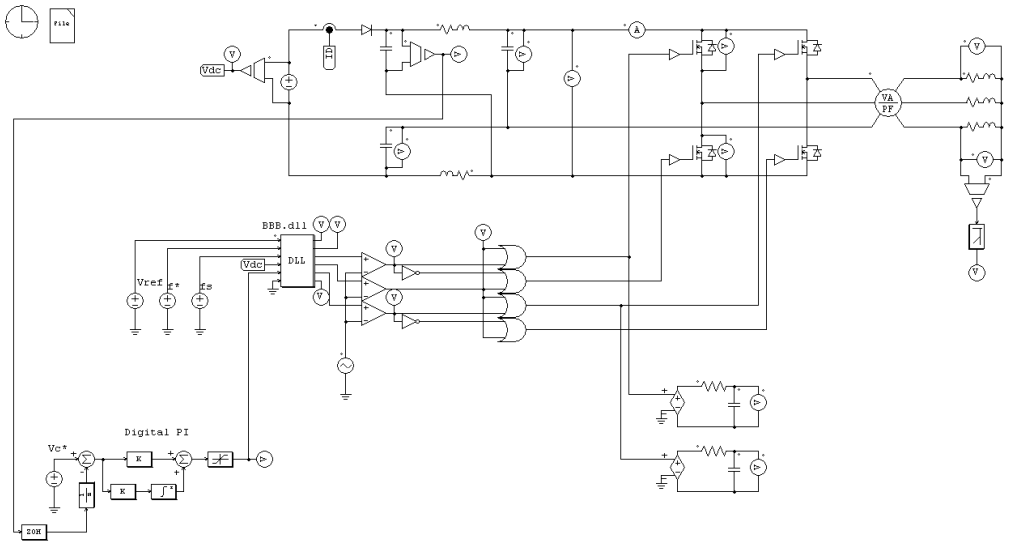

Fig. 2.21 Four-switch three-phase Z-source inverter with one PI controller

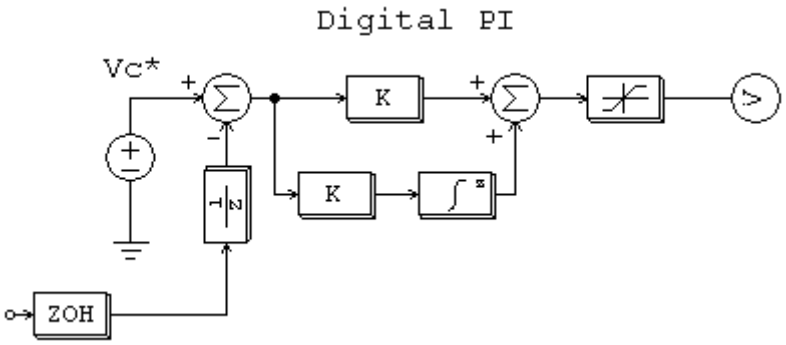

Fig. 2.22 PI controller for the Z-source capacitor voltage

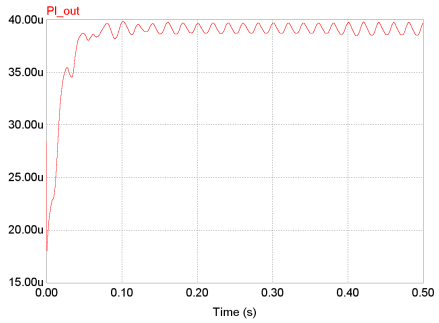

Fig. 2.23 PI controller output for a 2:1 voltage boost

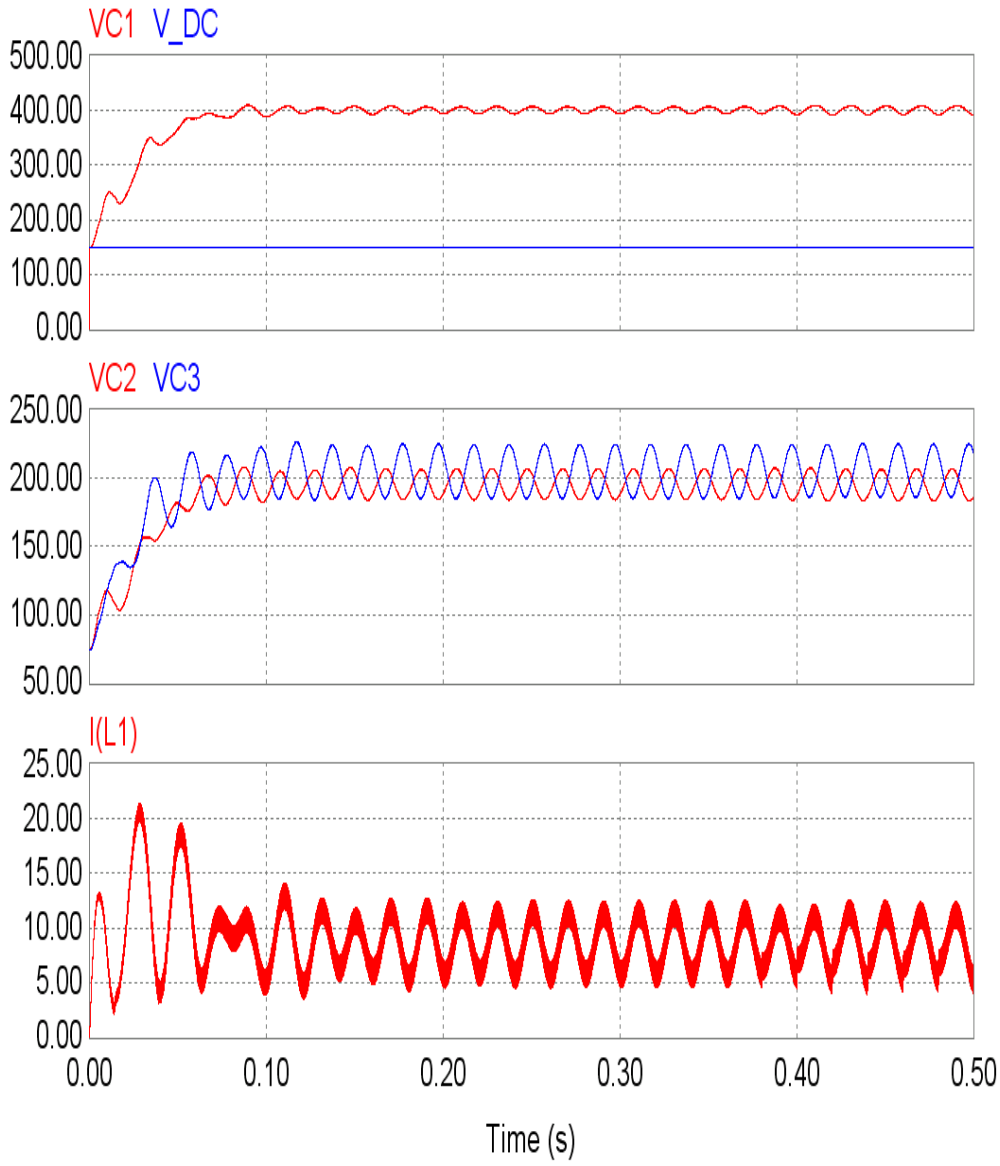

Fig. 2.24 Capacitor C1 voltage, input dc voltage, C2 and C3 capacitor voltages and L1 inductor current (from top to bottom)

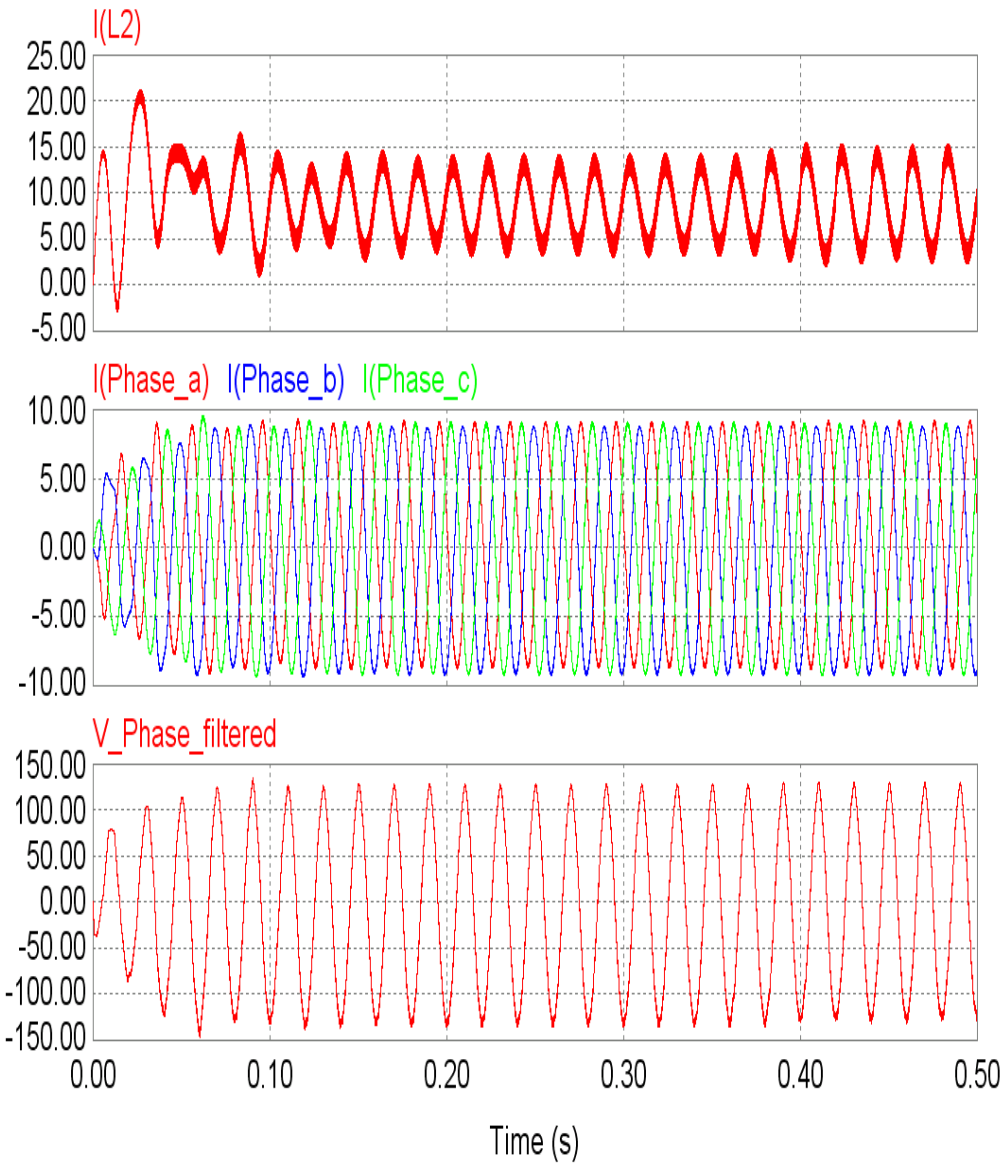

Fig. 2.25. L2 Z-source inductor current, load currents and the filtered phase voltage (from top to bottom)

We can see in Fig. 2.24 and Fig. 2.25 that not only the phase current and phase voltage are sinusoidal but the Z-source inductor currents as well.

2.5 Summary

This chapter presented the six-switch three-phase Z-source inverters. The four-switch VSIs has been presented in comparison with the three-phase VSIs and the space vector analysis baisc were also presented.

A new four-switch three-phase Z-source inverter topology has been proposed. Its operating states had been analysed based on the space phasors. A control algorithm has been presented. The presented analitical analysis of the proposed topology has been verified in simulation and experiments.

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CHAPTER 3 CONTROL AND DESIGN ASPECTS OF THE Z-SOURCE INVERTERS

3.1 Introduction

In the Z-source network the average capacitor voltage, being the average inverter bridge voltage, it has to be controlled. Without a careful design of the Z-source network elements, the capacitors and inductors, is not as easy to control it due to undesired operating modes of the Z-source inverter. The inrush current, which occurs at the connection of the voltage source to the Z-source inverter, is not less important because it can cause the failure of the front-end diode or the inverter bridge. This aspects will be adressed in this chapter after a thorough analysis of the important publications related to this issues.

In [1] for the control of the average capacitor voltage two control loops are used to show the good transient response of the Z-source inverter. One from the voltage error of the prescribed output voltage and the measured output voltage with a PI controller generates the prescribed voltage vector for the space vector algorithm and the other loop from the capacitor voltage error with a PI controller generates the ratio between the input dc voltage and the needed average capacitor voltage. This ratio is introduced in the voltage boost formula which calculates the shoot-through duty ratio. Even though the shoot-through time intervals are divided in 6 equal intervals over one switching period the inverter bridge may suffer from current overstress of the switches because the shortcircuits are made with only one leg at a time. The two control loops should be linked to assure optimum capacitor voltage boost.

Two shoot-through generation methods resulting naturally from the introduction of two carrier signals presented in [2] is intresting but they face some implementing problems of the two carrier signals on a dsp.

Maximum constant boost control presented in [3] overcomes the additional current stresses of the Z-source inductor at lower frequencies of the inverter ouput voltage in [4] but it needs an extra PWM pulse for the shoot-through pulse generation while the latter naturally generates the pulses (with some additional harware as we will see later) from the zero voltage states. However, the bottom line is what the application can afford: some additional control algorithm and an extra PWM output in the dsp or some extra hardware (control circuit).

Different operating states (five states) of the Z-source inverter are shown in [5] which depend on the inductance of the Z-source inductor. Even though these states, described by complicated equations, can be considered in the control loop and the size of the Z-source network can reduced with smaller inductance it is better to avoid these states in the design state of the Z-source inductor.

By state-space averaging of the two states of the Z-source network (shoot-through state and non shoot-through state) small signal analysis was done in [6]-[9] in oder to point out the performance and stability of the converter for paramter variations of the Z-source network elements or the shoot-through duty ratio variations. The RHP zero presence, which by the way is present in all boost converter topologies, was also pointed out in the control-to-output transfer function.

These small signal analysis provide useful information in the design of closed loop, multi input-multi output, control systems of the Z-source inverters.

The two control strategies of the peak dc-link voltage (actually the peak capacitor voltage which is not the same with the peak dc-link voltage) in [10][11] improve the system transient response and the controller design even more the system stability is enhanced.

Other control strategies are presented in [12] for dc-dc converters in [13] for photovoltaic panels (PV) with maximum poper point tracking strategy (MPPT) and in [14] for bi-directional adjustable speed drives (ASD) connected to the grid. Note in [14] that an additional switch and filter capacitor is needed between the Z-source network and the rectifier bridge.

In [15], besides a very good switching model for Matlab/Simulink of the Z-source network, gradual tunning of the active state in order to improve the transient response of the Z-source inverter is presented.

A good starting point for the Z-source inductor design based on the Z-source inductor current analysis is presented in [16] by avoiding the pseudo-active state.

3.2 Digital Simulation Issues

In the debugging process of the different control strategies [1]-[4] of the Z-source inverters the first step is to simulate them in a dedicated software like Matlab/Simulink, PSIM, PSpice, Saber etc. To develop a more complex control, the computational time of these softwares could be too long. To simplify the Z-source network model we can build a switching model based on the voltage and current equations of the Z-source network. The two state equations of the Z-source network in the non-shoot throguh state and the shoot-through states for the traditional Z-source inverter in [1] can be written as

$$\begin{bmatrix} \frac{d}{dt} i_{L1} \\ \frac{d}{dt} v_{C1} \\ \frac{d}{dt} i_{L2} \\ \frac{d}{dt} v_{C2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} & 0 & 0 \\ -\frac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L} \\ 0 & 0 & -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} \frac{d}{dt} i_{L1} \\ \frac{d}{dt} v_{C1} \\ \frac{d}{dt} i_{L2} \\ \frac{d}{dt} v_{C2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & \frac{1}{C} & 0 \\ 0 & -\frac{1}{L} & 0 & 0 \\ \frac{1}{C} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{V_{DC}}{L} \\ -\frac{i_{Load}}{C} \\ \frac{V_{DC}}{L} \\ -\frac{i_{Load}}{C} \end{bmatrix} \tag{3.2}$$

Equation (3.1) describes the shoot-through state and (3.2) describes the non-shoot-through state. Averageing the two equations we can obtain a state-space averaged model over one switching period T_s

$$\begin{bmatrix} \frac{d}{dt} i_{L1} \\ \frac{d}{dt} v_{C1} \\ \frac{d}{dt} i_{L2} \\ \frac{d}{dt} v_{C2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{D_{ST}}{L} & 0 & -\frac{D_A}{L} \\ -\frac{D_{ST}}{C} & 0 & \frac{D_A}{C} & 0 \\ 0 & -\frac{D_A}{L} & 0 & \frac{D_{ST}}{L} \\ \frac{D_A}{C} & 0 & -\frac{D_{ST}}{C} & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} D_A \frac{V_{DC}}{L} \\ -D_A \frac{i_{Load}}{C} \\ D_A \frac{V_{DC}}{L} \\ -D_A \frac{i_{Load}}{C} \end{bmatrix} \quad (3.3)$$

The state-space average model can be used for system performance analysis of the Z-source inverters [3.8]. The notations used in (3.1)-(3.3)
$C_1 = C_2 = C; L_1 = L_2 = L; D_A + D_{ST} = 1$.

Using (3.1) and (3.2) we can build the following switching-functional Z-source network in Matlab/Simulink

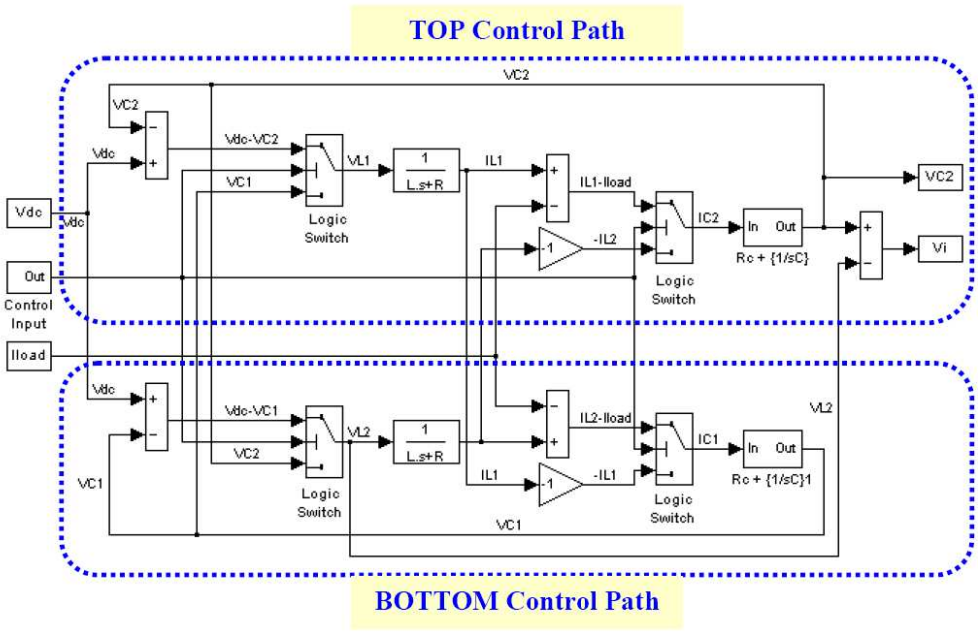


Fig. 3.1 Switching-functional model for Z-source network in Matlab/Simulink [8]

Note in Fig. 3.1 the control input to the logic switches makes the switch between the two equations (3.1) and (3.2).

3.3 Inrush current

At the moment of the connection of the dc source to the Z-source inverter the Z-sorce capacitors are discharged thus a great inrush current exists, which charges the capacitors to half the input dc voltage.after that the resonance between the Z-source capacitors and inductors takes place with large current and voltage

surge. Finally the capacitors get charged to the input dc voltage level. The current path of the inrush current is illustrated in Fig. 3.2.

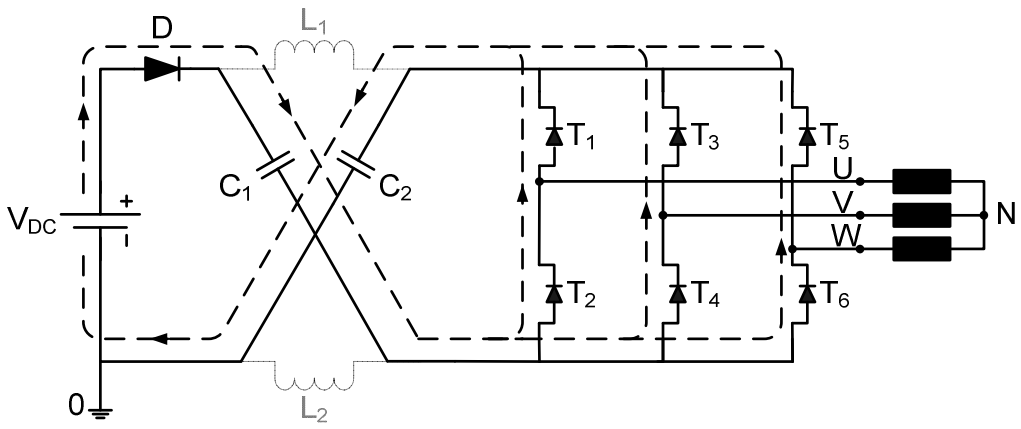


Fig. 3.2 Inrush current path at start-up

The inrush current goes through the front-end diode, the Z-source capacitors and the freewheeling diodes of the inverter bridge. A simulation was made to show the inrush current with the following circuit parameters

$L = L_1 = L_2 = 6.4mH; R_L = 0.7\Omega; C = C_1 = C_2 = 2200uF; R_C = 0.05\Omega$
$V_{DC} = 250V$

and the internal resistance of the voltage source and the resistance of each inverter leg was considered

$R_{VDC} = R_{PhaseLeg} = 0.1\Omega$

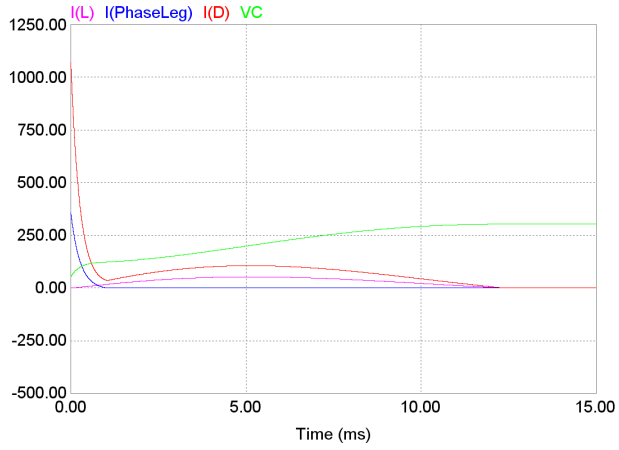


Fig. 3.3 The inrush diode, Z-inductor, inverter phase leg currents and the voltage across the Z-source capacitor

The inrush currents and voltages are illustrated in Fig. 3.3. The inherent property of the Z-source topology is that it can not be soft-started without additional circuitry and these high currents could destroy the front-end diode or the inverter bridge.

3.4 Z-Source Capacitor Voltage Control

The average capacitor voltage can be considered the Z-source network output due to the fact that is equal to the average voltage seen by the inverter bridge even if the peak dc-link voltage is considerably greater as we see in Chapter 1.

The proposed control algorithm presented in [1] is illustrated in Fig. 3.4

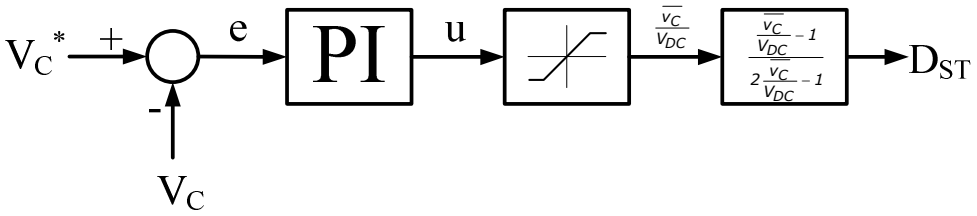


Fig. 3.4 Capacitor voltage control using a PI controller

The PI controller outputs the voltage ratio between the capacitor voltage and the input DC voltage. The PI controller can be implemented digitally using the trapezoidal integration rule

$$u(t) = K_p e(t) + uI(t-1) + \frac{T_s}{2}\left[\frac{K_p}{T_i}\left(e(t) - e(t-1)\right)\right] \tag{3.4}$$

where Kp is the proportional coefficient Ti the integration time constant Ts the switching frequency and uI(t-1) is the previous output of the integral term. The C code of the PI controller law with output limitations described in (3.4) is given below

```
PI_out=PI_out_next;
//Sample the input of the PI controller
ER=Vc_star-Vc;
//Calculate the PI controller output using Trapezoidal Rule
PI_out_next=Kp*ER+Iprev+Ts/2*(Kp/Ti*(ER+ERprev));
Iprev=Iprev+Ts/2*(Kp/Ti*(ER+ERprev));
ERprev=ER;
if(PI_out_next>PI_out_max)
PI_out_next=PI_out_max;
if(PI_out_next<PI_out_min)
PI_out_next=PI_out_min;
```

The control method presented in Fig. 3.5 uses the measured capacitor voltage. Another capacitor voltage control method, which uses only the measured input dc voltage, is described in [16] which uses the following expression to calculate the shoot-through duty ratio

$$D_{ST} = \frac{1}{2} - \frac{V_{DC}}{2\left(V_{DC} - 2\bar{v}_C^*\right)} \tag{3.5}$$

3.5 Maximum Boost Control of the Z-Source Inverter

The peak sinusoidal output voltage is given by the product of the modulation index and the boost factor (the shoot-through duty ratio) called the buck-boost factor multyplied by half the input dc voltage. Therefore the desired peak output voltage can be obtained by adjusting both terms of the buck-boost factor even though this could result in a non-optimal adjust of the buck-boost factor. The buck-boost factor can be rewritten as

$$\frac{\hat{v}_{ac}}{V_{DC}/2} = MB \tag{3.6}$$

with the notations used in chapter 1.

As eq. 3.6 suggests that for a desired buck-boost factor which is optimal regarding mainly the voltage stress of the inverter bridge and the voltage boost the modulation index should be maximized and the boost factor should be minimized. The next section will show how the maximum modulation index M can be obtained and the minimum boost factor B for a given buck-boost factor MB and it also investigates the voltage boost and the voltage stresses of the inverter bridge.

Using $D_{ST} = 1 - M$ for the boost factor in eq. 2.13 we get

$$B = \frac{1}{1 - 2(1 - M)} = \frac{1}{2M - 1} \tag{3.8}$$

Therefore the voltage gain will be (using eq. 1.13 and eq. 3.8)

$$G = MB = \frac{\hat{v}_{ac}}{V_{DC}/2} = \frac{M}{2M - 1} \tag{3.9}$$

And the modulation index for a given voltage boost can be described as

$$M = \frac{G}{2G - 1} \tag{3.10}$$

The peak voltage stress of the inverter bridge is proportinal with the boost factor

$$\hat{V}_{DC-Link} = BV_{DC} = \frac{G}{M}V_{DC} = \frac{G}{\frac{G}{2G - 1}}V_{DC} = (2G - 1)V_{DC} \tag{3.11}$$

Based on eq. (3.9) the voltage gain versus the modulation index is represented in Fig. 3.4. and the switches voltage stress versus the voltage gain is represented in Fig. 2.5. It can be noticed that for M=1 no voltage boost can be produced. For a low modulation index the voltage boost can be considerably high

but this results in a greater voltage stress of the inverter bridge. The operation region is the shaded area under the curve described by eq. (3.9). For M equal to 0.5 the voltage gain increases to infinite (see the horizontal interrupted line). Hence modulation indexes should be higher than 0.5 for voltage gains greater than 1. For a voltage gain of 2 the peak voltage stress of the inverter bridge/input dc voltage is 3, 50% higher than the voltage gain (see Fig. 3.5)

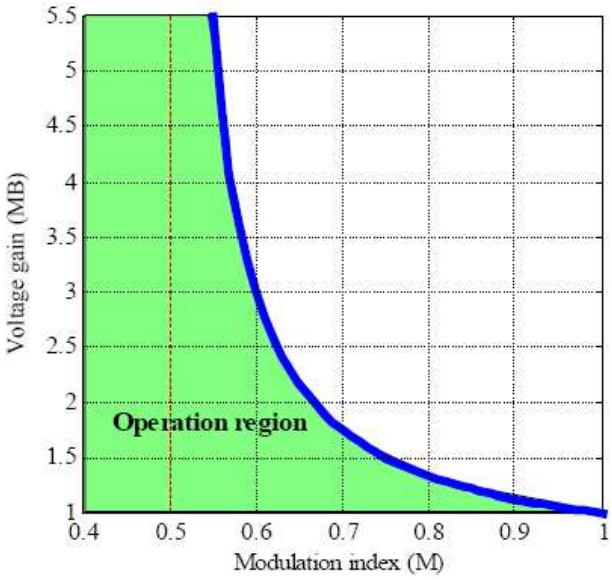


Fig.3.4 Voltage gain (MB) versus Modulation index (M) for constant shoot-through duty ratio (DST=1-M=const).

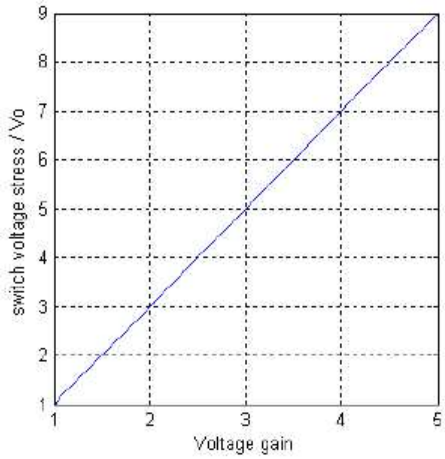


Fig.3.5. Peak inverter bridge voltage stress/input dc voltage versus voltage gain (MB) for constant shoot-through duty ratio (DST=1-M=const).

One of the simplest methods to generate shoot-through states in order to obtain a voltage boost without affecting the output voltage is to generate them

during the zero voltage vectors. Although it does not affect the output voltage waveforms it is dependent on the modulation index M. If the modulation index decreases the boost factor B can be increased. Without overriding the six active states of the inverter with shoot-through states the boost factor is limited to 1-M. This means that the maximum constant boost factor for a given modulation index M is 1-M. In Fig. 3.6. the constant shoot-through time generation is illustrated. Three shoot-through time intervals are evidentiated with gray bars from top to bottom.

The notations in the figure are as follows:

- T1,T2,T3,T4,T5,T6 – gating pulses for the six transistors of the inverter bridge
- ST – shoot-through pulses
- Va,Vb,Vc – the three sinusoidal refrence signals
- Vtri – the triangular carrier signal
- VP,VN – positiv and negativ peak of the sinusoidal refrence signals respectively proportional with the modulation index

For a constant shoot-through duty ratio (see the signal at the bottom of Fig. 3.6) the maximum shoot-through time duration, if we take a look at Fig. 3.6, is genrerated by the intersection of the triangular carrier signal with the two signals VP and VN and is equal with the time interval of the tail of the triangular signals exceeding VP and VN. In Fig. 3.6. the constat shoot-through duty ratio is chosen to be maximum possible (1-M). The maximum allowed constant shoot-through duty ratio for a given modulation is not equal with the zero voltage vectors' time interval over each switching perod. If we get closer in time to one of the peaks of the three sinusoidal refrence signals the maximum shoot-through duty ratio is approximately equal with the zero voltage time intervals. In Fig. 3.6. this moments in time are shown with interrupted lines at $\pi/6, \pi/2, 5\pi/6$ and so on. Between two interrupted lines the zero voltage time intervals are always longer than the maximum allowed shoot-through time intervals. So in between two interrupted lines the shoot-trough time interval could be longer than the constant maximum shoot-through time interval without changing the modulation index M. Varying the shoot-through time interval between two interrupted lines according to the variation of the zero voltage time intervals results in a higher average voltage boost. During each 60 degrees (between two interrupted lines) the shoot-through time interval variation follows the same variation pattern. Hence it is enough to calculate the average duty cycle over 60 degrees for example from $\pi/6$ to $\pi/2$.

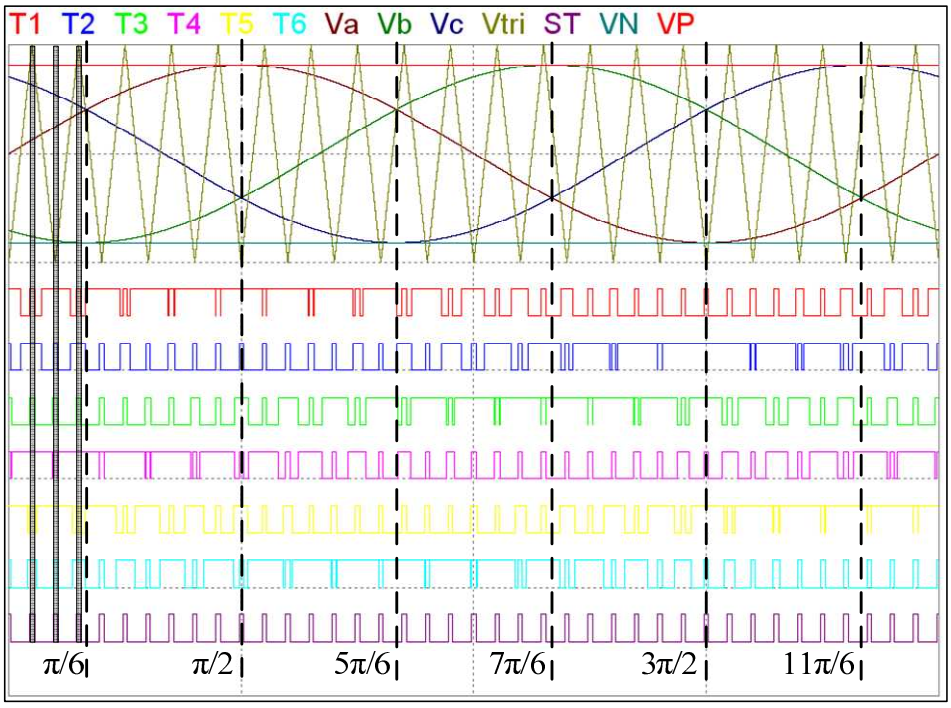


Fig.3.6 Carrier-based PWM control with constant boost control (shoot-through time placed during zero voltage time intervals)

Let us redraw the interval $\pi/6$ to $\pi/2$ with the shoot-through time interval equal with the zero voltage intervals during each switching period. The varying width gray bars in Fig. 3.6 illustrate the variation of the shoot-through time intervals with the zero voltage time intervals. In order to calculate the average boost factor first we have to calculate the average duty ratio for the shoot-through pulses shown at the bottom of Fig. 3.6. In the first step we will consider only one switching period and we will get to a formula for the zero voltage time intervals. For a carrer signal frequency much more higher than the frequency of the sinusoidal reference signals the reference sinusoidal voltages can be considered constant over one switching period. This is shown in Fig. 3.6.

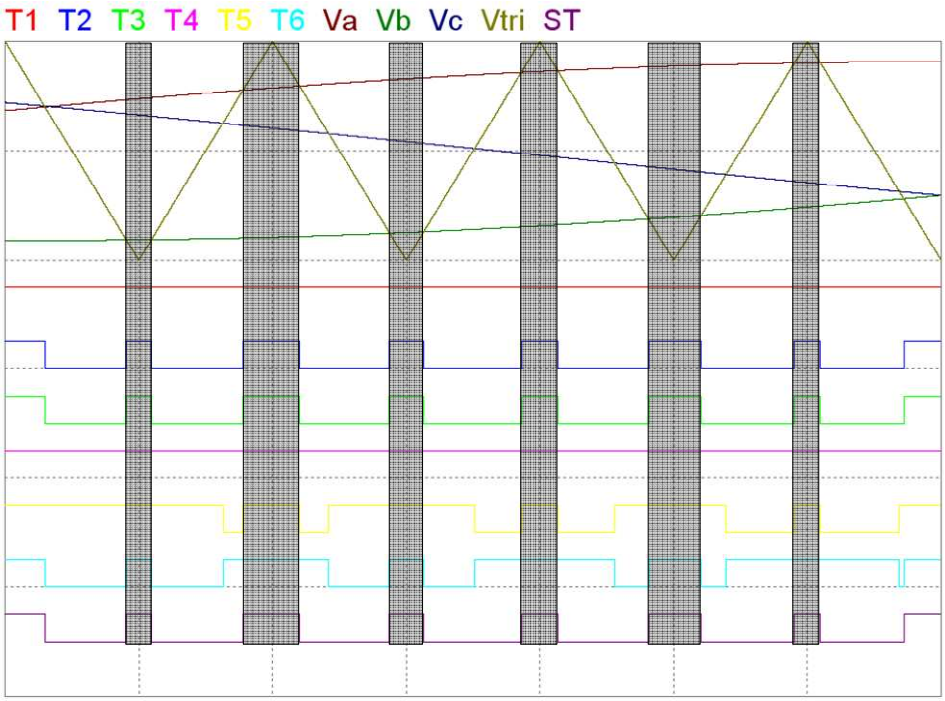


Fig.3.7.Carrier-based PWM control with varying shoot-through time interval (shoot-through time interval equal with the zero voltage time interval). Interval from $\pi/6$ to $\pi/2$

The averaged value of the three reference sinusoidal waveforms over one switching period T_s in Fig. 3.8 can be expressed as

$$\begin{aligned} V_a &= \frac{T_s}{2} M \sin(\alpha) \\ V_b &= \frac{T_s}{2} M \sin\left(\alpha - \frac{2\pi}{3}\right) \\ V_c &= \frac{T_s}{2} M \sin\left(\alpha - \frac{4\pi}{3}\right) \end{aligned} \tag{3.12}$$

where α is the electrical degree, M the modulation index and $\frac{T_s}{2}$ the height of the carrier signal. In the considered switching period in Fig. 3.8 the zero voltage vector time intervals (shoot-through time intervals) are delimited by the minimum and the maximum sinusoidal reference voltages in this case Va and Vb.

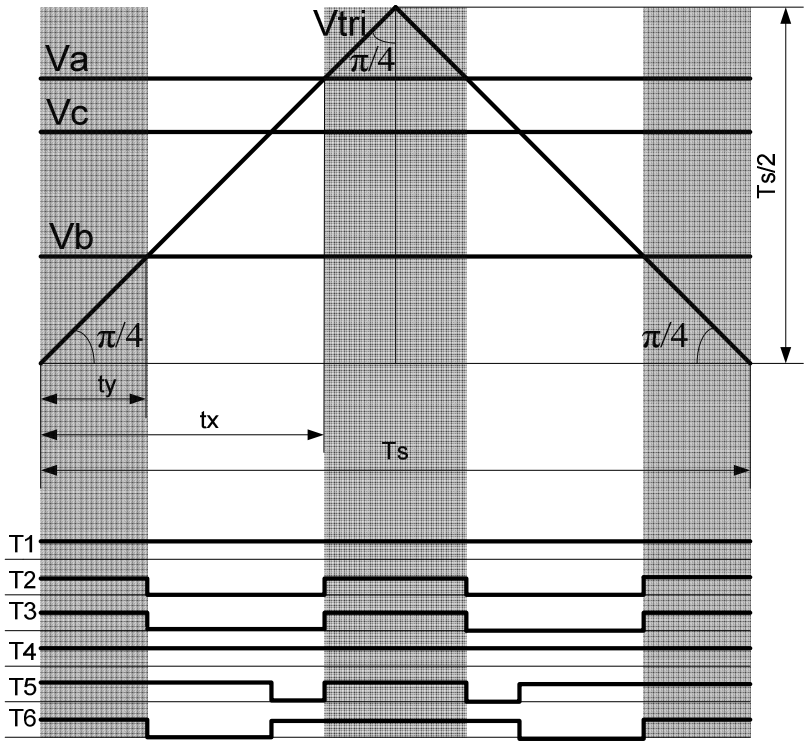


Fig.3.8 Signal generation for carrier-based PWM control with varying shoot-through time interval (shoot-through time interval equal with the zero voltage time interval)

The shoot-through time interval during the switching period can be described by

$$t_0 = t_{ST} = 2\left(T_s - t_x + t_y\right) = 2T_s - 2\left(t_x - t_y\right) \tag{3.12}$$

where t_0 is the zero voltage time interval.

By elementary tigonometric manipulations for t_x and t_y we get

$$\begin{aligned} t_x &= V_a = \frac{T_s}{2} M \sin(\alpha) \\ t_y &= V_b = \frac{T_s}{2} M \sin\left(\alpha - \frac{2\pi}{3}\right) \end{aligned} \tag{3.13}$$

With eq. 3.12. and eq. 3.13. the shoot-through duty ratio can be described by

$$D_{ST} = \frac{2 - \left(M \sin(\alpha) - M \sin\left(\alpha - \frac{2\pi}{3}\right)\right)}{2} \tag{3.14}$$

Next the average duty ratio in the interval $\left(\frac{\pi}{6},\frac{\pi}{2}\right)$ can be expressed by integrating the expression of D_{ST} on this interval with the independent variable α

$$\overline{D_{ST}} = \frac{\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} 2d\alpha - \left(\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} M\sin(\alpha)d\alpha - \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} M\sin\left(\alpha-\frac{2\pi}{3}\right)d\alpha\right)}{\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} 2d\alpha} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \tag{3.15}$$

The average boost factor can be expressed as

$$\overline{B} = \frac{1}{1-2\overline{D_{ST}}} = \frac{\pi}{3\sqrt{3}M-\pi} \tag{3.16}$$

With the shoot-through duty cycle equal to the zero voltage duty cycle all the time the voltage gain can be expressed as a function only of the modulation index

$$M\overline{B} = \frac{\pi M}{3\sqrt{3}M-\pi} \tag{3.17}$$

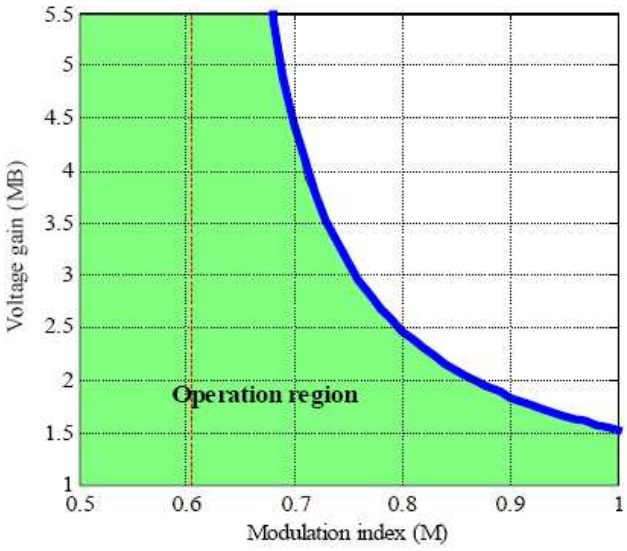


Fig.3.9 Voltage gain (MB) versus Modulation index (M) for varying shoot-through duty ratio with the zero voltage vector duty ratio.

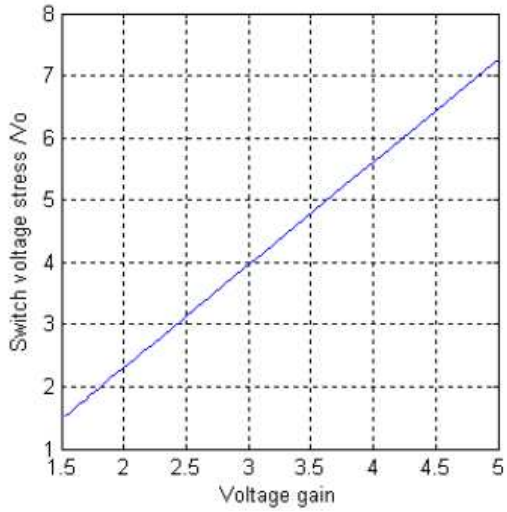


Fig.3.10 Average inverter bridge voltage stress/input dc voltage versus voltage gain (MB) for varying shoot-through duty ratio with the zero voltage vector duty ratio.

The voltage gain versus the modulation index is represented in Fig 3.8. In this case the modulation index for which the voltage gain is infinite is at $\frac{\pi}{3\sqrt{3}}$. The operation region got larger than in Fig. 3.8. Comparing Fig. 3.8 to Fig. 3.9. it can be noticed that in Fig. 3.9. at modulation index M=1 the voltage gain MB=1.5 which might be surpriseing. If we take a closer look at Fig. 3.7. we will see that even though for $\alpha = \frac{\pi}{2}$ and the peak refrence sinusoidal voltage $\hat{V}_a = \hat{V}_{tri}$ the shoot-through duty ratio is zero for $\frac{\pi}{3} < \alpha < \frac{\pi}{2}$ the shoot-through duty ratio is different from zero. The voltage gain versus the modulation index is represented in Fig. 3.10. and is described by (using eq. (3.17) and eq. (3.18))

$$M = \frac{\pi G}{3\sqrt{3}G - \pi} \tag{3.18}$$

The average voltage stress across the inverter bridge will be

$$\overline{V}_{DC-Link} = \overline{B}V_{DC} = \frac{\pi}{3\sqrt{3}M - \pi}V_{DC} = \frac{3\sqrt{3}G - \pi}{\pi}V_{DC} \tag{3.19}$$

Due to the fact that the boost-factor B varies in the interval $\pi/6$ to $\pi/2$ the voltage across the z-source network capacitors will also vary if it is small. For large z-source network capacitors the peak voltage stress of the inverter bridge could be considered to be equal with the average voltage stress

$$\hat{V}_{DC-Link} = \overline{V}_{DC-Link} = \overline{B}V_{DC} = \frac{\pi}{3\sqrt{3}M - \pi}V_{DC} = \frac{3\sqrt{3}\overline{G} - \pi}{\pi}V_{DC} \tag{3.20}$$

As a result of the variation of the shoot-through duty ratio with the variation of the zero voltage vector duty ratio for the same voltage gain as in Fig. 3.9. ($D_{ST} = 1 - M = const.$) the voltage stress across the inverter bridge is lower.

By injecting third harmonic components the modulation index can be extended even more. The reference sinusoidal voltages with the injected third harmonic components will be

$$\begin{aligned} Va &= M\frac{V_{DC}}{2}\left(sin(\alpha) + \frac{1}{6}sin(3\alpha)\right) \\ Vb &= M\frac{V_{DC}}{2}\left(sin\left(\alpha - \frac{2\pi}{3}\right) + \frac{1}{6}sin\left(3\left(\alpha - \frac{2\pi}{3}\right)\right)\right) \\ Vc &= M\frac{V_{DC}}{2}\left(sin\left(\alpha - \frac{4\pi}{3}\right) + \frac{1}{6}sin\left(3\left(\alpha - \frac{4\pi}{3}\right)\right)\right) \end{aligned} \tag{3.21}$$

with the maximum modulation index $M = \frac{2}{\sqrt{3}} = 1.154$.

The pulse generation strategy for the carrier-based PWM control with third harmonic injection and variable shoot-through duty shown in Fig. 3.11. is similar to the case without signal injection.

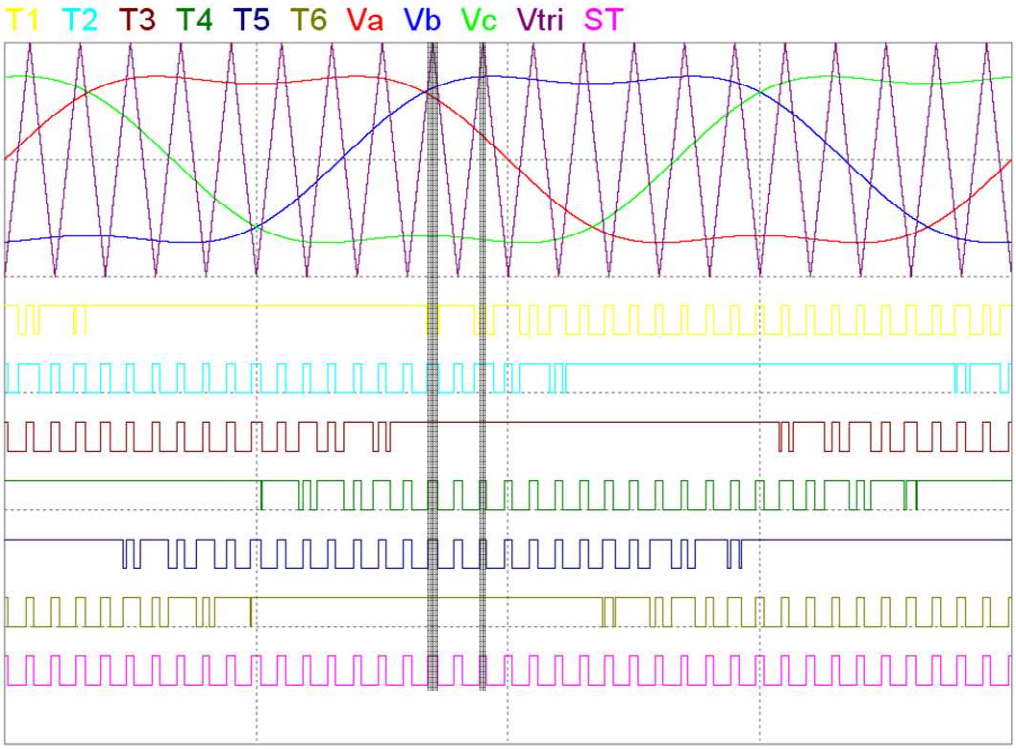


Fig. 3.11 Carrier-based PWM control with 3rd harmonic injection and varying shoot-through time interval (shoot-through time interval equal with the zero voltage time interval)

Following the same steps as in the previous case the shoot-through duty ratio over one switching period, the average shoot-through duty ratio, the average boost-factor and the voltage gain will be expressed.

Thus the average shoot-through duty ratio over one switching period is

$$D_{ST} = \frac{2 - M\left(\sin(\alpha) + \frac{1}{6}\sin(3\alpha) - \sin\left(\alpha - \frac{2\pi}{3}\right) - \frac{1}{6}\sin\left(3\left(\alpha - \frac{2\pi}{3}\right)\right)\right)}{2} \tag{3.22}$$

Integrating the above expression of D_{ST} on the interval $\pi/6$ to $\pi/2$ leads to the average shoot-through duty ratio

$$\overline{D_{ST}} = \frac{\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} 2d\alpha - M\left(\int_{\frac{\pi}{6}}^{\frac{\pi}{2}}\left(sin(\alpha)+\frac{1}{6}sin(3\alpha)\right)d\alpha - \int_{\frac{\pi}{6}}^{\frac{\pi}{2}}\left(sin\left(\alpha-\frac{2\pi}{3}\right)+\frac{1}{6}sin\left(3\left(\alpha-\frac{2\pi}{3}\right)\right)\right)d\alpha\right)}{\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} 2d\alpha}$$

$$\overline{D}_{ST} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \tag{3.23}$$

Finally the boost factor and the voltage gain

$$\overline{B} = \frac{1}{1-2\overline{D_{ST}}} = \frac{\pi}{3\sqrt{3}M-\pi} \tag{3.24}$$

$$G = M\overline{B} = \frac{\pi M}{3\sqrt{3}M-\pi} \tag{3.25}$$

Despite the injected 3rd harmonic components in the reference sinusoidal voltages the expressions of $D_{ST}, \overline{D}_{ST}, B$ and G did not change thus the voltage stress across the inverter bridge remains the same (see Fig. 3.12 and Fig. 3.13). With the 3rd harmonic injection the modulation index M has been increased for voltage gains between 1 and 1.5 (Fig. 3.12).

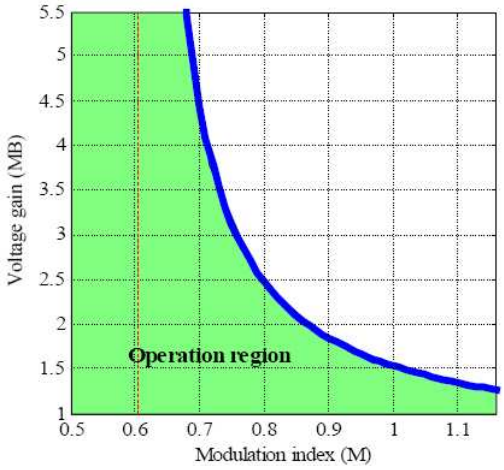


Fig.3.12 Voltage gain (MB) versus Modulation index (M) for varying shoot-through duty ratio with the zero voltage vector duty ratio (3rd harmonic injection).

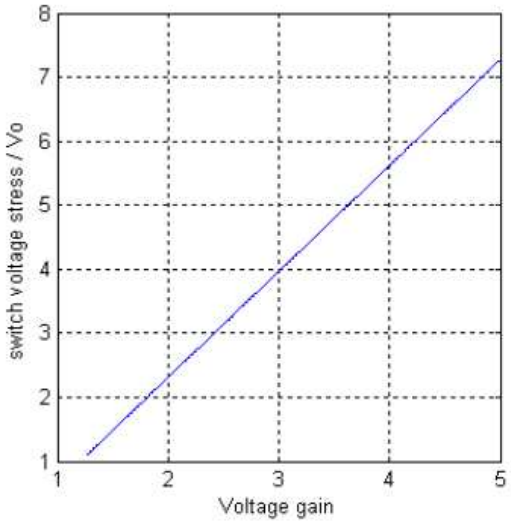


Fig.3.13 Average inverter bridge voltage stress/input dc voltage versus voltage gain (MB) for varying shoot-through duty ratio with the zero voltage vector duty ratio (3rd harmonic injection)

3.5.1 Hardware Implementation of the varying shoot-through pulses with the zero voltage vector pulses

The shoot-through signals can be generated in two ways: in the control program in the signal processor or hardware by extra gates added between the signal processor which generates the gating signals for the six switches of the inverter bridge and the drivers of the switches.

Usually the six PWM outputs of a digital signal processor used to control a three-phase inverter bridge are set to the complementary mode, meaning that if one transistor on a phase leg is on the other one is off. Briefly one way to generate the shoot-through signals in the control program is to override the complementary PWM outputs during the zero voltage time intervals which means that at least one extra timer (or extra PWM output synchronized with the 6 PWM signal generation internal unit) should be used, besides the PWM generation internal module of the signal processor, to determine the moments in time when the PWM outputs has to be overridden. Therefore the traditional space vector PWM generation algorithm has to be modified.

Without modifying the traditional space vector PWM algorithm the shoot-through signals can be generated by extra hardware thanks to the characteristics of the two control algorithms presented in the previous section: the shoot-through duty ratio=zero voltage duty ratio all the time. The schematic of the extra hardware needed between the DSP and the drivers of the inverter bridge is shown in Fig. 3.14.

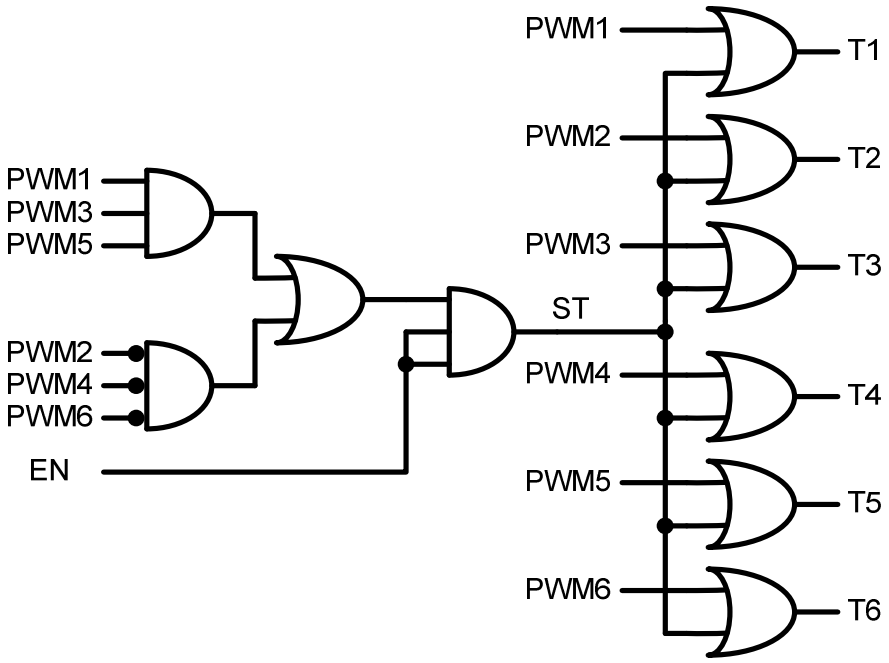


Fig.3.14. Hardware variable shoot-through signal generation (shoot-through duty ratio=zero voltage duty ratio)

After the complementary initialization of the PWM module in the DSP the PWM output signals of the DSP for the lower switches PWM2, PWM4 and PWM6 are on while the PWM signals for the upper switches PWM1, PWM3 and PWM5 are off. This state could be set well before the SVPWM algorithm starts. Thus the enable bit has to be kept low until the SVPWM algorithm starts in order to avoid a long shoot-through state which could lead to the failure of the inverter. The triple input AND gate for the upper switches PWM1, PWM3 and PWM5 monitors the zero voltages generated by turning on all the upper switches and outputs one if all of them are on while the 3 input NAND gate does the same thing for the lower switches of the inverter bridge. The two gates together cover the two zero voltage states. The or gate multiplies the two outputs and if the 3 input AND gate's enable is on it sends the resulting shoot-through state signals to the output 2 input OR gates which override the PWM input if ST is on.

The enable pin can be used to switch of the boost action of the control algorigthm if the prescribed output voltage level is lower than the input dc voltage. Thereby the voltage stresses of the inverter bridge will be reduced.

3.6 Pseudo-Active State of the Z-Source Inverter

So far the analysis of the voltages across the inductors and the capacitors of the Z-source network leaded to the formulae of the voltage gain and the voltage stresses of the inverter bridge. A closer analysis of the currents in the Z-source network reveals an other operation state of the converter. For this scope we will consider a three-phase Z-source inverter with wye connected load Fig. 3.15.

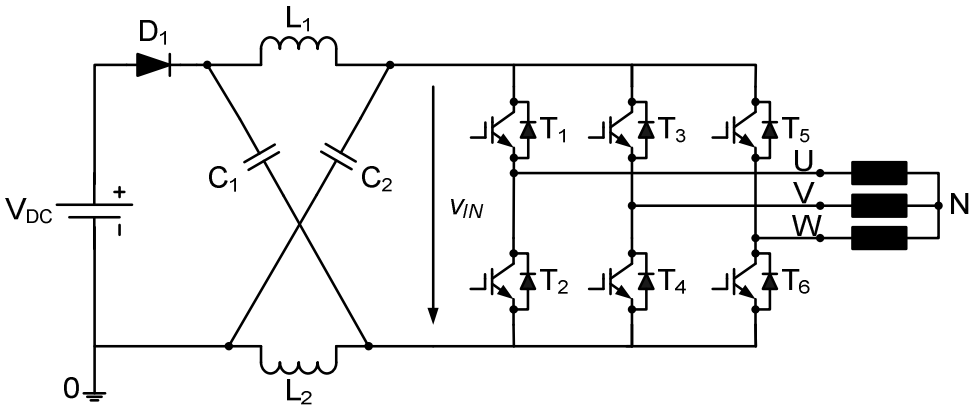
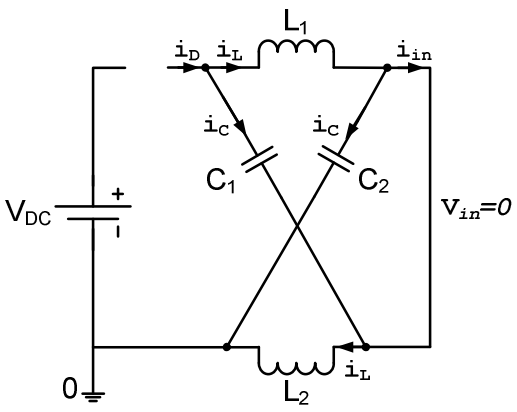


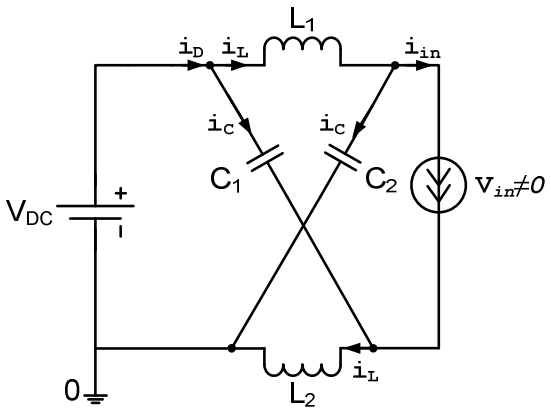
Fig. 3.15 Three-phase Z-source inverter

We have seen that mainly it has two operating states: the shoot-through state and the non shoot-through state or the active state. For the current analysis we assume that the shoot-through states are generated only during the zero voltage vectors and they have a shorter time interval than the zero voltage vector, the PWM signal generation is done with a middle aligned triangular carrier signal. The two inductors inductances are equal to each other as well as the two capacitors of the Z-source network.

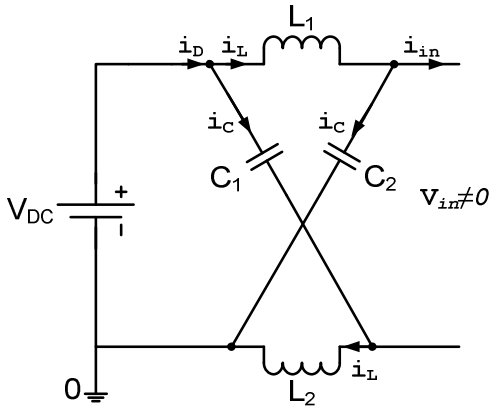
With the shoot-through time interval not necessarily equal to the zero voltage time interval we have three equivalent states for the three-phase Z-source inverter in Fig. 3.16.



a)



b)



c)

Fig. 3.16 The equivalent circuits for a) shoot-through state b) active state and c) zero voltage state

In the shoot-through state in Fig. 3.16a. the currents are

$$\begin{aligned} i_D &= 0 \\ i_L &= i_D - i_C = -i_C \\ i_{in} &= i_L - i_C = 2i_L \end{aligned} \tag{3.26}$$

The relationships between the currents in the active state when the power from the input is delivered to the output (the diode is conducting) are

$$\begin{aligned} i_C &= i_L - i_{in} \\ i_D &= i_L + i_C = 2i_L - i_{in} \\ i_{in} &= 2i_L - i_D \end{aligned} \tag{3.27}$$

Finally in the zero state when the inverter bridge current i_{in} is zero the inverter bridge is in one of the two zero voltage states all the upper switches or all the lower switches are on

$$\begin{aligned} i_{in} &= 0 \\ i_C &= i_L - i_{in} = i_L \\ i_D &= i_L + i_C = 2i_L \end{aligned} \tag{3.28}$$

Investigating the current levels of the three different states we will notice that in the zero state the current through the diode depends only on the current through the inductors on the other hand during the active states it depends on the current through the inductor and the dc-link current i_{in}

$$i_D = 2i_L - i_i \tag{3.29}$$

In the shoot-through state the diode is not conducting as illustrated in Fig. 3.16a and in eq. (3.26) because the voltage at the cathode of the diode is twice the capacitor voltage and at the anode is the input dc voltage so the diode is reverse-biased. We know that when the current through the diode gets negative the diode stops conducting therefore in eq. (3.29) if the dc link current becomes greater than twice the inductor current the front-end diode of the z-source network stops conducting. Considering that this situation could occur during the active state (power delivered to the load), if

$$i_{in} \geq 2i_L \tag{3.30}$$

In this state only the Z-source network will deliver power to the load. This state will be called the pseudo-active state.
The equivalent circuit of the pseudo-active state is shown in Fig. 3.17.

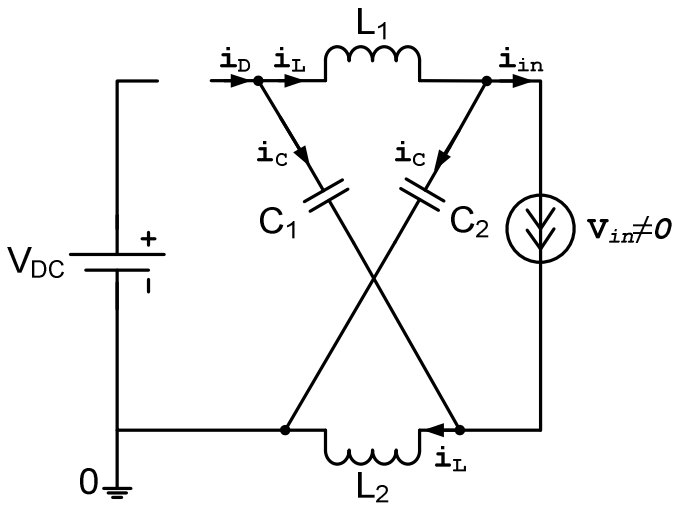


Fig. 3.17 The equivalent circuit of the pseudo-active state

The relationships between the current in the equivalent circuit in Fig. 3.17. can be expressed as

$$\begin{aligned} i_D &= 0 \\ i_C &= i_D - i_L = -i_L \\ i_{in} &= i_L - i_C = 2i_L \\ i_{in} &= \frac{1}{2} i_{in} \end{aligned} \tag{3.31}$$

What happens in the pseudo-active state is that the dc-link current i_{in} becomes 0.5 times greater than the current through the inductors and as a consequence the front-end diode stops conducting. Because the load inductance is much greater than the Z-source network inductors' inductance the dc link current during the pseudo active state could be considered constant and equal with twice the inductor current

$$\begin{aligned} i_{in} &= 2i_L = const \\ v_L &= L\frac{di_L}{dt} = 0 \\ v_{in} &= \overline{v_C} - v_L = \overline{v_C} \end{aligned} \tag{3.32}$$

As eq. (3.32) shows, during the pseudo-active state, the voltage across the inverter bridge drops from V_C to $2V_C$-V_{DC}.

Let us examine the voltages across the inverter bridge and across the inductor in the four possible states:

the shoot-through state $v_{in} = 0, v_L = \overline{v_C}$

- the active state $v_{in} = 2\overline{v_C} - V_{DC}, v_L = \overline{v_C} - V_{DC}$
- the zero state $v_{in} = 2\overline{v_C} - V_{DC}, v_L = \overline{v_C} - V_{DC}$
- the pseudo-active state $v_{in} = \overline{v_C}, v_L = 0$

It can be noticed that during the pseudo-active state the voltage across the inverter bridge is not equal with the voltage in the active state. In the derivation of the relationship between $\overline{v_C}$ and V_{DC} the starting point was the zero average voltage across the inductors in steady-steady. Note that in pseudo-active state the voltage across the inductors is zero. Therefore the formula for the average capacitor voltage will be different.

The voltage across the inductor will be integrated again in order to obtain the new formula

$$\begin{aligned} V_L &= \frac{1}{T_s}\int_0^{T_s} v_L(t)dt = 0 \\ &\frac{1}{T_s}\left(\overline{v_C}t_{ST} + \left(V_{DC} - \overline{v_C}\right)\left(T_s - t_{ST} - t_{PA}\right) + 0 \cdot t_{PA}\right) = 0 \\ \overline{v_C} &= \frac{1 - D_{ST} - D_{PA}}{1 - 2D_{ST} - D_{PA}} V_{DC} \end{aligned} \tag{3.33}$$

where $D_{PA} = \frac{t_{PA}}{T_s}$ is the duty ratio of the pseudo-active state and $T_S - t_{ST} - t_{PA}$ is the active state time duration.

As eq. (8.8) shows the average voltage across the capacitor becomes greater in the presence of the pseudo-active state.

For the graphical representation of the last eq. in (3.33) we will consider the shoot-through state duty ratio $D_{ST} = 0.3$ and the pseudo-active state $D_{PA} \in [0,0.2]$.

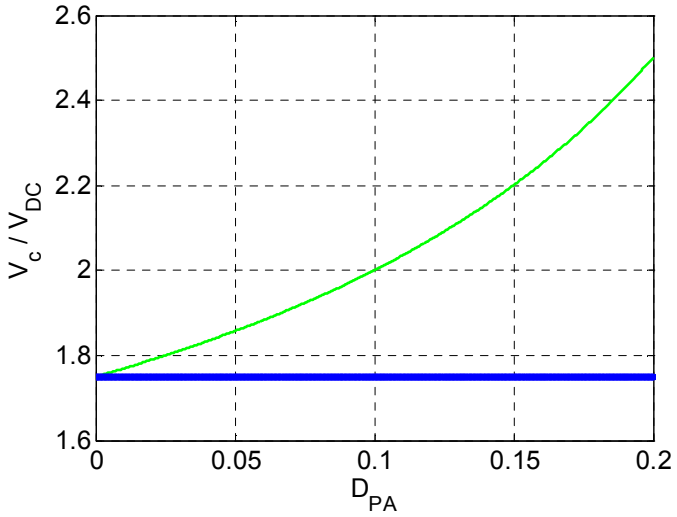


Fig. 3.18 The ratio between the capacitor voltage and the input voltage $\frac{\overline{v_C}}{V_{DC}}$ as a function of the pseudo-active state

In Fig. 3.18 the horizontal line represents the ratio VC/VDC for no pseudo-active state.

The most important thing to be kept in mind is that the pseudo-active state is generated by the load current not by the control. Through a careful design of the z-source network inductors the pseudo-active state thus simplifying the control algorithm.

3.6.1 Pseudo-active state average duty ratio

As we have seen in the previous section the pseudo-active state depends on the z-source inductor inductances, the instantaneous dc-link current $i_{in}(t)$ and the load parameters. In the following the average pseudo-active state will be derived. In the upper part of Fig. 3.19 we have the instantaneous dc-link voltage waveform in the presence of the pseudo-active state t_{PA}.

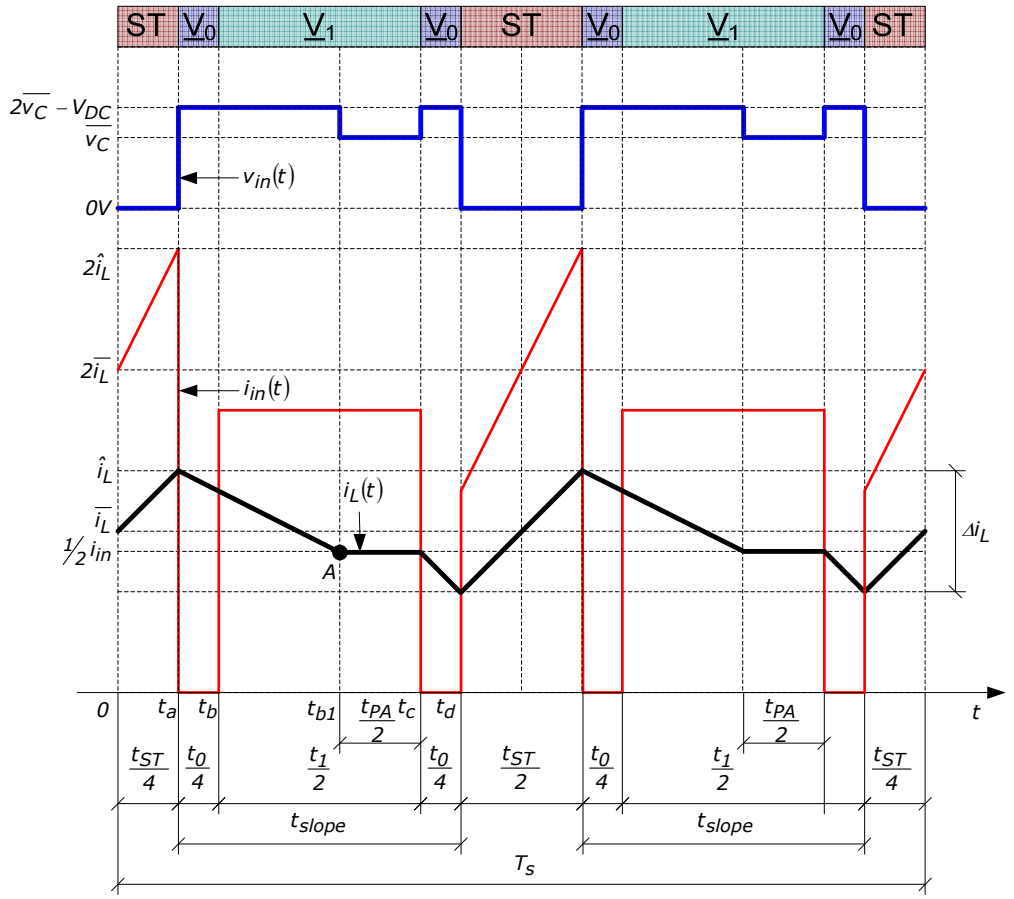


Fig. 3.19 Dc-link voltage $v_{in}(t)$, dc-link current $i_{in}(t)$ and z-source inductor current $i_L(t)$ in the presence of the pseudo-active state t_{PA}

The average of this voltage can be expressed as

$$\overline{v_{in}} = \frac{1}{T_s}\int_0^{T_s} v_{in}(t)dt = \frac{1}{t_{slope}}\int_0^{t_{slope}} v_{in}(t)dt = \frac{1}{t_{slope}}\left(\left(2\overline{v_C} - V_{DC}\right)\left(t_{slope} - t_{PA}\right) + \overline{v_C}t_{PA}\right) \quad (3.34)$$

Substituting the formula for $\overline{v_C}$ in (3.33) into (3.34) we get

$$\overline{v_{in}} = \left(\frac{1 - D_{ST} - D_{PA}}{1 - 2D_{ST} - D_{PA}}\frac{1}{1 - D_{ST}}\right)V_{DC} = B_{PA}V_{DC} \quad (3.35)$$

where B_{PA} is the new boost factor.
In case of a constant shoot-through duty ratio we have

$$D_{ST} = 1 - M \tag{3.36}$$

Using (3.36) in (3.35)

$$B_{PA} = \frac{M - D_{PA}}{2M - 1 - D_{PA}} \frac{1}{M}, D_{PA} = \frac{1}{t_{PA}} \tag{3.37}$$

The peak phase voltage can be expressed

$$\hat{v}_{ac} = MB_{PA} \frac{V_{DC}}{2} = \frac{1 - D_{ST} - D_{PA}}{2(1 - 2D_{ST} - D_{PA})} V_{DC} \tag{3.38}$$

During a switching period we know the constant shoot-through time duration but the zero voltage vector and the pseudo-active state time durations change, in one period T of the fundamental output current, as we walk along the time axis in Fig. 8.5.
The average zero voltage duty ratio can be defined by

$$\overline{D_0} = \frac{1}{T} \int_0^T D_0(\alpha) d\alpha = \frac{1}{\frac{5\pi}{6} - \frac{\pi}{6}} \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} D_0(\alpha) d\alpha \tag{3.39}$$

In Fig. 3.20 the zero voltage duty ratio is

$$D_0(\alpha) = 1 - D_1(\alpha) - D_{ST} \tag{3.40}$$

where

$$D_1(\alpha) = \frac{1}{2} + \frac{1}{2} M \sin(\alpha) = \frac{1}{2} + \frac{1}{2}(1 - D_{ST}) \sin(\alpha) \tag{3.41}$$

Substituting (8.41) with (8.40) for the average duty ratio (8.39) we obtain

$$\overline{D_0} = \frac{1}{2}\left(1 - \frac{3\sqrt{3}}{2\pi} - \left(2 - \frac{3\sqrt{3}}{2\pi}\right) D_{ST}\right) \tag{3.42}$$

The average dc-link current $\overline{i_{in}}$ can be given by

$$\overline{i_{in}} = \frac{1}{T} \int_0^T i_{in}(\alpha) d\alpha = \frac{1}{\frac{5\pi}{6} - \frac{\pi}{6}} \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} \hat{i}_{ac} \sin(\alpha) d\alpha = \frac{3}{\pi} \hat{i}_{ac} \tag{3.43}$$

The voltage across the inductor is

$$u_L = L \frac{\Delta i}{\Delta t} \text{ or } \Delta t = L \frac{\Delta i}{u_L} \tag{3.44}$$

Applying (8.44) on the down-slope of the inductor waveform in the interval $[t_a, t_{b1}]$

$$\begin{aligned}\Delta t = t_a - t_{b1} &= \frac{L}{\overline{v_C} - V_{DC}}\left(\hat{i}_L - \frac{1}{2}\overline{i_{in}}\right) = \frac{L}{\overline{v_C} - V_{DC}}\left(\overline{i_L} + \frac{1}{2}\Delta L - \frac{1}{2}\overline{i_{in}}\right) \\ &= \frac{L}{\overline{v_C} - V_{DC}}\left(\frac{P_{out}}{V_{DC}} + \frac{\overline{v_C}}{L}\frac{t_{ST}}{4} - \frac{1}{2}\frac{3}{\pi}\hat{i}_{ac}\right)\end{aligned} \tag{3.45.1}$$

Another way to express Δt using only time variables (see Fig. 3.19) would be

$$\Delta t = t_{slope} - \frac{\overline{t_{PA}}}{2} - \overline{D_0}\frac{T_s}{2} = \frac{T_s}{2}\left(1 - \frac{3\sqrt{3}}{2\pi}\right) - \frac{1}{2}\left(1 - \frac{3\sqrt{3}}{2\pi}\right)\frac{t_{ST}}{4} - \overline{t_{PA}} \tag{3.45.2}$$

Finally using (3.33) in (8.45.2) from the two expression of Δt we obtain the average duty ratio for the pseudo-active state

$$\overline{D_{PA}} = \frac{\frac{4f_s L}{\overline{v_C} - V_{DC}}\left(\frac{P_{out}}{V_{DC}} - \frac{1}{2}\frac{\pi}{3}\hat{i}_{ac}\right) + \left(1 + \frac{3\sqrt{3}}{2\pi}\right)\left(\frac{\overline{v_C} - V_{DC}}{2\overline{v_C} - V_{DC}} - 1\right) + \frac{\overline{v_C}}{2\overline{v_C} - V_{DC}}}{\left(1 + \frac{3\sqrt{3}}{2\pi}\right)\frac{\overline{v_C} - V_{DC}}{2\overline{v_C} - V_{DC}} + \frac{\overline{v_C}}{2\overline{v_C} - V_{DC}} - 2}$$

(8.46)

3.6.2 Design of the Z-source Inductor

In order to derive the formula for the Z-source inductor we will analyse the inductor and the dc-link voltage waveforms during one switching period. During one switching period in the active state time interval the dc-link current i_{in} has two current levels due to the two consecutive active vectors. In the analysis of the currents we will consider a sample switching period at the peak current in phase U (or the values of the phase currents at 0 electrical degrees) thus only one voltage vector will be during the active state (only one current level).

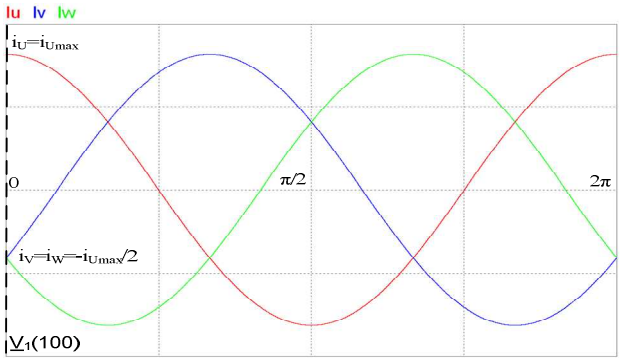


Fig. 3.20 Load current waveforms

$$i_U = \sqrt{2}I\cos(0) = \sqrt{2}I$$
$$i_V = i_W = \sqrt{2}I\cos\left(0 - \frac{2\pi}{3}\right) = -\frac{1}{2}\sqrt{2}I$$

The equivalent circuit of the load during the active state is shown in Fig. 3.21.

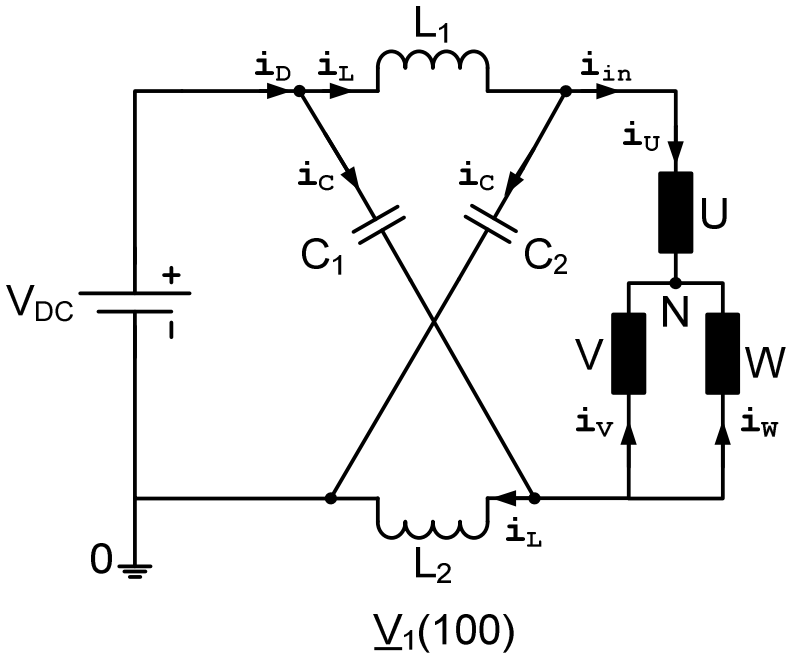


Fig. 3.21 The load equivalent circuit for the active state

Next the instantaneous dc-link i_{in} current the inductor i_L current and twice of the inductor current $2i_L$ waveforms are illustrated in Fig. 3.22.

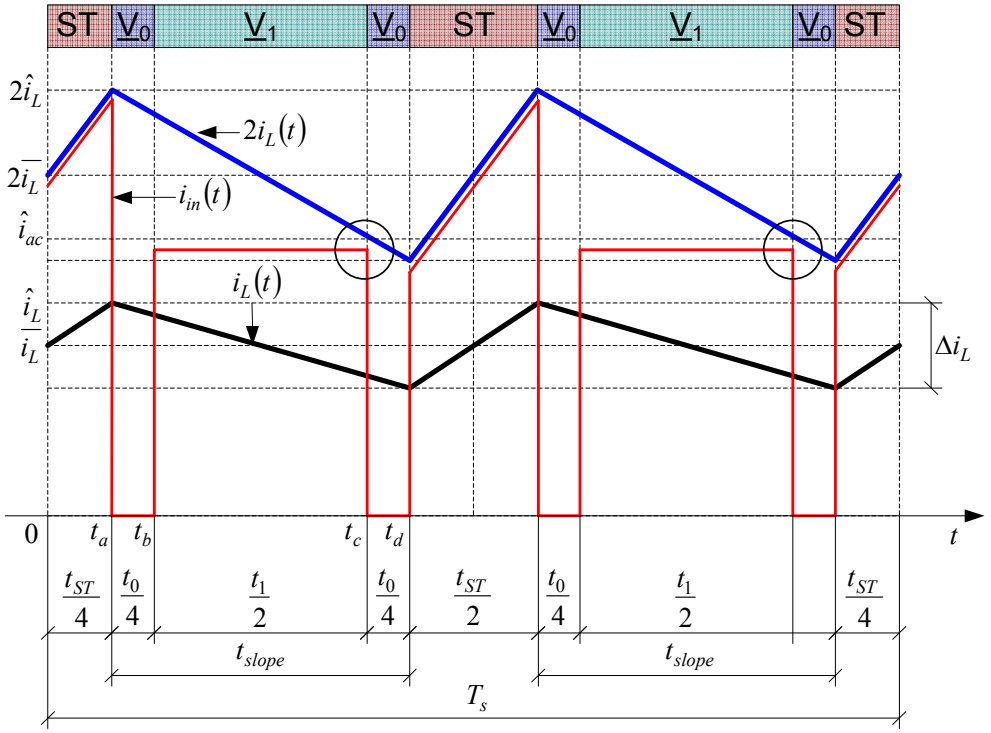


Fig. 3.22 The dc-link current iin the Z-source inductor current iL and 2iL during one switching period Ts

In Fig. 3.22 the dc-link current i_{in} was a little bit scaled down to avoid the overlap with some portions of the inductor current waveform. The zoomed current waveforms in Fig. 3.22 are the currents for the equivalent circuit presented in Fig. 3.20.

The notations used in Fig 3.22 are as follows

- $\hat{i}_L, \overline{i_L}$ - peak and average inductor current
- $\hat{i}_{ac}$ - the peak of the sinusoidal load current
- t_0, t_{ST}, t_1 - zero voltage vector time duration, shoot-through time duration, and active voltage time duration

where

$$t_1 + t_0 + t_{ST} = T_s \tag{3.47}$$

The condition which should be met in order to avoid the pseudo-active state is

$$2i_L(t) \geq i_{in}(t) \text{ and } t_b < t < t_c \tag{3.48}$$

The expression above has to be satisfied all the time. In the considered switching period in Fig. 3.22 the dc-link current during the zero voltage vector $\overline{V_0}$ time intervals is zero, during the active voltage vector $\overline{V_1}$ time intervals is equal with the

peak output current, due to the considered situation in Fig. 3.22, while during the shoot-through time intervals ST it is twice the inductor current. As we can see in Fig. 3.22 the boundary in time where the Z-source inverter enters the pseudo-active state, twice the inductor current becomes equal with the dc link current, is at t_c where the down-slope of the twice the inductor current waveform would intersect the dc link current waveform (see the small circles in Fig.3.22). Hence this intersection of the two waveforms has to be avoided.

The voltage across the Z-source inductor during the $0 \le t \le t_{slope}$ is described by

$$\overline{v_L} = L\frac{di_L(t)}{dt} = V_{DC} - \overline{v_C} \tag{3.49}$$

The inductor current has its maximum at t_a and its minimum at t_d. In this time interval the instantaneous inductor current can be described by the equation of a straight line

$$i_L(t) = \frac{V_{DC} - \overline{v_C}}{L}t + \hat{i}_L, \quad 0 \le t \le t_{slope} \tag{3.50}$$

The peak inductor current can be expressed as

$$\hat{i}_L = \overline{i_L} + \frac{1}{2}\Delta i_L \tag{3.51}$$

where the expression of the peak-peak inductor current is

$$\Delta i_L = \left|\frac{V_{DC} - \overline{v_C}}{L}\right| t_{slope} = \frac{\overline{v_C} - V_{DC}}{L}t_{slope} \tag{3.52}$$

Substituting (3.51) into (3.52)

$$\hat{i}_L = \overline{i_L} + \frac{1}{2}\frac{\overline{v_C} - V_{DC}}{L}t_{slope} \tag{3.53}$$

By inserting (3.53) into (3.50) and in order to avoid the pseudo-active state (3.48) it will look like

$$\begin{aligned} &2\left(\frac{V_{DC} - \overline{v_C}}{L}\left(t_{slope} - \frac{t_0}{4}\right) + \overline{i_L} + \frac{\overline{v_C} - V_{DC}}{L}\frac{t_{slope}}{2}\right) \ge i_{in}(t) \\ &\frac{V_{DC} - \overline{v_C}}{L}\left(t_{slope} - \frac{t_0}{4}\right) + 2\overline{i_L} \ge i_{in}(t) \\ &t_{slope} = \frac{T_s - t_{ST}}{2} \\ &t_a \le t \le t_c \end{aligned} \tag{3.54}$$

From (3.54) the expression of the Z-source inductor inductance can be derived

$$L \geq \frac{\overline{v_C} - V_{DC}}{2f_s\left(2\overline{i_L} - i_{in}(t)\right)}\left(1 - D_{ST} - 2D_0\right)$$
$$D_0 = \frac{t_0}{T_s}, f_s = \frac{1}{T_s} \tag{3.55}$$

It can be noticed in (3.55) that the size of the inductor is inversely proportional to the switching frequency and directly proportional to the shoot-through duty ratio and the zero voltage duty ratio and the dc-link current. The worst situation is obtained for i_{in} equal with the peak ac output current and zero voltage vector duty ratio equal with 0. However the deduced formula for the inductor is switching pattern dependent. For the worst case

$$L \geq \frac{\overline{v_C} - V_{DC}}{2f_s\left(2\overline{i_L} - \hat{i}_{ac}\right)}\left(1 - D_0\right) \tag{3.56}$$

For a three-phase Z-source inverter with wye connected three phase load with known output power, power factor, line-to-line voltage and varying dc input voltage we have

$$P_{out} = P_{DC} = V_{DC}\overline{i_{DC}} \tag{3.57}$$

The average input current

$$\overline{i_{DC}} = \frac{P_{out}}{V_{DC}} \tag{3.58}$$

To make fully use of the average dc-link voltage (the average voltage across the Z-source capacitor) the average capacitor voltage can be expressed as

$$\overline{v_C} = 2\hat{v}_{ac} \tag{3.59}$$

And the shoot-through duty ratio using (7) will be

$$D_{ST} = \frac{2\hat{v}_{ac} - V_{DC}}{4\hat{v}_{ac} - V_{DC}} \tag{3.60}$$

For the wye connected load the peak output phase voltage can be expressed by

$$\hat{v}_{ac} = \frac{\sqrt{2}}{\sqrt{3}}\hat{v}_{LL} \tag{3.61}$$

The output power

$$P_{out} = \sqrt{3}u_{ac_{eff\_line}}i_{ac_{eff\_line}}\cos(\phi) \tag{3.62}$$

Using (3.59)(3.61) and (3.62) the peak output phase current is given by

$$\hat{i}_{ac} = \frac{\sqrt{2}}{\sqrt{3}} \frac{P_{out}}{\hat{v}_{LL} \cos(\phi)} \tag{3.63}$$

The average inductor current in steady-state is equal with the average input current

$$\overline{i_L} = \overline{i_{DC}} = \frac{P_{out}}{V_{DC}} \tag{3.64}$$

Finally using (3.29)(3.60)(3.61) and (3.64) in the expression of the inductance we get

$$L \geq \frac{\hat{v}_{LL}{}^2 \cos(\phi)\left(4\hat{v}_{LL}V_{DC} - \sqrt{6}V_{DC}{}^2\right)}{\sqrt{6}f_s P_{out}\left(V_{DC}{}^2 - \left(\frac{8}{\sqrt{6}}\hat{v}_{LL} + \sqrt{6}\hat{v}_{LL}\cos(\phi)\right)V_{DC} + 8\hat{v}_{LL}{}^2\cos(\phi)\right)} \tag{3.65}$$

The maximum value for L can be obtained for

$$\frac{dL}{d\overline{v_C}} = 0 \tag{3.66}$$

Solving (3.66) we get

$$V_{DC} = \frac{4\sqrt{6}\hat{v}_{LL}\cos(\phi) \pm 4\hat{v}_{LL}\sqrt{3\cos^2(\phi) - 2\cos(\phi)}}{2 + 3\cos(\phi)} \tag{3.67}$$

Further investigations can be made in order to get a more realistic formula for the Z-source inductance in (3.56) because in this case the worst case scenario was considered, which may not occur during the operation of the inverter.

3.6.3 Dimensioning of the Z-source capacitor

We assume that all the energy stored in the capacitors is delivered to the load during one switching period

$$P_{out} = \frac{\frac{1}{2}C_{tot}V_{C\,max}{}^2 - \frac{1}{2}C_{tot}V_{C\,min}{}^2}{T_s} \tag{3.68}$$

where

$$C_{tot} = C_1 + C_2 = 2C \tag{3.69}$$

and due to the shoot-through state the switching frequency gets doubled

$$P_{out} = 2C\frac{V_{C\,max}{}^2 - V_{C_{min}}{}^2}{T_s} \tag{3.70}$$

For a desired ripple voltage ΔV_C

$$\begin{aligned} V_{C\,max} &= \overline{v_C} + \frac{1}{2}\Delta V_c \\ V_{C\,min} &= \overline{v_C} - \frac{1}{2}\Delta V_c \end{aligned} \tag{3.71}$$

Substituting (3.71) into the expression of the output power (3.70) and rewriting it for the considered ripple voltage we get the formula for the capacitance

$$C = \frac{P_{out}}{4\Delta C f_s \overline{v_C}} \tag{3.72}$$

Summary

Different simulation methods of the Z-source inverters have been explained. Inherent topology problems like huge inrush current have been pointed out. A few Z-source capacitor voltage control strategies were presented. Boost control strategies were explained as well as Z-source inductor and capacitor design algorithms which avoid the pseudo active state.

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CHAPTER 4 IMPROVED THREE-PHASE Z-SOURCE INVERTERS

4.1 Introduction

The improved Z-source inverter with six switches proposed in [1] in 2009 is a single stage buck-boost inverter as the Z-source inverter presented in [2]. Fundamentally it consist of the same components: the front end diode, the two port X shaped network formed by two identical inductors and two identical capacitors, the six switch inverter bridge and one dc voltage source which can be a solar panel, fuel cell or the rectified output voltage of a permanent magnet synchronous generator connected to a wind turbine. Even though it incorporates the same components by rearranging Fig 4.1 the elements enhances its properties. The two drawbacks which are overcome by the new topology would be

- the inrush current and the resonance of the Z-source capacitors and inductors at start-up which could cause failure of the devices
- the high average Z-source capacitor's voltage which is always equal to the average dc-link voltage

Several other current and voltage fed new Z-source topologies proposed by the same authors can be found in [3].

Simple constant boost control with third harmonic signal injection in the reference sinusoidal signals [4], well-known from the traditional Z-source inverter, is used in case of the improved topology in order to increase the modulation index and reduce the voltage and current stress of the inverter bridge.

The feed-forward plus feedback control for the improved Z-source and not only presented in [5] uses only the measured input dc voltage for rough regulation of the shoot-through state and the measured peak output voltage is used for precise adjust of the shoot-through duty cycle. This method assures fast response for load and input voltage variations without taking into account the Z-source network model.

4.2 Six Switch Improved Three-Phase Z-Source Inverter

The recently proposed switched inductor Z-source inverter [6] has a higher voltage gain then the traditional one and the improved Z-source topologies but it has extra diodes and inductors in the Z-source network. The improved Z-source inverter topology with six switches is shown in Fig. 4.1

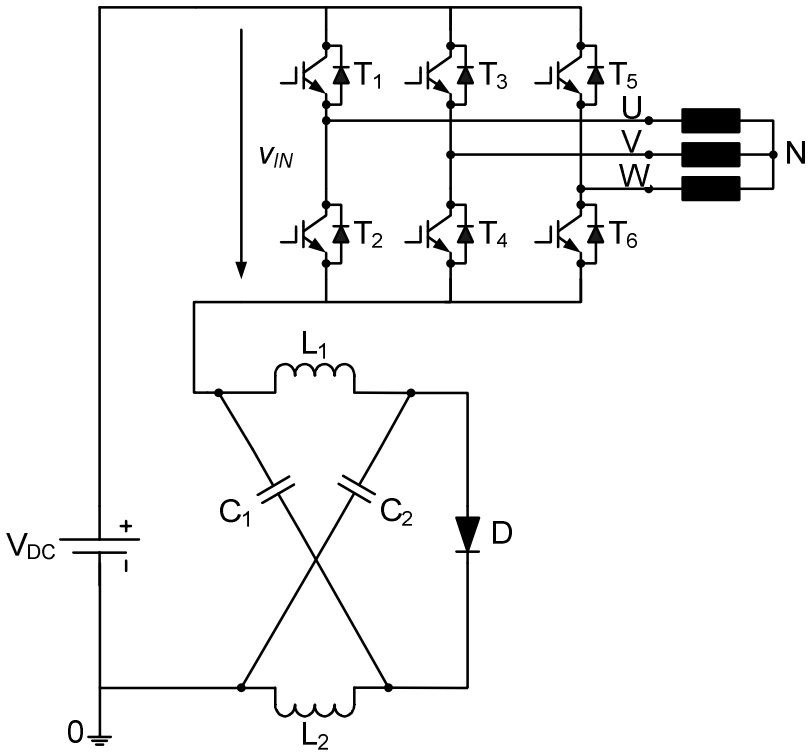
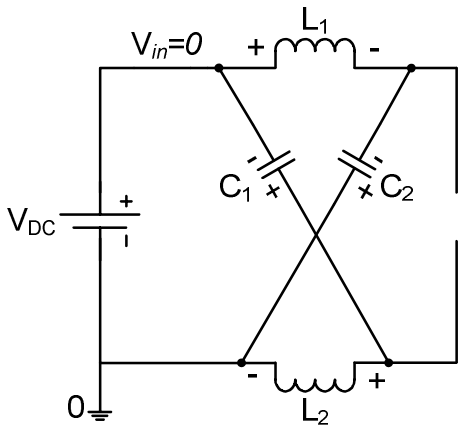


Fig. 4.1.Improved Z-source inverter with six switches

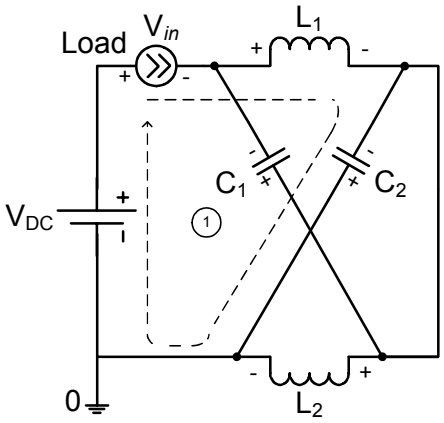
Fig. 5.1 clearly shows that the front end diode D and the inverter bridge changed places.

4.2.1 Principle of Operation. Voltage Gain

The improved Z-source inverter topology has two operating states like the traditional one: one shoot-through state generating the desired voltage boost and one non-shoot-through state when the average dc-link voltage is pulse width modulated by the inverter bridge. The two equivalent circuits of the two states are shown in Fig. 4.2.



a)



b)

Fig. 4.2. Equivalent circuits of the improved Z-source inverter a) shoot-through state b) non shoot-through state

As we can see in Fig. 4.2 in both states the voltage across the capacitors changed polarity compared to the traditional Z-source inverter (see in chapter 2). In the shoot-through state, as we expected, the diode stops conducting Fig. 4.2a). In the shoot-through state all the switches in the inverter bridge are turned on thus the voltage across the inverter bridge is zero. In the non shoot-through state it conducts. Writing Kirchhoff's voltage law in the shoot-through state the voltage across the inductor is given by

$$v_L = V_{DC} + \overline{v_C} \tag{4.1}$$

Note that even though the voltage across the capacitors being zero the voltages across the inductors will be equal with the input voltage and with the

polarity of the inductor voltage shown in Fig. 4.2a) therefore at the cathode of the diode the voltage potential is $+V_{DC}$ and at the anode of the diode is $-V_{DC}$. That is why the diode is not conducting because is inversely polarized.
In the non shoot-through state the voltage across the inductor can be defined by

$$v_L = -\overline{v_C} \tag{4.2}$$

The non shoot-through state includes the active states as well as the zero voltage states of the inverter bridge.

Through the average voltage across the inductor in steady state during one switching period we get the shoot-through duty ratio

$$\begin{aligned} \overline{v_L} &= \frac{1}{T_S}\int_0^{T_S} v_L(t) = 0 \\ \overline{v_L} &= \frac{1}{T_S}\left(t_{ST}\left(V_{DC} + \overline{v_C}\right) + \left(T_S - t_{ST}\right)\left(-\overline{v_C}\right)\right) = 0 \\ \overline{v_C} &= \frac{D_{ST}}{1-2D_{ST}} V_{DC} \end{aligned} \tag{4.3}$$

In (4.3) for zero shoot-through duty ratio the voltage across the capacitor is zero meaning that the voltage across the capacitor can be gradually increased.

As demonstrated in [1] the voltage ripple of the capacitors, the Z-source inductor current ripple, the input current ripple and the inverter bridge peak voltage stress are the same as in case of the traditional Z-source inverter. However, there remains one delicate aspect, which needs further investigation, of the operation in the non shoot-through state: whether the diode is conducting or not in this state. Looking at the currents in the non shoot-through state we can say one thing for sure: the diode is conducting only when the inductor instantaneous current in this sate is greater than half the dc-link voltage.

The duty ratio versus the ratio of the average capacitor voltage of the Z-source network and the input dc voltage is represented graphically in Fig. 4.3.

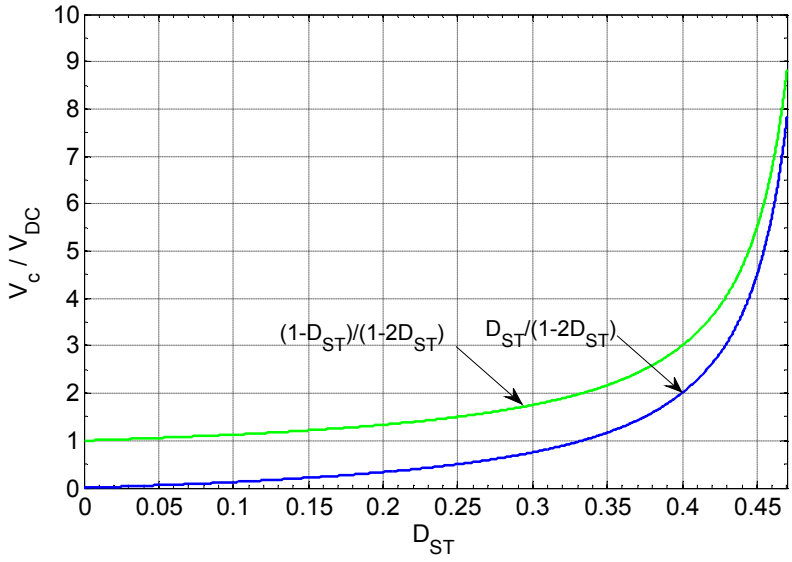


Fig. 4.3 VC/VDC versus DST for the traditional and for the improved Z-source inverter

It can be seen in Fig. 4.3. that the ratio between the average capacitor voltage and the input dc voltage starts from zero or for zero shoot-through duty ratio the capacitor voltage is zero. As a result of the circuit configuration the capacitor voltage can be increased gradually from zero.
The average dc-link voltage is given by (see Fig. 4.1)

$$\overline{v_{in}} = V_{DC} + \overline{v_L} + \overline{v_C} \tag{4.4}$$

but the average inductor voltage

$$\overline{v_L} = 0 \tag{4.5}$$

So, the average dc-link voltage, for this improved topology, is greater with the input voltage compared to the average dc-link voltage in the traditional Z-source inverter topology

$$\overline{v_{in}} = V_{DC} + \overline{v_C} \tag{4.6}$$

while the average dc-link voltage of the traditional Z-source inverter is the average Z-source capacitor voltage. In other words for the same average dc-link voltage the capacitor voltage stress for the improved topology is lower than for the traditional one thus low voltage capacitors can be used. Still the peak voltage stress across the inverter bridge remains the same.

4.3 Proposed Improved Four-Switch Three-Phase Z-source Inverter

The improved z-source inverter with 6 switches got better properties by the rearrangement of the circuit elements of a traditional Z-source inverter with six switches. One way to further improve the characteristics of the Z-source inverters is to reduce the number of switches Fig. 5.4. This of course introduces some control difficulties and it has some output limitations but eliminates the cost of two switches and their driver circuits. The proposed improved Z-source inverter with four switches leaves the main elements in the same place as in case of the improved Z-source inverter with six switches. It uses only four switches and the floating load terminal, which was connected to the eliminated inverter leg, is connected at the common point of two capacitors used instead of one of the Z-source network capacitors.

The derivation of the different operating states of the proposed topology and finally the switching times calculation is based on the theory for four-switch three phase inverters presented in [8]

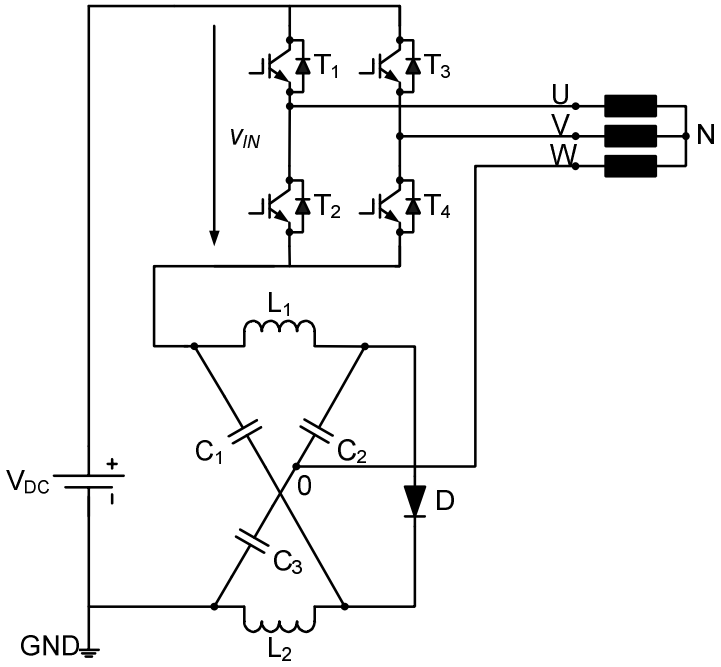


Fig. 4.4 Improved Z-source inverter with 4 switches

It can be easily demonstrated, by the integration of the voltage across one inductor, that the voltage boost formula (4.3) used at the improved six switch topology is valid for the proposed topology in Fig. 4.4 as well. The improved Z-source inverter with four switches has one more operating state, the shoot-through state, compared to the four switch three-phase inverters. The shoot-through state is generated with all the switches on. By interfering in the topology of the Z-source

network the shoot-through state becomes not only a voltage boost state but also an active state for the inverter at the same time as we will se later. Only the shoot-through state's equivalent circuit will be drawn to point out the duality of this state.

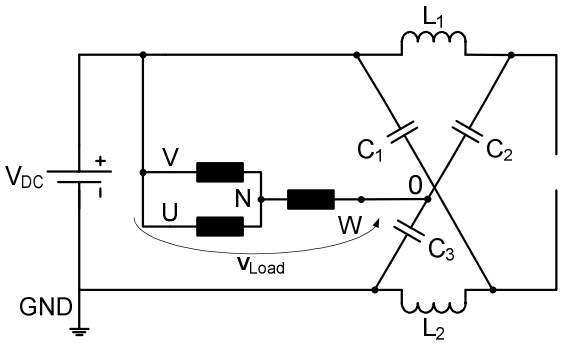


Fig. 4.5 Shoot-through state equivalent circuit of the improved Z-source four switch inverter

The load voltage across the load phases is the sum of half the average capacitor voltage and the input dc voltage

$$v_{Load} = \frac{\overline{v_C}}{2} + V_{DC} \tag{4.7}$$

With the chosen reference potential the common mode of the two capacitors the five possible switching states are illustrated in Table. 4.1.

	T_1	T_2	T_3	T_4
S_1	0	1	0	1
S_2	1	0	0	1
S_3	1	0	1	0
S_4	0	1	1	0
S_{ST}	1	1	1	1

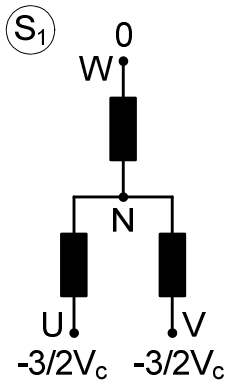
0 – switch off

1 – switch on

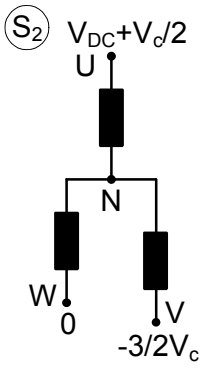
S_x – switching state

Table 4.1 The five possible switching states

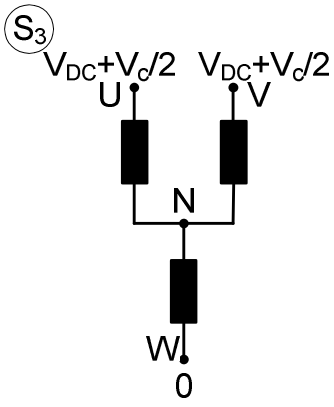
The load terminal voltages refrenced to „0" are shown in Fig. 4.6.



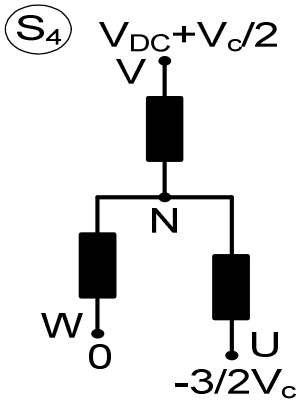
$$v_{U0} = -\frac{3}{2}\overline{v_C}$$
$$v_{V0} = -\frac{3}{2}\overline{v_C}$$
$$v_{W0} = 0$$



$$v_{U0} = V_{DC} + \frac{\overline{v_C}}{2}$$
$$v_{V0} = -\frac{3}{2}\overline{v_C}$$
$$v_{W0} = 0$$



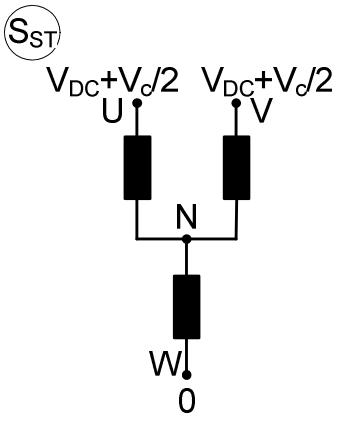
$$v_{U0} = V_{DC} + \frac{\overline{v_C}}{2}$$
$$v_{V0} = V_{DC} + \frac{\overline{v_C}}{2}$$
$$v_{C0} = 0$$



$$v_{U0} = -\frac{3}{2}\overline{v_C}$$

$$v_{V0} = V_{DC} + \frac{\overline{v_C}}{2}$$

$$v_{W0} = 0$$



$$v_{U0} = V_{DC} + \frac{\overline{v_C}}{2}$$

$$v_{V0} = V_{DC} + \frac{\overline{v_C}}{2}$$

$$v_{C0} = 0$$

Fig. 4.6 Load terminal voltage potentials at different switching states

The load terminal to neutral N voltages (the phase voltages) for the five switching states using the voltage potentials in Fig. 4.6 can be expressed as

Switching state S1

$$\begin{aligned} v_{UN} &= -\frac{\overline{v_C}}{2} \\ v_{VN} &= -\frac{\overline{v_C}}{2} \\ v_{WN} &= +\overline{v_C} \end{aligned} \tag{4.8}$$

Switching state S2

$$\begin{aligned} v_{UN} &= \frac{5}{6}\overline{v_C} + \frac{2}{3}V_{DC} \\ v_{VN} &= -\frac{7}{6}\overline{v_C} - \frac{1}{3}V_{DC} \\ v_{WN} &= \frac{1}{3}\overline{v_C} - \frac{1}{3}V_{DC} \end{aligned} \tag{4.9}$$

Switching state S3

$$\begin{aligned} v_{UN} &= \frac{1}{6}\overline{v_C} + \frac{1}{3}V_{DC} \\ v_{VN} &= \frac{1}{6}\overline{v_C} + \frac{1}{3}V_{DC} \\ v_{WN} &= -\frac{1}{3}\overline{v_C} - \frac{2}{3}V_{DC} \end{aligned} \tag{4.10}$$

Switching state S4

$$\begin{aligned} v_{UN} &= -\frac{7}{6}\overline{v_C} - \frac{1}{3}V_{DC} \\ v_{VN} &= \frac{5}{6}\overline{v_C} + \frac{2}{3}V_{DC} \\ v_{WN} &= \frac{1}{3}\overline{v_C} - \frac{1}{3}V_{DC} \end{aligned} \tag{4.11}$$

ST switching state SST

$$\begin{aligned} v_{UN} &= \frac{1}{6}\overline{v_C} + \frac{1}{3}V_{DC} \\ v_{VN} &= \frac{1}{6}\overline{v_C} + \frac{1}{3}V_{DC} \\ v_{WN} &= -\frac{1}{3}\overline{v_C} - \frac{2}{3}V_{DC} \end{aligned} \tag{4.12}$$

Note that in the shoot-through state the phase voltages are the same as in state S3.

From the five switching states we will get five voltage space phasors in the complex plane by substituting the three phase voltage expressions from the five switching states (4.8)-(4.12) into the definition of the voltage space phasor

$$\begin{aligned} \underline{V}_1 &= \left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right)\overline{v_C} \\ \underline{V}_2 &= \left(\frac{5}{6} - j\frac{\sqrt{3}}{2}\right)\overline{v_C} + \frac{2}{3}V_{DC} \\ \underline{V}_3 &= \left(\frac{1}{6} + j\frac{\sqrt{3}}{6}\right)\overline{v_C} + \left(\frac{1}{3} + j\frac{\sqrt{3}}{3}\right)V_{DC} \\ \underline{V}_4 &= \left(-\frac{7}{6} + j\frac{\sqrt{3}}{6}\right)\overline{v_C} + \left(-\frac{1}{3} + j\frac{\sqrt{3}}{3}\right)V_{DC} \\ \underline{V}_{ST} &= \underline{V}_3 = \left(\frac{1}{6} + j\frac{\sqrt{3}}{6}\right)\overline{v_C} + \left(\frac{1}{3} + j\frac{\sqrt{3}}{3}\right)V_{DC} \end{aligned} \tag{4.13}$$

As we could have expected the space voltage phasor corresponding to the shoot-through state and state 3 are identical. Therefore in the complex plane the two space phasors will have the same orientation and amplitude.

Finally the expressions of the u_α and u_β components of a desired voltage space phasor $\underline{u}_S$ using can be given by

$$\begin{aligned} u_\alpha &= \frac{V_{DC}}{6T_S}\left(2(2k-1)(t_2 - t_1 - 2t_4) + T_S(k+2)\right) \\ u_\beta &= \frac{\sqrt{3}V_{DC}}{6T_S}\left(2(2k+1)(-t_1 - t_2) + T_S(k+2)\right) \\ k &= \frac{\overline{v_C}}{V_{DC}} \end{aligned} \tag{4.14}$$

With proper control algorithm the desired voltage space-phasor can be generated from the five available in (4.14)

4.3.1 Simulation Results

Digital simulations were made in PSIM to partially validate the theory of the improved Z-source inverter with four switches. The circuit in Fig. 4.4 was implemented in PSIM and the control algorithm based on (4.14) was written in C code to generate the gating signals for the four switches. The load used was a wye connected three-phase RL load. The simulated circuit parameters were as follows:

$$\begin{aligned} &V_{DC} = 100V; L_1 = L_2 = 6.4mH; C_1 = 470uF; \\ &C_2 = C_3 = 940\mu F; R_{L1} = R_{L2} = 0.9\Omega \\ &k^* = 2; f^* = 50Hz \\ &f_S = 10kHz \\ &R_{Load\_Phase} = 15\Omega \\ &L_{Load\_phase} = 60mH \end{aligned}$$

In Fig. 4.7 we can see the capacitor voltages and the L_1 Z-source inductor current. We can notice that the two series capacitor voltages have almost the same average value. In Fig. 4.8 besides the L_2 inductor current and the load current we have the filtered phase voltage. Fig. 4.9 shows the instantaneous and average dc-link voltage. As we can see in Fig 4.7 and Fig. 4.9 the dc-link voltage is not equal anymore to the average C_1 voltage as in the case of the traditional Z-source inverters. Thus for the same voltage boost a higher average input dc-link voltage can be obtained.

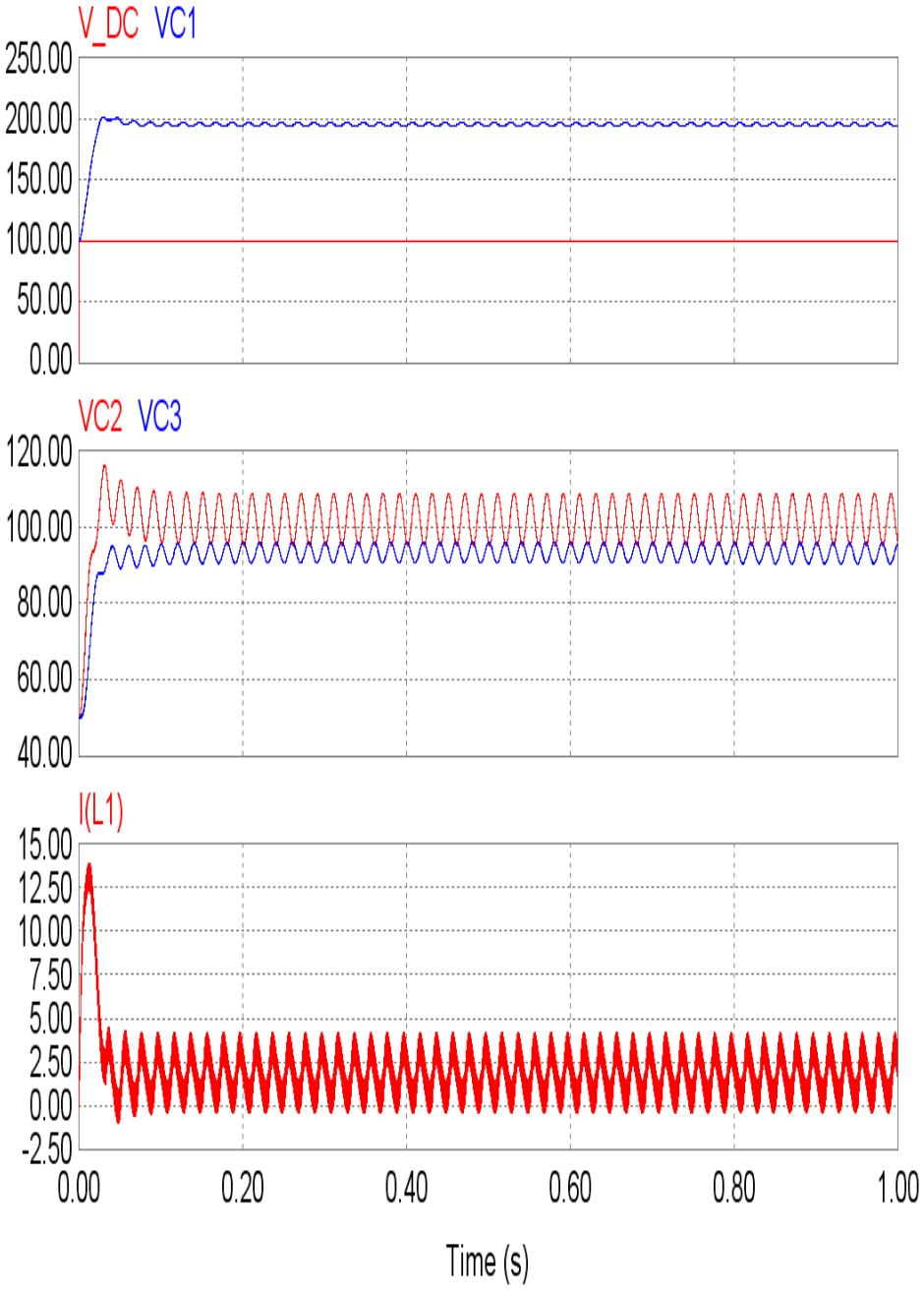


Fig. 4.7 The input voltage VDC, the capacitor voltage C1, C2 and C3 capacitor voltages, L1 inductor current (from top to bottom)

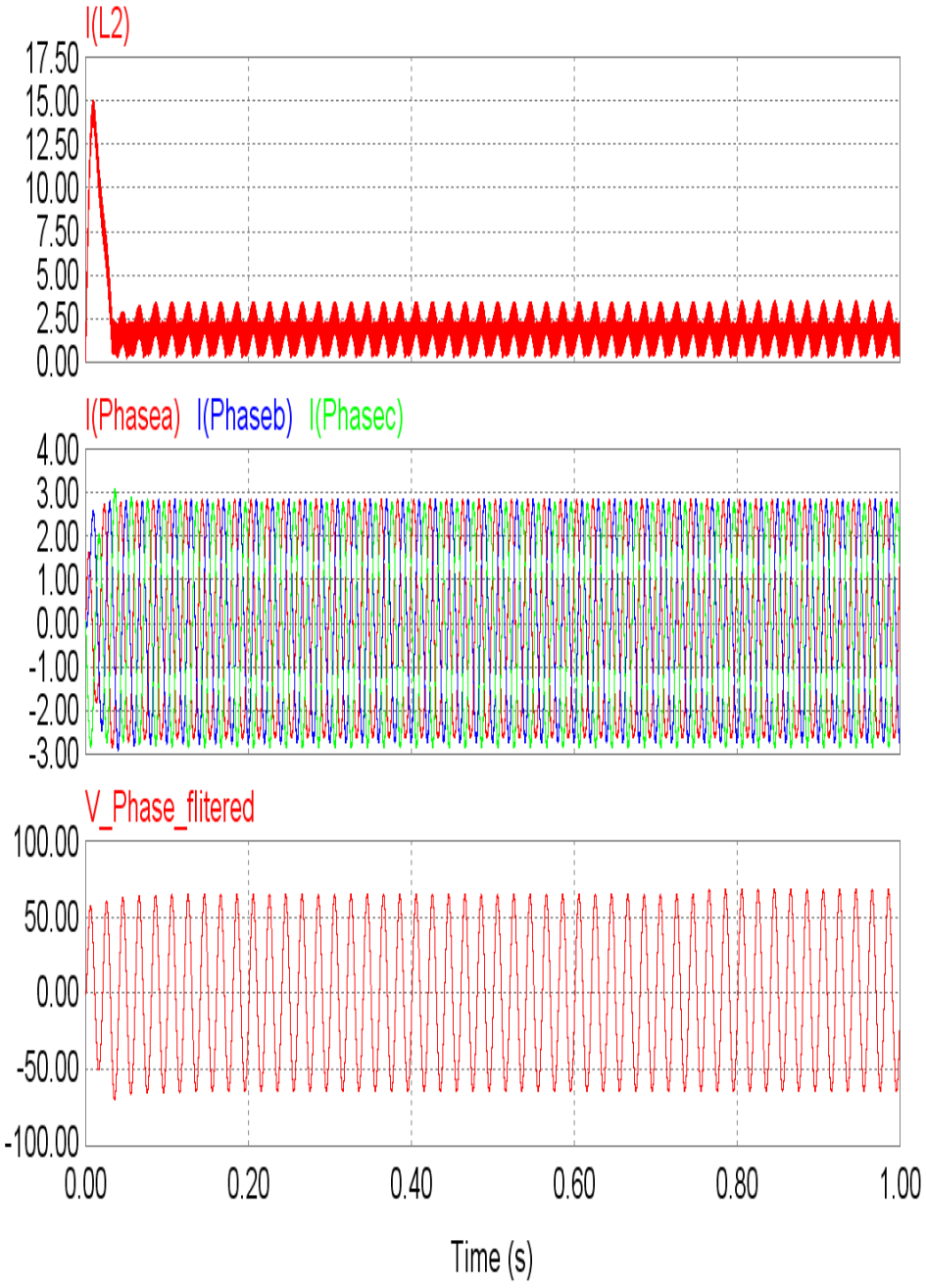


Fig. 4.8 L2 inductor current, the load phase currents, filtered phase voltage (from top to bottom)

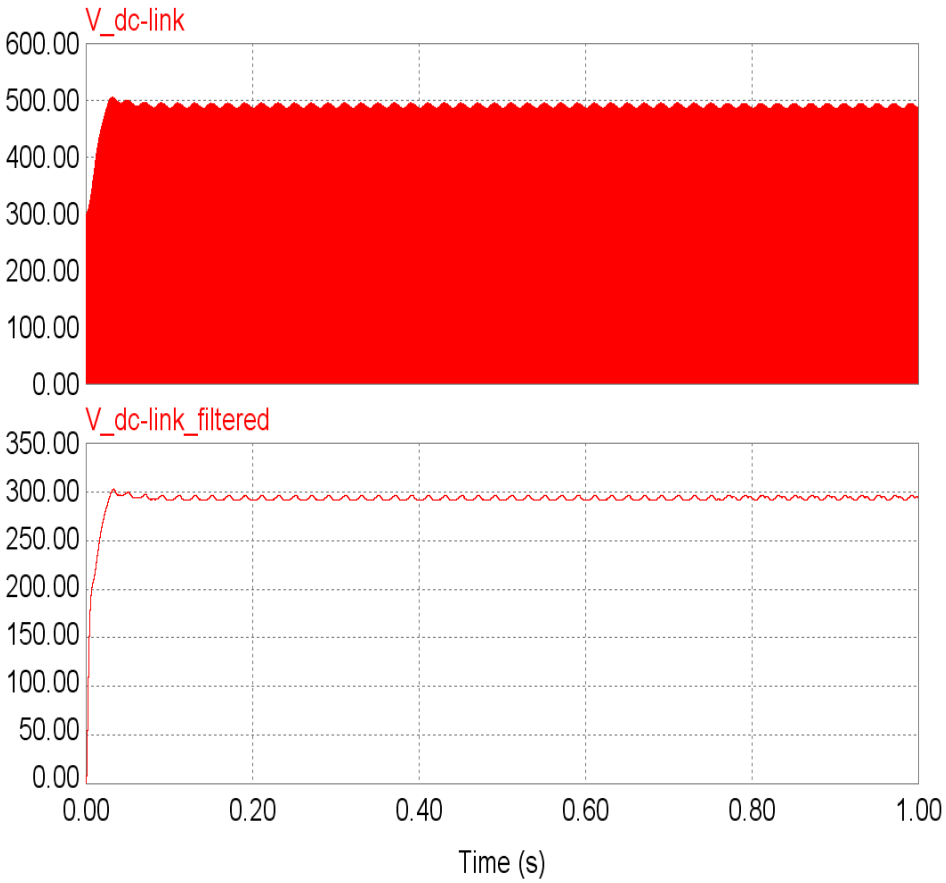


Fig. 4.9 The instantaneous dc-link voltage and the filtered dc-link voltage (from top to bottom)

4.4 Summary

This chapter presented the improved Z-source topology derived from the traditional Z-source inverter. New improved four-switch three-phase topology has been presented with detailed space vector analysis. Based on the space vector analysis the control algorithm was written in C and finally digital simulations were carried out to verify the theory.

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CHAPTER 5 SWITCHED-CAPACITOR HYBRID DC-AC PWM CONVERTERS

5.1 Introduction

This chapter presents a control algorithm for the newly proposed diode-assisted buck-boost voltage-source inverters (VSIs), with high voltage gain, which takes into account the changing of the dc-link voltage (two leveled) during one switching period due to the parallel charging and series discharging of the capacitors in the diode-capacitor network. Additionally it lowers the components voltage ratings.

In dc-ac applications where at the input there is a solar panel, fuel-cells or series ultra-capacitors the input voltage is low compared to the desired dc-link voltage for a VSI and it varies in a wide range. Hence the boost converter between the VSI and the dc voltage source should have a high voltage gain and a good voltage sag override capability. The two dc-ac converters called diode-assisted buck-boost VSIs [1] with a proper control algorithm can easily satisfy the above mentioned demands. The voltage boost algorithm used in [1] works well only for very high voltage gain and for moderate voltage gain (when the desired output voltage is not so high and the voltage boost might be reduced to lower the losses) it needs some modifications in the control algorithm.

The new high gain dc-dc converter presented in [2] contains the circuit analysis and the design guidelines for the converter and by the elimination of the output LC filter the dc-ac circuit presented in [1] can be obtained, of course with proper control algorithm.

By combining a step-up or step-down structure with the well known buck, buck-boost, boost, Cuk, Sepic and Zeta converters [3] new high step-up/step down voltage gain dc-dc converters can be obtained and eliminating the output filter of these dc-dc converters and adding appropriate control new high voltage gain step-up/step down dc-ac converters can be realized.

Charging in parallel of two inductors and discharging them in series can lead to high voltage gain as presented in [4].

Despite the fact that the boost-switched capacitor-inverter with a multilevel waveform output [5] uses the same topology as in [1] it provides an output frequency equal with half the switching frequency of the boost switch thus it is suitable only for high frequency ac power supplies [7]. Other topologies having multilevel output waveforms suffer from EMI interference problems [8] or they are voltage level number limited [6].

Topologies of dc-ac converters with enhanced functionality has been reported in [9]-[11].

The extreme minimum and maximum duty cycles of the buck or boost converters lead to poor efficiencies of the converter. Using the transformer concept on voltage regulators can drag the duty cycle in a realistic interval, from a practical point of view, thus increasing the efficiency[12]. Some applications in the field of microprocessors need under 1V supply voltage which has to deliver high currents and deal with fast dynamics [13].

From the energy level comparison in the inductor in [3] the quadratic converters got in the frist place before the hybrid dc-dc topologies [3] and the traditional buck/boost or buck-boost topologies. In other words the quadratic converters [14] [15] need a bigger inductor. Even more they may present some current and voltage overstresses.

High voltage gain applications are also in the automobile industry for high intensity discharge lamps [16] or in the telecomunication industry (e.g. from 45V-380V dc battery-inverter dc-link[17]).

The flyback converter has a high voltage gain but due to the leakage inductance the switch suffers from high voltage stress. With adequate leakage-inductance energy recycling techniques [18]-[20] the voltage stress can be reduced.

From a functional point of view the switched-capacitor hybrid dc-ac PWM VSIs (or diode-assisted PWM VSIs) can be divided into two stages: voltage boost circuit (formed by an inductor and a transistor) plus a diode-capacitor network – dc-dc voltage conversion – and the VSI part – dc-ac conversion Fig. 6.1 and Fig.6.2.

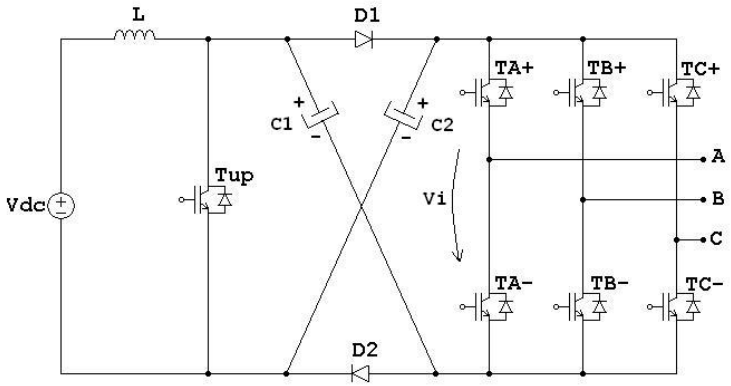


Fig.5.1 Cuk-derived buck-boost VSI

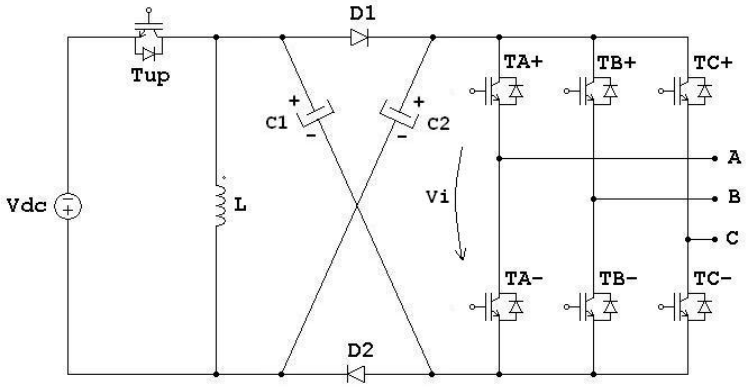


Fig. 5.2 Sepic-derived buck-boost VSI

The two VSIs in Fig. 5.1 and Fig. 5.2, combining a Cuk or Sepic dc-dc converter with a VSI have the ability to charge in parallel and discharge in series the

two capacitors in the diode-capacitor network. This parallel charging and series discharging introduces a voltage level change in the instantaneous input dc-link voltage V_i of the inverter bridge during one switching period T_S. So the dc-link voltage has two different constant values during one switching period of the converter if all transistors operate at the same switching frequency. In traditional space vector modulation (SVM) algorithms the dc-link voltage is considered to be constant during one switching period, thus these algorithms can be applied only on portions of the switching period where the dc-link voltage is constant [1]. In the two control strategies presented in [1] active vectors are applied only when the two capacitors are in series, "filling" the remained parts of the switching period with zero voltage vectors. The drawback of this control strategy is that the inverter poorly utilizes the available dc-link voltage especially when the voltage boost is small.

The boost-switched capacitor single-phase inverter with five-level output voltage presented in [6] fully utilizes the dc-link voltage but unfortunately the frequency of the output voltage of the inverter stage is constant and is half the switching frequency of the boost stage. The main characteristics of these VSIs are:

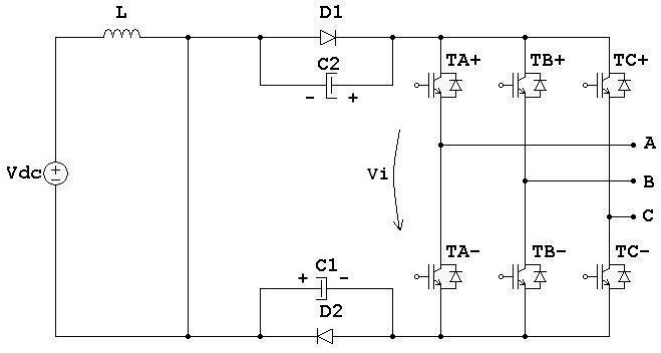
- the voltage boost is realized in one stage
- high voltage gain
- during the voltage boost the intermediate circuit is reconfigured because of the diode-capacitor network and the dc input voltage seen by the VSI is changed during one switching period

This last characteristic is exploited in this chapter in order to fully utilize the dc-link voltage, to increase the voltage gain even more and to decrease the elements voltage ratings.

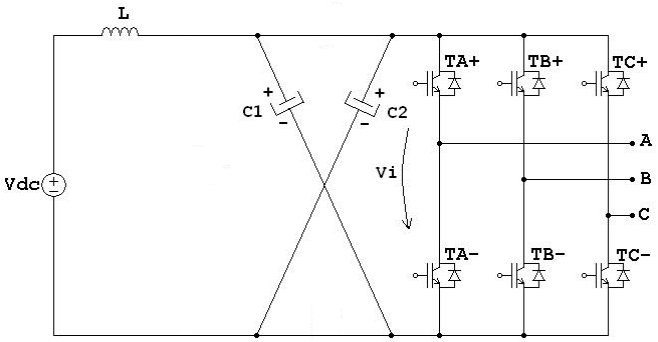
In the following the improved control algorithm for each of the two buck-boost VSI topologies will be presented separately after that digital simulations and experimental results validate the proposed improved control.

5.2 Improved Control of the Cuk-Derived Buck-Boost VSI

The two equivalent circuits for the Cuk-derived buck-boost VSIs when T_{up} is on and when T_{up} is off are shown in Fig. 5.3. a and b.



a)



b)

Fig. 5.3 Equivalent circuits of a Cuk-derived buck-boost VSI a) Tup on b) Tup off

Writing the equation of the rise and fall time of the current in the inductor L we can derive the voltages across the capacitors C_1 and C_2 as

$$\frac{V_{dc}}{L} D_{up} T_s = \frac{V_C - V_{dc}}{L} (1 - D_{up}) T_s \tag{5.1}$$

$$V_C = V_{C1} = V_{C2} = \frac{1}{1 - D_{up}} V_{dc} \tag{5.2}$$

where $D_{up} = \frac{t_{up}}{T_s}$ is the duty cycle of the gating signals of the transistor T_{up}.

It can be seen in Fig. 5.3 that during the on state of transistor T_{up} the instantaneous DC-link voltage V_i is $V_{C1}+V_{C2}=2V_C$ and during T_{up} off it is V_C.

The question is how this changing dc-link voltage, during one switching period, can be used efficiently in the SVM algorithm. During one switching period two active voltage vectors are used as well as one zero voltage vector. In a traditional SVM algorithm the two active and one zero voltage vectors' application time is calculated with a constant dc-link voltage.

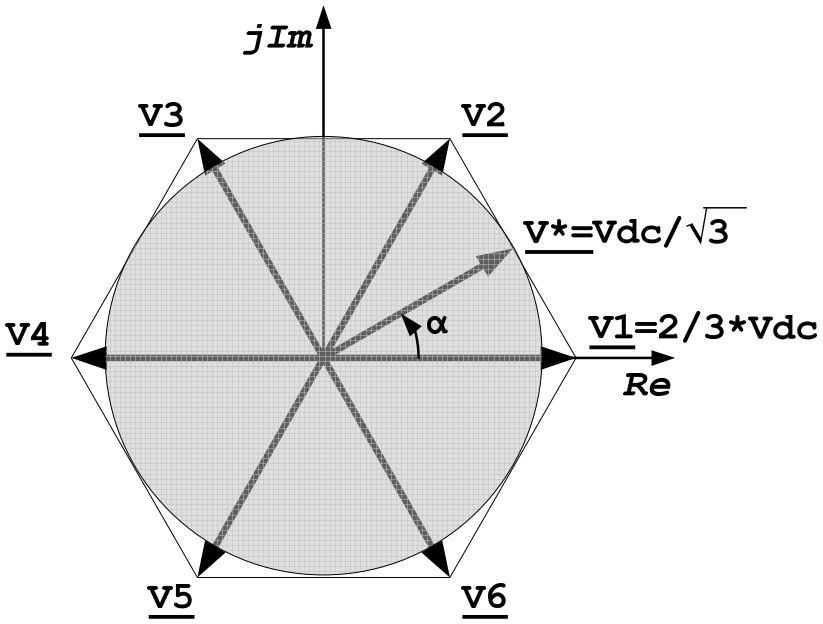


Fig. 5.4 Locations of the switching state vectors and their maximum lenght

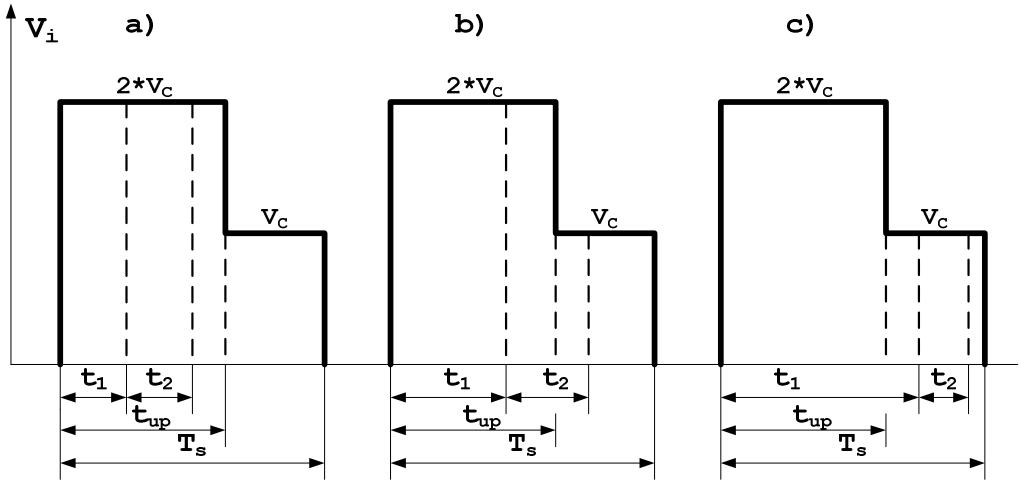


Fig. 5.5 Instantaneous DC-link voltage during one switching period Ts and the possible positioning of t1 and t2 for the diode-assisted buck-boost VSI

Referring to the first sector, the stator voltage vector can be expressed as

$$\underline{V^*} = \frac{1}{T_s}\left(t_1\underline{V_1} + t_2\underline{V_2}\right) \tag{5.3}$$

Note that the two time intervals t_1 and t_2 are calculated with a constant dc-link voltage during the switching period but our dc-link voltage is not constant it has two

dc levels during T_s Fig. 5.5. During the boost time interval t_{up} the input dc-link voltage V_i is equal with $2V_C$ and during T_s-t_{up} it is equal with V_C.

For a prescribed voltage boost t_{up} we have a two-leveled dc-link voltage V_i and three possible placements of the two active voltage vector time intervals t_1 and t_2.Fig. 5.5. The first situation is for very high voltage boost, for D_{up} greater than 0.76 and it is neglected in our control algorithm [1].

As a first step in the development of the proposed improved control algorithm we consider an average dc-link voltage V_{DC2} during T_s. The average dc-link voltage used in both control algorithms in [1] is V_{DC1}.(3) which for the same required output voltage by the load is greater than V_{DC2}.

Why is the average DC-link voltage so important? Because this gives the maximum length of the switching state vectors and finally the linear modulation range.

The two average dc-link voltages V_{DC1} and V_{DC2} during T_s and the maximum dc-link voltage V_{DClink} are derived in (5.3) where D_{up} is the boost duty ratio $D_{up}=t_{up}/T_s$. With the average dc-link voltage V_{DC2} we calculate t_{10} and t_{20} time intervals for the two switching state vectors V_1 and V_2 respectively with a traditional space vector modulation (SVM) algorithm afterwards we readjust the length of these time durations taking into account the instantaneous dc-link voltage V_i obtaining t_1 and t_2 in Fig. 5.5.

$$V_{DC1} = D_{up}\,2V_C = \frac{2D_{up}}{1-D_{up}}V_{dc}$$

$$V_{DC2} = D_{up}\,2V_C + (1-D_{up})V_C = \frac{1+D_{up}}{1-D_{up}}V_{dc} \qquad (5.3)$$

$$V_{DCLink} = \frac{2}{1-D_{up}}V_{dc}$$

It is obvious (see eq. 3) that with V_{DC2}, which fully utilizes the dc-link voltage, we can get much longer switching state voltage vectors than with V_{DC1} for the same voltage boost.

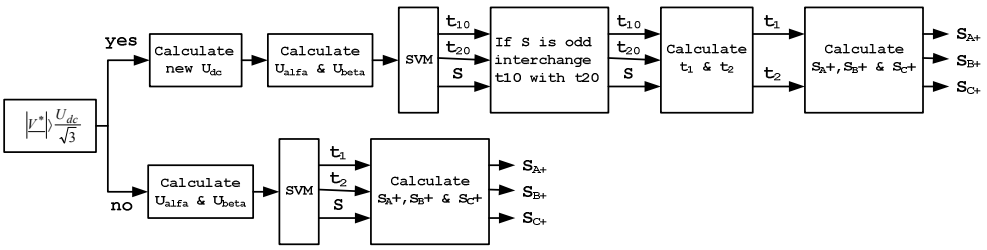


Fig. 5.6 Control algorithm for Cuk-derived buck-boost VSIs

Thus for the same length of the prescribed voltage vector V* a smaller voltage boost is needed, when using V_{DC2} instead of V_{DC1}. Furthermore, the voltage ratings of the components will be lower.

In order to fully utilize the dc-link voltage and to operate in the linear modulation zone the length of the prescribed voltage vector V* gives the needed voltage boost and it is equal with $1/\sqrt{3}$ times the average DC- link voltage V_{DC2}.

From

$$\left|\underline{V^*}\right| = \frac{V_{DC2}}{\sqrt{3}} \tag{5.4}$$

using (5.3) one can obtain

$$D_{up} = \frac{\frac{\sqrt{3}}{V_{dc}}\left|\underline{V^*}\right| - 1}{1 + \frac{\sqrt{3}}{V_{dc}}\left|\underline{V^*}\right|} \tag{5.5}$$

The voltage boost is introduced only when the length of the prescribed voltage vector V* exceeds the linear modulation zone, the area delimited by the circle. The modulation index is always 1 when voltage boost is needed. This way the dc-link voltage is fully utilized.

Once we got t_{10} and t_{20} with V_{DC2} the next step is to determine the relative position of t_{10}, t_{20} and t_{up} to each other and finally to adjust them to obtain t_1 and t_2.

$$\frac{2}{3}\frac{t_{10}}{T_s}\frac{1+D_{up}}{1-D_{up}}V_{dc} \le \frac{2}{3}\frac{t_{up}}{T_s}2\frac{1}{1-D_{up}} \tag{5.6}$$

Equation (5.6) will tell us the relative position of t_{10}, t_{20} and t_{up} to each other.
But first a switching pattern has to be chosen. The gating pulses of the transistors will be left aligned.
By simplifying (5.6) we get

$$t_{10} \le \frac{2D_{up}}{1+D_{up}}T_s \tag{5.7}$$

If (5.7) is true than we have the case in Fig. 5.5b and t_1 and t_2 can be expressed as

$$\begin{aligned} t_1 &= t_{10}\left(1+D_{up}\right) \\ t_2 &= t_{20}\left(1+D_{up}\right) - t_{up} + t_1 \end{aligned} \tag{5.8}$$

If (5.7) is not satisfying for t_1 and t_2 we get the following expressions Fig. 6.5c

$$\begin{aligned} t_1 &= t_{10}\left(1+D_{up}\right) - t_{up} \\ t_2 &= t_{20}\left(1+D_{up}\right) \end{aligned} \tag{5.9}$$

Now the case in Fig. 5.5a will be analyzed (which results from both control algorithms in [1]). We have to determine the minimum D_{up} for which $t_{up}=t_1+t_2$. The sum between t_1 and t_2 (one of them is equal with 0) is minimum when t_0 is maximum and t_0 is maximum for $\alpha = n\pi/3$ where $n = \overline{0,6}$. For α =0 we have

$$\underline{V^*} = \frac{t_1}{T_s}\underline{V_1} \tag{5.10}$$

$$\frac{V_{DC2}}{\sqrt{3}} = \frac{t_1}{T_s}\frac{2}{3}V_{DC2}$$
$$\frac{t_1}{T_s}V_{DC2} = D_{UP}\,2V_C \qquad (5.11)$$

From (5.11) the D_{upmin} for the case in Fig. 5.5a is 0.76. The above calculations demonstrate that for a boost duty ratio lower than 0.76 case a) in Fig. 5.5 never appears so we can skip this case from the control algorithm.
The left aligned gating signal generation is shown in Fig. 5.7.

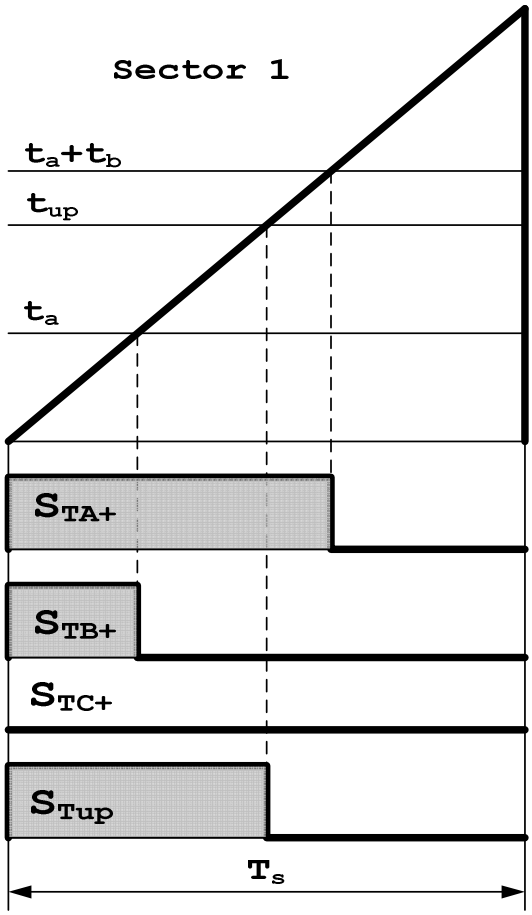


Fig. 5.7 Left-aligned gating signal generation for the 7 transistors in the Cuk-derived buck-boost VSI

It can be noticed in Fig. 5.8 that for a desired average dc-link voltage VDCLink avg* if using V_{DC2} instead of V_{DC1} we will have a smaller boost factor and a smaller voltage rating for the inverter bridge (the input voltage V_{dc}=100V).

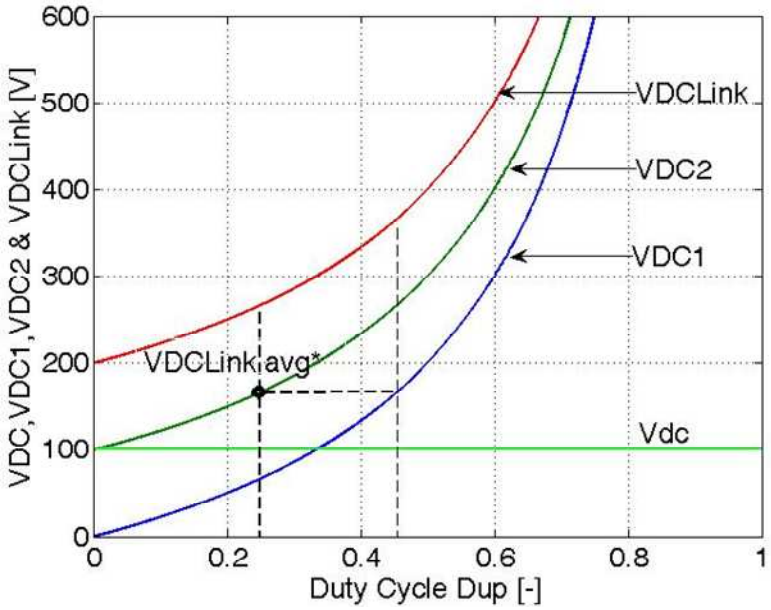


Fig. 5.8 Relationship between VDC1, VDC2, the maximum DC-link voltage VDCLink and Dup for Vdc=100V

In the following section we will move on to the Sepic-derived buck-boost VSI control which we will see is similar to the Cuk derived one.

5.3 Improved Control of the Sepic-Derived Buck-Boost VSI

For the Sepic-derived buck-boost VSI presented in Fig. 5.2 we have the two equivalent circuits shown in Fig. 5.9 a and b for the ON and OFF states of T_{up}. During the boost time interval and the OFF time interval of T_{up} the dc-link voltage is $2V_C + V_{dc}$ and respectively V_C.

The voltage across the capacitors can be derived as

$$V_C = V_{C1} = V_{C2} = \frac{D_{up}}{1 - D_{up}} V_{dc} \tag{5.12}$$

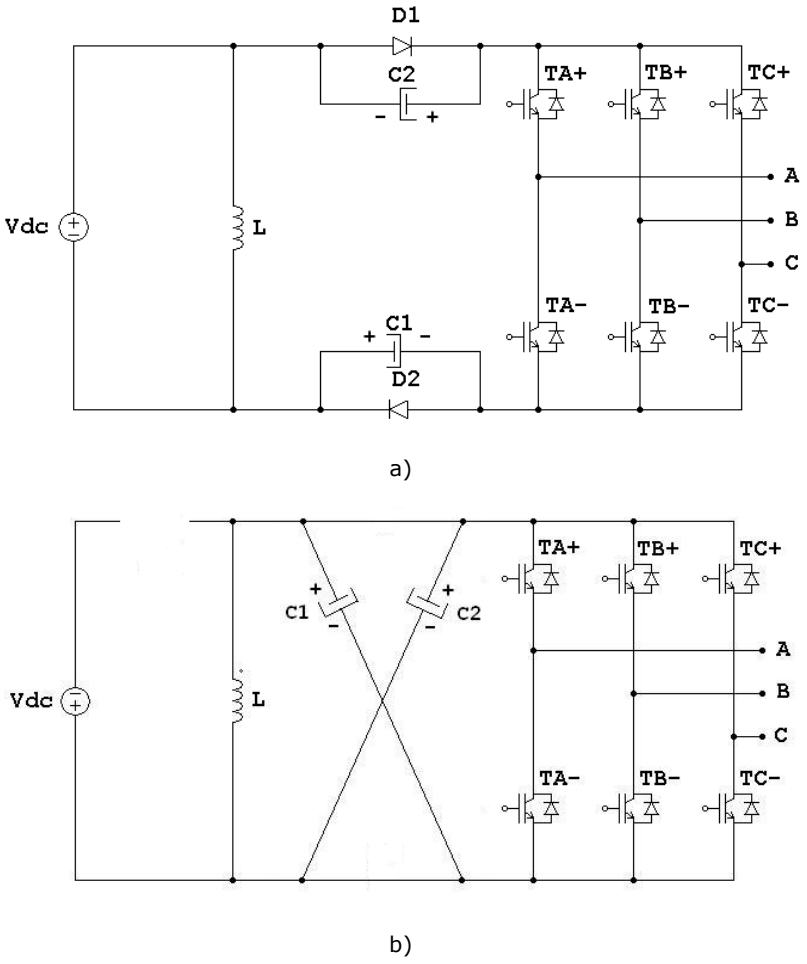


Fig. 5.9 Equivalent circuits of a Sepic-derived buck-boost VSI a) Tup on b) Tup off

The average voltages V_{DC1} (used in [1]), V_{DC2} and the maximum voltage stress of the inverter bridge have the following expressions

$$V_{DC1} = \frac{D_{up} + D_{up}^2}{1 - D_{up}} V_{dc}$$
$$V_{DC2} = \frac{2D_{up}}{1 - D_{up}} V_{dc} \qquad (5.13)$$
$$V_{DCLink} = \frac{1 + D_{up}}{1 - D_{up}} V_{dc}$$

Fig. 5.10 shows the relationship between V_{DC1}, V_{DC2}, the inverter transistor bridge voltage rating V_{DCLink} and the boost factor D_{up} for an input voltage of V_{dc}=100V.

The same pattern used for the Cuk-derived buck-boost VSI control algorithm can also be applied for the Sepic-derived buck-boost VSI to get to the formulae of t_{10} and t_{20}.

After we have calculated the preliminary t_{10} and t_{20} time intervals with (5.12) and (5.13) the final t_1 and t_2 can be derived from (5.14)

$$t_{10} \le \frac{1+D_{up}}{2} T_s \tag{5.14}$$

For the last two situations in Fig. 5.5b and 5.5c the expressions for t_1 and t_2 can be presented as

$$\begin{aligned} t_1 &= t_{10} \frac{2D_{up}}{1+D_{up}} \\ t_2 &= 2t_{20} + \frac{t_1 - t_{up}}{D_{up}} \end{aligned} \tag{5.15}$$

and

$$\begin{aligned} t_1 &= 2t_{10} - T_s \\ t_2 &= 2t_{20} \end{aligned} \tag{5.16}$$

Following the same path shown in (5.10) and (5.11) the minimum boost duty ratio D_{upmin}, for which the first situation in Fig. 5.5a has to be considered in the control algorithm, can be easily calculated and is equal with 0.73.

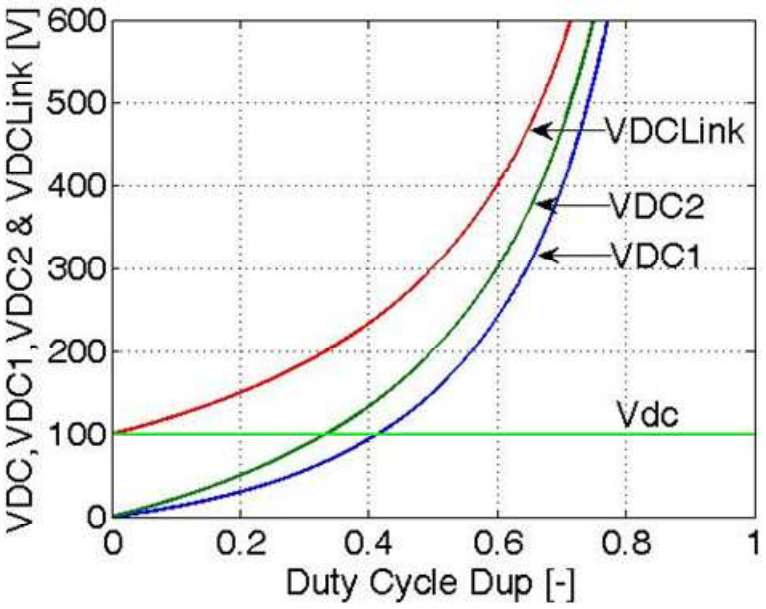


Fig. 5.10 Relationship between VDC1, VDC2, the maximum DC-link voltage VDCLink and Dup for Vdc=100V

5.4 Simulation Results

The improved control algorithm was simulated in PSIM and validated through experiments on a Cuk-derived buck-boost VSI. The circuit parameters, for simulation and experiments, of the Cuk-derived buck-boost VSI with a three-phase RL load were as follows

$$V_{dc} = 70V; L = 1.4mH; C_1 = C_2 = 680\mu F;$$
$$R_{Phase} = 10\Omega; L_{Load} = 10mH;$$
$$f_s = 10kHz;$$

The integration step size is 5 microseconds.

For 1 second the prescribed voltage vector length is V*=60V and the output fundamental frequency is equal with 50Hz (boost time interval) after that for 1 second V*=30V and the output fundamental frequency is equal with 20Hz (no boost). This algorithm is repeated over and over to show that the proposed control algorithm of the dc-ac converter works well even when there is no need for voltage boost.

Fig. 12 shows the boost duty ratio and the phase and line voltages.

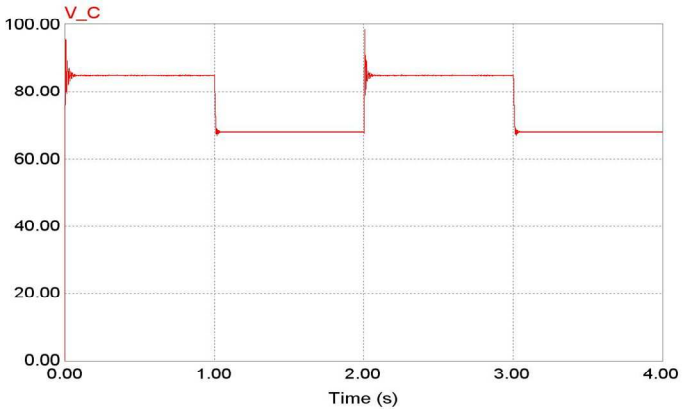


Fig. 5.11 Simulated voltage waveform across capacitor C1

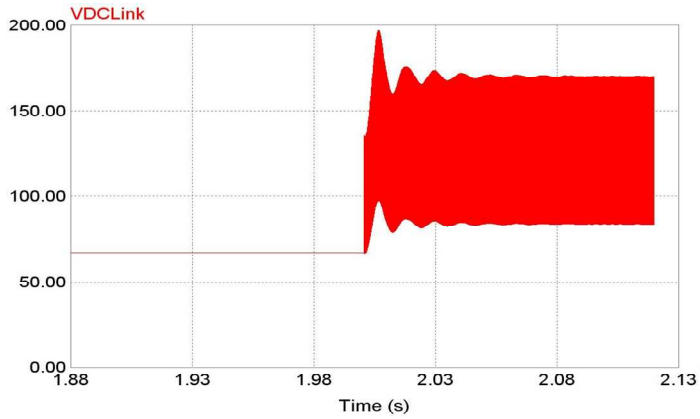


Fig. 5.12 Simulated dc-link voltage waveform during voltage boost and no-boost

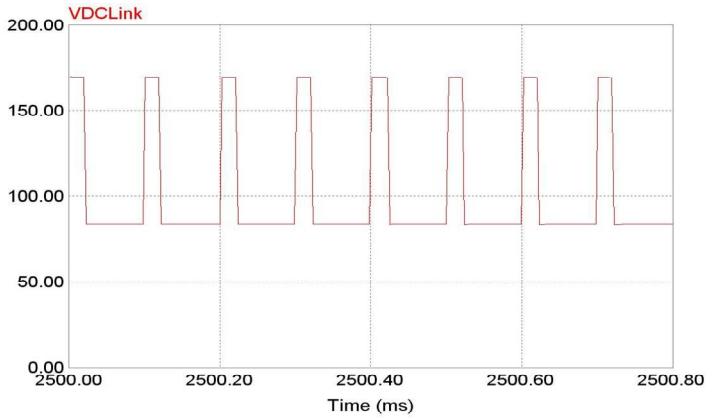


Fig. 5.13 Simulated zoomed dc-link voltage waveform during voltage boost

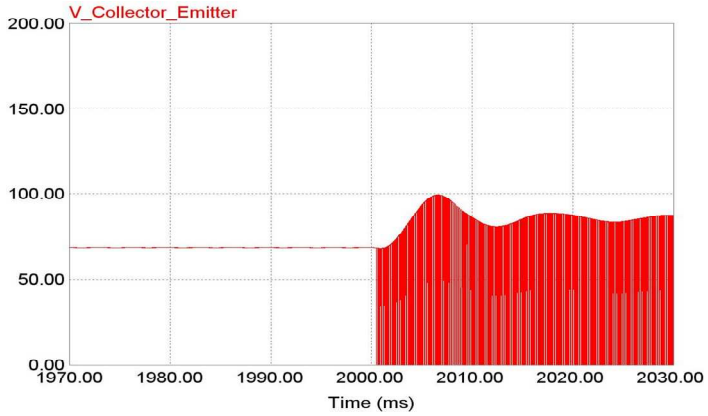


Fig. 5.13 Simulated collector-emitter voltage waveform of the boost transistor Tup

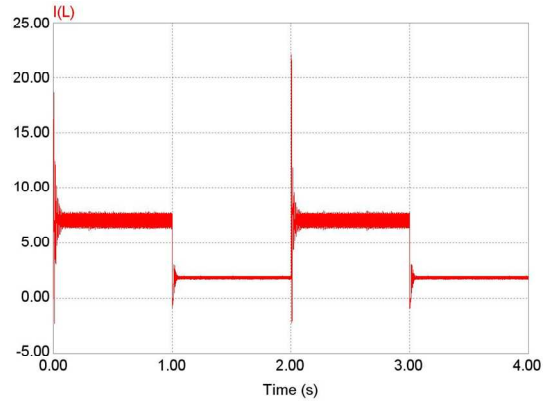


Fig. 5.14 Simulated boost inductor L current waveform

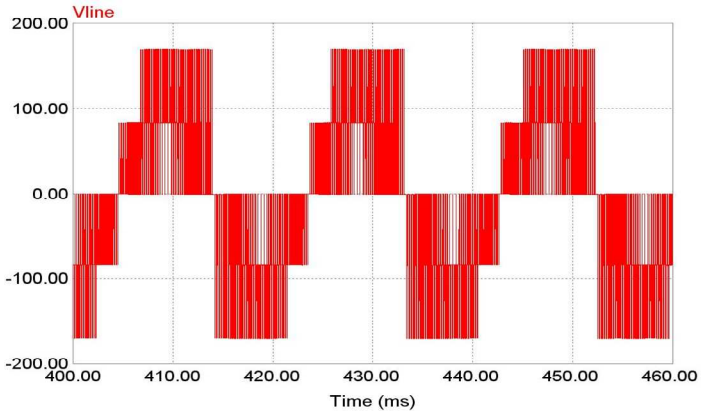


Fig. 5.15 Simulated line to line output voltage waveform during voltage boost

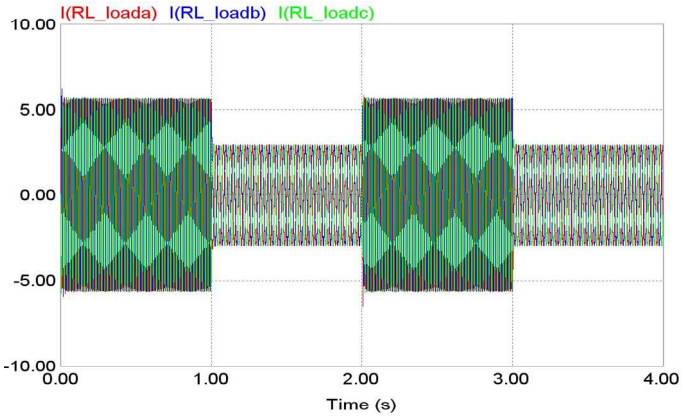


Fig. 5.16 Simulated load phase current waveforms

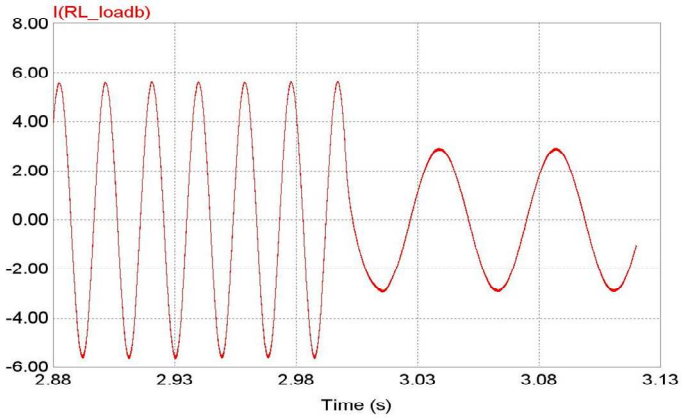


Fig. 5.17 Simulated phase current waveform at the boundary of the voltage boost and no voltage boost intervals

5.5 Experimental Results

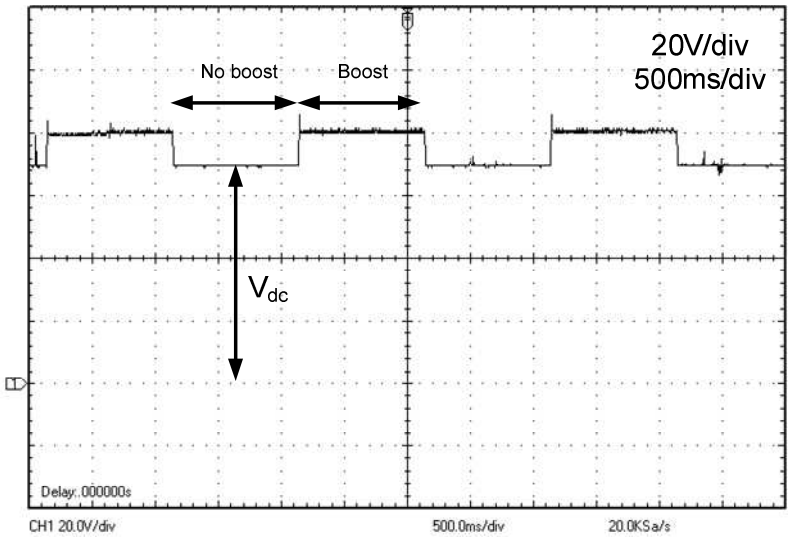


Fig. 5.18 Experimental voltage waveform across capacitor C1

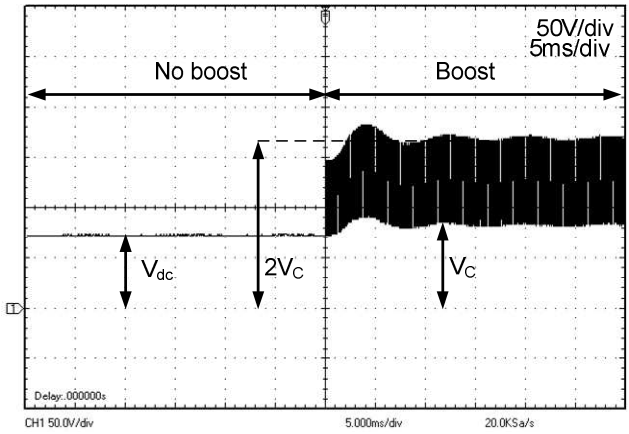


Fig. 5.19 Experimental dc-link voltage waveform

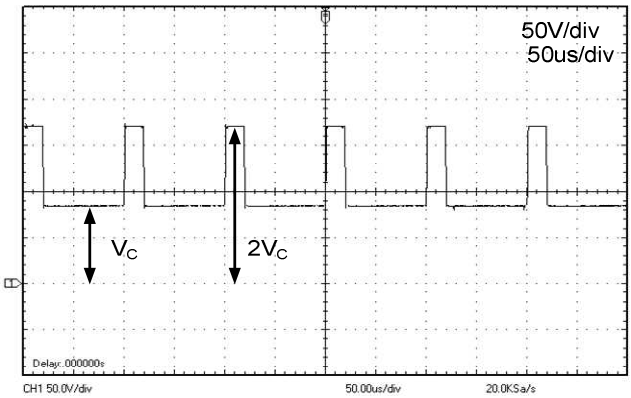


Fig. 5.20 Experimental zoomed dc-link voltage waveform during voltage boost

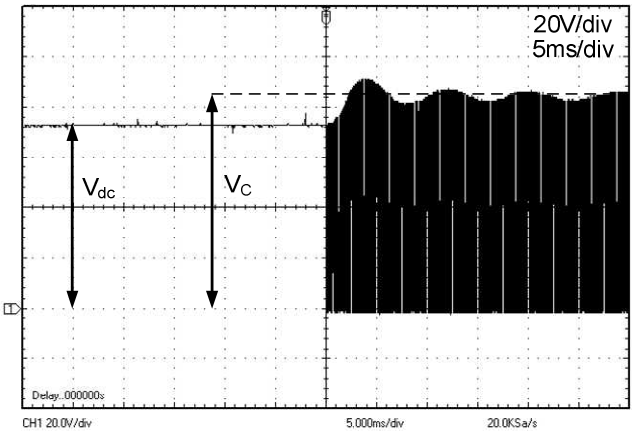


Fig. 5.21 Experimental collector-emitter voltage waveform of the boost transistor Tup

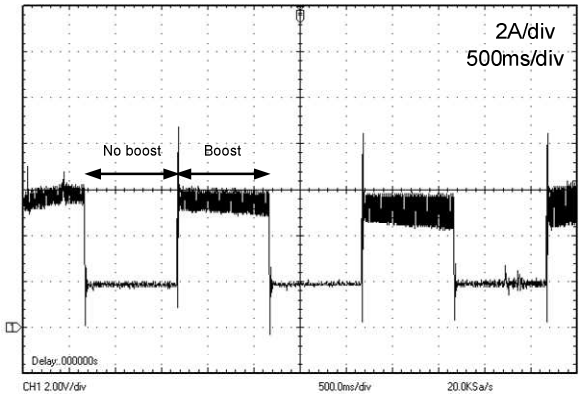


Fig. 5.22 Experimental boost inductor L current waveform

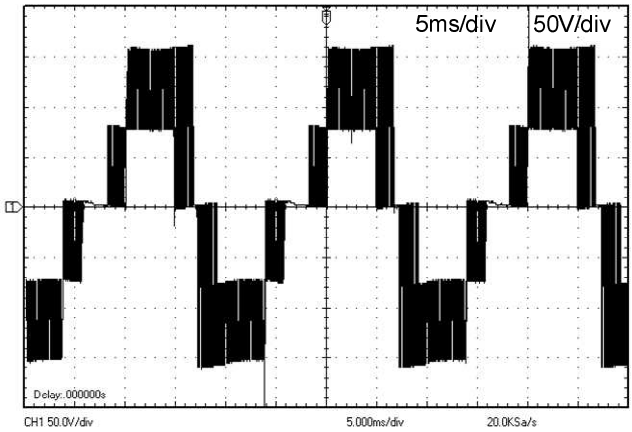


Fig. 5.23 Experimental line to line output voltage waveform during voltage boost

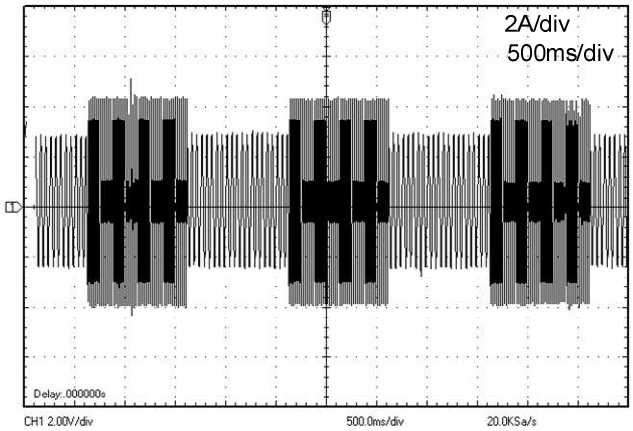


Fig. 5.24 Experimental current waveform through one phase of the load

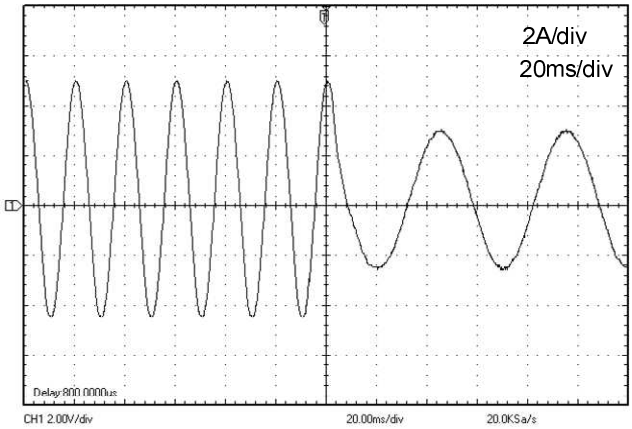


Fig. 5.25 Experimental phase current waveform at the boundary of the voltage boost and no voltage boost intervals

The experimental and simulated capacitor voltages in Fig. 5.11 and Fig. 5.18 clearly show that when there is no need for voltage boost in the dc-link, the voltage across the capacitors is equal with the supply voltage V_{dc}. The two leveled DC-link voltage during voltage boost is evidenced by Fig. 5.12, 5.13 and Fig 5.19, 5.20. Fig. 5.14 and Fig. 5.21 show that the maximum voltage stress across the boost transistor T_{up} during voltage boost is equal with the voltage across the capacitors V_c even though the maximum voltage across the inverter IGBT bridge when T_{up} is on is equal with twice the voltage across the capacitors Fig. 5.13 and Fig. 5.20.

The experimental current of the boost inductor L in Fig. 14 is similar to the simulated one in Fig 5.22.

Furthermore it can be seen in Fig. 5.15 – Fig. 5.17 and Fig. 5.23-Fig. 5.24 that the line to line experimental voltages and the RL load experimental currents are close to those in simulation.

For the simulation of the control algorithm for a Sepic-derived buck-boost VSI the equations for t_1 and t_2 (5.8) and (5.9) has to be changed with (5.15) and (5.16) and transistor T_{up} switches places with the inductor L.

The control algorithm illustrated in Fig.5.6 was implemented on a dsPIC30F3011 16-bit digital signal processor and the oscilloscope used for the acquisitions was DSO3062A 60MHz, 1Gs/s from Agilent Technologies. The control program was written in C.

5.6 Summary

Swtiching capacitor high gain dc-ac converters were presented. A new control algorithm for the high gain VSIs has been derived which works even for moderate voltage boost. The control algorithm was simulated and tested on a laboratory setup. Finally the simulated and experimental waveform were presented and discussed.

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CHAPTER 6 EXPERIMENTAL SETUP

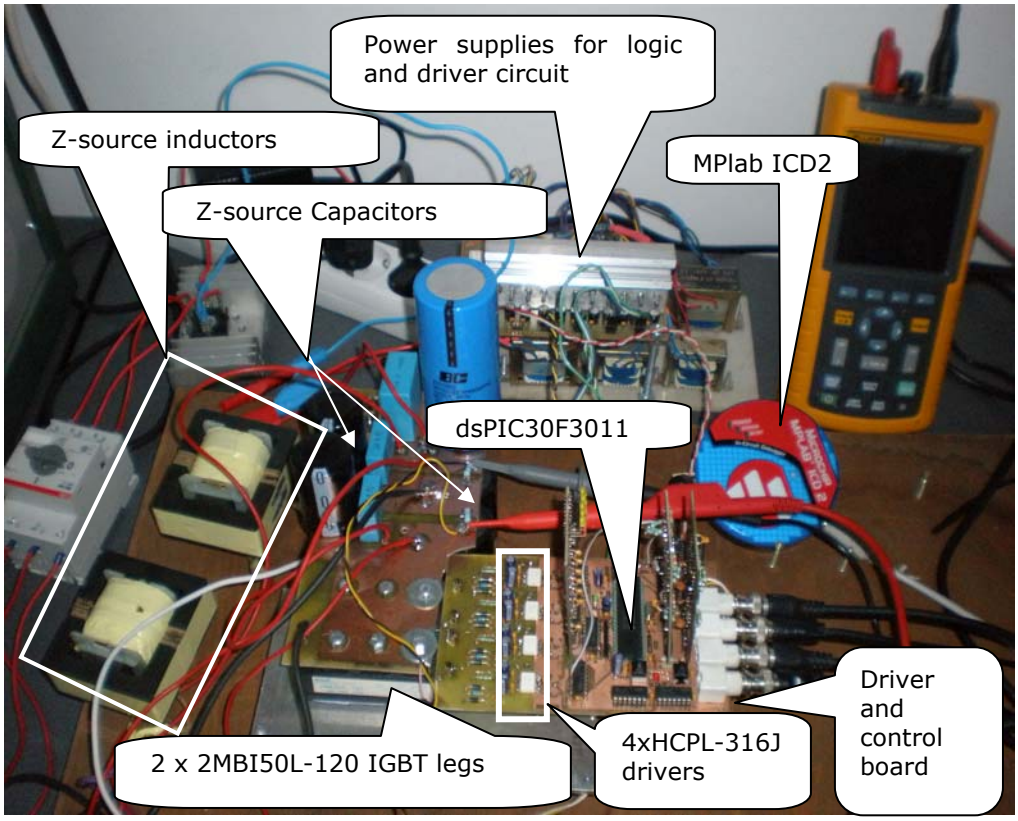

Fig 1. Laboratory setup for Z-source inverter experiments

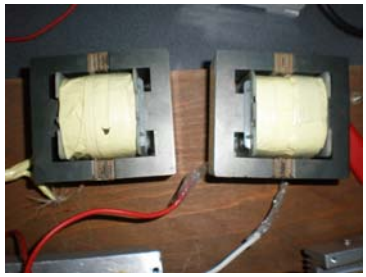

Fig. 2 Z-source inductors

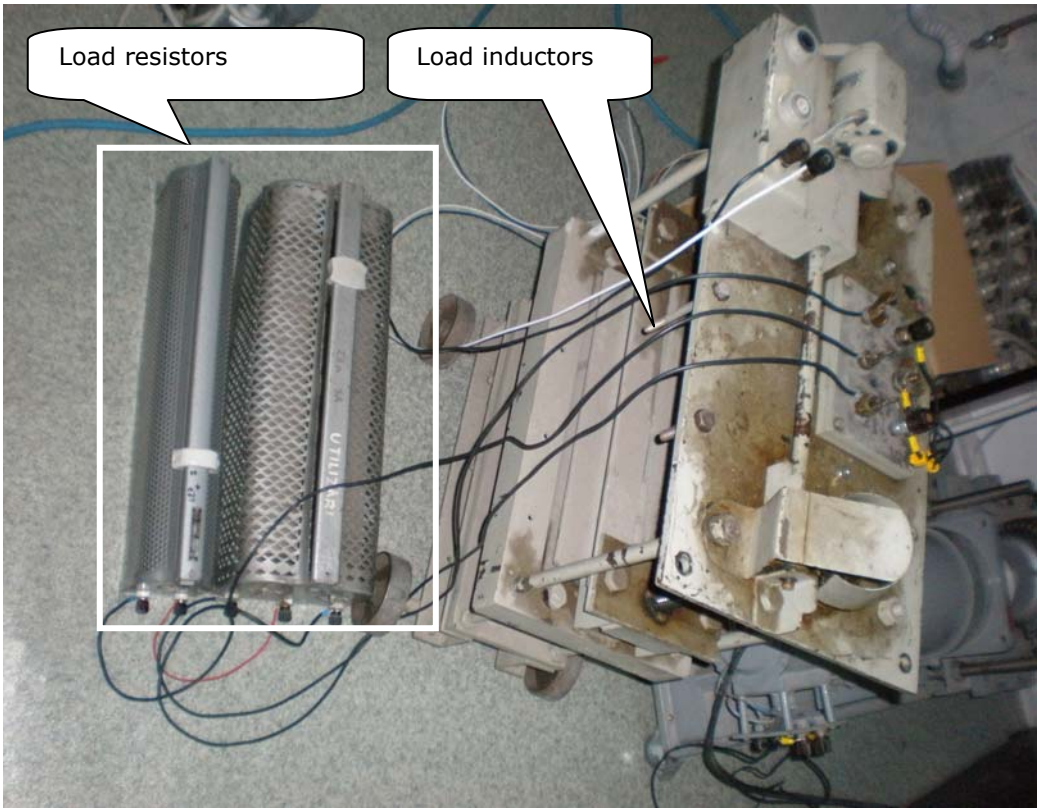

Fig. 3 The used RL load

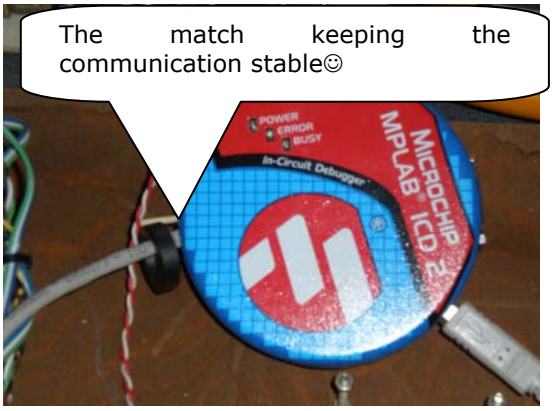

Fig. 4 MPlab ICD2 programmer and debugger

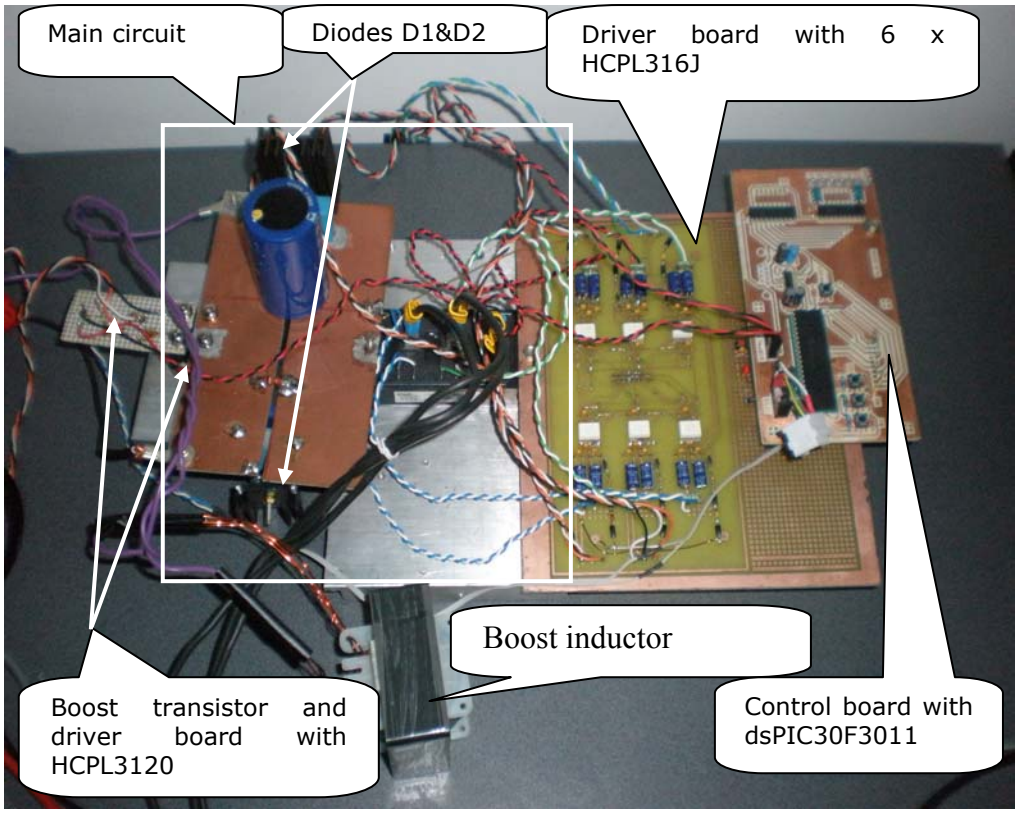

Fig. 5 Setup for switched-capacitor hybrid DC-AC PWM converter

Fig. 6 Boost inductor

In Fig. 1 we can see the laboratory setup used to carry out the experiments for the Z-source topologies. In Fig. 2 we have the used Z-source inductors which have 6.4mH each. In Fig. 3 the used RL load is illustrated. The programmer used to program the dsPIC30F3011 with the C code control algorithm was a low cost programmer and debugger from Microchip called ICD2 Fig. 4. In Fig. 5 and Fig. 6 we

have the laboratory setup used for the switched-capacitor hybrid DC-AC PWM converters with high gain. The load was the same as for the Z-source topologies Fig. 3.

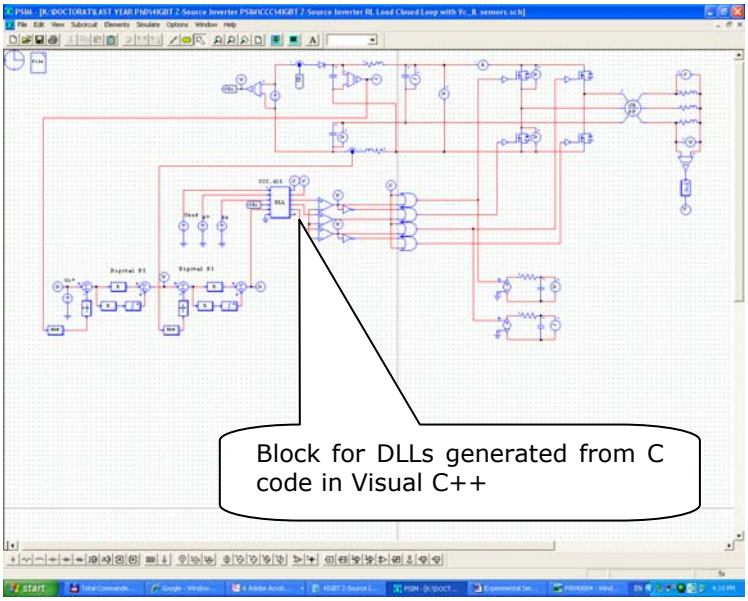

Fig. 7 PSIM software for circuit simulation

The dedicated software for electrical circuit simulation PSIM6.0 was used to simulate the proposed topologies. Each control algorithm was written in C code in Visual C++. From this C code DLL control files for PSIM were generated. Next the control C code with small modifications was compiled in MPlab 7.0 (see Fig. 8) and dsp code was generated. The dsPIC30F3011 was programmed with ICD2.

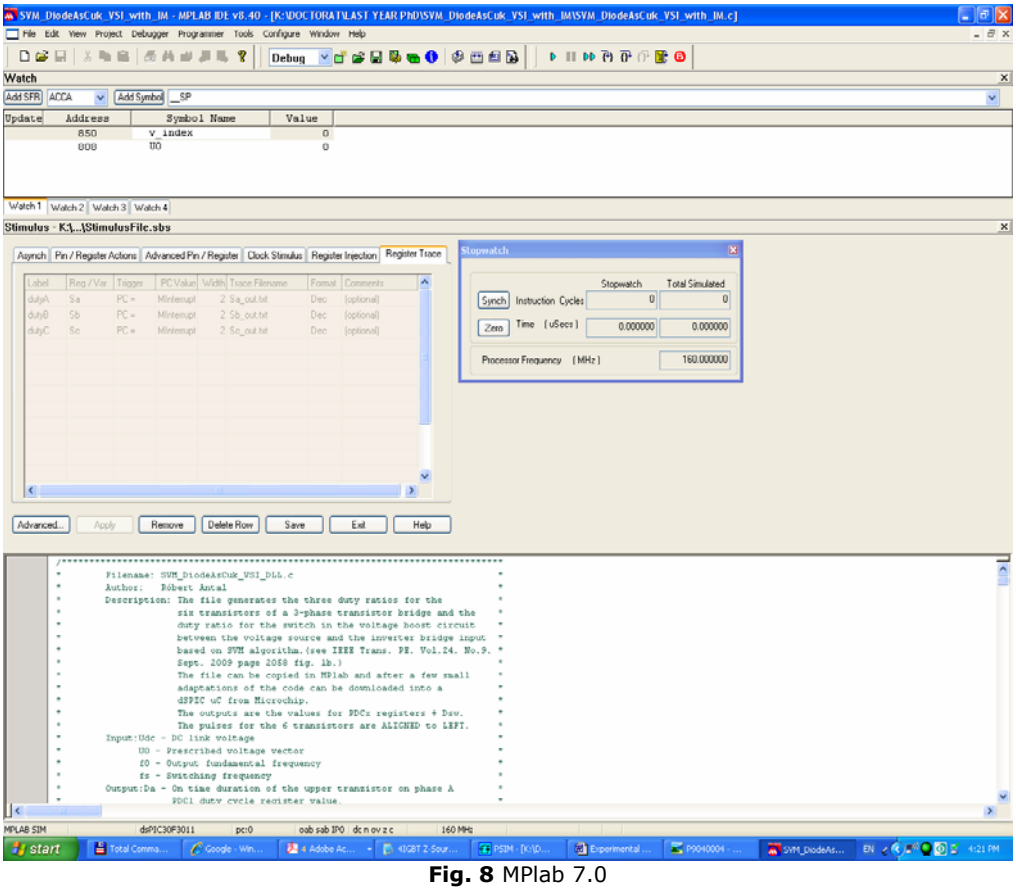

Fig. 8 MPlab 7.0

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CHAPTER 7 ORIGINAL CONTRIBUTIONS AND CONCLUSIONS

The dc output voltage of the enviroment friendly electrical energy generation systems fluctuates in a wide range and usually its voltage level is less than the input voltage desired at the input of a DC-AC converter. The voltage can be boosted with a DC-DC converter to the desired voltage level for the DC-AC stage or with a DC-AC converter including a Z-source network. The combination of the Z-source network and a traditional single or three-phase inverter enhances the properties of the DC-AC stage thus providing the ability to boost the input voltage and to override the voltage sags. One way to further improve the properties of the DC-AC stage is to reduce the number of switches in the single/three-phase inverter bridge from four/six to two/four. Based on the above listed reasoning the original contributions and conclusions of the author would be the following:

- Comprehensive study of the single and three-phase Z-source inverters with four respectively six switches has been carried out. The relevant formulae describing the operation of a Z-source inverter were pointed out;
- Three new Z-source inverter topologies (one single-phase and two three-phase Z-source inverter topologies) were proposed
- The operation and the different operating states of the proposed topologies were analyzed in detail and finally equations describing the operation of the proposed Z-source topologies were derived
- Based on the analytically derived equations the new Z-source topologies were validated through digital simulations
- Two of the three proposed Z-source inverters were validated through experiments

Another drawback of the alternative electrical energy sources is the low output voltage level which has to be greatly boosted to obtain acceptable voltage level at the DC-AC conversion stage input in order to be able to deliver energy to the grid. The Cuk and Sepic derived switched-capacitor DC-AC PWM converters have a high voltage gain therefore these topologies can be used to obtain in the same time high voltage boost and ac output voltage. Related to these topologies with high voltage gain the following original contributions can be found in the thesis:

- A new efficient control algorithm for the high voltage gain switched-capacitor DC-AC PWM converters was proposed in order to lower the inverter bridge voltage stresses through optimal voltage gain generation and full use of the volt-second product available at the input of the three-phase inverter transistor bridge
- The proposed control algorithm was validated by simulations and experiments

Finally, the original contributions related to the used laboratory setups:

- Two laboratory setups were designed and build by the author from scratch in order to validate the proposed Z-source inverter topologies and the control algorithm for the switched-capacitor DC-AC PWM converters experimentally
- The control algorithms used in experiments were implemented on a low cost digital signal processor dsPIC30F3011. The control programs were written in C language

AUTHOR'S PAPERS RELATED TO THE PH.D. THESIS

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